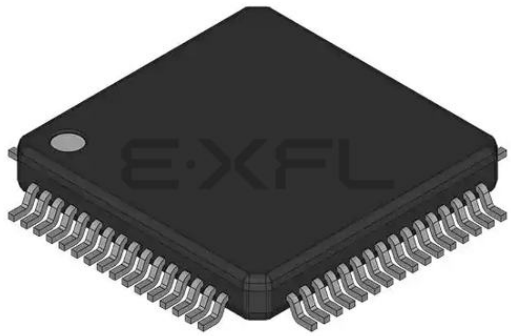

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Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.9K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=s9s08lg32j0vlh

Freescale Semiconductor, Inc.
Data Sheet Addendum

Document Number: MC9S08LG32AD
Rev. 0, 04/2015

Addendum to Rev. 9 of the MC9S08LG32 Series Covers: MC9S08LG32 and MC9S08LG16

This addendum identifies changes to Rev. 9 of the MC9S08LG32 Series data sheet (covering MC9S08LG32 and MC9S08LG16). The changes described in this addendum have not been implemented in the specified pages.

1 Add min values for I_{IC} (DC injection current)

Location:	Table 8. DC Characteristics, Page 14

In Table 8, “DC Characteristics,” add min values for I_{IC} (row number 14) as follows:

Num	C	Characteristic		Symbol	Min	Typ[1]	Max	Unit
14	D	DC injection current [5, 6, 7] $V_{IN} < V_{SS}$ (min) $V_{IN} > V_{DD}$ (max)	Single pin limit	I_{IC}	**-0.2**	—	2	mA
			Total MCU limit, includes sum of all stressed pins		**-5**	—	25	mA

2 Change the max value of t_{LPO} (low power oscillator period)

Location:	Table 14. Control Timing, Page 29

In Table 14, “Control Timing,” change the max value of t_{LPO} (row number 2) from 1300 to 1500 µs.

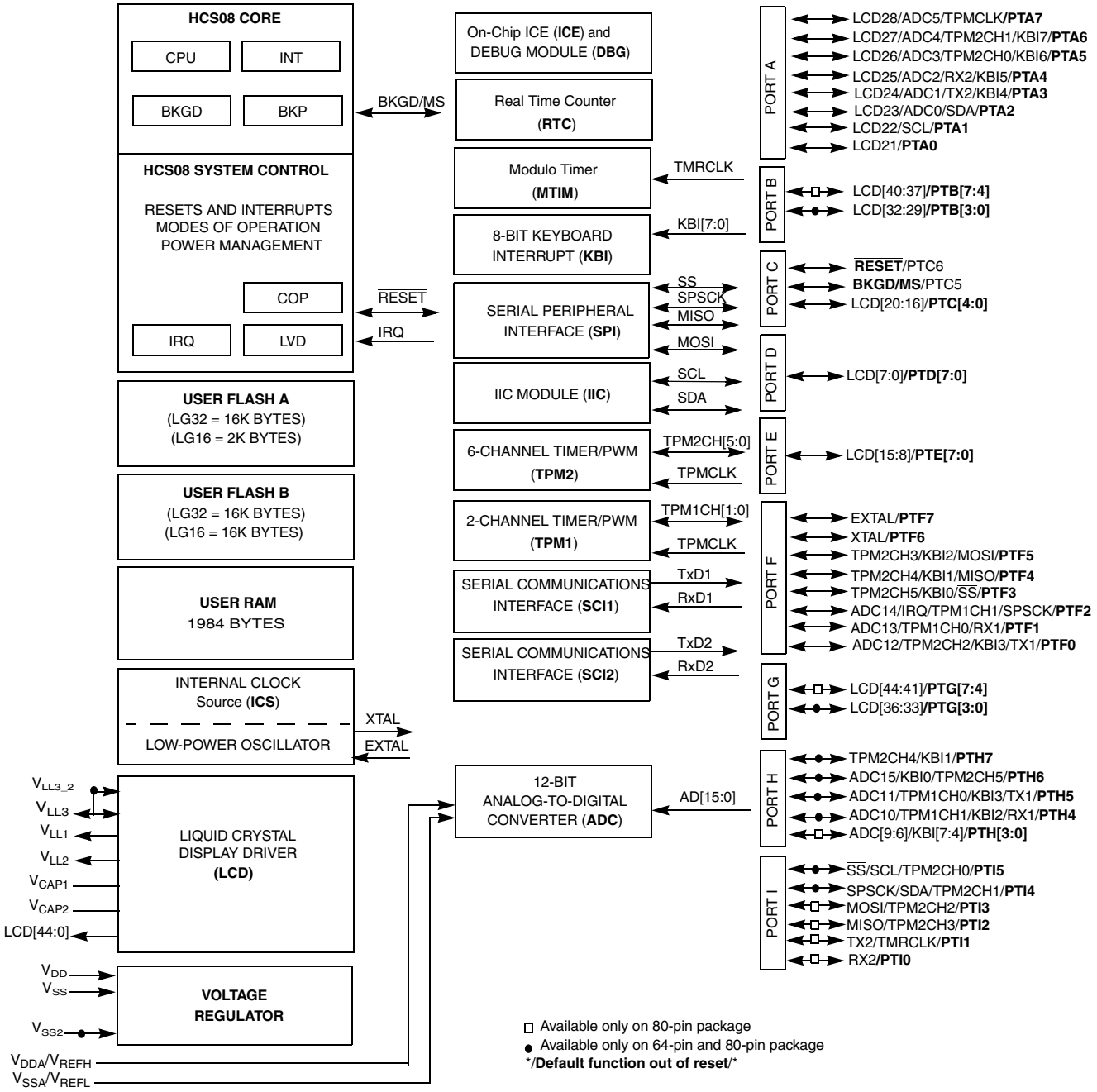


Figure 1. MC9S08LG32 Series Block Diagram

Table 1. MC9S08LG32 Series Features by MCU and Package

Feature	MC9S08LG32			MC9S08LG16	
Flash size (bytes)	32,768			18,432	
RAM size (bytes)	1984				
Pin quantity	80	64	48	64	48
ADC	16 ch	12 ch	9 ch	12 ch	9 ch
LCD	8 x 37 4 x 41	8 x 29 4 x 33	8 x 21 4 x 25	8 x 29 4 x 33	8 x 21 4 x 25
ICE + DBG	yes				
ICS	yes				
IIC	yes				
IRQ	yes				
KBI	8 pin				
GPIOs	69	53	39	53	39
RTC	yes				
MTIM	yes				
SCI1	yes				
SCI2	yes				
SPI	yes				
TPM1 channels	2				
TPM2 channels	6				
XOSC	yes				

1 Pin Assignments

This section shows the pin assignments for the MC9S08LG32 series devices. The priority of functions on a pin is in ascending order from left to right and bottom to top. Another view of pinouts and function priority is given in Table 2.

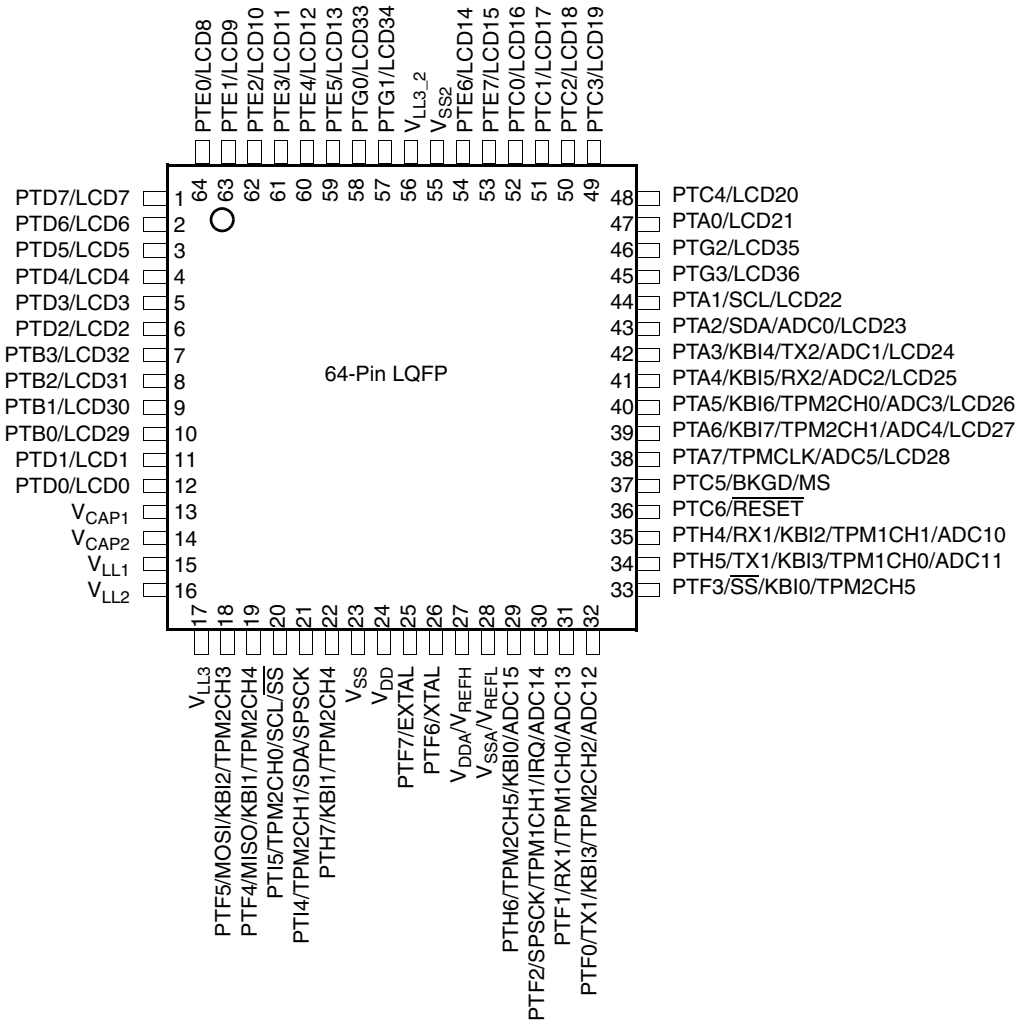


Figure 3. 64-Pin LQFP

NOTE

V_{REFH}/V_{REFL} are internally connected to V_{DDA}/V_{SSA}.

Table 2. Pin Availability by Package Pin-Count

Packages			<-- Lowest **Priority** --> Highest				
80	**64**	**48**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
1	1	1	PTD7	LCD7	—	—	—
2	2	2	PTD6	LCD6	—	—	—
3	3	3	PTD5	LCD5	—	—	—
4	4	4	PTD4	LCD4	—	—	—
5	5	5	PTD3	LCD3	—	—	—
6	6	6	PTD2	LCD2	—	—	—
7	7	—	PTB3	LCD32	—	—	—
8	8	—	PTB2	LCD31	—	—	—
9	—	—	PTB7	LCD40	—	—	—
10	—	—	PTB6	LCD39	—	—	—
11	—	—	PTB5	LCD38	—	—	—
12	—	—	PTB4	LCD37	—	—	—
13	9	—	PTB1	LCD30	—	—	—
14	10	—	PTB0	LCD29	—	—	—
15	11	7	PTD1	LCD1	—	—	—
16	12	8	PTD0	LCD0	—	—	—
17	13	9	V_{CAP1}	—	—	—	—
18	14	10	V_{CAP2}	—	—	—	—
19	15	11	V_{LL1}	—	—	—	—
20	16	12	V_{LL2}	—	—	—	—
21	17	13	V_{LL3}	—	—	—	—
22	18	14	PTF5	MOSI	KBI2	TPM2CH3	—
23	19	15	PTF4	MISO	KBI1	TPM2CH4	—
24	20	—	PTI5	TPM2CH0	SCL	$\overline{SS}$	—
25	21	—	PTI4	TPM2CH1	SDA	SPSCK	—
26	—	—	PTI3	TPM2CH2	MOSI	—	—
27	—	—	PTI2	TPM2CH3	MISO	—	—
28	—	—	PTI1	TMRCLK	TX2	—	—
29	—	—	PTI0	RX2	—	—	—
30	22	—	PTH7	KBI1	TPM2CH4	—	—
31	23	16	V_{SS}	—	—	—	—
32	24	17	V_{DD}	—	—	—	—
33	25	18	PTF7	EXTAL	—	—	—
34	26	19	PTF6	XTAL	—	—	—
35	27	20	V_{DDA}	V_{REFH}	—	—	—
36	28	21	V_{SSA}	V_{REFL}	—	—	—
37	29	—	PTH6	TPM2CH5	KBI0	ADC15	—
38	30	22	PTF2	SPSCK	TPM1CH1	IRQ	ADC14

Table 2. Pin Availability by Package Pin-Count (continued)

Packages			<-- Lowest **Priority** --> Highest				
80	**64**	**48**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
39	31	23	PTF1	RX1	TPM1CH0	ADC13	—
40	32	24	PTF0	TX1	KBI3	TPM2CH2	ADC12
41	33	25	PTF3	$\overline{SS}$	KBI0	TPM2CH5	—
42	34	—	PTH5	TX1	KBI3	TPM1CH0	ADC11
43	35	—	PTH4	RX1	KBI2	TPM1CH1	ADC10
44	—	—	PTH3	KBI7	ADC9	—	—
45	—	—	PTH2	KBI6	ADC8	—	—
46	—	—	PTH1	KBI5	ADC7	—	—
47	—	—	PTH0	KBI4	ADC6	—	—
48	36	26	PTC6	$\overline{RESET}$	—	—	—
49	37	27	PTC5	BKGD/MS	—	—	—
50	38	28	PTA7	TPMCLK	ADC5	LCD28	—
51	39	29	PTA6	KBI7	TPM2CH1	ADC4	LCD27
52	40	30	PTA5	KBI6	TPM2CH0	ADC3	LCD26
53	41	31	PTA4	KBI5	RX2	ADC2	LCD25
54	42	32	PTA3	KBI4	TX2	ADC1	LCD24
55	43	33	PTA2	SDA	ADC0	LCD23	—
56	44	34	PTA1	SCL	LCD22	—	—
57	45	—	PTG3	LCD36	—	—	—
58	46	—	PTG2	LCD35	—	—	—
59	47	35	PTA0	LCD21	—	—	—
60	48	36	PTC4	LCD20	—	—	—
61	49	37	PTC3	LCD19	—	—	—
62	50	38	PTC2	LCD18	—	—	—
63	51	39	PTC1	LCD17	—	—	—
64	52	40	PTC0	LCD16	—	—	—
65	53	41	PTE7	LCD15	—	—	—
66	54	42	PTE6	LCD14	—	—	—
67	55	—	V_{SS2}	—	—	—	—
68	56	—	V_{LL3_2}	—	—	—	—
69	—	—	PTG7	LCD44	—	—	—
70	—	—	PTG6	LCD43	—	—	—
71	—	—	PTG5	LCD42	—	—	—
72	—	—	PTG4	LCD41	—	—	—
73	57	—	PTG1	LCD34	—	—	—
74	58	—	PTG0	LCD33	—	—	—
75	59	43	PTE5	LCD13	—	—	—
76	60	44	PTE4	LCD12	—	—	—

Table 7. ESD and Latch-Up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	2500	—	V
2	Charge device model (CDM)	V_{CDM}	750	—	V
3	Latch-up current at T_A = 85 °C	I_{LAT}	±100	—	mA

1 Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

2.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 8. DC Characteristics

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1	—	Operating Voltage	—	2.7	—	5.5	V
2	P	Output high voltage — Low Drive (PTxDSn = 0) 5 V, I_{Load} = –2 mA 3 V, I_{Load} = –0.6 mA	V_{OH}	 V_{DD} – 0.8 V_{DD} – 0.8	 — —	 — —	V
		Output high voltage — High Drive (PTxDSn = 1) V 5 V, I_{Load} = –10 mA 3 V, I_{Load} = –3 mA		 V_{DD} – 0.8 V_{DD} – 0.8	 — —	 — —	
3	P	Output low voltage — Low Drive (PTxDSn = 0) 5 V, I_{Load} = 2 mA 3 V, I_{Load} = 0.6 mA	V_{OL}	—	 — —	 0.8 0.8	V
		Output low voltage — High Drive (PTxDSn = 1) 5 V, I_{Load} = 10 mA 3 V, I_{Load} = 3 mA			 — —	 0.8 0.8	
4	P	Output high current — Max total I_{OH} for all ports 5 V 3 V	I_{OHT}	—	—	 100 60	mA
5	C	Output high current — Max total I_{OL} for all ports 5 V 3 V	I_{OLT}	—	—	 100 60	mA
6	P	Bandgap voltage reference	V_{BG}	—	1.225	—	V
7	P	Input high voltage; all digital inputs	V_{IH}	0.65 x V_{DD}	—	—	V
8	P	Input low voltage; all digital inputs	V_{IL}	—	—	0.35 x V_{DD}	V
9	P	Input hysteresis; all digital inputs	V_{hys}	0.06 x V_{DD}	—	—	mV
10	P	Input leakage current; input only pins[2] V_{In} = V_{DD} or V_{SS}	$\lvert I_{In} \rvert$	—	0.1	1	μA
11	P	High impedence (off-state) leakage current V_{In} = V_{DD} or V_{SS}	$\lvert I_{OZ} \rvert$	—	0.1	1	μA
12	P	Internal pullup resistors[3]	R_{PU}	20	45	65	kΩ
13	P	Internal pulldown resistors[4]	R_{PD}	20	45	65	kΩ

2.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 9. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
1	C	Run supply current FEI mode, all modules on	RI_{DD}	20 MHz	3	16.38	27.85	mA	–40 °C to 85 °C
	C						28.05		–40 °C to105 °C
	C			1 MHz		1.67	2.84		–40 °C to 85 °C
	C						2.87		–40 °C to105 °C
	P			20 MHz	5	16.55	28.14	mA	–40 °C to 85 °C
	P						28.35		–40 °C to105 °C
	C			1 MHz		1.77	3.01		–40 °C to 85 °C
	C						3.05		–40 °C to105 °C
2	T	Run supply current FEI mode, all modules off	RI_{DD}	20 MHz	3	11.9	20.25	mA	–40 °C to 85 °C
	T						21.72		–40 °C to105 °C
	T			1 MHz		1.16	1.95		–40 °C to 85 °C
	T						1.98		–40 °C to105 °C
	T			20 MHz	5	12.68	21.56	mA	–40 °C to 85 °C
	T						23.12		–40 °C to105 °C
	T			1 MHz		1.4	2.39		–40 °C to 85 °C
	T						2.41		–40 °C to105 °C
3	T	Wait mode supply current FEI mode, all modules off	WI_{DD}	20 MHz	3	7.9	13.42	mA	–40 °C to 85 °C
	T						13.59		–40 °C to105 °C
	T			1 MHz		0.88	1.49		–40 °C to 85 °C
	T						1.51		–40 °C to105 °C
	P			20 MHz	5	8.13	13.81	mA	–40 °C to 85 °C
	P						13.98		–40 °C to105 °C
	T			1 MHz		1.12	1.91		–40 °C to 85 °C
	T						1.94		–40 °C to105 °C
4	C	Stop2 mode supply current	$S2I_{DD}$	n/a	3	1.1	16.0	µA	–40 °C to 85 °C
	C						39.0		–40 °C to105 °C
	P				5	1.2	18.7	µA	–40 °C to 85 °C
	P						46.1		–40 °C to105 °C
5	C	Stop3 mode supply current No clocks active	$S3I_{DD}$	n/a	3	1.2	22.4	µA	–40 °C to 85 °C
	C						56.2		–40 °C to105 °C
	P				5	1.32	25.5	µA	–40 °C to 85 °C
	P						63.9		–40 °C to105 °C

Table 12. 12-bit ADC Operating Conditions (continued)

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Input Resistance	—	R_{ADIN}	—	5	7	kΩ	—
Analog Source Resistance	12-bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz	R_{AS}	 — —	 — —	 2 5	kΩ	External to MCU
	10-bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz		 — —	 — —	 5 10		
	8-bit mode (all valid f_{ADCK})		—	—	10		
ADC Conversion Clock Freq.	High Speed (ADLPC = 0)	f_{ADCK}	0.4	—	8.0	MHz	—
	Low Power (ADLPC = 1)		0.4	—	4.0		

1 Typical values assume V_{DDAD} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

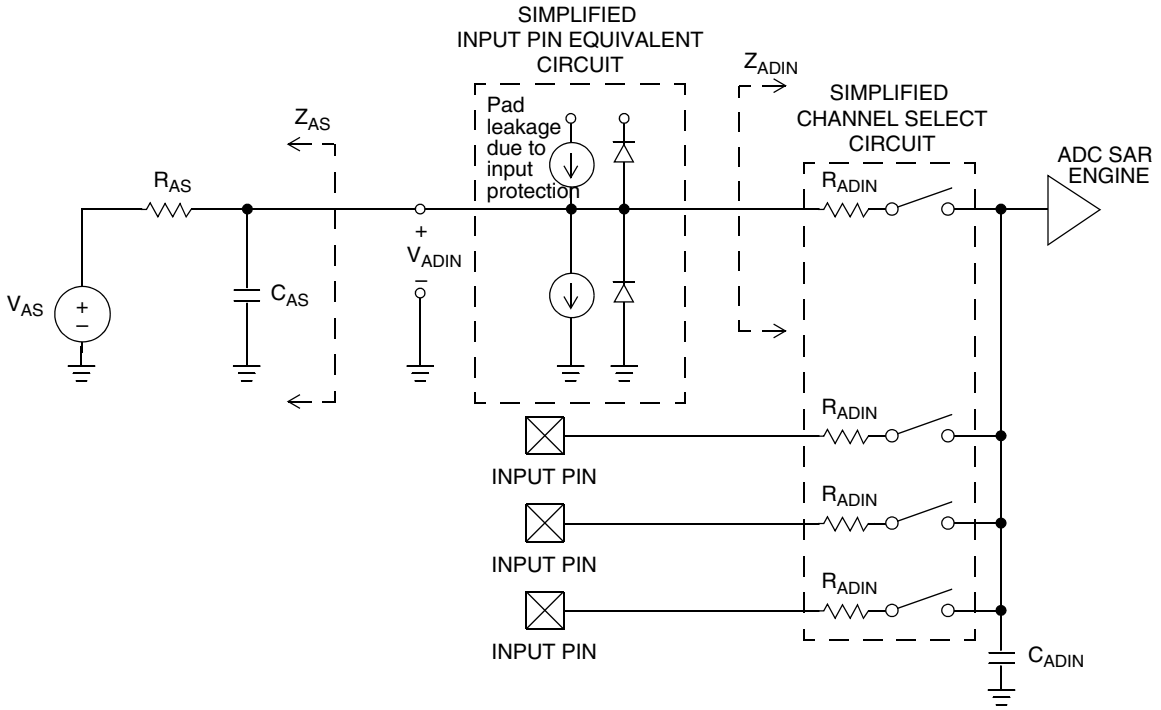


Figure 18. ADC Input Impedance Equivalency Diagram

Table 13. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD}) (continued)

Num	C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
13	T	Full-Scale Error	12-bit mode	E_{FS}	—	±1	—	LSB[2]	V_{ADIN} = V_{DDAD}
	P		10-bit mode		—	±0.5	±1		
	T		8-bit mode		—	±0.5	±0.5		
14	D	Quantization Error	12-bit mode	E_Q	—	–1 to 0	—	LSB[2]	—
			10-bit mode		—	—	±0.5		
			8-bit mode		—	—	±0.5		
15	D	Input Leakage Error	12-bit mode	E_{IL}	—	±1	—	LSB[2]	Pad leakage[4] * R_{AS}
			10-bit mode		—	±0.2	±2.5		
			8-bit mode		—	±0.1	±1		
16	C	Temp Sensor Slope	–40 °C to 25 °C	m	—	1.646	—	mV/°C	—
			25 °C to 125°C		—	1.769	—		
17	C	Temp Sensor Voltage	25 °C	V_{TEMP25}	—	701.2	—	mV	—

1 Typical values assume V_{DDAD} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

3 Monotonicity and no-missing-codes guaranteed in 10-bit and 8-bit modes

4 Based on input pad leakage current. Refer to pad electricals.

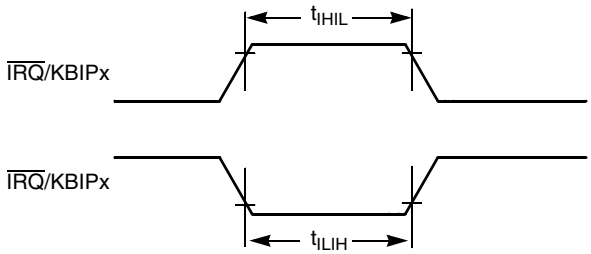


Figure 20. IRQ/KBIPx Timing

2.11.2 TPM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 15. TPM Input Timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

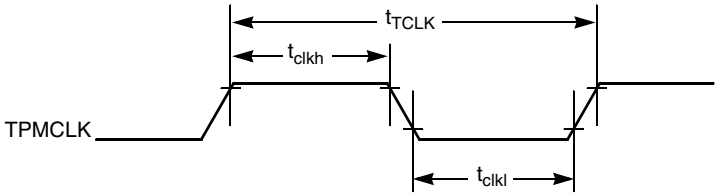


Figure 21. Timer External Clock

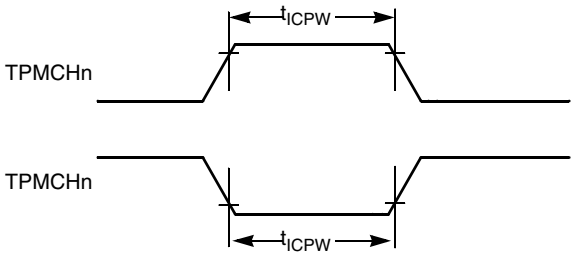


Figure 22. Timer Input Capture Pulse

2.11.3 SPI Timing

Table 16 and Figure 23 through Figure 26 describe the timing requirements for the SPI system.

Table 16. SPI Timing

No.	C	Function	Symbol	Min	Max	Unit
—	D	Operating frequency Master Slave	f_{op}	 $f_{Bus}/2048$ 0	 $f_{Bus}/2$ $f_{Bus}/4$	Hz
①	D	SPSCK period Master Slave	t_{SPSCK}	 2 4	 2048 —	 t_{cyc} t_{cyc}
②	D	Enable lead time Master Slave	t_{Lead}	 1/2 1	 — —	 t_{SPSCK} t_{cyc}
③	D	Enable lag time Master Slave	t_{Lag}	 1/2 1	 — —	 t_{SPSCK} t_{cyc}
④	D	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	 $t_{cyc} - 30$ $t_{cyc} - 30$	 1024 t_{cyc} —	 ns ns
⑤	D	Data setup time (inputs) Master Slave	t_{SU}	 15 15	 — —	 ns ns
⑥	D	Data hold time (inputs) Master Slave	t_{HI}	 0 25	 — —	 ns ns
⑦	D	Slave access time	t_a	—	1	t_{cyc}
⑧	D	Slave MISO disable time	t_{dis}	—	1	t_{cyc}
⑨	D	Data valid (after SPSCK edge) Master Slave	t_v	 — —	 25 25	 ns ns
⑩	D	Data hold time (outputs) Master Slave	t_{HO}	 0 0	 — —	 ns ns
⑪	D	Rise time Input Output	 t_{RI} t_{RO}	 — —	 $t_{cyc} - 25$ 25	 ns ns
⑫	D	Fall time Input Output	 t_{FI} t_{FO}	 — —	 $t_{cyc} - 25$ 25	 ns ns

2.12 LCD Specifications

Table 17. LCD Electricals, 3 V Glass

C	Characteristic	Symbol	Min	Typ	Max	Units
D	VLL3 Supply Voltage	VLL3	2.7	—	5.5	V
D	LCD Frame Frequency	f_{Frame}	28	30	64	Hz
D	LCD Charge Pump Capacitance	C_{LCD}	—	100	100	pF
D	LCD Bypass Capacitance	C_{BYLCD}	—	100	100	
D	LCD Glass Capacitance	C_{glass}	—	2000	8000	

2.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section.

Table 18. Flash Characteristics

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage for program/erase –40 °C to 85 °C	$V_{prog/erase}$	2.7		5.5	V
D	Supply voltage for read operation	V_{Read}	2.7		5.5	V
D	Internal FCLK frequency[1]	f_{FCLK}	150		200	kHz
D	Internal FCLK period (1/FCLK)	t_{Fcyc}	5		6.67	µs
C	Byte program time (random location)[2]	t_{prog}	9			t_{Fcyc}
C	Byte program time (burst mode)[2]	t_{Burst}	4			t_{Fcyc}
C	Page erase time[2]	t_{Page}	4000			t_{Fcyc}
C	Mass erase time[2]	t_{Mass}	20,000			t_{Fcyc}
D	Byte program current[3]	R_{IDDBP}	—	4	—	mA
D	Page erase current[3]	R_{IDDPE}	—	6	—	mA
C	Program/erase endurance[4] T_L to T_H = –40 °C to + 85 °C T = 25 °C		10,000	— 100,000	— —	cycles
C	Data retention[5]	t_{D_ret}	15	100	—	years

1 The frequency of this clock is controlled by a software setting.

2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

3 The program and erase currents are additional to the standard run I_{DD}. These values are measured at room temperatures with V_{DD} = 5.0 V, bus frequency = 4.0 MHz.

4 **Typical endurance for flash** was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to *Engineering Bulletin EB619, Typical Endurance for Nonvolatile Memory.*

5 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25 °C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to *Engineering Bulletin EB618, Typical Data Retention for Nonvolatile Memory.*

2.14 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

2.14.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East).

The maximum radiated RF emissions of the tested configuration in all orientations are less than or equal to the reported emissions levels.

Table 19. Radiated Emissions, Electric Field

Parameter	Symbol	Conditions	Frequency	f_{OSC}/f_{BUS}	Level[1] (Max)	Unit
Radiated emissions, electric field	V_{RE_TEM}	V_{DD} = 5.5 T_A = +25 °C Package type = 80 LQFP	0.15 – 50 MHz	4 MHz crystal 16 MHz bus	10	dBμV
			50 – 150 MHz		14	
			150 – 500 MHz		8	
			500 – 1000 MHz		5	
			IEC Level		L	—
			SAE Level		2	—

1 Data based on qualification test results.

2.14.2 Conducted Transient Susceptibility

Microcontroller transient conducted susceptibility is measured in accordance with an internal Freescale test method. The measurement is performed with the microcontroller installed on a custom EMC evaluation board and running specialized EMC test software designed in compliance with the test method. The conducted susceptibility is determined by injecting the transient susceptibility signal on each pin of the microcontroller. The transient waveform and injection methodology is based on IEC 61000-4-4 (EFT/B). The transient voltage required to cause performance degradation on any pin in the tested configuration is greater than or equal to the reported levels unless otherwise indicated by footnotes below Table 20.

Table 20. Conducted Susceptibility, EFT/B

Parameter	Symbol	Conditions	f_{OSC}/f_{BUS}	Result	Amplitude[1] (Min)	Unit
Conducted susceptibility, electrical fast transient/burst (EFT/B)	V_{CS_EFT}	V_{DD} = 5.5 T_A = +25 °C Package type = 80-pin LQFP	4 kHz crystal 4 MHz bus	A B C D	>4.0[2] >4.0[3] >4.0[4] >4.0	kV

1 Data based on qualification test results. Not tested in production.

2 Exceptions as covered in footnotes 3 and 4.

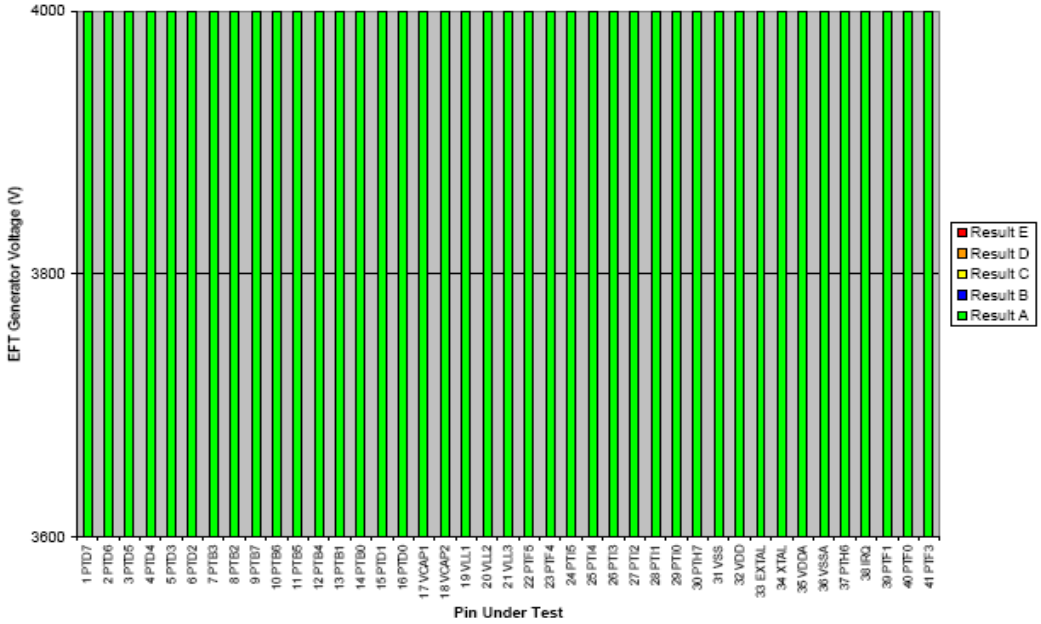
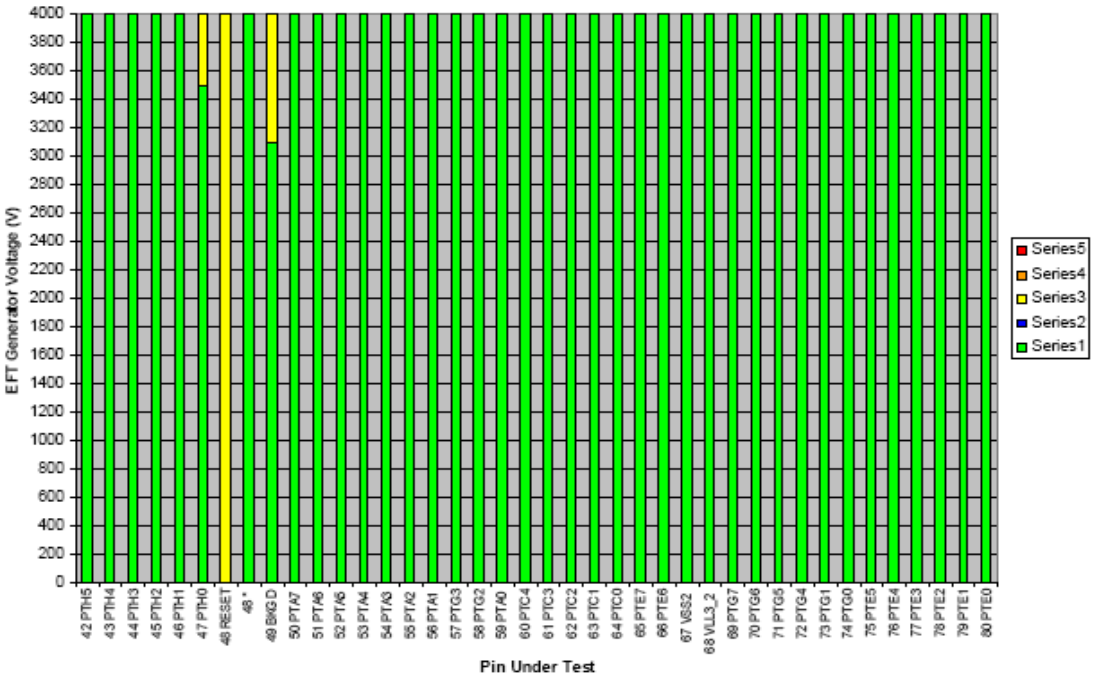


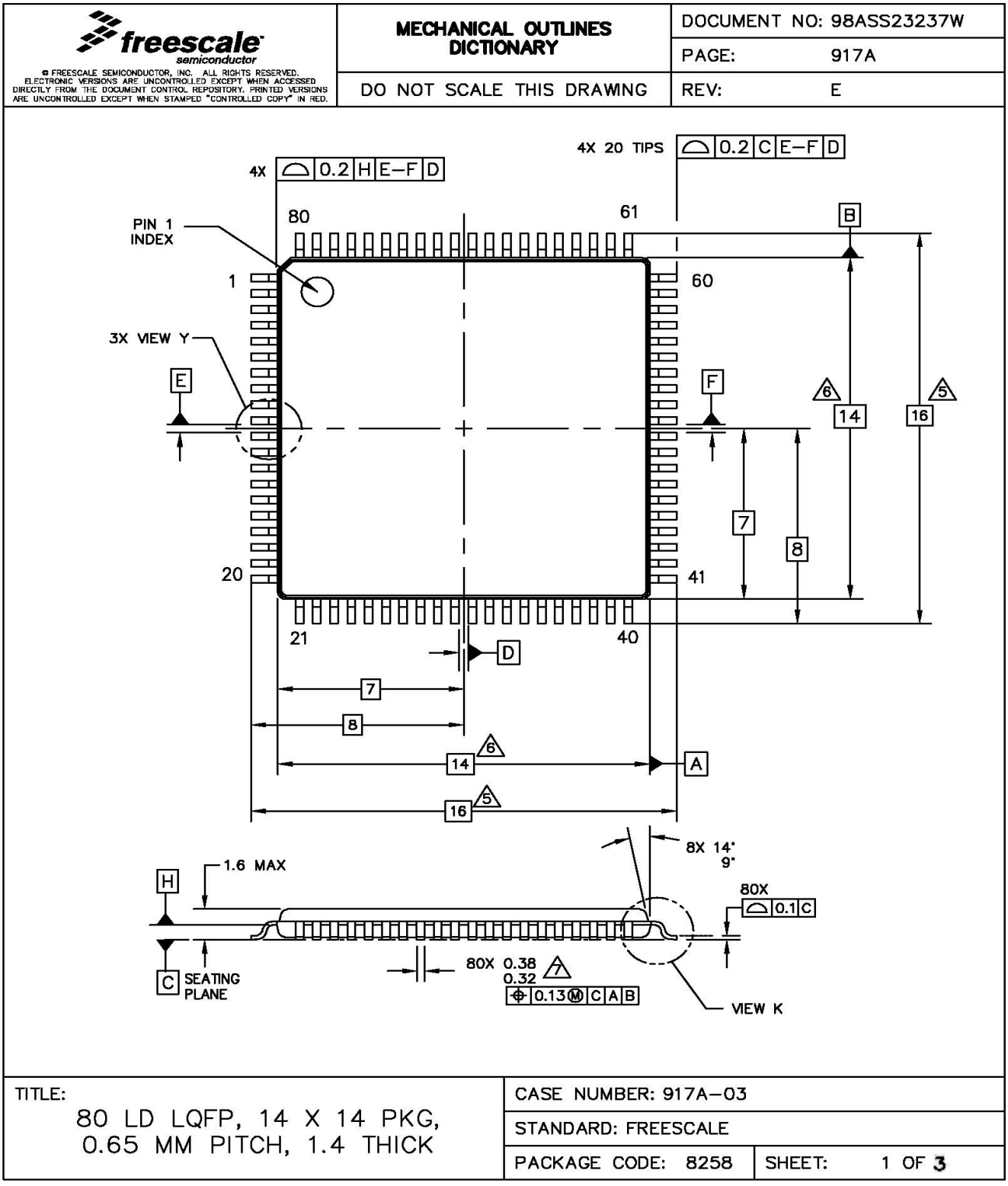
Figure 29. 4 MHz, Negative Polarity Pins 1 – 41



Note:
RESET retested with 0.1 μF capacitor from pin to ground is Class A compliant as shown by 48*.

Figure 30. 4 MHz, Negative Polarity Pins 42 – 80

4.1.1 80-pin LQFP



freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23237W
		PAGE: 917A
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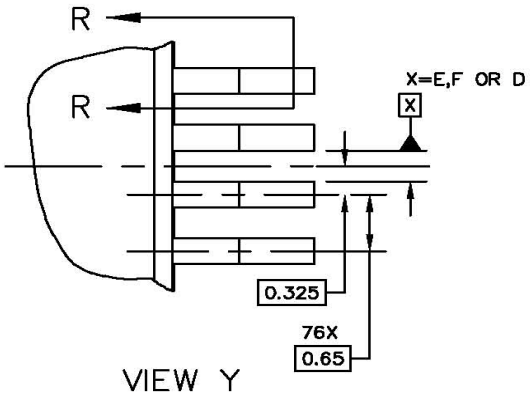
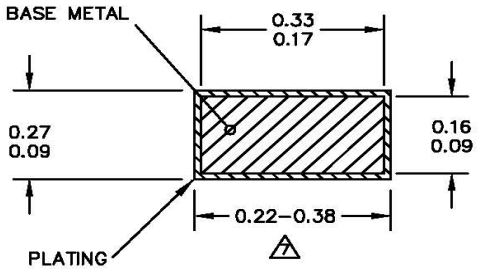
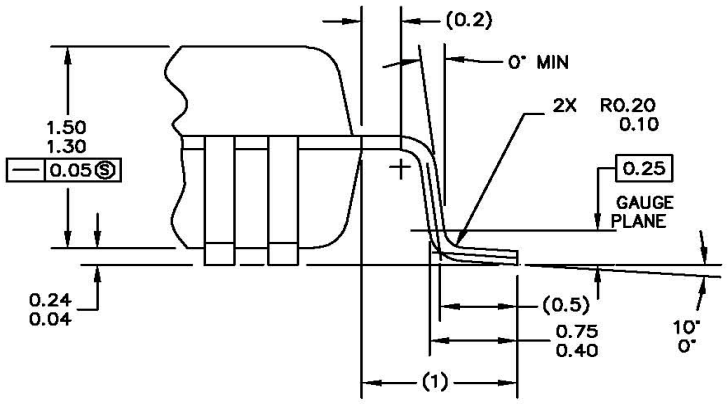


VIEW Y



SECTION R–R
ROTATED 90° CW



VIEW K

TITLE: 80 LD LQFP, 14 X 14 PKG, 0.65 MM PITCH, 1.4 THICK	CASE NUMBER: 917A–03	
	STANDARD: FREESCALE	
	PACKAGE CODE: 8258	SHEET: 2 OF 3

freescale semiconductor

MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23234W
	PAGE: 840F
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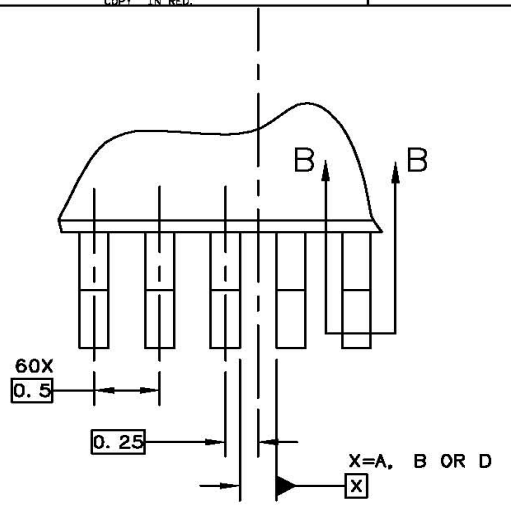
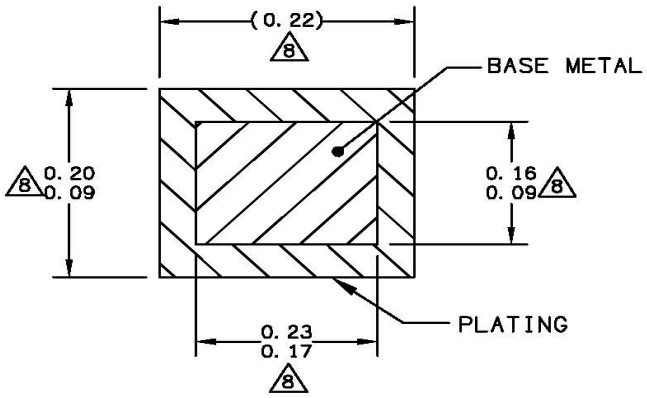
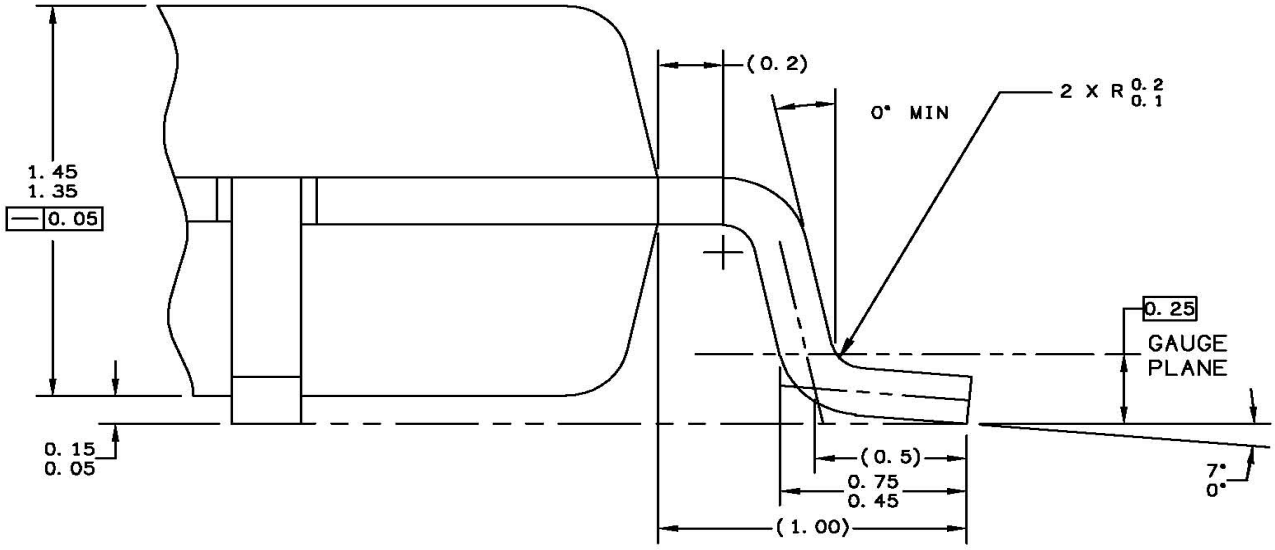


VIEW Y



SECTION B–B



VIEW AA

TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	CASE NUMBER: 840F–02	
	STANDARD: JEDEC MS–026 BCD	
	PACKAGE CODE: 8426	SHEET: 2 OF 3

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23234W
		PAGE: 840F
	DO NOT SCALE THIS DRAWING	REV: E

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.

TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	CASE NUMBER: 840F–02	
	STANDARD: JEDEC MS–026 BCD	
	PACKAGE CODE: 8426	SHEET: 3 OF 3

Figure 34. 64-pin LQFP Package Drawing (Case 840F, Doc #98ASS23234W)

5 Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web are the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://www.freescale.com

The following revision history table summarizes changes contained in this document.

Table 24. Revision History

Revision	Date	Description of Changes
1	8/2008	First Initial release.
2	9/2008	Second Initial Release.
3	11/2008	Alpha Customer Release.
4	2/2009	Launch Release.
5	4/2009	Added EMC Radiated Emission and Transient Susceptibility data in Table 19 and Table 20.
6	4/2009	Updated EMC performance data.
7	8/2009	Updated auto part numbers, changed TCLK, T0CH0, T0CH1, T1CH0, T1CH1, T1CH2, T1CH3, T1CH3, T1CH4, and T1CH5 to TPMCLK, TPM0CH0, TPM0CH1,TPM1CH0, TPM1CH1, TPM1CH2, TPM1CH3, TPM1CH4, and TPM1CH5, and changed the maximum LCD frame frequency to 64 Hz.
8	8/2011	Updated Table “ICS Frequency Specifications (Temperature Range = –40 ×C to 105 ×C Ambient)”. Changed the value of row 8 column C from C to P.
9	9/2011	Updated Table “ICS Frequency Specifications (Temperature Range = –40 ×C to 105 ×C Ambient)”. Removed Footnote from Row 8. Updated the Revision History