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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	69
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.9K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9s08lg32j0vlk

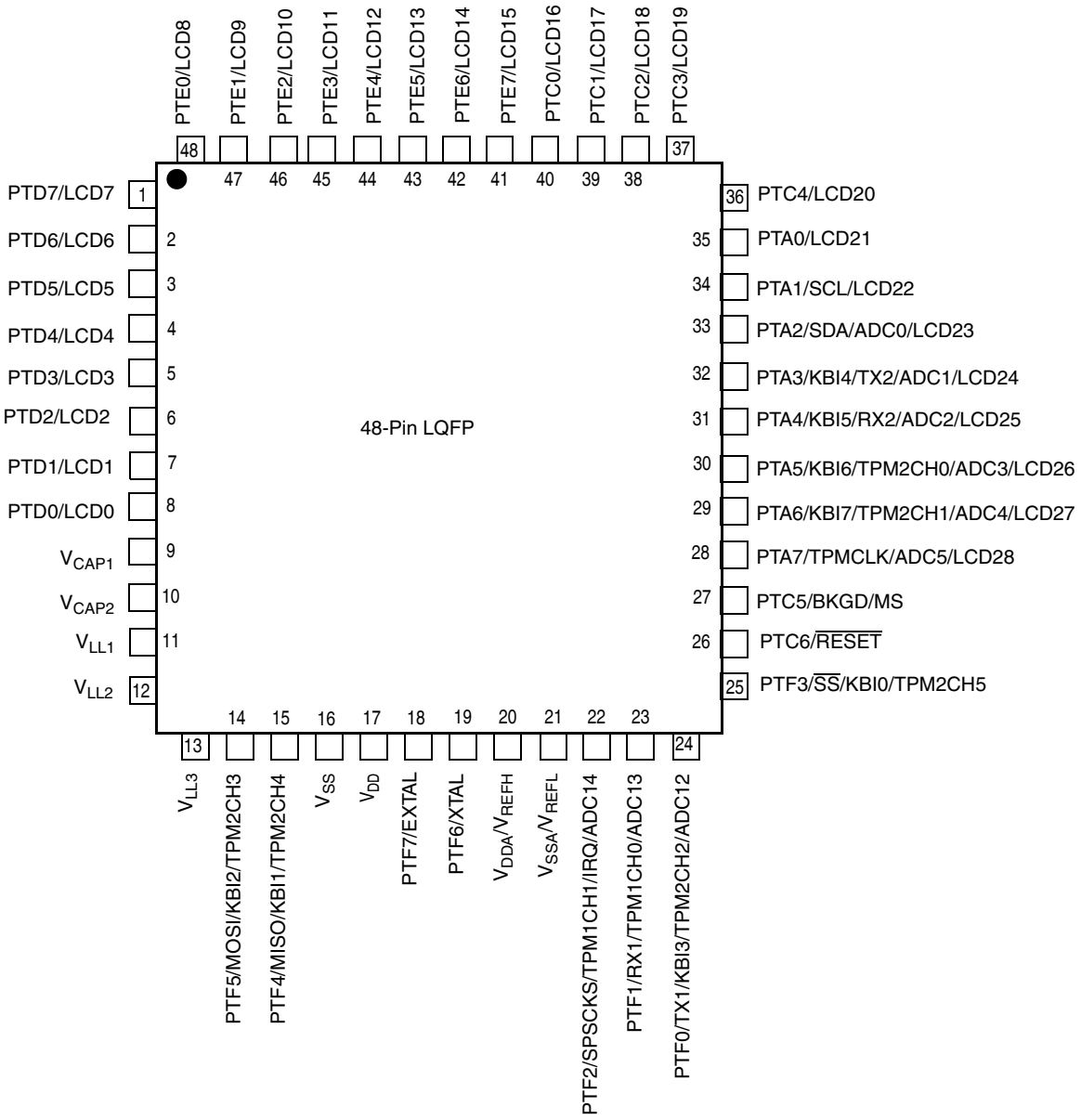


Figure 4. 48-Pin LQFP

NOTE

V_{REFH}/V_{REFL} are internally connected to V_{DDA}/V_{SSA}.

Table 2. Pin Availability by Package Pin-Count

Packages			<-- Lowest **Priority** --> Highest				
80	**64**	**48**	**Port Pin**	**Alt 1**	**Alt 2**	**Alt 3**	**Alt 4**
1	1	1	PTD7	LCD7	—	—	—
2	2	2	PTD6	LCD6	—	—	—
3	3	3	PTD5	LCD5	—	—	—
4	4	4	PTD4	LCD4	—	—	—
5	5	5	PTD3	LCD3	—	—	—
6	6	6	PTD2	LCD2	—	—	—
7	7	—	PTB3	LCD32	—	—	—
8	8	—	PTB2	LCD31	—	—	—
9	—	—	PTB7	LCD40	—	—	—
10	—	—	PTB6	LCD39	—	—	—
11	—	—	PTB5	LCD38	—	—	—
12	—	—	PTB4	LCD37	—	—	—
13	9	—	PTB1	LCD30	—	—	—
14	10	—	PTB0	LCD29	—	—	—
15	11	7	PTD1	LCD1	—	—	—
16	12	8	PTD0	LCD0	—	—	—
17	13	9	V_{CAP1}	—	—	—	—
18	14	10	V_{CAP2}	—	—	—	—
19	15	11	V_{LL1}	—	—	—	—
20	16	12	V_{LL2}	—	—	—	—
21	17	13	V_{LL3}	—	—	—	—
22	18	14	PTF5	MOSI	KBI2	TPM2CH3	—
23	19	15	PTF4	MISO	KBI1	TPM2CH4	—
24	20	—	PTI5	TPM2CH0	SCL	$\overline{SS}$	—
25	21	—	PTI4	TPM2CH1	SDA	SPSCK	—
26	—	—	PTI3	TPM2CH2	MOSI	—	—
27	—	—	PTI2	TPM2CH3	MISO	—	—
28	—	—	PTI1	TMRCLK	TX2	—	—
29	—	—	PTI0	RX2	—	—	—
30	22	—	PTH7	KBI1	TPM2CH4	—	—
31	23	16	V_{SS}	—	—	—	—
32	24	17	V_{DD}	—	—	—	—
33	25	18	PTF7	EXTAL	—	—	—
34	26	19	PTF6	XTAL	—	—	—
35	27	20	V_{DDA}	V_{REFH}	—	—	—
36	28	21	V_{SSA}	V_{REFL}	—	—	—
37	29	—	PTH6	TPM2CH5	KBI0	ADC15	—
38	30	22	PTF2	SPSCK	TPM1CH1	IRQ	ADC14

2.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 9. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
1	C	Run supply current FEI mode, all modules on	RI_{DD}	20 MHz	3	16.38	27.85	mA	–40 °C to 85 °C
	C						28.05		–40 °C to105 °C
	C			1 MHz		1.67	2.84		–40 °C to 85 °C
	C						2.87		–40 °C to105 °C
	P			20 MHz	5	16.55	28.14	mA	–40 °C to 85 °C
	P						28.35		–40 °C to105 °C
	C			1 MHz		1.77	3.01		–40 °C to 85 °C
	C						3.05		–40 °C to105 °C
2	T	Run supply current FEI mode, all modules off	RI_{DD}	20 MHz	3	11.9	20.25	mA	–40 °C to 85 °C
	T						21.72		–40 °C to105 °C
	T			1 MHz		1.16	1.95		–40 °C to 85 °C
	T						1.98		–40 °C to105 °C
	T			20 MHz	5	12.68	21.56	mA	–40 °C to 85 °C
	T						23.12		–40 °C to105 °C
	T			1 MHz		1.4	2.39		–40 °C to 85 °C
	T						2.41		–40 °C to105 °C
3	T	Wait mode supply current FEI mode, all modules off	WI_{DD}	20 MHz	3	7.9	13.42	mA	–40 °C to 85 °C
	T						13.59		–40 °C to105 °C
	T			1 MHz		0.88	1.49		–40 °C to 85 °C
	T						1.51		–40 °C to105 °C
	P			20 MHz	5	8.13	13.81	mA	–40 °C to 85 °C
	P						13.98		–40 °C to105 °C
	T			1 MHz		1.12	1.91		–40 °C to 85 °C
	T						1.94		–40 °C to105 °C
4	C	Stop2 mode supply current	$S2I_{DD}$	n/a	3	1.1	16.0	µA	–40 °C to 85 °C
	C						39.0		–40 °C to105 °C
	P				5	1.2	18.7	µA	–40 °C to 85 °C
	P						46.1		–40 °C to105 °C
5	C	Stop3 mode supply current No clocks active	$S3I_{DD}$	n/a	3	1.2	22.4	µA	–40 °C to 85 °C
	C						56.2		–40 °C to105 °C
	P				5	1.32	25.5	µA	–40 °C to 85 °C
	P						63.9		–40 °C to105 °C

Table 9. Supply Current Characteristics (continued)

Num	C	Parameter		Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
6	T	Stop2 adders:	RTC using LPO	—	n/a	3	210	—	nA	–40 °C to 105 °C
			RTC using low power crystal oscillator				4.25	—	µA	
			LCD[2] with rbias (Low Gain)				1.2[3]	—		
			LCD[2] with rbias (High Gain)				18[4]	—		
			LCD[2] with Cpump				4.05[3]	—		–40 °C to 85 °C
			RTC using LPO			5	210	—	nA	–40 °C to 105 °C
			RTC using low power crystal oscillator				4.22	—	µA	
			LCD[2] with rbias (Low Gain)				1.5[3]	—		
			LCD[2] with rbias (High Gain)				32[4]	—		
			LCD[2] with Cpump				7.12[3]	—		–40 °C to 85 °C
7	T	Stop3 adders:	RTC using LPO	—	n/a	3	210	—	nA	–40 °C to 105 °C
			RTC using low power crystal oscillator				4.75	—	µA	
			LCD[2] with rbias (Low Gain)				1.2[3]	—		
			LCD[2] with rbias (High Gain)				18[4]	—		
			LCD[2] with Cpump				4.35[3]	—		–40 °C to 85 °C
			RTC using LPO			5	230	—	nA	–40 °C to 105 °C
			RTC using low power crystal oscillator				4.74	—	µA	
			LCD[2] with rbias (Low Gain)				1.5[3]	—		
			LCD[2] with rbias (High Gain)				32[4]	—		
			LCD[2] with Cpump				7.49[3]	—		–40 °C to 85 °C

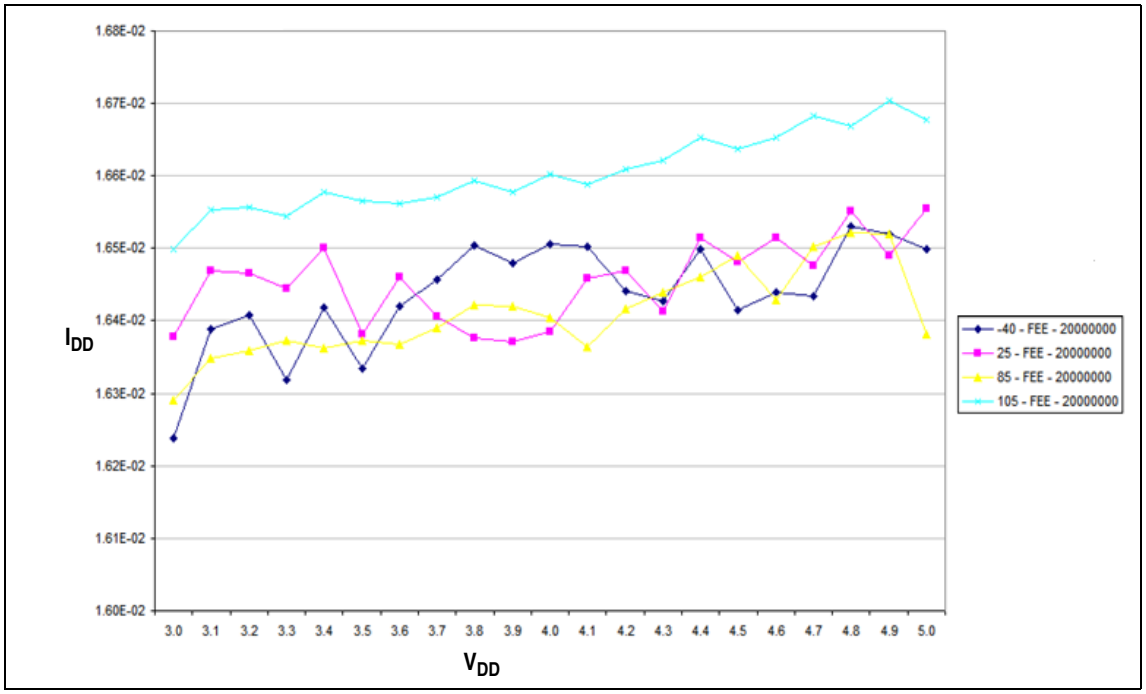


Figure 12. Typical Run I_{DD} for FEE Mode at 20 MHz

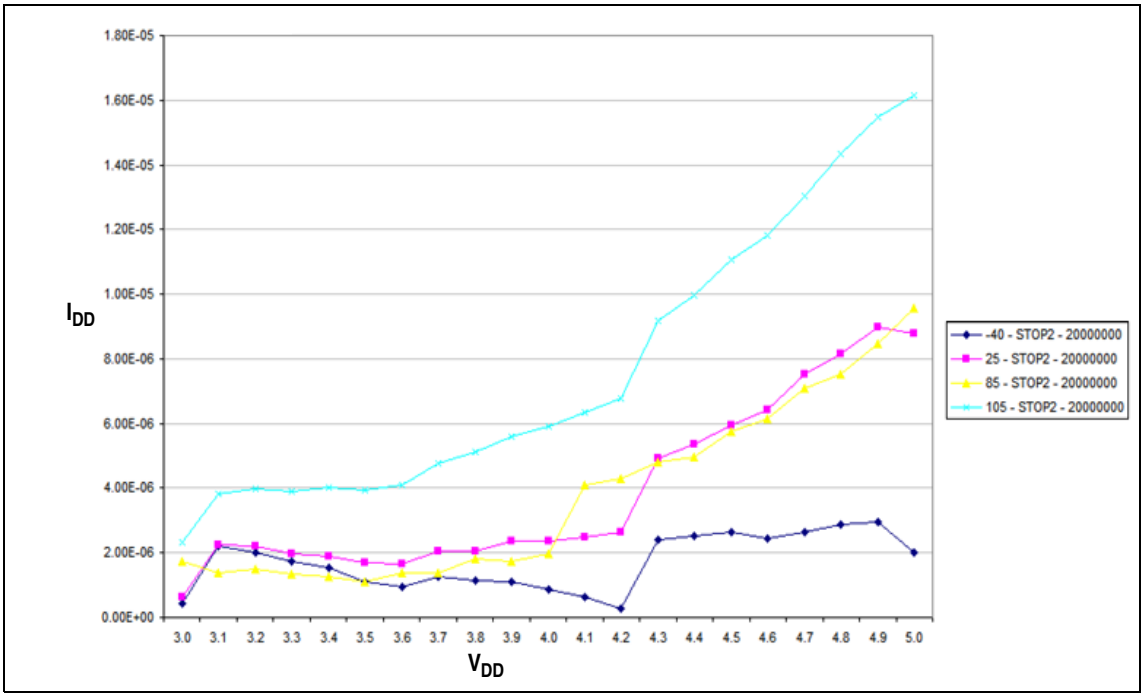


Figure 13. Typical Stop2 I_{DD}

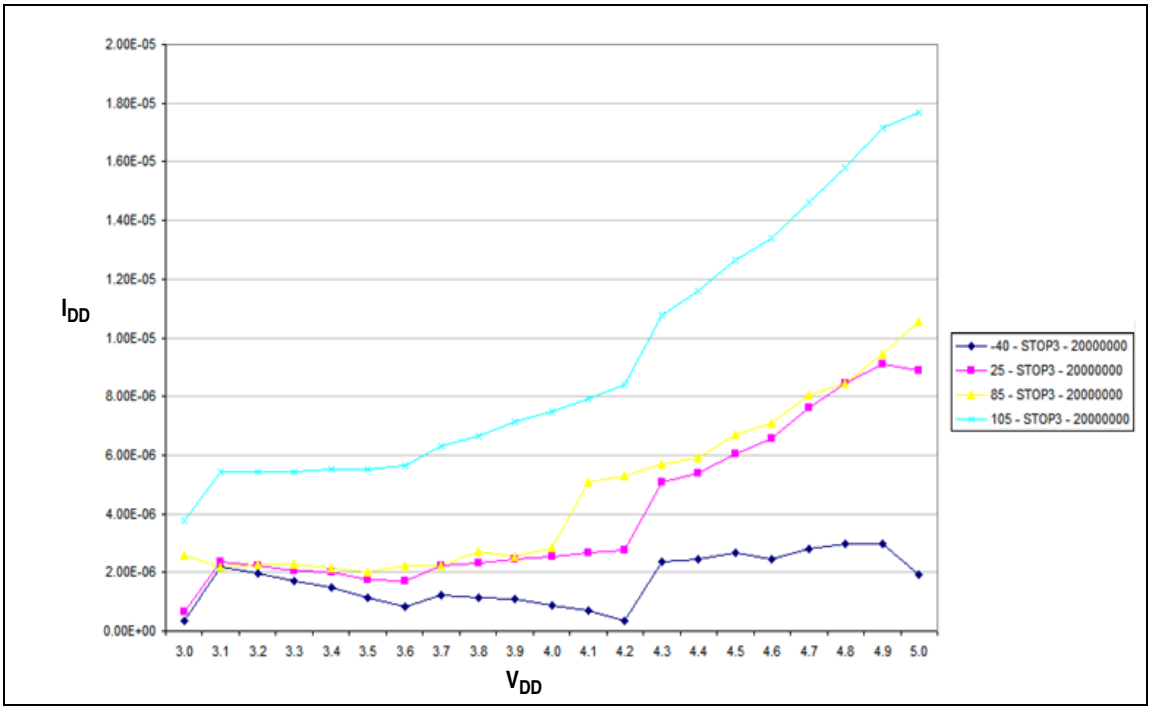


Figure 14. Typical Stop3 I_{DD}

2.8 External Oscillator (XOSC) Characteristics

Table 10. Oscillator Electrical Specifications (Temperature Range = –40 °C to 105 °C Ambient)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1	D	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) • Low range (RANGE = 0) • High range (RANGE = 1) FEE or FBE mode[2] • High range (RANGE = 1, HGO = 1) BLPE mode • High range (RANGE = 1, HGO = 0) BLPE mode	 f_{lo} f_{hi} f_{hi-hgo} f_{hi-lp}	 32 1 1 1	 — — — —	 38.4 5 16 8	 kHz MHz MHz MHz
2	D	Load capacitors	C_1 C_2	See crystal or resonator manufacturer's recommendation.			

Table 10. Oscillator Electrical Specifications (Temperature Range = –40 °C to 105 °C Ambient) (continued)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
3	D	Feedback resistor • Low range (32 kHz to 100 kHz) • High range (1 MHz to 16 MHz)	R_F	 — —	 10 1	 — —	MΩ
4	D	Series resistor • Low range, low gain (RANGE = 0, HGO = 0) • Low range, high gain (RANGE = 0, HGO = 1)	R_S		 0 100		kΩ
5	D	Series resistor • High range, low gain (RANGE = 1, HGO = 0) • High range, high gain (RANGE = 1, HGO = 1) ≥8 MHz 4 MHz 1 MHz	R_S	 — — —	 0 0 0	 0 10 20	kΩ
6	T	Crystal start-up time[3, 4] • Low range (HGO = 0) • Low range (HGO = 1) • High range (HG0 = 0)[5] • High range (HG0 = 1)[5]	 $t_{CSTL-LP}$ $t_{CSTL-HGO}$ $t_{CSTH-LP}$ $t_{CSTH-HGO}$	 — — — —	 500 3570 4 4	 — — — —	ms
7	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) • FEE or FBE mode[2] • BLPE mode	f_{extal}	 0.03125 0	 — —	 5 40	MHz

1 Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.

2 When ICS is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

3 This parameter is characterized and not tested on each device.

4 Proper PC board layout procedures must be followed to achieve specifications.

5 4 MHz crystal

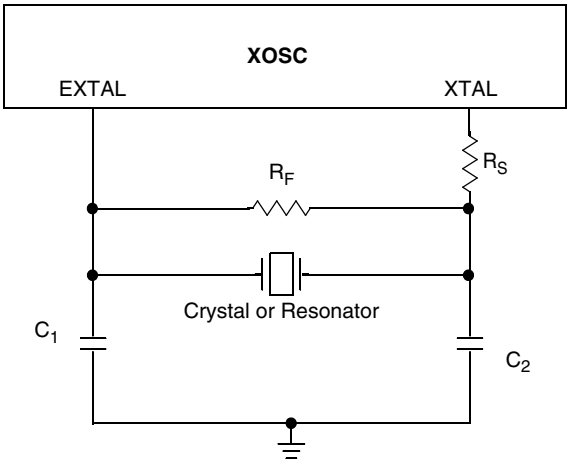


Figure 15. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

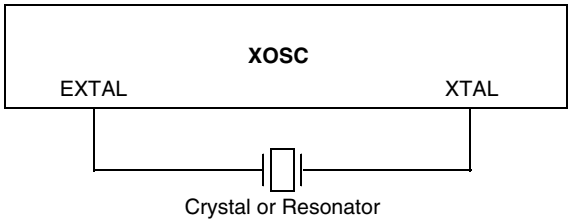


Figure 16. Typical Crystal or Resonator Circuit: Low Range/Low Power

2.9 Internal Clock Source (ICS) Characteristics

Table 11. ICS Frequency Specifications (Temperature Range = –40 °C to 105 °C Ambient)

Num	C	Characteristic		Symbol	Min	Typ[1]	Max	Unit
1	P	Average internal reference frequency — factory trimmed at VDD = 5.0 V and temperature = 25 °C		f_{int_ft}	—	32.768	—	kHz
2	C	Average internal reference frequency — user trimmed		f_{int_t}	31.25	—	39.0625	kHz
3	C	Internal reference start-up time		t_{IRST}	—	60	100	µs
4	P	DCO output frequency range — trimmed[2]	Low range (DRS = 00)	f_{dco_t}	16	—	20	MHz
	P		Mid range (DRS = 01)		32	—	40	
5	P	DCO output frequency[2] Reference = 32768 Hz and DMX32 = 1	Low range (DRS = 00)	f_{dco_DMX32}	—	19.92	—	MHz
	P		Mid range (DRS = 01)		—	39.85	—	
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)[3]		$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	$\%f_{dco}$
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)[3]		$\Delta f_{dco\_res\_t}$	—	±0.2	±0.4	$\%f_{dco}$
8	P	Total deviation of trimmed DCO output frequency over voltage and temperature		Δf_{dco_t}	—	–1.0 to +0.5	±2	$\%f_{dco}$
9	C	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0 °C to 70 °C[3]		Δf_{dco_t}	—	±0.5	±1	$\%f_{dco}$
10	C	FLL acquisition time[3, 4]		$t_{Acquire}$	—	—	1	mS
11	C	Long term jitter of DCO output clock (averaged over 2 ms interval)[5]		C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1 Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.

2 The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

3 This parameter is characterized and not tested on each device.

4 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

5 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in the crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

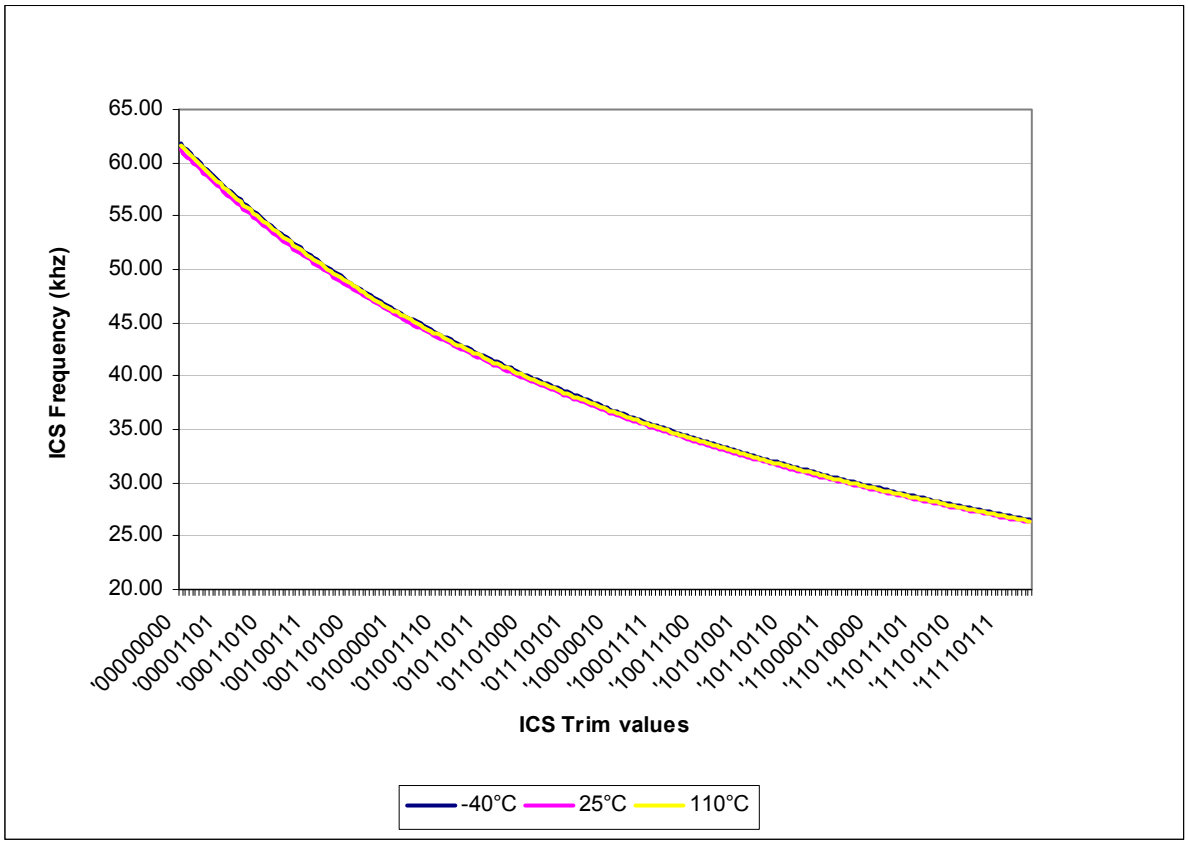


Figure 17. Internal Oscillator Deviation from Trimmed Frequency

2.10 ADC Characteristics

Table 12. 12-bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDAD}	2.7	—	5.5	V	—
	Delta to V_{DD} ($V_{DD} - V_{DDAD}$)[2]	ΔV_{DDAD}	–100	0	+100	mV	—
Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSAD}$)[2]	ΔV_{SSAD}	–100	0	+100	mV	—
Ref Voltage High	—	V_{REFH}	—	—	—	V	V_{REFH} shorted to V_{DDAD}
Ref Voltage Low	—	V_{REFL}	—	—	—	V	V_{REFL} shorted to V_{SSAD}
Input Voltage	—	V_{ADIN}	V_{REFL}	—	V_{REFH}	V	—
Input Capacitance	—	C_{ADIN}	—	4.5	5.5	pF	—

Table 13. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD})

Num	C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
1	T	Supply Current ADLPC = 1 ADLSMP = 1 ADCO = 1	—	I_{DDAD}	—	195	—	µA	—
2	T	Supply Current ADLPC = 1 ADLSMP = 0 ADCO = 1	—	I_{DDAD}	—	347	—	µA	—
3	T	Supply Current ADLPC = 0 ADLSMP = 1 ADCO = 1	—	I_{DDAD}	—	407	—	µA	—
4	P	Supply Current ADLPC = 0 ADLSMP = 0 ADCO = 1	—	I_{DDAD}	—	0.755	1	mA	—
5	—	Supply Current	Stop, Reset, Module Off	IDDAD		0.011	1	µA	—
6	P	ADC Asynchronous Clock Source	High Speed (ADLPC=0)	f_{ADACK}	2	3.3	5	MHz	t_{ADACK} = $1/f_{ADACK}$
			Low Power (ADLPC=1)		1.25	2	3.3		
7	C	Conversion Time (Including sample time)	Short sample (ADLSMP=0)	t_{ADC}	—	20	—	ADCK cycles	See *ADC chapter in the LG32 Reference Manual* for conversion time variances
			Long sample (ADLSMP=1)		—	40	—		
8	C	Sample Time	Short sample (ADLSMP=0)	t_{ADS}	—	3.5	—	ADCK cycles	
			Long sample (ADLSMP=1)		—	23.5	—		
9	T	Total Unadjusted Error	12-bit mode	E_{TUE}	—	±3.0	—	LSB^2	Includes quantization
	P		10-bit mode		—	±1	±2.5		
	T		8-bit mode		—	±0.5	±1		
10	T	Differential Non-Linearity	12-bit mode	DNL	—	±1.75	—	LSB^2	
	P		10-bit mode[3]		—	±0.5	±1.0		
	T		8-bit mode[3]		—	±0.3	±0.5		
11	T	Integral Non-Linearity	12-bit mode	INL	—	±1.5	—	LSB^2	
	P		10-bit mode		—	±0.5	±1		
	T		8-bit mode		—	±0.3	±0.5		
12	T	Zero-Scale Error	12-bit mode	E_{ZS}	—	±1.5	—	LSB^2	V_{ADIN} = V_{SSAD}
	P		10-bit mode		—	±0.5	±1.5		
	T		8-bit mode		—	±0.5	±0.5		

2.11.3 SPI Timing

Table 16 and Figure 23 through Figure 26 describe the timing requirements for the SPI system.

Table 16. SPI Timing

No.	C	Function	Symbol	Min	Max	Unit
—	D	Operating frequency Master Slave	f_{op}	 $f_{Bus}/2048$ 0	 $f_{Bus}/2$ $f_{Bus}/4$	Hz
①	D	SPSCK period Master Slave	t_{SPSCK}	 2 4	 2048 —	 t_{cyc} t_{cyc}
②	D	Enable lead time Master Slave	t_{Lead}	 1/2 1	 — —	 t_{SPSCK} t_{cyc}
③	D	Enable lag time Master Slave	t_{Lag}	 1/2 1	 — —	 t_{SPSCK} t_{cyc}
④	D	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	 $t_{cyc} - 30$ $t_{cyc} - 30$	 1024 t_{cyc} —	 ns ns
⑤	D	Data setup time (inputs) Master Slave	t_{SU}	 15 15	 — —	 ns ns
⑥	D	Data hold time (inputs) Master Slave	t_{HI}	 0 25	 — —	 ns ns
⑦	D	Slave access time	t_a	—	1	t_{cyc}
⑧	D	Slave MISO disable time	t_{dis}	—	1	t_{cyc}
⑨	D	Data valid (after SPSCK edge) Master Slave	t_v	 — —	 25 25	 ns ns
⑩	D	Data hold time (outputs) Master Slave	t_{HO}	 0 0	 — —	 ns ns
⑪	D	Rise time Input Output	 t_{RI} t_{RO}	 — —	 $t_{cyc} - 25$ 25	 ns ns
⑫	D	Fall time Input Output	 t_{FI} t_{FO}	 — —	 $t_{cyc} - 25$ 25	 ns ns

2.12 LCD Specifications

Table 17. LCD Electricals, 3 V Glass

C	Characteristic	Symbol	Min	Typ	Max	Units
D	VLL3 Supply Voltage	VLL3	2.7	—	5.5	V
D	LCD Frame Frequency	f_{Frame}	28	30	64	Hz
D	LCD Charge Pump Capacitance	C_{LCD}	—	100	100	pF
D	LCD Bypass Capacitance	C_{BYLCD}	—	100	100	
D	LCD Glass Capacitance	C_{glass}	—	2000	8000	

2.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section.

Table 18. Flash Characteristics

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage for program/erase –40 °C to 85 °C	$V_{prog/erase}$	2.7		5.5	V
D	Supply voltage for read operation	V_{Read}	2.7		5.5	V
D	Internal FCLK frequency[1]	f_{FCLK}	150		200	kHz
D	Internal FCLK period (1/FCLK)	t_{Fcyc}	5		6.67	µs
C	Byte program time (random location)[2]	t_{prog}	9			t_{Fcyc}
C	Byte program time (burst mode)[2]	t_{Burst}	4			t_{Fcyc}
C	Page erase time[2]	t_{Page}	4000			t_{Fcyc}
C	Mass erase time[2]	t_{Mass}	20,000			t_{Fcyc}
D	Byte program current[3]	R_{IDDBP}	—	4	—	mA
D	Page erase current[3]	R_{IDDPE}	—	6	—	mA
C	Program/erase endurance[4] T_L to T_H = –40 °C to + 85 °C T = 25 °C		10,000	— 100,000	— —	cycles
C	Data retention[5]	t_{D_ret}	15	100	—	years

1 The frequency of this clock is controlled by a software setting.

2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

3 The program and erase currents are additional to the standard run I_{DD}. These values are measured at room temperatures with V_{DD} = 5.0 V, bus frequency = 4.0 MHz.

4 **Typical endurance for flash** was evaluated for this product family on the 9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to *Engineering Bulletin EB619, Typical Endurance for Nonvolatile Memory.*

5 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25 °C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to *Engineering Bulletin EB618, Typical Data Retention for Nonvolatile Memory.*

2.14 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

2.14.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East).

The maximum radiated RF emissions of the tested configuration in all orientations are less than or equal to the reported emissions levels.

Table 19. Radiated Emissions, Electric Field

Parameter	Symbol	Conditions	Frequency	f_{OSC}/f_{BUS}	Level[1] (Max)	Unit
Radiated emissions, electric field	V_{RE_TEM}	V_{DD} = 5.5 T_A = +25 °C Package type = 80 LQFP	0.15 – 50 MHz	4 MHz crystal 16 MHz bus	10	dBμV
			50 – 150 MHz		14	
			150 – 500 MHz		8	
			500 – 1000 MHz		5	
			IEC Level		L	—
			SAE Level		2	—

1 Data based on qualification test results.

2.14.2 Conducted Transient Susceptibility

Microcontroller transient conducted susceptibility is measured in accordance with an internal Freescale test method. The measurement is performed with the microcontroller installed on a custom EMC evaluation board and running specialized EMC test software designed in compliance with the test method. The conducted susceptibility is determined by injecting the transient susceptibility signal on each pin of the microcontroller. The transient waveform and injection methodology is based on IEC 61000-4-4 (EFT/B). The transient voltage required to cause performance degradation on any pin in the tested configuration is greater than or equal to the reported levels unless otherwise indicated by footnotes below Table 20.

Table 20. Conducted Susceptibility, EFT/B

Parameter	Symbol	Conditions	f_{OSC}/f_{BUS}	Result	Amplitude[1] (Min)	Unit
Conducted susceptibility, electrical fast transient/burst (EFT/B)	V_{CS_EFT}	V_{DD} = 5.5 T_A = +25 °C Package type = 80-pin LQFP	4 kHz crystal 4 MHz bus	A B C D	>4.0[2] >4.0[3] >4.0[4] >4.0	kV

1 Data based on qualification test results. Not tested in production.

2 Exceptions as covered in footnotes 3 and 4.

The susceptibility performance classification is described in Table 21.

Table 21. Susceptibility Performance Classification

Result	Performance Criteria	
A	No failure	The MCU performs as designed during and after exposure.
B	Self-recovering failure	The MCU does not perform as designed during exposure. The MCU returns automatically to normal operation after exposure is removed.
C	Soft failure	The MCU does not perform as designed during exposure. The MCU does not return to normal operation until exposure is removed and the RESET pin is asserted.
D	Hard failure	The MCU does not perform as designed during exposure. The MCU does not return to normal operation until exposure is removed and the power to the MCU is cycled.
E	Damage	The MCU does not perform as designed during and after exposure. The MCU cannot be returned to proper operation due to physical damage or other permanent performance degradation.

3 Ordering Information

This section contains ordering information for MC9S08LG32 and MC9S08LG16 devices.

Table 22. Device Numbering System

Device Number[1]	Memory		Temperature Range (°C)	LCD Mode Operation	Available Packages[2]
	FLASH	RAM			
Auto					
S9S08LG32J0CLK	32 KB	1984	-40 °C to +85 °C	Charge Pump	80-pin LQFP
S9S08LG32J0CLH					64-pin LQFP
S9S08LG32J0CLF					48-pin LQFP
S9S08LG32J0VLK	32 KB	1984	-40 °C to +105 °C	Register Bias	80-pin LQFP
S9S08LG32J0VLH					64-pin LQFP
S9S08LG32J0VLF					48-pin LQFP
S9S08LG16J0VLH	18 KB	1984			64-pin LQFP
S9S08LG16J0VLF					48-pin LQFP
IMM					
MC9S08LG32CLK	32 KB	1984	-40 °C to + 85 °C	Charge Pump	80-pin LQFP
MC9S08LG32CLH					64-pin LQFP
MC9S08LG32CLF					48-pin LQFP
MC9S08LG16CLH	18 KB	1984			64-pin LQFP
MC9S08LG16CLF					48-pin LQFP

1 See the *MC9S08LG32 Reference Manual* (document MC9S08LG32RM), for a complete description of modules included on each device.

2 See Table 23 for package information.

3.1 Device Numbering System

Example of the device numbering system:

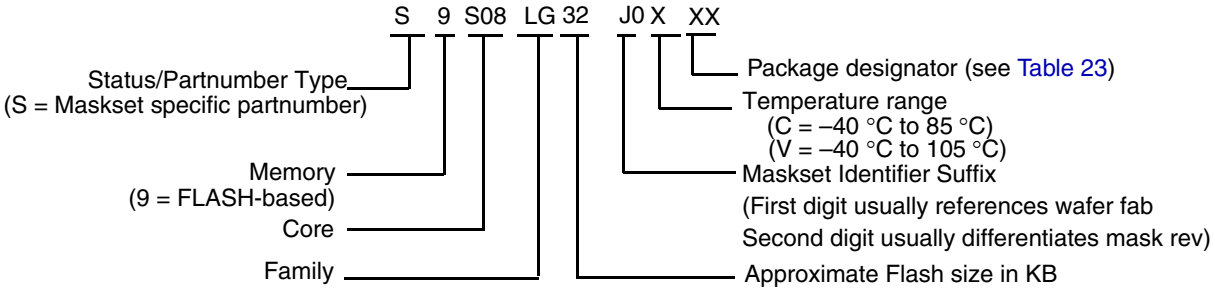


Figure 31. Device Number Example for Auto Parts

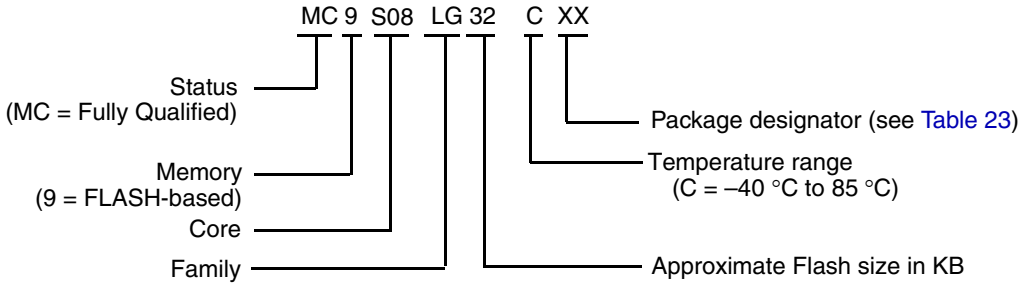


Figure 32. Device Number Example for IMM Parts

4 Package Information

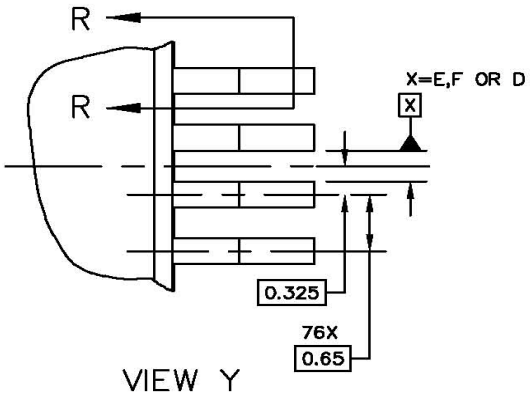
Table 23. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
80	Low Quad Flat Package	LQFP	LK	917A	98ASS23237W
64	Low Quad Flat Package	LQFP	LH	840F	98ASS23234W
48	Low Quad Flat Package	LQFP	LF	932	98ASH00962A

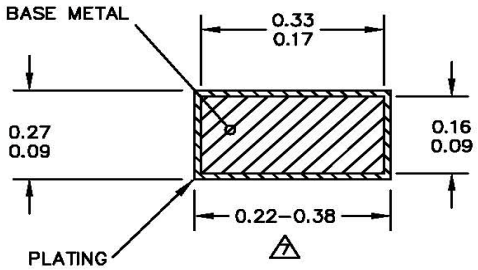
4.1 Mechanical Drawings

The following pages are mechanical drawings for the packages described in Table 23. For the latest available drawings please visit our web site (http://www.freescale.com) and enter the package's document number into the keyword search box.

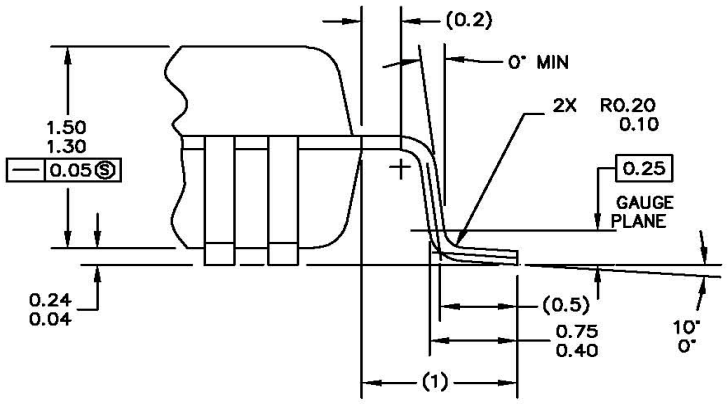
freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23237W
		PAGE: 917A
	DO NOT SCALE THIS DRAWING	REV: E



VIEW Y



SECTION R–R
ROTATED 90° CW

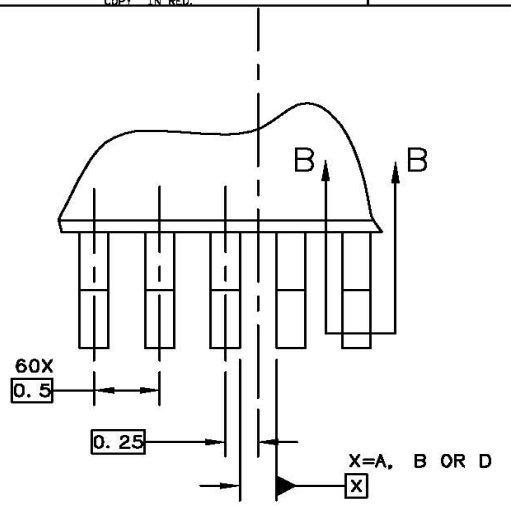


VIEW K

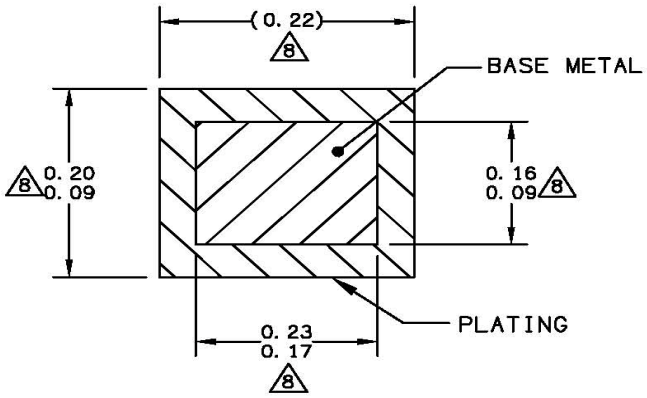
TITLE: 80 LD LQFP, 14 X 14 PKG, 0.65 MM PITCH, 1.4 THICK	CASE NUMBER: 917A–03	
	STANDARD: FREESCALE	
	PACKAGE CODE: 8258	SHEET: 2 OF 3

freescale semiconductor

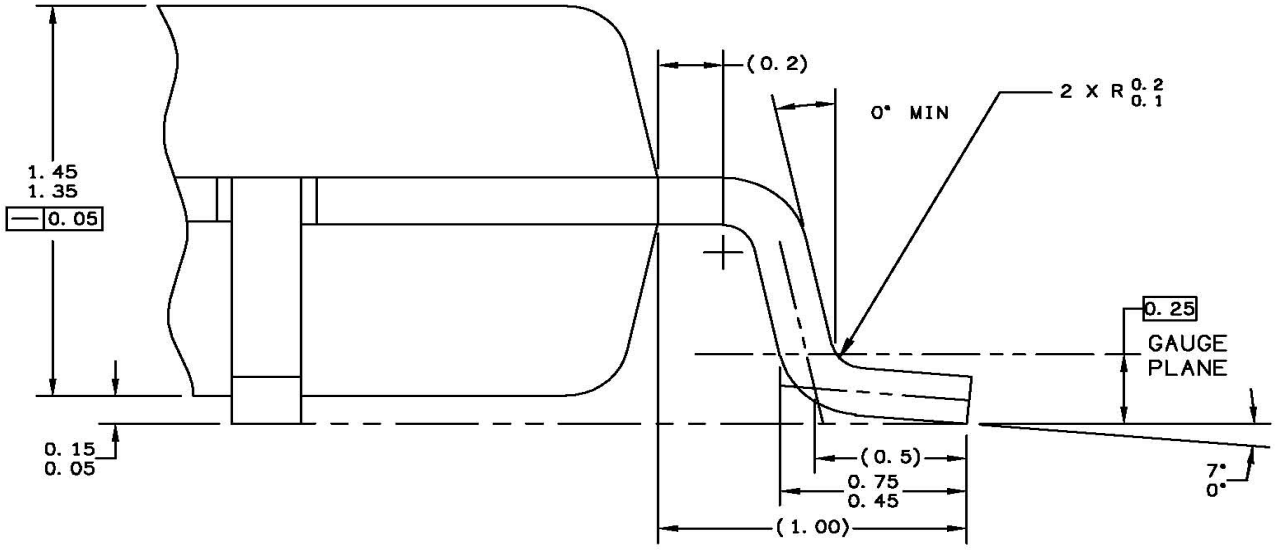
MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23234W
	PAGE: 840F
DO NOT SCALE THIS DRAWING	REV: E



VIEW Y



SECTION B–B



VIEW AA

TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	CASE NUMBER: 840F–02	
	STANDARD: JEDEC MS–026 BCD	
	PACKAGE CODE: 8426	SHEET: 2 OF 3

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23234W
		PAGE: 840F
	DO NOT SCALE THIS DRAWING	REV: E

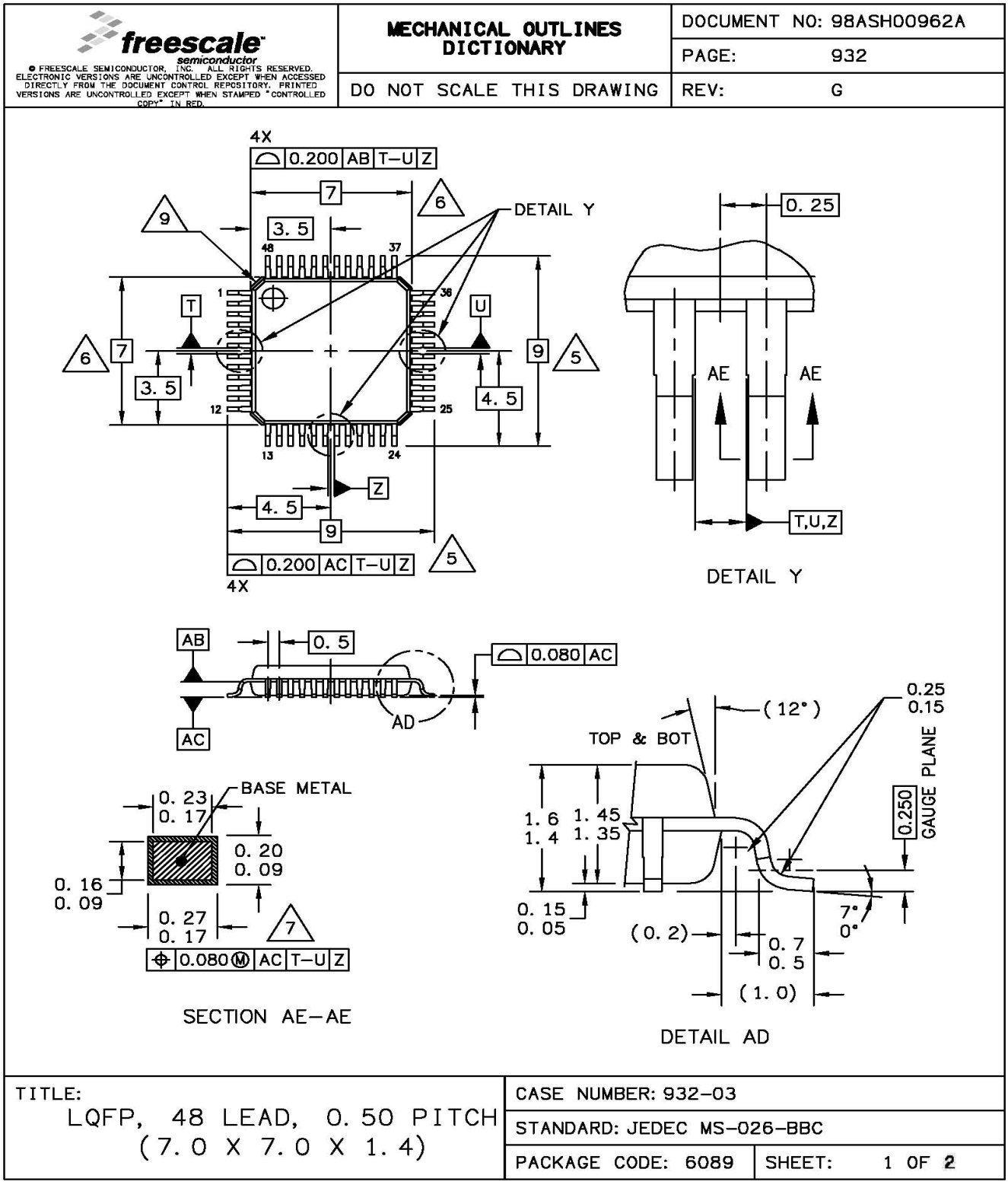
NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.

TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	CASE NUMBER: 840F–02	
	STANDARD: JEDEC MS–026 BCD	
	PACKAGE CODE: 8426	SHEET: 3 OF 3

Figure 34. 64-pin LQFP Package Drawing (Case 840F, Doc #98ASS23234W)

4.1.3 48-pin LQFP



5 Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web are the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://www.freescale.com

The following revision history table summarizes changes contained in this document.

Table 24. Revision History

Revision	Date	Description of Changes
1	8/2008	First Initial release.
2	9/2008	Second Initial Release.
3	11/2008	Alpha Customer Release.
4	2/2009	Launch Release.
5	4/2009	Added EMC Radiated Emission and Transient Susceptibility data in Table 19 and Table 20.
6	4/2009	Updated EMC performance data.
7	8/2009	Updated auto part numbers, changed TCLK, T0CH0, T0CH1, T1CH0, T1CH1, T1CH2, T1CH3, T1CH3, T1CH4, and T1CH5 to TPMCLK, TPM0CH0, TPM0CH1,TPM1CH0, TPM1CH1, TPM1CH2, TPM1CH3, TPM1CH4, and TPM1CH5, and changed the maximum LCD frame frequency to 64 Hz.
8	8/2011	Updated Table “ICS Frequency Specifications (Temperature Range = –40 ×C to 105 ×C Ambient)”. Changed the value of row 8 column C from C to P.
9	9/2011	Updated Table “ICS Frequency Specifications (Temperature Range = –40 ×C to 105 ×C Ambient)”. Removed Footnote from Row 8. Updated the Revision History