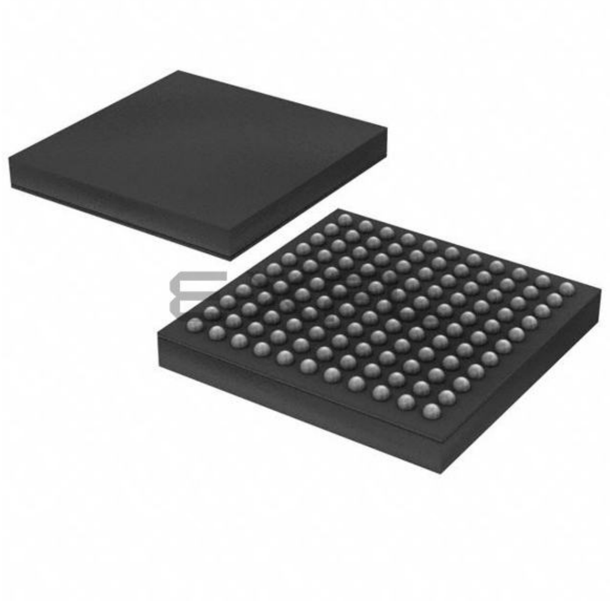
# Silicon Labs - EFM32WG295F64-BGA120 Datasheet



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## Applications of "Embedded - Microcontrollers"

| **Details** | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Core Processor | ARM® Cortex®-M4F |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 93 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.98V ~ 3.8V |
| Data Converters | A/D 8x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 120-VFBGA |
| Supplier Device Package | 120-BGA (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/efm32wg295f64-bga120 |

# 1 Ordering Information

Table 1.1 (p. 2) shows the available EFM32WG295 devices.

***Table 1.1. Ordering Information***

| Ordering Code | Flash (kB) | RAM (kB) | Max Speed (MHz) | Supply Voltage (V) | Temperature (ºC) | Package |
|---|---|---|---|---|---|---|
| EFM32WG295F64-BGA120 | 64 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | BGA120 |
| EFM32WG295F128-BGA120 | 128 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | BGA120 |
| EFM32WG295F256-BGA120 | 256 | 32 | 48 | 1.98 - 3.8 | -40 - 85 | BGA120 |

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### 2.1.27 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface (LESENSE$^{TM}$), is a highly configurable sensor interface with support for up to 16 individually configurable sensors. By controlling the analog comparators and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable FSM which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

### 2.1.28 Backup Power Domain

The backup power domain is a separate power domain containing a Backup Real Time Counter, BURTC, and a set of retention registers, available in all energy modes. This power domain can be configured to automatically change power source to a backup battery when the main power drains out. The backup power domain enables the EFM32WG295 to keep track of time and retain data, even if the main power source should drain out.

### 2.1.29 Advanced Encryption Standard Accelerator (AES)

The AES accelerator performs AES encryption and decryption with 128-bit or 256-bit keys. Encrypting or decrypting one 128-bit data block takes 52 HFCORECLK cycles with 128-bit keys and 75 HFCORECLK cycles with 256-bit keys. The AES module is an AHB slave which enables efficient access to the data and key registers. All write accesses to the AES module must be 32-bit operations, i.e. 8- or 16-bit operations are not supported.

### 2.1.30 General Purpose Input/Output (GPIO)

In the EFM32WG295, there are 93 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advanced configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 16 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

## 2.2 Configuration Summary

The features of the EFM32WG295 is a subset of the feature set described in the EFM32WG Reference Manual. Table 2.1 (p. 7) describes device specific implementation of the features.

*Table 2.1. Configuration Summary*

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M4 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |

| Module | Configuration | Pin Connections |
|---|---|---|
| PRS | Full configuration | NA |
| EBI | Full configuration | EBI_A[27:0], EBI_AD[15:0], EBI_ARDY, EBI_ALE, EBI_BL[1:0], EBI_CS[3:0], EBI_CSTFT, EBI_DCLK, EBI_DTEN, EBI_HSNC, EBI_NANDREn, EBI_NANDWEn, EBI_REn, EBI_VSNC, EBI_WEn |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| I2C1 | Full configuration | I2C1_SDA, I2C1_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | Full configuration with I2S | US2_TX, US2_RX, US2_CLK, US2_CS |
| UART0 | Full configuration | U0_TX, U0_RX |
| UART1 | Full configuration | U1_TX, U1_RX |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| LEUART1 | Full configuration | LEU1_TX, LEU1_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| TIMER3 | Full configuration | TIM3_CC[2:0] |
| RTC | Full configuration | NA |
| BURTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| PCNT2 | Full configuration, 8-bit count register | PCNT2_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:0], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[7:0], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[1:0], DAC0_OUTxALT |
| OPAMP | Full configuration | Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx |
| AES | Full configuration | NA |
| GPIO | 93 pins | Available pins are shown in Table 4.3 (p. 67) |

## 2.3 Memory Map

The *EFM32WG295* memory map is shown in Figure 2.2 (p. 9), with RAM and Flash sizes for the largest memory configuration.

## 3.6 Power Management

The EFM32WG requires the AVDD_x, VDD_DREG and IOVDD_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, "AN0002 EFM32 Hardware Design Considerations".

***Table 3.6. Power Management***

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{BODextthr-}$ | BOD threshold on falling external supply voltage | | 1.74 | | 1.96 | V |
| $V_{BODextthr+}$ | BOD threshold on rising external supply voltage | | | 1.85 | 1.98 | V |
| $V_{PORthr+}$ | Power-on Reset (POR) threshold on rising external supply voltage | | | | 1.98 | V |
| $t_{RESET}$ | Delay from reset is released until program execution starts | Applies to Power-on Reset, Brown-out Reset and pin reset. | | 163 | | µs |
| $C_{DECOUPLE}$ | Voltage regulator decoupling capacitor. | X5R capacitor recommended. Apply between DECOUPLE pin and GROUND | | 1 | | µF |

## 3.7 Flash

***Table 3.7. Flash***

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $EC_{FLASH}$ | Flash erase cycles before failure | | 20000 | | | cycles |
| $RET_{FLASH}$ | Flash data retention | $T_{AMB}$<150°C | 10000 | | | h |
| | | $T_{AMB}$<85°C | 10 | | | years |
| | | $T_{AMB}$<70°C | 20 | | | years |
| $t_{W\_PROG}$ | Word (32-bit) programming time | | 20 | | | µs |
| $t_{PERASE}$ | Page erase time | | 20 | 20.4 | 20.8 | ms |
| $t_{DERASE}$ | Device erase time | | 40 | 40.8 | 41.6 | ms |
| $I_{ERASE}$ | Erase current | | | | 7[1] | mA |
| $I_{WRITE}$ | Write current | | | | 7[1] | mA |
| $V_{FLASH}$ | Supply voltage during flash erase and write | | 1.98 | | 3.8 | V |

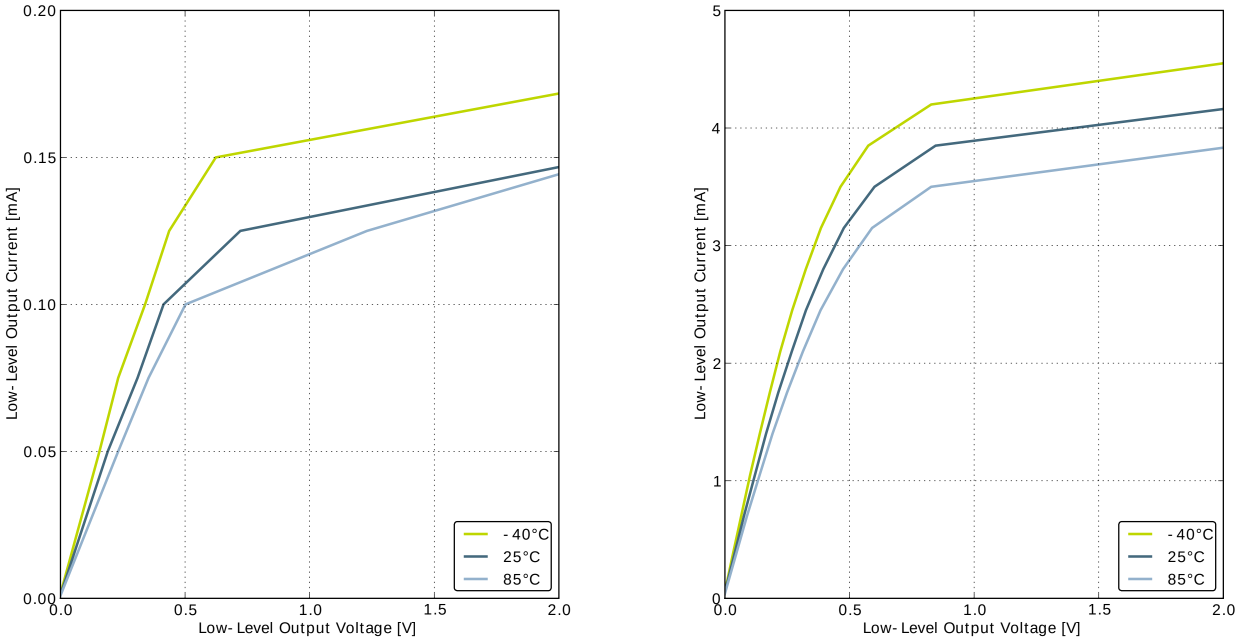
[1] Measured at 25°C

## 3.8 General Purpose Input Output

*Table 3.8. GPIO*

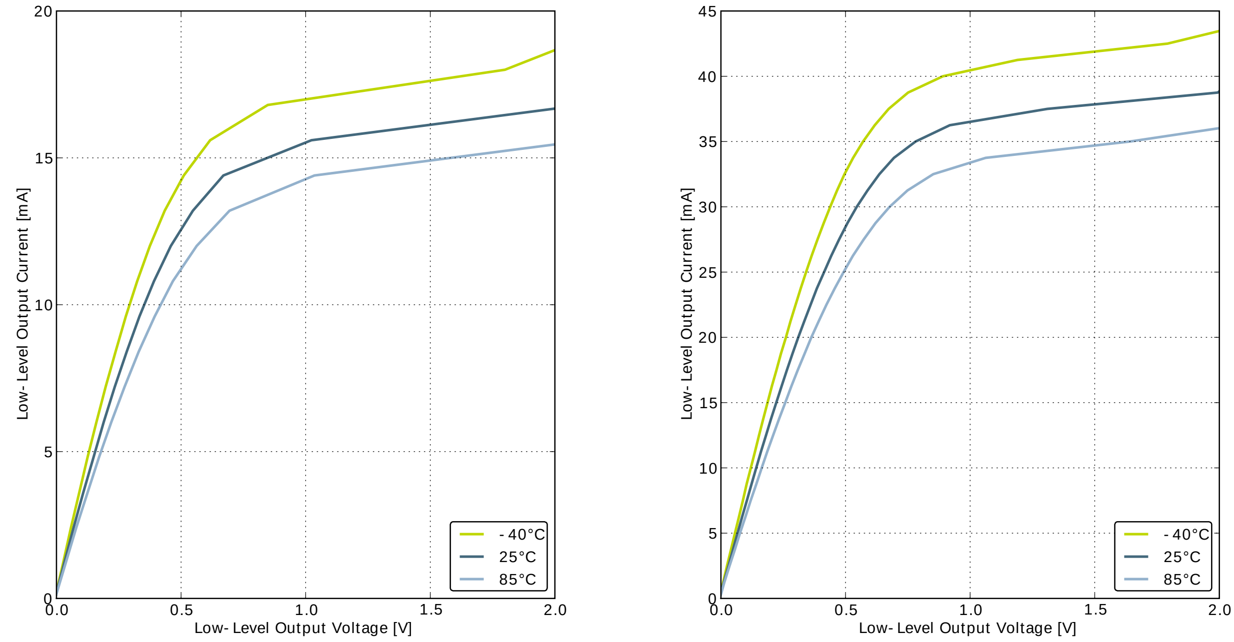
| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IOIL}$ | Input low voltage | | | | $0.30V_{DD}$ | V |
| $V_{IOIH}$ | Input high voltage | | $0.70V_{DD}$ | | | V |
| $V_{IOOH}$ | Output high voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD) | Sourcing 0.1 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST | | $0.80V_{DD}$ | | V |
| | | Sourcing 0.1 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST | | $0.90V_{DD}$ | | V |
| | | Sourcing 1 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW | | $0.85V_{DD}$ | | V |
| | | Sourcing 1 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW | | $0.90V_{DD}$ | | V |
| | | Sourcing 6 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD | $0.75V_{DD}$ | | | V |
| | | Sourcing 6 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD | $0.85V_{DD}$ | | | V |
| | | Sourcing 20 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH | $0.60V_{DD}$ | | | V |
| | | Sourcing 20 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH | $0.80V_{DD}$ | | | V |
| $V_{IOOL}$ | Output low voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD) | Sinking 0.1 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOWEST | | $0.20V_{DD}$ | | V |
| | | Sinking 0.1 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOWEST | | $0.10V_{DD}$ | | V |
| | | Sinking 1 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = LOW | | $0.10V_{DD}$ | | V |
| | | Sinking 1 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = LOW | | $0.05V_{DD}$ | | V |
| | | Sinking 6 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = STANDARD | | | $0.30V_{DD}$ | V |
| | | Sinking 6 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD | | | $0.20V_{DD}$ | V |
| | | Sinking 20 mA, $V_{DD}$=1.98 V, GPIO_Px_CTRL DRIVEMODE = HIGH | | | $0.35V_{DD}$ | V |

Figure 3.11. Typical Low-Level Output Current, 2V Supply Voltage



GPIO_Px_CTRL DRIVEMODE = LOWEST

GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD

GPIO_Px_CTRL DRIVEMODE = HIGH

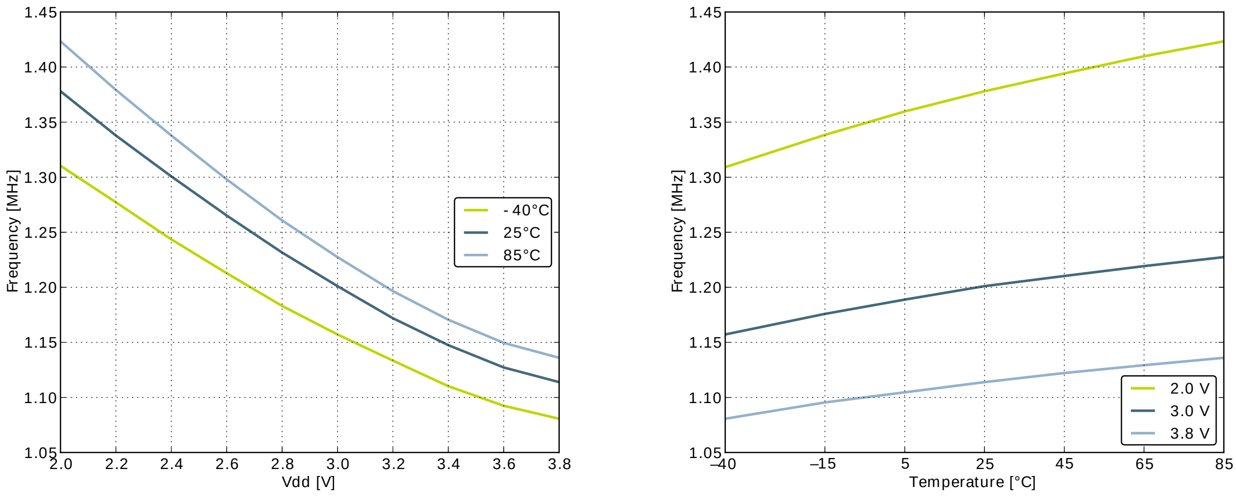
## 3.9.4 HFRCO

*Table 3.12. HFRCO*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HFRCO}$ | Oscillation frequency, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | 28 MHz frequency band | 27.5 | 28.0 | 28.5 | MHz |
| | | 21 MHz frequency band | 20.6 | 21.0 | 21.4 | MHz |
| | | 14 MHz frequency band | 13.7 | 14.0 | 14.3 | MHz |
| | | 11 MHz frequency band | 10.8 | 11.0 | 11.2 | MHz |
| | | 7 MHz frequency band | 6.48 | 6.60 | 6.72 | MHz |
| | | 1 MHz frequency band | 1.15 | 1.20 | 1.25 | MHz |
| $t_{HFRCO\_settling}$ | Settling time after start-up | $f_{HFRCO}$ = 14 MHz | | 0.6 | | Cycles |
| $I_{HFRCO}$ | Current consumption | $f_{HFRCO}$ = 28 MHz | | 165 | 215 | µA |
| | | $f_{HFRCO}$ = 21 MHz | | 134 | 175 | µA |
| | | $f_{HFRCO}$ = 14 MHz | | 106 | 140 | µA |
| | | $f_{HFRCO}$ = 11 MHz | | 94 | 125 | µA |
| | | $f_{HFRCO}$ = 6.6 MHz | | 77 | 105 | µA |
| | | $f_{HFRCO}$ = 1.2 MHz | | 25 | 40 | µA |
| $DC_{HFRCO}$ | Duty cycle | $f_{HFRCO}$ = 14 MHz | 48.5 | 50 | 51 | % |
| $TUNESTEP_{HFRCO}$ | Frequency step for LSB change in TUNING value | | | 0.3[1] | | % |

[1] The TUNING field in the CMU_HFRCOCTRL register may be used to adjust the HFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the HFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

*Figure 3.18. Calibrated HFRCO 1 MHz Band Frequency vs Supply Voltage and Temperature*

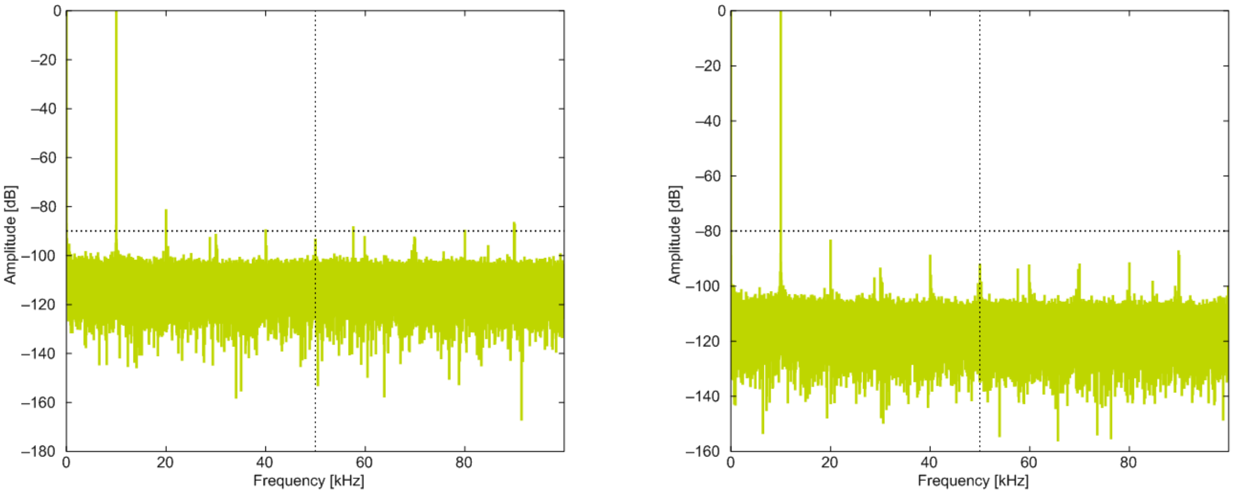


| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | erence voltage on channel 6 | | | | | |
| $V_{ADCCMIN}$ | Common mode input range | | 0 | | $V_{DD}$ | V |
| $I_{ADCIN}$ | Input current | 2pF sampling capacitors | | <100 | | nA |
| $CMRR_{ADC}$ | Analog input common mode rejection ratio | | | 65 | | dB |
| $I_{ADC}$ | Average active current | 1 MSamples/s, 12 bit, external reference | | 351 | | µA |
| | | 10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b00 | | 67 | | µA |
| | | 10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b01 | | 63 | | µA |
| | | 10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b10 | | 64 | | µA |
| $I_{ADCREF}$ | Current consumption of internal voltage reference | Internal voltage reference | | 65 | | µA |
| $C_{ADCIN}$ | Input capacitance | | | 2 | | pF |
| $R_{ADCIN}$ | Input ON resistance | | 1 | | | MOhm |
| $R_{ADCFILT}$ | Input RC filter resistance | | | 10 | | kOhm |
| $C_{ADCFILT}$ | Input RC filter/decoupling capacitance | | | 250 | | fF |
| $f_{ADCCLK}$ | ADC Clock Frequency | | | | 13 | MHz |
| $t_{ADCCONV}$ | Conversion time | 6 bit | 7 | | | ADC-CLK Cycles |
| | | 8 bit | 11 | | | ADC-CLK Cycles |
| | | 12 bit | 13 | | | ADC-CLK Cycles |
| $t_{ADCACQ}$ | Acquisition time | Programmable | 1 | | 256 | ADC-CLK Cycles |
| $t_{ADCACQVDD3}$ | Required acquisition time for VDD/3 reference | | 2 | | | µs |
| $t_{ADCSTART}$ | Startup time of reference generator | | | 5 | | µs |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | 1 MSamples/s, 12 bit, differential, internal 2.5V reference | | 64 | | dB |
| | | 1 MSamples/s, 12 bit, differential, 5V reference | | 54 | | dB |
| | | 1 MSamples/s, 12 bit, differential, $V_{DD}$ reference | | 66 | | dB |
| | | 1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference | | 68 | | dB |
| | | 200 kSamples/s, 12 bit, single ended, internal 1.25V reference | | 61 | | dB |
| | | 200 kSamples/s, 12 bit, single ended, internal 2.5V reference | | 65 | | dB |
| | | 200 kSamples/s, 12 bit, single ended, $V_{DD}$ reference | | 66 | | dB |
| | | 200 kSamples/s, 12 bit, differential, internal 1.25V reference | | 63 | | dB |
| | | 200 kSamples/s, 12 bit, differential, internal 2.5V reference | | 66 | | dB |
| | | 200 kSamples/s, 12 bit, differential, 5V reference | | 66 | | dB |
| | | 200 kSamples/s, 12 bit, differential, $V_{DD}$ reference | 62 | 66 | | dB |
| | | 200 kSamples/s, 12 bit, differential, $2xV_{DD}$ reference | | 69 | | dB |
| $SFDR_{ADC}$ | Spurious-Free Dynamic Range (SFDR) | 1 MSamples/s, 12 bit, single ended, internal 1.25V reference | | 64 | | dBc |
| | | 1 MSamples/s, 12 bit, single ended, internal 2.5V reference | | 76 | | dBc |
| | | 1 MSamples/s, 12 bit, single ended, $V_{DD}$ reference | | 73 | | dBc |
| | | 1 MSamples/s, 12 bit, differential, internal 1.25V reference | | 66 | | dBc |
| | | 1 MSamples/s, 12 bit, differential, internal 2.5V reference | | 77 | | dBc |
| | | 1 MSamples/s, 12 bit, differential, $V_{DD}$ reference | | 76 | | dBc |
| | | 1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference | | 75 | | dBc |
| | | 1 MSamples/s, 12 bit, differential, 5V reference | | 69 | | dBc |
| | | 200 kSamples/s, 12 bit, single ended, internal 1.25V reference | | 75 | | dBc |
| | | 200 kSamples/s, 12 bit, single ended, internal 2.5V reference | | 75 | | dBc |
| | | 200 kSamples/s, 12 bit, single ended, $V_{DD}$ reference | | 76 | | dBc |

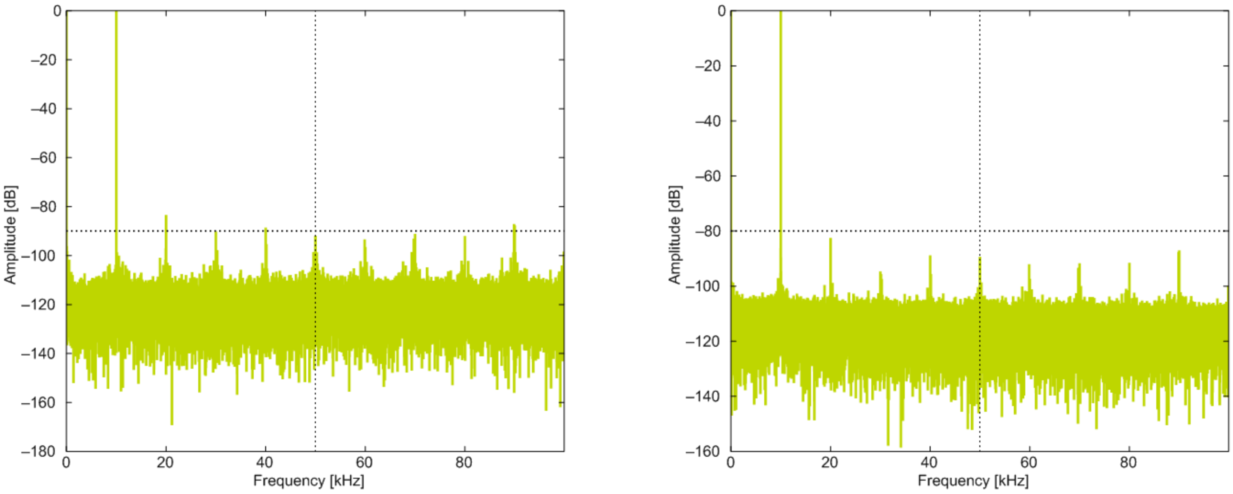
### 3.10.1 Typical performance

*Figure 3.26. ADC Frequency Spectrum, Vdd = 3V, Temp = 25°C*



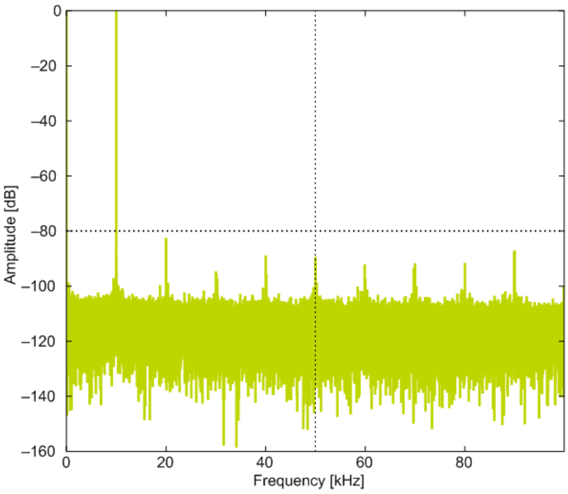
1.25V Reference

2.5V Reference



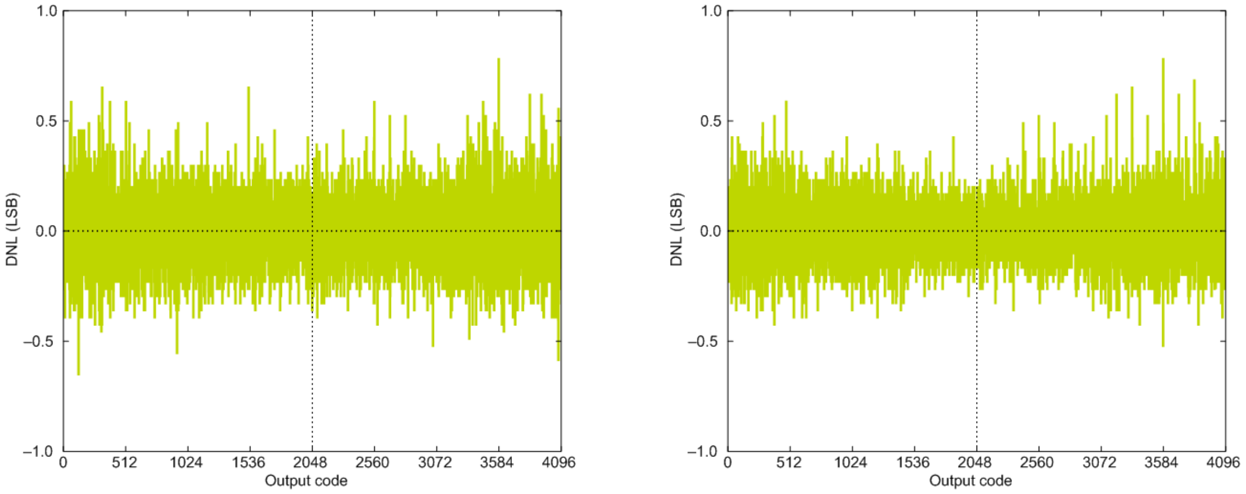
2XVDDVSS Reference

5VDIFF Reference



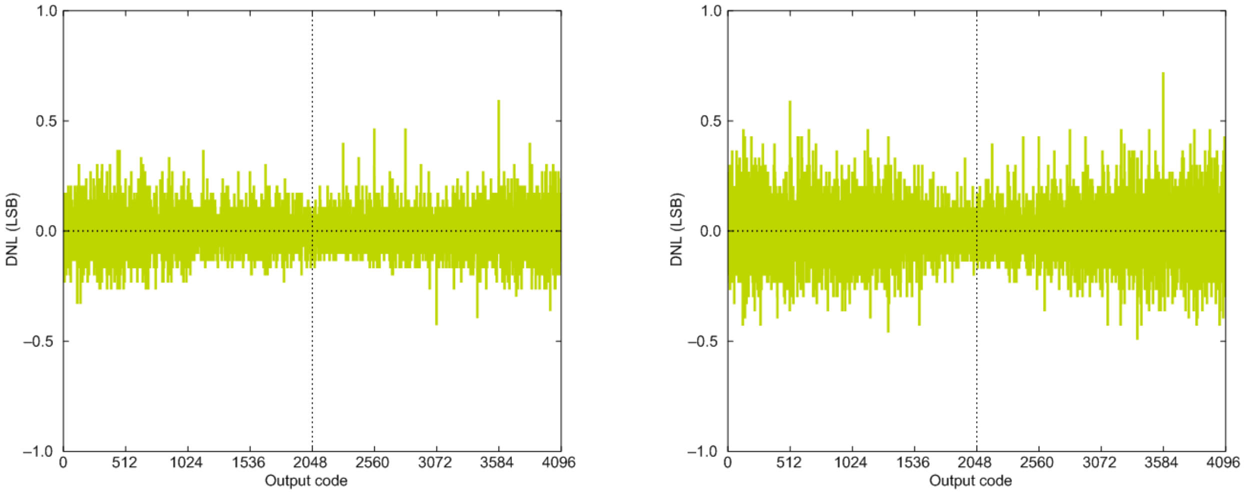
VDD Reference

**Figure 3.28. ADC Differential Linearity Error vs Code, Vdd = 3V, Temp = 25°C**



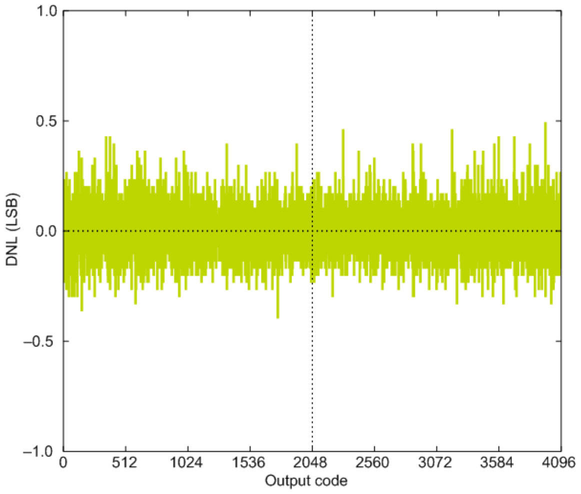
1.25V Reference

2.5V Reference



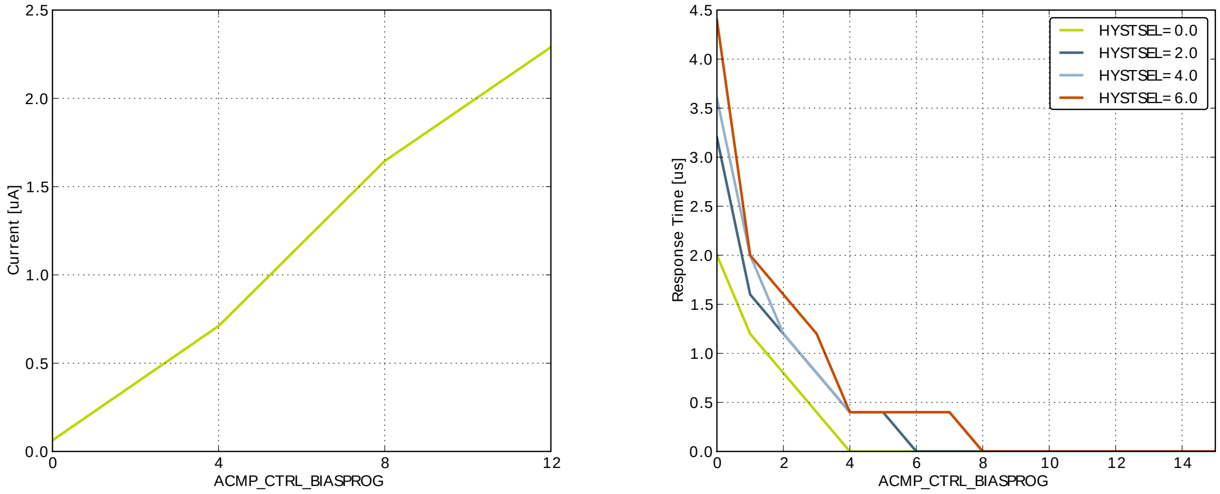
2XVDDVSS Reference

5VDIFF Reference



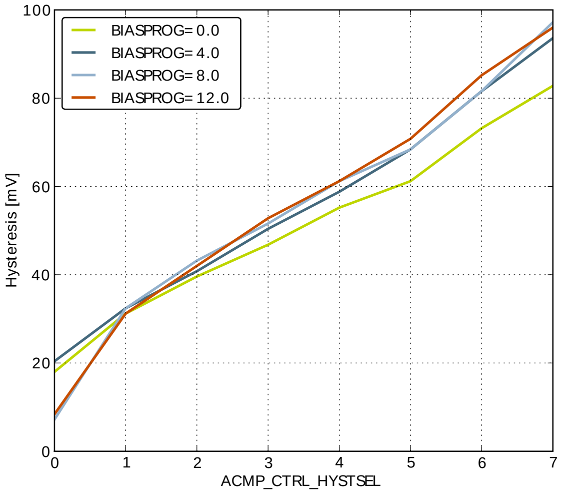
VDD Reference

***Figure 3.37. ACMP Characteristics, Vdd = 3V, Temp = 25°C, FULLBIAS = 0, HALFBIAS = 1***



Current consumption, HYSTSEL = 4

Response time



Hysteresis

### Table 3.20. EBI Write Enable Timing

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{OH\_WEn}$ [1,2,3,4] | Output hold time, from trailing EBI_WEn/ EBI_NANDWEn edge to EBI_AD, EBI_A, EBI_CSn, EBI_BLn invalid | -6.00 + (WRHOLD * $t_{HFCORECLK}$) | | | ns |
| $t_{OSU\_WEn}$ [1,2,3,4,5] | Output setup time, from EBI_AD, EBI_A, EBI_CSn, EBI_BLn valid to leading EBI_WEn/ EBI_NANDWEn edge | -14.00 + (WRSETUP * $t_{HFCORECLK}$) | | | ns |
| $t_{WIDTH\_WEn}$ [1,2,3,4,5] | EBI_WEn/EBI_NANDWEn pulse width | -7.00 + ((WRSTRB +1) * $t_{HFCORECLK}$) | | | ns |

[1] Applies for all addressing modes (figure only shows D16 addressing mode)

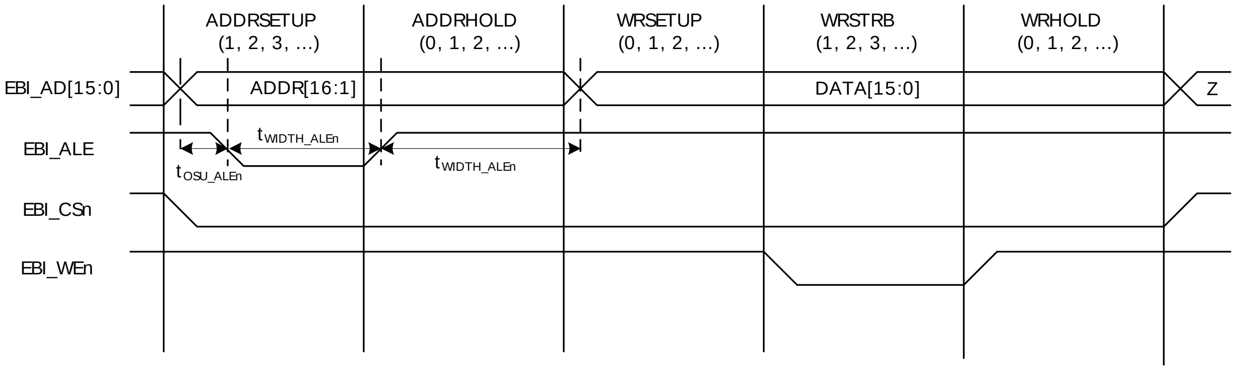
[2] Applies for both EBI_WEn and EBI_NANWEn (figure only shows EBI_WEn)

[3] Applies for all polarities (figure only shows active low signals)

[4] Measurement done at 10% and 90% of $V_{DD}$ (figure shows 50% of $_{VDD}$)

[5] The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFWE=0. The leading edge of EBI_WEn can be moved to the right by setting HALFWE=1. This decreases the length of $t_{WIDTH\_WEn}$ and increases the length of $t_{OSU\_WEn}$ by 1/2 * $t_{HFCLKNODIV}$.

### Figure 3.39. EBI Address Latch Enable Related Output Timing



### Table 3.21. EBI Address Latch Enable Related Output Timing

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{OH\_ALEn}$ [1,2,3,4] | Output hold time, from trailing EBI_ALE edge to EBI_AD invalid | -6.00 + (ADDRHOLD[5] * $t_{HFCORECLK}$) | | | ns |
| $t_{OSU\_ALEn}$ [1,2,4] | Output setup time, from EBI_AD valid to leading EBI_ALE edge | -13.00 + (0 * $t_{HFCORECLK}$) | | | ns |
| $t_{WIDTH\_ALEn}$ [1,2,3,4] | EBI_ALEn pulse width | -7.00 + (ADDRSETUP+1) * $t_{HFCORECLK}$) | | | ns |

[1] Applies to addressing modes D8A24ALE and D16A16ALE (figure only shows D16A16ALE)

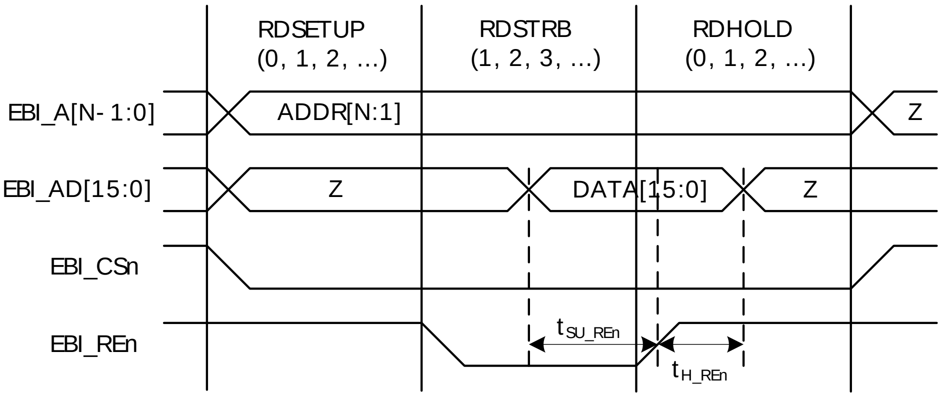
[2] Applies for all polarities (figure only shows active low signals)

[3] The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFALE=0. The trailing edge of EBI_ALE can be moved to the left by setting HALFALE=1. This decreases the length of $t_{WIDTH\_ALEn}$ and increases the length of tOH_ALEn by $t_{HFCORECLK}$ - 1/2 * $t_{HFCLKNODIV}$.

[4] Measurement done at 10% and 90% of $V_{DD}$ (figure shows 50% of $_{VDD}$)

[5] Figure only shows a write operation. For a multiplexed read operation the address hold time is controlled via the RDSETUP state instead of via the ADDRHOLD state.

### Figure 3.41. EBI Read Enable Related Timing Requirements



### Table 3.23. EBI Read Enable Related Timing Requirements

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{SU\_REn}$ [1][2][3][4] | Setup time, from EBI_AD valid to trailing EBI_REn edge | 37 | | | ns |
| $t_{H\_Ren}$ [1][2][3][4] | Hold time, from trailing EBI_REn edge to EBI_AD invalid | -1 | | | ns |

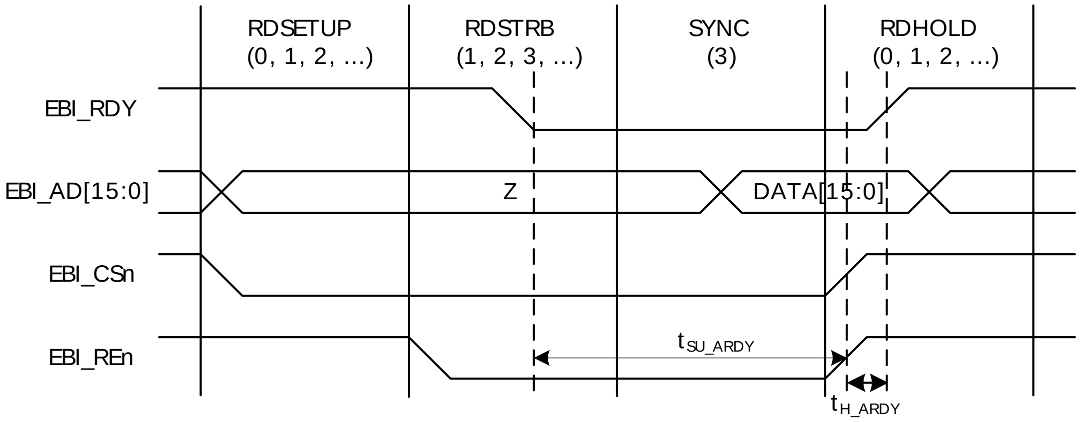
[1] Applies for all addressing modes (figure only shows D16A8).

[2] Applies for both EBI_REn and EBI_NANDREn (figure only shows EBI_REn)

[3] Applies for all polarities (figure only shows active low signals)

[4] Measurement done at 10% and 90% of $V_{DD}$ (figure shows 50% of $_{VDD}$)

### Figure 3.42. EBI Ready/Wait Related Timing Requirements



### Table 3.24. EBI Ready/Wait Related Timing Requirements

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{SU\_ARDY}$ [1][2][3][4] | Setup time, from EBI_ARDY valid to trailing EBI_REn, EBI_WEn edge | 37 + (3 * $t_{HFCORECLK}$) | | | ns |

| BGA120 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| H12 | PE2 | BU_VOUT | EBI_A09 #0 | TIM3_CC2 #1 | U1_TX #3 | ACMP0_O #1 |
| H13 | PC7 | ACMP0_CH7 | EBI_A06 #0/1/2 | | LEU1_RX #0<br>I2C0_SCL #2 | LES_CH7 #0<br>ETM_TD0 #2 |
| J1 | PD14 | | | | I2C0_SDA #3 | |
| J2 | PD15 | | | | I2C0_SCL #3 | |
| J3 | VSS | Ground | | | | |
| J11 | IOVDD_3 | Digital IO power supply 3. | | | | |
| J12 | PC6 | ACMP0_CH6 | EBI_A05 #0/1/2 | | LEU1_TX #0<br>I2C0_SDA #2 | LES_CH6 #0<br>ETM_TCLK #2 |
| J13 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | | |
| K1 | PC0 | ACMP0_CH0<br>DAC0_OUT0ALT #0/<br>OPAMP_OUT0ALT | EBI_A23 #0/1/2 | TIM0_CC1 #4<br>PCNT0_S0IN #2 | US0_TX #5<br>US1_TX #0<br>I2C0_SDA #4 | LES_CH0 #0<br>PRS_CH2 #0 |
| K2 | PC1 | ACMP0_CH1<br>DAC0_OUT0ALT #1/<br>OPAMP_OUT0ALT | EBI_A24 #0/1/2 | TIM0_CC2 #4<br>PCNT0_S1IN #2 | US0_RX #5<br>US1_RX #0<br>I2C0_SCL #4 | LES_CH1 #0<br>PRS_CH3 #0 |
| K3 | IOVDD_4 | Digital IO power supply 4. | | | | |
| K11 | VSS | Ground | | | | |
| K12 | VSS | Ground | | | | |
| K13 | PD8 | BU_VIN | | | | CMU_CLK1 #1 |
| L1 | PC2 | ACMP0_CH2<br>DAC0_OUT0ALT #2/<br>OPAMP_OUT0ALT | EBI_A25 #0/1/2 | TIM0_CDTI0 #4 | US2_TX #0 | LES_CH2 #0 |
| L2 | PC3 | ACMP0_CH3<br>DAC0_OUT0ALT #3/<br>OPAMP_OUT0ALT | EBI_NANDREn #0/1/2 | TIM0_CDTI1 #4 | US2_RX #0 | LES_CH3 #0 |
| L3 | PA7 | | EBI_CSTFT #0/1/2 | | | |
| L4 | IOVDD_5 | Digital IO power supply 5. | | | | |
| L5 | VSS | Ground | | | | |
| L6 | VSS | Ground | | | | |
| L7 | IOVDD_6 | Digital IO power supply 6. | | | | |
| L8 | PB9 | | EBI_A03 #0/1/2 | | U1_TX #2 | |
| L9 | PB10 | | EBI_A04 #0/1/2 | | U1_RX #2 | |
| L10 | PD0 | ADC0_CH0<br>DAC0_OUT0ALT #4/<br>OPAMP_OUT0ALT<br>OPAMP_OUT2 #1 | | PCNT2_S0IN #0 | US1_TX #1 | |
| L11 | PD1 | ADC0_CH1<br>DAC0_OUT1ALT #4/<br>OPAMP_OUT1ALT | | TIM0_CC0 #3<br>PCNT2_S1IN #0 | US1_RX #1 | DBG_SWO #2 |
| L12 | PD4 | ADC0_CH4<br>OPAMP_P2 | | | LEU0_TX #0 | ETM_TD2 #0/2 |
| L13 | PD7 | ADC0_CH7<br>DAC0_N1 /<br>OPAMP_N1 | | TIM1_CC1 #4<br>LETIM0_OUT1 #0<br>PCNT0_S1IN #3 | US1_TX #2<br>I2C0_SCL #1 | CMU_CLK0 #2<br>LES_ALTEX1 #0<br>ACMP1_O #2<br>ETM_TCLK #0 |
| M1 | PB7 | LFXTAL_P | | TIM1_CC0 #3 | US0_TX #4<br>US1_CLK #0 | |
| M2 | PC4 | ACMP0_CH4<br>DAC0_P0 / | EBI_A26 #0/1/2 | TIM0_CDTI2 #4<br>LETIM0_OUT0 #3 | US2_CLK #0<br>I2C1_SDA #0 | LES_CH4 #0 |

| BGA120 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| | | OPAMP_P0 | | PCNT1_S0IN #0 | | |
| M3 | PA8 | | EBI_DCLK #0/1/2 | TIM2_CC0 #0 | | |
| M4 | PA10 | | EBI_VSNC #0/1/2 | TIM2_CC2 #0 | | |
| M5 | PA13 | | EBI_A01 #0/1/2 | TIM2_CC1 #1 | | |
| M6 | PA14 | | EBI_A02 #0/1/2 | TIM2_CC2 #1 | | |
| M7 | RESETn | Reset input, active low.<br>To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | | |
| M8 | AVSS_1 | Analog ground 1. | | | | |
| M9 | AVDD_2 | Analog power supply 2. | | | | |
| M10 | AVDD_1 | Analog power supply 1. | | | | |
| M11 | AVSS_0 | Analog ground 0. | | | | |
| M12 | PD3 | ADC0_CH3<br>OPAMP_N2 | | TIM0_CC2 #3 | US1_CS #1 | ETM_TD1 #0/2 |
| M13 | PD6 | ADC0_CH6<br>DAC0_P1 /<br>OPAMP_P1 | | TIM1_CC0 #4<br>LETIM0_OUT0 #0<br>PCNT0_S0IN #3 | US1_RX #2<br>I2C0_SDA #1 | LES_ALTEX0 #0<br>ACMP0_O #2<br>ETM_TD0 #0 |
| N1 | PB8 | LFXTAL_N | | TIM1_CC1 #3 | US0_RX #4<br>US1_CS #0 | |
| N2 | PC5 | ACMP0_CH5<br>DAC0_N0 /<br>OPAMP_N0 | EBI_NANDWEn #0/1/2 | LETIM0_OUT1 #3<br>PCNT1_S1IN #0 | US2_CS #0<br>I2C1_SCL #0 | LES_CH5 #0 |
| N3 | PA9 | | EBI_DTEN #0/1/2 | TIM2_CC1 #0 | | |
| N4 | PA11 | | EBI_HSNC #0/1/2 | | | |
| N5 | PA12 | | EBI_A00 #0/1/2 | TIM2_CC0 #1 | | |
| N6 | PB11 | DAC0_OUT0 /<br>OPAMP_OUT0 | | TIM1_CC2 #3<br>LETIM0_OUT0 #1 | I2C1_SDA #1 | |
| N7 | PB12 | DAC0_OUT1 /<br>OPAMP_OUT1 | | LETIM0_OUT1 #1 | I2C1_SCL #1 | |
| N8 | AVSS_2 | Analog ground 2. | | | | |
| N9 | PB13 | HFXTAL_P | | | US0_CLK #4/5<br>LEU0_TX #1 | |
| N10 | PB14 | HFXTAL_N | | | US0_CS #4/5<br>LEU0_RX #1 | |
| N11 | AVDD_0 | Analog power supply 0. | | | | |
| N12 | PD2 | ADC0_CH2 | EBI_A27 #0/1/2 | TIM0_CC1 #3 | US1_CLK #1 | DBG_SWO #3 |
| N13 | PD5 | ADC0_CH5<br>OPAMP_OUT2 #0 | | | LEU0_RX #0 | ETM_TD3 #0/2 |

## 4.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in Table 4.2 (p. 62). The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note**

Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| EBI_REn | PF5 | PF9 | PF5 | | | | | External Bus Interface (EBI) Read Enable output. |
| EBI_VSNC | PA10 | PA10 | PA10 | | | | | External Bus Interface (EBI) TFT Vertical Synchronization pin. |
| EBI_WEn | PF4 | PF8 | PF4 | | | | | External Bus Interface (EBI) Write Enable output. |
| ETM_TCLK | PD7 | PF8 | PC6 | PA6 | | | | Embedded Trace Module ETM clock . |
| ETM_TD0 | PD6 | PF9 | PC7 | PA2 | | | | Embedded Trace Module ETM data 0. |
| ETM_TD1 | PD3 | PD13 | PD3 | PA3 | | | | Embedded Trace Module ETM data 1. |
| ETM_TD2 | PD4 | PB15 | PD4 | PA4 | | | | Embedded Trace Module ETM data 2. |
| ETM_TD3 | PD5 | PF3 | PD5 | PA5 | | | | Embedded Trace Module ETM data 3. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU1 | PA6 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU2 | PC9 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | PD15 | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | PD14 | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| I2C1_SCL | PC5 | PB12 | PE1 | | | | | I2C1 Serial Clock Line input / output. |
| I2C1_SDA | PC4 | PB11 | PE0 | | | | | I2C1 Serial Data input / output. |
| LES_ALTEX0 | PD6 | | | | | | | LESENSE alternate exite output 0. |
| LES_ALTEX1 | PD7 | | | | | | | LESENSE alternate exite output 1. |
| LES_ALTEX2 | PA3 | | | | | | | LESENSE alternate exite output 2. |
| LES_ALTEX3 | PA4 | | | | | | | LESENSE alternate exite output 3. |
| LES_ALTEX4 | PA5 | | | | | | | LESENSE alternate exite output 4. |
| LES_ALTEX5 | PE11 | | | | | | | LESENSE alternate exite output 5. |
| LES_ALTEX6 | PE12 | | | | | | | LESENSE alternate exite output 6. |
| LES_ALTEX7 | PE13 | | | | | | | LESENSE alternate exite output 7. |
| LES_CH0 | PC0 | | | | | | | LESENSE channel 0. |
| LES_CH1 | PC1 | | | | | | | LESENSE channel 1. |
| LES_CH2 | PC2 | | | | | | | LESENSE channel 2. |
| LES_CH3 | PC3 | | | | | | | LESENSE channel 3. |
| LES_CH4 | PC4 | | | | | | | LESENSE channel 4. |
| LES_CH5 | PC5 | | | | | | | LESENSE channel 5. |
| LES_CH6 | PC6 | | | | | | | LESENSE channel 6. |
| LES_CH7 | PC7 | | | | | | | LESENSE channel 7. |
| LES_CH8 | PC8 | | | | | | | LESENSE channel 8. |
| LES_CH9 | PC9 | | | | | | | LESENSE channel 9. |
| LES_CH10 | PC10 | | | | | | | LESENSE channel 10. |
| LES_CH11 | PC11 | | | | | | | LESENSE channel 11. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LES_CH12 | PC12 | | | | | | | LESENSE channel 12. |
| LES_CH13 | PC13 | | | | | | | LESENSE channel 13. |
| LES_CH14 | PC14 | | | | | | | LESENSE channel 14. |
| LES_CH15 | PC15 | | | | | | | LESENSE channel 15. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | | | | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | PB12 | PF1 | PC5 | | | | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | PE15 | PF1 | PA0 | | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | PE14 | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LEU1_RX | PC7 | PA6 | | | | | | LEUART1 Receive input. |
| LEU1_TX | PC6 | PA5 | | | | | | LEUART1 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | PE0 | PC0 | PD6 | | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | PE1 | PC1 | PD7 | | | | Pulse Counter PCNT0 input number 1. |
| PCNT1_S0IN | PC4 | PB3 | | | | | | Pulse Counter PCNT1 input number 0. |
| PCNT1_S1IN | PC5 | PB4 | | | | | | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | PD0 | PE8 | | | | | | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | PD1 | PE9 | | | | | | Pulse Counter PCNT2 input number 1. |
| PRS_CH0 | PA0 | PF3 | | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | PF4 | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | PF5 | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | PE8 | | | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | PF6 | PD1 | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | PF7 | PD2 | PC0 | PF1 | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | PF8 | PD3 | PC1 | PF2 | | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | PA3 | PC13 | PF3 | PC13 | PC2 | PF3 | | Timer 0 Complimentary Deat Time Insertion channel 0. |
| TIM0_CDTI1 | PA4 | PC14 | PF4 | PC14 | PC3 | PF4 | | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | PA5 | PC15 | PF5 | PC15 | PC4 | PF5 | | Timer 0 Complimentary Deat Time Insertion channel 2. |
| TIM1_CC0 | PC13 | PE10 | PB0 | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | PB1 | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | PB2 | PB11 | PC13 | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | PA8 | PA12 | PC8 | | | | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | PA9 | PA13 | PC9 | | | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | PA10 | PA14 | PC10 | | | | | Timer 2 Capture Compare input / output channel 2. |
| TIM3_CC0 | PE14 | PE0 | | | | | | Timer 3 Capture Compare input / output channel 0. |
| TIM3_CC1 | PE15 | PE1 | | | | | | Timer 3 Capture Compare input / output channel 1. |
| TIM3_CC2 | PA15 | PE2 | | | | | | Timer 3 Capture Compare input / output channel 2. |
| U0_RX | PF7 | PE1 | PA4 | PC15 | | | | UART0 Receive input. |
| U0_TX | PF6 | PE0 | PA3 | PC14 | | | | UART0 Transmit output. Also used as receive input in half duplex communication. |

# 5 PCB Layout and Soldering

## 5.1 Recommended PCB Layout

*Figure 5.1. BGA120 PCB Land Pattern*

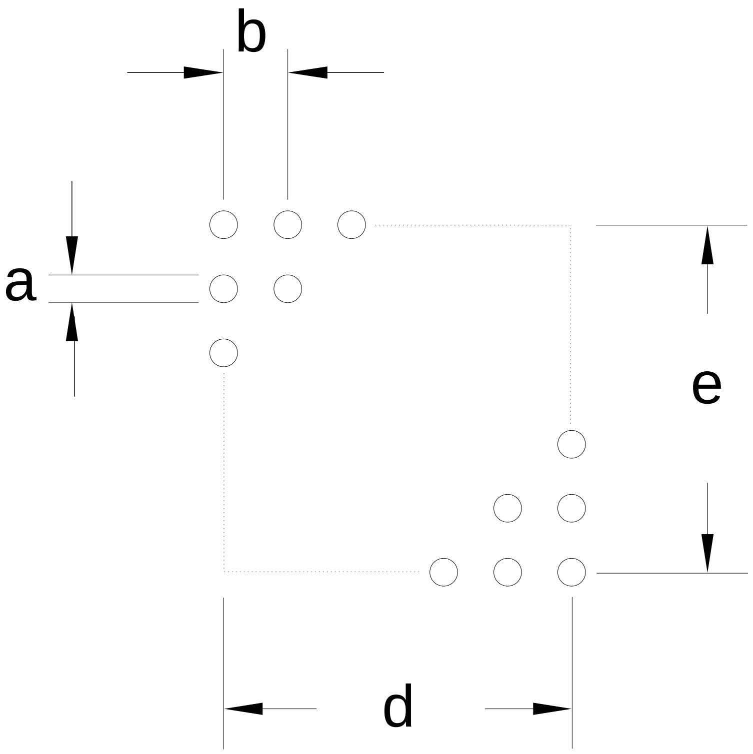


*Table 5.1. BGA120 PCB Land Pattern Dimensions (Dimensions in mm)*

| Symbol | Dim. (mm) |
|---|---|
| a | 0.25 |
| b | 0.50 |
| d | 6.00 |
| e | 6.00 |

# List of Equations