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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	EBI/EMI, I ² C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	93
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	120-VFBGA
Supplier Device Package	120-BGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32wg295f64-bga120t

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

2 System Summary

2.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M4, with DSP instruction support and floating-point unit, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32WG microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32WG295 devices. For a complete feature set and in-depth information on the modules, the reader is referred to the *EFM32WG Reference Manual*.

A block diagram of the EFM32WG295 is shown in Figure 2.1 (p. 3) .



Figure 2.1. Block Diagram

2.1.1 ARM Cortex-M4 Core

The ARM Cortex-M4 includes a 32-bit RISC processor, with DSP instruction support and floating-point unit, which can achieve as much as 1.25 Dhrystone MIPS/MHz. A Memory Protection Unit with support for up to 8 memory segments is included, as well as a Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep. The EFM32 implementation of the Cortex-M4 is described in detail in *ARM Cortex-M4 Devices Generic User Guide*.

2.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface and an Embedded Trace Module (ETM) for data/instruction tracing. In addition there is also a 1-wire Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages.

2.1.11 TFT Direct Drive

The EBI contains a TFT controller which can drive a TFT via a 565 RGB interface. The TFT controller supports programmable display and port sizes and offers accurate control of frequency and setup and hold timing. Direct Drive is supported for TFT displays which do not have their own frame buffer. In that case TFT Direct Drive can transfer data from either on-chip memory or from an external memory device to the TFT at low CPU load. Automatic alpha-blending and masking is also supported for transfers through the EBI interface.

2.1.12 Inter-Integrated Circuit Interface (I2C)

The I^2C module provides an interface between the MCU and a serial I^2C -bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the I^2C module, allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

2.1.13 Universal Synchronous/Asynchronous Receiver/Transmitter (US-ART)

The Universal Synchronous Asynchronous serial Receiver and Transmitter (USART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with ISO7816 SmartCards, IrDA and I2S devices.

2.1.14 Pre-Programmed UART Bootloader

The bootloader presented in application note AN0003 is pre-programmed in the device at factory. Autobaud and destructive write are supported. The autobaud feature, interface and commands are described further in the application note.

2.1.15 Universal Asynchronous Receiver/Transmitter (UART)

The Universal Asynchronous serial Receiver and Transmitter (UART) is a very flexible serial I/O module. It supports full- and half-duplex asynchronous UART communication.

2.1.16 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUARTTM, the Low Energy UART, is a UART that allows two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud/s. The LEUART includes all necessary hardware support to make asynchronous serial communication possible with minimum of software intervention and energy consumption.

2.1.17 Timer/Counter (TIMER)

The 16-bit general purpose Timer has 3 compare/capture channels for input capture and compare/Pulse-Width Modulation (PWM) output. TIMER0 also includes a Dead-Time Insertion module suitable for motor control applications.

2.1.18 Real Time Counter (RTC)

The Real Time Counter (RTC) contains a 24-bit counter and is clocked either by a 32.768 kHz crystal oscillator, or a 32.768 kHz RC oscillator. In addition to energy modes EM0 and EM1, the RTC is also

3 Electrical Characteristics

3.1 Test Conditions

3.1.1 Typical Values

The typical data are based on $T_{AMB}=25^{\circ}C$ and $V_{DD}=3.0$ V, as defined in Table 3.2 (p. 10), by simulation and/or technology characterisation unless otherwise specified.

3.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in Table 3.2 (p. 10), by simulation and/or technology characterisation unless otherwise specified.

3.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings, and functional operation under such conditions are not guaranteed. Stress beyond the limits specified in Table 3.1 (p. 10) may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in Table 3.2 (p. 10).

Symbol	Parameter	Condition	Min	Тур	Max	Unit
T _{STG}	Storage tempera- ture range		-40		150 ¹	°C
T _S	Maximum soldering temperature	Latest IPC/JEDEC J-STD-020 Standard			260	°C
V _{DDMAX}	External main sup- ply voltage		0		3.8	V
V _{IOPIN}	Voltage on any I/O pin		-0.3		V _{DD} +0.3	V

Table 3.1. Absolute Maximum Ratings

¹Based on programmed devices tested for 10000 hours at 150°C. Storage temperature affects retention of preprogrammed calibration values stored in flash. Please refer to the Flash section in the Electrical Characteristics for information on flash data retention for different temperatures.

3.3 General Operating Conditions

3.3.1 General Operating Conditions

Table 3.2. General Operating Conditions

Symbol	Parameter	Min	Тур	Мах	Unit
T _{AMB}	Ambient temperature range	-40		85	°C
V _{DDOP}	Operating supply voltage	1.98		3.8	V
f _{APB}	Internal APB clock frequency			48	MHz
f _{AHB}	Internal AHB clock frequency			48	MHz

Figure 3.22. Calibrated HFRCO 21 MHz Band Frequency vs Supply Voltage and Temperature



Figure 3.23. Calibrated HFRCO 28 MHz Band Frequency vs Supply Voltage and Temperature



3.9.5 AUXHFRCO

Table 3.13. AUXHFRCO

Symbol	Parameter	Condition	Min	Тур	Max	Unit
		28 MHz frequency band	27.5	28.0	28.5	MHz
		21 MHz frequency band	20.6	21.0	21.4	MHz
f	Oscillation frequen-	14 MHz frequency band	13.7	14.0	14.3	MHz
IAUXHFRCO	Cy, v _{DD} = 3.0 v, T _{AMB} =25°C	11 MHz frequency band	10.8	11.0	11.2	MHz
		7 MHz frequency band	6.48	6.60	6.72	MHz
		1 MHz frequency band	1.15	1.20	1.25	MHz
	_g Settling time after start-up	f _{AUXHFRCO} = 14 MHz		0.6		Cycles
DC _{AUXHFRCO}	Duty cycle	f _{AUXHFRCO} = 14 MHz	48.5	50	51	%
TUNESTEP _{AU} HFRCO	Frequency step for LSB change in TUNING value			0.3 ¹		%

¹The TUNING field in the CMU_AUXHFRCOCTRL register may be used to adjust the AUXHFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the AUXHFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

3.9.6 ULFRCO

Table 3.14. ULFRCO

Symbol	Parameter	Condition	Min	Тур	Max	Unit
f _{ULFRCO}	Oscillation frequen- cy	25°C, 3V	0.7		1.75	kHz
TC _{ULFRCO}	Temperature coeffi- cient			0.05		%/°C
VC _{ULFRCO}	Supply voltage co- efficient			-18.2		%/V

3.10 Analog Digital Converter (ADC)

Table 3.15. ADC

Symbol	Parameter	Condition	Min	Тур	Max	Unit
	Input voltage range	Single ended	0		V _{REF}	V
ADCIN	input voltage range	Differential	-V _{REF} /2		V _{REF} /2	V
VADCREFIN	Input range of exter- nal reference volt- age, single ended and differential		1.25		V _{DD}	V
V _{ADCREFIN_CH7}	Input range of ex- ternal negative ref- erence voltage on channel 7	See V _{ADCREFIN}	0		V _{DD} - 1.1	V
V _{ADCREFIN_CH6}	Input range of ex- ternal positive ref-	See V _{ADCREFIN}	0.625		V _{DD}	V



Symbol	Parameter	Condition	Min	Тур	Max	Unit
	erence voltage on channel 6					
V _{ADCCMIN}	Common mode in- put range		0		V _{DD}	V
	Input current	2pF sampling capacitors		<100		nA
CMRR _{ADC}	Analog input com- mon mode rejection ratio			65		dB
		1 MSamples/s, 12 bit, external reference		351		μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP- MODE in ADCn_CTRL set to 0b00		67		μΑ
I _{ADC}	Average active cur- rent	10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP- MODE in ADCn_CTRL set to 0b01		63		μΑ
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP- MODE in ADCn_CTRL set to 0b10		64		μΑ
I _{ADCREF}	Current consump- tion of internal volt- age reference	Internal voltage reference		65		μΑ
C _{ADCIN}	Input capacitance			2		pF
R _{ADCIN}	Input ON resistance		1			MOhm
R _{ADCFILT}	Input RC filter resis- tance			10		kOhm
C _{ADCFILT}	Input RC filter/de- coupling capaci- tance			250		fF
f _{ADCCLK}	ADC Clock Fre- quency				13	MHz
		6 bit	7			ADC- CLK Cycles
t _{ADCCONV}	Conversion time	8 bit	11			ADC- CLK Cycles
		12 bit	13			ADC- CLK Cycles
t _{ADCACQ}	Acquisition time	Programmable	1		256	ADC- CLK Cycles
t _{ADCACQVDD3}	Required acquisi- tion time for VDD/3 reference		2			μs
t _{ADCSTART}	Startup time of ref- erence generator			5		μs



Figure 3.24. Integral Non-Linearity (INL)



Figure 3.25. Differential Non-Linearity (DNL)



3.10.1 Typical performance

Figure 3.26. ADC Frequency Spectrum, Vdd = 3V, Temp = 25°C



3072

3072

3584

4096

3584

4096

Figure 3.27. ADC Integral Linearity Error vs Code, Vdd = 3V, Temp = 25°C





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Figure 3.28. ADC Differential Linearity Error vs Code, Vdd = 3V, Temp = 25°C





Figure 3.31. ADC Temperature sensor readout



3.11 Digital Analog Converter (DAC)

Table 3.16. DAC

Symbol	Parameter	Condition	Min	Тур	Мах	Unit
V	Output voltage	VDD voltage reference, single ended	0		V _{DD}	V
V DACOUT	range	VDD voltage reference, differ- ential	-V _{DD}		V _{DD}	V
V _{DACCM}	Output common mode voltage range		0		V _{DD}	V
	Active current in-	500 kSamples/s, 12 bit		400 ¹		μA
I _{DAC}	cluding references	100 kSamples/s, 12 bit		200 ¹		μA
	for 2 channels	1 kSamples/s 12 bit NORMAL		17 ¹		μA
SR _{DAC}	Sample rate				500	ksam- ples/s
	DAC clock frequen- cy	Continuous Mode			1000	kHz
f _{DAC}		Sample/Hold Mode			250	kHz
		Sample/Off Mode			250	kHz
CYC _{DACCONV}	Clock cyckles per conversion			2		
t _{DACCONV}	Conversion time		2			μs
t _{DACSETTLE}	Settling time			5		μs
SNR _{DAC}		500 kSamples/s, 12 bit, sin- gle ended, internal 1.25V refer- ence		58		dB
	Signal to Noise Ra- tio (SNR)	500 kSamples/s, 12 bit, single ended, internal 2.5V reference		59		dB
		500 kSamples/s, 12 bit, differ- ential, internal 1.25V reference		58		dB



Symbol	Parameter	Condition	Min	Тур	Max	Unit
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1, Unity Gain		13	25	μA
		(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0		101		dB
G _{OL}	Open Loop Gain	(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1		98		dB
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1		91		dB
		(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0		6.1		MHz
GBW _{OPAMP}	Gain Bandwidth Product	(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1		1.8		MHz
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1		0.25		MHz
		(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0, CL=75 pF		64		0
PM _{OPAMP}	Phase Margin	(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1, C _L =75 pF		58		o
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1, C _L =75 pF		58		0
R _{INPUT}	Input Resistance			100		Mohm
R _{LOAD}	Load Resistance		200			Ohm
I _{LOAD_DC}	DC Load Current				11	mA
Vinduz	Input Voltage	OPAxHCMDIS=0	V _{SS}		V_{DD}	V
VINPU1	input voltage	OPAxHCMDIS=1	V _{SS}		V _{DD} -1.2	V
V _{OUTPUT}	Output Voltage		V _{SS}		V_{DD}	V
Vereer	Input Offset Voltage	Unity Gain, V _{SS} <v<sub>in<v<sub>DD, OPAxHCMDIS=0</v<sub></v<sub>	-13	0	11	mV
VOFFSET	input Onset Voltage	Unity Gain, V _{SS} <v<sub>in<_{DD}-1.2, OPAxHCMDIS=1</v<sub>		1		mV
V _{OFFSET_DRIFT}	Input Offset Voltage Drift				0.02	mV/°C
		(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0		3.2		V/µs
SR _{OPAMP}	Slew Rate	(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1		0.8		V/µs
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1		0.1		V/µs
N	Voltage Notice	V _{out} =1V, RESSEL=0, 0.1 Hz <f<10 khz,="" opax-<br="">HCMDIS=0</f<10>		101		μV _{RMS}
N _{OPAMP}	Voltage Noise	V _{out} =1V, RESSEL=0, 0.1 Hz <f<10 khz,="" opax-<br="">HCMDIS=1</f<10>		141		μV _{RMS}



Figure 3.34. OPAMP Negative Power Supply Rejection Ratio



Figure 3.35. OPAMP Voltage Noise Spectral Density (Unity Gain) Vout=1V



Figure 3.36. OPAMP Voltage Noise Spectral Density (Non-Unity Gain)



3.13 Analog Comparator (ACMP)

Table 3.18. ACMP

Symbol	Parameter	Condition	Min	Тур	Max	Unit
V _{ACMPIN}	Input voltage range		0		V _{DD}	V
V _{ACMPCM}	ACMP Common Mode voltage range		0		V _{DD}	V
		BIASPROG=0b0000, FULL- BIAS=0 and HALFBIAS=1 in ACMPn_CTRL register		0.1	0.4	μA
I _{ACMP}	Active current	BIASPROG=0b1111, FULL- BIAS=0 and HALFBIAS=0 in ACMPn_CTRL register		2.87	15	μA
		BIASPROG=0b1111, FULL- BIAS=1 and HALFBIAS=0 in ACMPn_CTRL register		195	520	μA
IACMPREF	Current consump- tion of internal volt-	Internal voltage reference off. Using external voltage refer- ence		0		μA
	age reference	Internal voltage reference		5		μA
VACMPOFFSET	Offset voltage	BIASPROG= 0b1010, FULL- BIAS=0 and HALFBIAS=0 in ACMPn_CTRL register	-12	0	12	mV
V _{ACMPHYST}	ACMP hysteresis	Programmable		17		mV
		CSRESSEL=0b00 in ACMPn_INPUTSEL		39		kOhm
Decement	Capacitive Sense	CSRESSEL=0b01 in ACMPn_INPUTSEL		71		kOhm
KCSRES	Internal Resistance	CSRESSEL=0b10 in ACMPn_INPUTSEL		104		kOhm
		CSRESSEL=0b11 in ACMPn_INPUTSEL		136		kOhm
t _{ACMPSTART}	Startup time				10	μs

The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given in Equation 3.1 (p. 47). $I_{ACMPREF}$ is zero if an external voltage reference is used.

Total ACMP Active Current

 $I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF}$

(3.1)

Table 3.29. SPI Master Timing with SSSEARLY and SMSDELAY

Symbol	Parameter	Condition	Min	Тур	Мах	Unit
t _{SCLK} ¹²	SCLK period		2 * t _{HFPER-} CLK			ns
t _{CS_MO} ¹²	CS to MOSI		-2.00		2.00	ns
t _{SCLK_MO} ¹²	SCLK to MOSI		-1.00		3.00	ns
t _{SU_MI} 12	MISO setup time	IOVDD = 3.0 V	-32.00			ns
t _{H_MI} 12	MISO hold time		63.00			ns

¹Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)

 $^2\text{Measurement}$ done at 10% and 90% of V_DD (figure shows 50% of $_\text{VDD})$

Figure 3.44. SPI Slave Timing



Table 3.30. SPI Slave Timing

Symbol	Parameter	Min	Тур	Max	Unit
t _{SCLK_} sl ^{1 2}	SCKL period	6 * t _{HFPER-} CLK			ns
t _{SCLK_hi} ^{1 2}	SCLK high period	3 * t _{HFPER-} CLK			ns
t _{SCLK_lo} ¹²	SCLK low period	3 * t _{HFPER-} CLK			ns
t _{CS_ACT_MI} ¹²	CS active to MISO	5.00		35.00	ns
t _{CS_DIS_MI} ¹²	CS disable to MISO	5.00		35.00	ns
t _{SU_MO} ^{1 2}	MOSI setup time	5.00			ns
t _{H_MO} ^{1 2}	MOSI hold time	2 + 2 * t _{HF-} PERCLK			ns
t _{SCLK_MI} ¹²	SCLK to MISO	7 + t _{HFPER-} CLK		42 + 2 * t _{HFPERCLK}	ns

¹Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0) 2 Measurement done at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

Table 3.31. SPI Slave Timing with SSSEARLY and SMSDELAY

Symbol	Parameter	Min	Тур	Max	Unit
t _{SCLK_sl} 12	SCKL period	6 * t _{HFPER-}			ns
		CLK			

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Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
EBI_A25	PC2	PC2	PC2					External Bus Interface (EBI) address output pin 25.
EBI_A26	PC4	PC4	PC4					External Bus Interface (EBI) address output pin 26.
EBI_A27	PD2	PD2	PD2					External Bus Interface (EBI) address output pin 27.
EBI_AD00	PE8	PE8	PE8					External Bus Interface (EBI) address and data input / output pin 00.
EBI_AD01	PE9	PE9	PE9					External Bus Interface (EBI) address and data input / output pin 01.
EBI_AD02	PE10	PE10	PE10					External Bus Interface (EBI) address and data input / output pin 02.
EBI_AD03	PE11	PE11	PE11					External Bus Interface (EBI) address and data input / output pin 03.
EBI_AD04	PE12	PE12	PE12					External Bus Interface (EBI) address and data input / output pin 04.
EBI_AD05	PE13	PE13	PE13					External Bus Interface (EBI) address and data input / output pin 05.
EBI_AD06	PE14	PE14	PE14					External Bus Interface (EBI) address and data input / output pin 06.
EBI_AD07	PE15	PE15	PE15					External Bus Interface (EBI) address and data input / output pin 07.
EBI_AD08	PA15	PA15	PA15					External Bus Interface (EBI) address and data input / output pin 08.
EBI_AD09	PA0	PA0	PA0					External Bus Interface (EBI) address and data input / output pin 09.
EBI_AD10	PA1	PA1	PA1					External Bus Interface (EBI) address and data input / output pin 10.
EBI_AD11	PA2	PA2	PA2					External Bus Interface (EBI) address and data input / output pin 11.
EBI_AD12	PA3	PA3	PA3					External Bus Interface (EBI) address and data input / output pin 12.
EBI_AD13	PA4	PA4	PA4					External Bus Interface (EBI) address and data input / output pin 13.
EBI_AD14	PA5	PA5	PA5					External Bus Interface (EBI) address and data input / output pin 14.
EBI_AD15	PA6	PA6	PA6					External Bus Interface (EBI) address and data input / output pin 15.
EBI_ALE	PF3	PC11	PC11					External Bus Interface (EBI) Address Latch Enable output.
EBI_ARDY	PF2	PF2	PF2					External Bus Interface (EBI) Hardware Ready Control input.
EBI_BL0	PF6	PF6	PF6					External Bus Interface (EBI) Byte Lane/Enable pin 0.
EBI_BL1	PF7	PF7	PF7					External Bus Interface (EBI) Byte Lane/Enable pin 1.
EBI_CS0	PD9	PD9	PD9					External Bus Interface (EBI) Chip Select output 0.
EBI_CS1	PD10	PD10	PD10					External Bus Interface (EBI) Chip Select output 1.
EBI_CS2	PD11	PD11	PD11					External Bus Interface (EBI) Chip Select output 2.
EBI_CS3	PD12	PD12	PD12					External Bus Interface (EBI) Chip Select output 3.
EBI_CSTFT	PA7	PA7	PA7					External Bus Interface (EBI) Chip Select output TFT.
EBI_DCLK	PA8	PA8	PA8					External Bus Interface (EBI) TFT Dot Clock pin.
EBI_DTEN	PA9	PA9	PA9					External Bus Interface (EBI) TFT Data Enable pin.
EBI_HSNC	PA11	PA11	PA11					External Bus Interface (EBI) TFT Horizontal Synchronization pin.
EBI_NANDREn	PC3	PC3	PC3					External Bus Interface (EBI) NAND Read Enable output.
EBI_NANDWEn	PC5	PC5	PC5					External Bus Interface (EBI) NAND Write Enable output.



Alternate			L	OCATIC	N			
Functionality	0	1	2	3	4	5	6	Description
U1_RX	PC13	PF11	PB10	PE3				UART1 Receive input.
U1_TX	PC12	PF10	PB9	PE2				UART1 Transmit output. Also used as receive input in half duplex communication.
US0_CLK	PE12	PE5	PC9	PC15	PB13	PB13		USART0 clock input / output.
US0_CS	PE13	PE4	PC8	PC14	PB14	PB14		USART0 chip select input / output.
	DE44	DEC	DO10	DE40	DDa	DOA		USART0 Asynchronous Receive.
050_KX	PETT	PEO	PC10	PE12	PB8	PC1		USART0 Synchronous mode Master Input / Slave Output (MISO).
								USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.
US0_TX	PE10	PE7	PC11	PE13	PB7	PC0		USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2	PF0					USART1 clock input / output.
US1_CS	PB8	PD3	PF1					USART1 chip select input / output.
								USART1 Asynchronous Receive.
US1_RX	PC1	PD1	PD6					USART1 Synchronous mode Master Input / Slave Output (MISO).
	Doo		507					USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.
051_1X	PCU	PD0	PD7					USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4	PB5						USART2 clock input / output.
US2_CS	PC5	PB6						USART2 chip select input / output.
								USART2 Asynchronous Receive.
US2_RX	PC3	PB4						USART2 Synchronous mode Master Input / Slave Output (MISO).
	DCC	DDO						USART2 Asynchronous Transmit.Also used as receive input in half duplex communication.
052_13	P62	PB3						USART2 Synchronous mode Master Output / Slave Input (MOSI).

4.3 GPIO Pinout Overview

The specific GPIO pins available in *EFM32WG295* is shown in Table 4.3 (p. 67). Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port in indicated by a number from 15 down to 0.

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Port B	PB15	PB14	PB13	PB12	PB11	PB10	PB9	PB8	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Port C	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Port D	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Port F	-	-	-	PF12	PF11	PF10	PF9	PF8	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0

Table 4.3. GPIO Pinout

4.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32WG295 is shown in Figure 4.2 (p. 68).

A Disclaimer and Trademarks

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