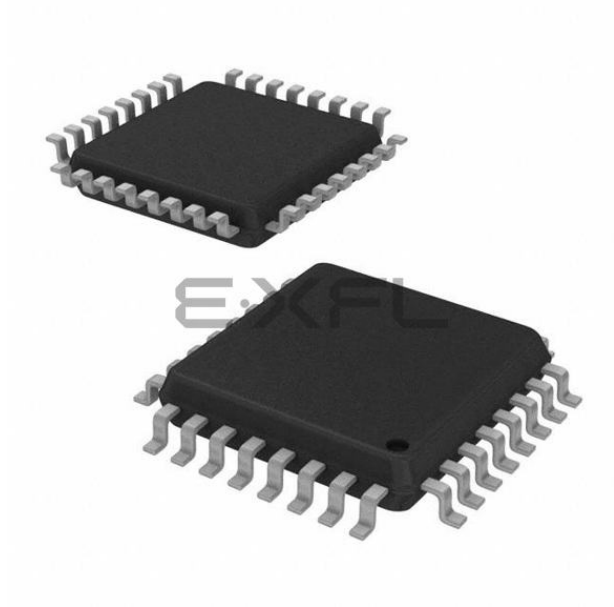

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SIO, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	29
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f632kpmc-g-sne2

Part number / Parameter	MB95F632H	MB95F633H	MB95F634H	MB95F636H	MB95F632K	MB95F633K	MB95F634K	MB95F636K
External interrupt	10 channels							
	• Interrupt by edge detection (The rising edge, falling edge, and both edges can be selected.) • It can be used to wake up the device from different standby modes.							
On-chip debug	• 1-wire serial control • It supports serial writing (asynchronous mode).							
UART/SIO	1 channel							
	• Data transfer with UART/SIO is enabled. • It has a full duplex double buffer, variable data length (5/6/7/8 bits), an internal baud rate generator and an error detection function. • It uses the NRZ type transfer format. • LSB-first data transfer and MSB-first data transfer are available to use. • Both clock asynchronous (UART) serial data transfer and clock synchronous (SIO) serial data transfer are enabled.							
I^2C bus interface	1 channel							
	• Master/slave transmission and reception • It has the following functions: bus error function, arbitration function, transfer direction detection function, wake-up function, and functions of generating and detecting repeated START conditions.							
8/16-bit PPG	3 channels							
	• Each channel can be used as an “8-bit timer × 2 channels” or a “16-bit timer × 1 channel”. • The counter operating clock can be selected from eight clock sources.							
16-bit PPG timer	1 channel							
	• PWM mode and one-shot mode are available to use. • The counter operating clock can be selected from eight clock sources. • It supports external trigger start. • It can work independently or together with the multi-pulse generator.							
16-bit reload timer	1 channel							
	• Two clock modes and two counter operating modes are available to use. • It can output square wave. • Count clock: it can be selected from internal clocks (seven types) and external clocks. • Two counter operating modes: reload mode and one-shot mode • It can work independently or together with the multi-pulse generator.							
Multi-pulse generator (for DC motor control)	• 16-bit PPG timer: 1 channel • 16-bit reload timer operations: toggle output, one-shot output • Event counter: 1 channel • Waveform sequencer (including a 16-bit timer equipped with a buffer and a compare clear function)							
Watch prescaler	Eight different time intervals can be selected.							
Comparator	1 channel							

<table>
<tr><th>Part number
Parameter</th><th>MB95F632H</th><th>MB95F633H</th><th>MB95F634H</th><th>MB95F636H</th><th>MB95F632K</th><th>MB95F633K</th><th>MB95F634K</th><th>MB95F636K</th></tr>
<tr><td>Flash memory</td><td colspan="8">• It supports automatic programming (Embedded Algorithm), and program/erase/erase-suspend/erase-resume commands.
• It has a flag indicating the completion of the operation of Embedded Algorithm.
• Flash security feature for protecting the content of the Flash memory
<table><tr><td>Number of program/erase cycles</td><td>1000</td><td>10000</td><td>100000</td></tr><tr><td>Data retention time</td><td>20 years</td><td>10 years</td><td>5 years</td></tr></table></td></tr>
<tr><td>Standby mode</td><td colspan="8">There are four standby modes as follows:
• Stop mode
• Sleep mode
• Watch mode
• Time-base timer mode
In standby mode, two further options can be selected: normal standby mode and deep standby mode.</td></tr>
<tr><td>Package</td><td colspan="8">LQB032
PDS032
WNP032</td></tr>
</table>

2. Packages And Corresponding Products

Part number / Package	MB95F632H	MB95F633H	MB95F634H	MB95F636H	MB95F632K	MB95F633K	MB95F634K	MB95F636K
LQB032	O	O	O	O	O	O	O	O
PDS032	O	O	O	O	O	O	O	O
WNP032	O	O	O	O	O	O	O	O

O: Available

3. Differences Among Products And Notes On Product Selection

- Current consumption
  When using the on-chip debug function, take account of the current consumption of Flash memory program/erase.
  For details of current consumption, see “Electrical Characteristics”.

- Package
  For details of information on each package, see “Packages And Corresponding Products” and “Package Dimension”.

- Operating voltage
  The operating voltage varies, depending on whether the on-chip debug function is used or not.
  For details of operating voltage, see “Electrical Characteristics”.

- On-chip debug function

5. Pin Functions

Pin no.		Pin name	I/O circuit type*4	Function	I/O type			
LQFP32*1, QFN32*2	SH-DIP32*3				Input	Output	OD*5	PU*6
1	5	PG2	C	General-purpose I/O port	Hysteresis	CMOS	—	O
		X1A		Subclock I/O oscillation pin				
		SNI2		Trigger input pin for the position detection function of the MPG waveform sequencer				
2	6	PG1	C	General-purpose I/O port	Hysteresis	CMOS	—	O
		X0A		Subclock input oscillation pin				
		SNI1		Trigger input pin for the position detection function of the MPG waveform sequencer				
3	7	V_{CC}	—	Power supply pin	—	—	—	—
4	8	C	—	Decoupling capacitor connection pin	—	—	—	—
5	9	P67	D	General-purpose I/O port High-current pin	Hysteresis	CMOS	—	O
		PPG21		8/16-bit PPG ch. 2 output pin				
		TRG1		16-bit PPG timer ch. 1 trigger input pin				
		OPT5		MPG waveform sequencer output pin				
6	10	P66	D	General-purpose I/O port High-current pin	Hysteresis	CMOS	—	O
		PPG20		8/16-bit PPG ch. 2 output pin				
		PPG1		16-bit PPG timer ch. 1 output pin				
		OPT4		MPG waveform sequencer output pin				
7	11	P65	D	General-purpose I/O port High-current pin	Hysteresis	CMOS	—	O
		PPG11		8/16-bit PPG ch. 1 output pin				
		OPT3		MPG waveform sequencer output pin				
8	12	P64	D	General-purpose I/O port High-current pin	Hysteresis	CMOS	—	O
		EC1		8/16-bit composite timer ch. 1 clock input pin				
		PPG10		8/16-bit PPG ch. 1 output pin				
		OPT2		MPG waveform sequencer output pin				

Pin no.		Pin name	I/O circuit type*4	Function	I/O type			
LQFP32*1, QFN32*2	SH-DIP32*3				Input	Output	OD*5	PU*6
22	26	P11	G	General-purpose I/O port	Hysteresis	CMOS	—	O
		PPG11		8/16-bit PPG ch. 1 output pin				
23	27	P12	H	General-purpose I/O port	Hysteresis	CMOS	O	—
		DBG		DBG input pin				
		EC0		8/16-bit composite timer ch. 0 clock input pin				
24	28	P13	G	General-purpose I/O port	Hysteresis	CMOS	—	O
		PPG00		8/16-bit PPG ch. 0 output pin				
25	29	P14	G	General-purpose I/O port	Hysteresis	CMOS	—	O
		UCK0		UART/SIO ch. 0 clock I/O pin				
		PPG01		8/16-bit PPG ch. 0 output pin				
26	30	P15	G	General-purpose I/O port	Hysteresis	CMOS	—	O
		UO0		UART/SIO ch. 0 data output pin				
		PPG20		8/16-bit PPG ch. 2 output pin				
27	31	P16	J	General-purpose I/O port	CMOS	CMOS	—	O
		UI0		UART/SIO ch. 0 data input pin				
		PPG21		8/16-bit PPG ch. 2 output pin				
28	32	P17	G	General-purpose I/O port	Hysteresis	CMOS	—	O
		TO1		16-bit reload timer ch. 1 output pin				
		SNI0		Trigger input pin for the position detection function of the MPG waveform sequencer				
29	1	PF2	A	General-purpose I/O port	Hysteresis	CMOS	O	—
		$\overline{RST}$		Reset pin Dedicated reset pin on MB95F632H/F633H/F634H/ F636H				
30	2	PF0	B	General-purpose I/O port	Hysteresis	CMOS	—	—
		X0		Main clock input oscillation pin				
31	3	PF1	B	General-purpose I/O port	Hysteresis	CMOS	—	—
		X1		Main clock I/O oscillation pin				
32	4	V_{SS}	—	Power supply pin (GND)	—	—	—	—

O: Available

*1: LQB032
*2: WNP032
*3: PDS032

*4: For the I/O circuit types, see “I/O Circuit Type”.
*5: N-ch open drain
*6: Pull-up

causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

- **Surface Mount Type**

  Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

  You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

- **Lead-Free Packaging**

  CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

- **Storage of Semiconductor Devices**

  Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

  (1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.

  (2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
  When you open Dry Package that recommends humidity 40% to 70% relative humidity.

  (3) When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.

  (4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

- **Baking**

  Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

  Condition: 125°C/24 h

- **Static Electricity**

  Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

  (1) Maintain relative humidity in the working environment between 40% and 70%.
  Use of an apparatus for ion generation may be needed to remove electricity.

  (2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.

  (3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
  Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.

  (4) Ground all fixtures and instruments, or protect with anti-static measures.

  (5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

9. Pin Connection

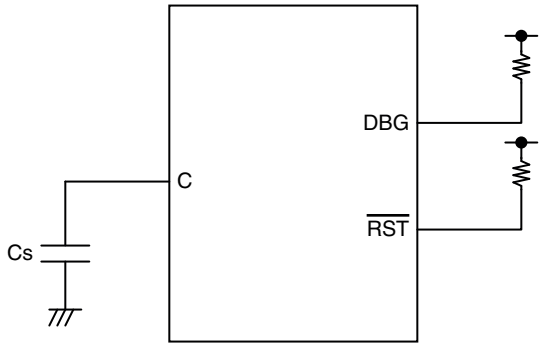
- Treatment of unused pins
  If an unused input pin is left unconnected, a component may be permanently damaged due to malfunctions or latch-ups. Always pull up or pull down an unused input pin through a resistor of at least 2 kΩ. Set an unused input/output pin to the output state and leave it unconnected, or set it to the input state and treat it the same as an unused input pin. If there is an unused output pin, leave it unconnected.

- Power supply pins
  To reduce unnecessary electro-magnetic emission, prevent malfunctions of strobe signals due to an increase in the ground level, and conform to the total output current standard, always connect the V_{CC} pin and the V_{SS} pin to the power supply and ground outside the device. In addition, connect the current supply source to the V_{CC} pin and the V_{SS} pin with low impedance.
  It is also advisable to connect a ceramic capacitor of approximately 0.1 µF as a bypass capacitor between the V_{CC} pin and the V_{SS} pin at a location close to this device.

- DBG pin
  Connect the DBG pin to an external pull-up resistor of 2 kΩ or above.
  After power-on, ensure that the DBG pin does not stay at “L” level until the reset output is released.
  The DBG pin becomes a communication pin in debug mode. Since the actual pull-up resistance depends on the tool used and the interconnection length, refer to the tool document when selecting a pull-up resistor.

- $\overline{RST}$ pin
  Connect the $\overline{RST}$ pin to an external pull-up resistor of 2 kΩ or above.
  To prevent the device from unintentionally entering the reset mode due to noise, minimize the interconnection length between a pull-up resistor and the $\overline{RST}$ pin and that between a pull-up resistor and the V_{CC} pin when designing the layout of the printed circuit board.
  The PF2/$\overline{RST}$ pin functions as the reset input/output pin after power-on. In addition, the reset output of the PF2/$\overline{RST}$ pin can be enabled by the RSTOE bit in the SYSC register, and the reset input function and the general-purpose I/O function can be selected by the RSTEN bit in the SYSC register.
- C pin
  Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The decoupling capacitor for the V_{CC} pin must have a capacitance equal to or larger than the capacitance of C_S. For the connection to a decoupling capacitor C_S, see the diagram below. To prevent the device from unintentionally entering a mode to which the device is not set to transit due to noise, minimize the distance between the C pin and C_S and the distance between C_S and the V_{SS} pin when designing the layout of a printed circuit board.

- DBG/$\overline{RST}$/C pins connection diagram



- Note on serial communication
  In serial communication, reception of wrong data may occur due to noise or other causes. Therefore, design a printed

14. I/O Map

Address	Register abbreviation	Register name	R/W	Initial value
0x0000	PDR0	Port 0 data register	R/W	0b00000000
0x0001	DDR0	Port 0 direction register	R/W	0b00000000
0x0002	PDR1	Port 1 data register	R/W	0b00000000
0x0003	DDR1	Port 1 direction register	R/W	0b00000000
0x0004	—	(Disabled)	—	—
0x0005	WATR	Oscillation stabilization wait time setting register	R/W	0b11111111
0x0006	PLLC	PLL control register	R/W	0b000X0000
0x0007	SYCC	System clock control register	R/W	0bXXX11011
0x0008	STBC	Standby control register	R/W	0b00000000
0x0009	RSRR	Reset source register	R/W	0b000XXXXX
0x000A	TBTC	Time-base timer control register	R/W	0b00000000
0x000B	WPCR	Watch prescaler control register	R/W	0b00000000
0x000C	WDTC	Watchdog timer control register	R/W	0b00XX0000
0x000D	SYCC2	System clock control register 2	R/W	0bXXXX0011
0x000E	STBC2	Standby control register 2	R/W	0b00000000
0x000F to 0x0015	—	(Disabled)	—	—
0x0016	PDR6	Port 6 data register	R/W	0b00000000
0x0017	DDR6	Port 6 direction register	R/W	0b00000000
0x0018 to 0x0027	—	(Disabled)	—	—
0x0028	PDRF	Port F data register	R/W	0b00000000
0x0029	DDRF	Port F direction register	R/W	0b00000000
0x002A	PDRG	Port G data register	R/W	0b00000000
0x002B	DDRG	Port G direction register	R/W	0b00000000
0x002C	PUL0	Port 0 pull-up register	R/W	0b00000000
0x002D	PUL1	Port 1 pull-up register	R/W	0b00000000
0x002E to 0x0032	—	(Disabled)	—	—
0x0033	PUL6	Port 6 pull-up register	R/W	0b00000000
0x0034	—	(Disabled)	—	—
0x0035	PULG	Port G pull-up register	R/W	0b00000000
0x0036	T01CR1	8/16-bit composite timer 01 status control register 1	R/W	0b00000000

Address	Register abbreviation	Register name	R/W	Initial value
0x0037	T00CR1	8/16-bit composite timer 00 status control register 1	R/W	0b00000000
0x0038	T11CR1	8/16-bit composite timer 11 status control register 1	R/W	0b00000000
0x0039	T10CR1	8/16-bit composite timer 10 status control register 1	R/W	0b00000000
0x003A	PC01	8/16-bit PPG timer 01 control register	R/W	0b00000000
0x003B	PC00	8/16-bit PPG timer 00 control register	R/W	0b00000000
0x003C	PC11	8/16-bit PPG timer 11 control register	R/W	0b00000000
0x003D	PC10	8/16-bit PPG timer 10 control register	R/W	0b00000000
0x003E	PC21	8/16-bit PPG timer 21 control register	R/W	0b00000000
0x003F	PC20	8/16-bit PPG timer 20 control register	R/W	0b00000000
0x0040	TMCSRH1	16-bit reload timer control status register (upper)	R/W	0b00000000
0x0041	TMCSRL1	16-bit reload timer control status register (lower)	R/W	0b00000000
0x0042	CMR0C	Comparator control register	R/W	0b00000101
0x0043	—	(Disabled)	—	—
0x0044	PCNTH1	16-bit PPG status control register (upper)	R/W	0b00000000
0x0045	PCNTL1	16-bit PPG status control register (lower)	R/W	0b00000000
0x0046, 0x0047	—	(Disabled)	—	—
0x0048	EIC00	External interrupt circuit control register ch. 0/ch. 1	R/W	0b00000000
0x0049	EIC10	External interrupt circuit control register ch. 2/ch. 3	R/W	0b00000000
0x004A	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	0b00000000
0x004B	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	0b00000000
0x004C	EIC01	External interrupt circuit control register ch. 8/ch. 9	R/W	0b00000000
0x004D	—	(Disabled)	—	—
0x004E	LVDR	LVD reset voltage selection ID register	R/W	0b00000000
0x004F	—	(Disabled)	—	—
0x0050	SCR	LIN-UART serial control register	R/W	0b00000000
0x0051	SMR	LIN-UART serial mode register	R/W	0b00000000
0x0052	SSR	LIN-UART serial status register	R/W	0b00001000
0x0053	RDR	LIN-UART receive data register	R/W	0b00000000
	TDR	LIN-UART transmit data register		
0x0054	ESCR	LIN-UART extended status control register	R/W	0b00000100
0x0055	ECCR	LIN-UART extended communication control register	R/W	0b000000XX
0x0056	SMC10	UART/SIO serial mode control register 1	R/W	0b00000000
0x0057	SMC20	UART/SIO serial mode control register 2	R/W	0b00100000
0x0058	SSR0	UART/SIO serial status and data register	R/W	0b00000001
0x0059	TDR0	UART/SIO serial output data register	R/W	0b00000000

Address	Register abbreviation	Register name	R/W	Initial value
0x0F80	WRARH0	Wild register address setting register (upper) ch. 0	R/W	0b00000000
0x0F81	WRARL0	Wild register address setting register (lower) ch. 0	R/W	0b00000000
0x0F82	WRDR0	Wild register data setting register ch. 0	R/W	0b00000000
0x0F83	WRARH1	Wild register address setting register (upper) ch. 1	R/W	0b00000000
0x0F84	WRARL1	Wild register address setting register (lower) ch. 1	R/W	0b00000000
0x0F85	WRDR1	Wild register data setting register ch. 1	R/W	0b00000000
0x0F86	WRARH2	Wild register address setting register (upper) ch. 2	R/W	0b00000000
0x0F87	WRARL2	Wild register address setting register (lower) ch. 2	R/W	0b00000000
0x0F88	WRDR2	Wild register data setting register ch. 2	R/W	0b00000000
0x0F89 to 0x0F91	—	(Disabled)	—	—
0x0F92	T01CR0	8/16-bit composite timer 01 status control register 0	R/W	0b00000000
0x0F93	T00CR0	8/16-bit composite timer 00 status control register 0	R/W	0b00000000
0x0F94	T01DR	8/16-bit composite timer 01 data register	R/W	0b00000000
0x0F95	T00DR	8/16-bit composite timer 00 data register	R/W	0b00000000
0x0F96	TMCR0	8/16-bit composite timer 00/01 timer mode control register	R/W	0b00000000
0x0F97	T11CR0	8/16-bit composite timer 11 status control register 0	R/W	0b00000000
0x0F98	T10CR0	8/16-bit composite timer 10 status control register 0	R/W	0b00000000
0x0F99	T11DR	8/16-bit composite timer 11 data register	R/W	0b00000000
0x0F9A	T10DR	8/16-bit composite timer 10 data register	R/W	0b00000000
0x0F9B	TMCR1	8/16-bit composite timer 10/11 timer mode control register	R/W	0b00000000
0x0F9C	PPS01	8/16-bit PPG01 cycle setting buffer register	R/W	0b11111111
0x0F9D	PPS00	8/16-bit PPG00 cycle setting buffer register	R/W	0b11111111
0x0F9E	PDS01	8/16-bit PPG01 duty setting buffer register	R/W	0b11111111
0x0F9F	PDS00	8/16-bit PPG00 duty setting buffer register	R/W	0b11111111
0x0FA0	PPS11	8/16-bit PPG11 cycle setting buffer register	R/W	0b11111111
0x0FA1	PPS10	8/16-bit PPG10 cycle setting buffer register	R/W	0b11111111
0x0FA2	PDS11	8/16-bit PPG11 duty setting buffer register	R/W	0b11111111
0x0FA3	PDS10	8/16-bit PPG10 duty setting buffer register	R/W	0b11111111
0x0FA4	PPGS	8/16-bit PPG start register	R/W	0b00000000
0x0FA5	REVC	8/16-bit PPG output inversion register	R/W	0b00000000
0x0FA6	PPS21	8/16-bit PPG21 cycle setting buffer register	R/W	0b11111111
0x0FA7	PPS20	8/16-bit PPG20 cycle setting buffer register	R/W	0b11111111

Address	Register abbreviation	Register name	R/W	Initial value
0x0FA8	TMRH1	16-bit reload timer timer register (upper)	R/W	0b00000000
	TMRLRH1	16-bit reload timer reload register (upper)		
0x0FA9	TMRL1	16-bit reload timer timer register (lower)	R/W	0b00000000
	TMRLRL1	16-bit reload timer reload register (lower)		
0x0FAA	PDS21	8/16-bit PPG21 duty setting buffer register	R/W	0b11111111
0x0FAB	PDS20	8/16-bit PPG20 duty setting buffer register	R/W	0b11111111
0x0FAC to 0x0FAF	—	(Disabled)	—	—
0x0FB0	PDCRH1	16-bit PPG downcounter register (upper)	R	0b00000000
0x0FB1	PDCRL1	16-bit PPG downcounter register (lower)	R	0b00000000
0x0FB2	PCSRH1	16-bit PPG cycle setting buffer register (upper)	R/W	0b11111111
0x0FB3	PCSRL1	16-bit PPG cycle setting buffer register (lower)	R/W	0b11111111
0x0FB4	PDUTH1	16-bit PPG duty setting buffer register (upper)	R/W	0b11111111
0x0FB5	PDUTL1	16-bit PPG duty setting buffer register (lower)	R/W	0b11111111
0x0FB6 to 0x0FBB	—	(Disabled)	—	—
0x0FBC	BGR1	LIN-UART baud rate generator register 1	R/W	0b00000000
0x0FBD	BGR0	LIN-UART baud rate generator register 0	R/W	0b00000000
0x0FBE	PSSR0	UART/SIO dedicated baud rate generator prescaler select register	R/W	0b00000000
0x0FBF	BRSR0	UART/SIO dedicated baud rate generator baud rate setting register	R/W	0b00000000
0x0FC0 to 0x0FC2	—	(Disabled)	—	—
0x0FC3	AIDRL	A/D input disable register (lower)	R/W	0b00000000
0x0FC4	OPDBRH0	16-bit MPG output data buffer register (upper) ch. 0	R/W	0b00000000
0x0FC5	OPDBRL0	16-bit MPG output data buffer register (lower) ch. 0	R/W	0b00000000
0x0FC6	OPDBRH1	16-bit MPG output data buffer register (upper) ch. 1	R/W	0b00000000
0x0FC7	OPDBRL1	16-bit MPG output data buffer register (lower) ch. 1	R/W	0b00000000
0x0FC8	OPDBRH2	16-bit MPG output data buffer register (upper) ch. 2	R/W	0b00000000
0x0FC9	OPDBRL2	16-bit MPG output data buffer register (lower) ch. 2	R/W	0b00000000
0x0FCA	OPDBRH3	16-bit MPG output data buffer register (upper) ch. 3	R/W	0b00000000
0x0FCB	OPDBRL3	16-bit MPG output data buffer register (lower) ch. 3	R/W	0b00000000
0x0FCC	OPDBRH4	16-bit MPG output data buffer register (upper) ch. 4	R/W	0b00000000
0x0FCD	OPDBRL4	16-bit MPG output data buffer register (lower) ch. 4	R/W	0b00000000

Address	Register abbreviation	Register name	R/W	Initial value
0x0FCE	OPDBRH5	16-bit MPG output data buffer register (upper) ch. 5	R/W	0b00000000
0x0FCF	OPDBRL5	16-bit MPG output data buffer register (lower) ch. 5	R/W	0b00000000
0x0FD0	OPDBRH6	16-bit MPG output data buffer register (upper) ch. 6	R/W	0b00000000
0x0FD1	OPDBRL6	16-bit MPG output data buffer register (lower) ch. 6	R/W	0b00000000
0x0FD2	OPDBRH7	16-bit MPG output data buffer register (upper) ch. 7	R/W	0b00000000
0x0FD3	OPDBRL7	16-bit MPG output data buffer register (lower) ch. 7	R/W	0b00000000
0x0FD4	OPDBRH8	16-bit MPG output data buffer register (upper) ch. 8	R/W	0b00000000
0x0FD5	OPDBRL8	16-bit MPG output data buffer register (lower) ch. 8	R/W	0b00000000
0x0FD6	OPDBRH9	16-bit MPG output data buffer register (upper) ch. 9	R/W	0b00000000
0x0FD7	OPDBRL9	16-bit MPG output data buffer register (lower) ch. 9	R/W	0b00000000
0x0FD8	OPDBRHA	16-bit MPG output data buffer register (upper) ch. A	R/W	0b00000000
0x0FD9	OPDBRLA	16-bit MPG output data buffer register (lower) ch. A	R/W	0b00000000
0x0FDA	OPDBRHB	16-bit MPG output data buffer register (upper) ch. B	R/W	0b00000000
0x0FDB	OPDBRLB	16-bit MPG output data buffer register (lower) ch. B	R/W	0b00000000
0x0FDC	OPDUR	16-bit MPG output data register (upper)	R	0b0000XXXX
0x0FDD	OPDLR	16-bit MPG output data register (lower)	R	0bXXXXXXXX
0x0FDE	CPCUR	16-bit MPG compare clear register (upper)	R/W	0bXXXXXXXX
0x0FDF	CPCLR	16-bit MPG compare clear register (lower)	R/W	0bXXXXXXXX
0x0FE0, 0x0FE1	—	(Disabled)	—	—
0x0FE2	TMBUR	16-bit MPG timer buffer register (upper)	R	0bXXXXXXXX
0x0FE3	TMBLR	16-bit MPG timer buffer register (lower)	R	0bXXXXXXXX
0x0FE4	CRTH	Main CR clock trimming register (upper)	R/W	0b000XXXXX
0x0FE5	CRTL	Main CR clock trimming register (lower)	R/W	0b000XXXXX
0x0FE6	—	(Disabled)	—	—
0x0FE7	CRTDA	Main CR clock temperature dependent adjustment register	R/W	0b000XXXXX
0x0FE8	SYSC	System configuration register	R/W	0b11000011
0x0FE9	CMCR	Clock monitoring control register	R/W	0b00000000
0x0FEA	CMDR	Clock monitoring data register	R	0b00000000
0x0FEB	WDTH	Watchdog timer selection ID register (upper)	R	0bXXXXXXXX
0x0FEC	WDTL	Watchdog timer selection ID register (lower)	R	0bXXXXXXXX
0x0FED, 0x0FEE	—	(Disabled)	—	—
0x0FEF	WICR	Interrupt pin selection circuit control register	R/W	0b01000000
0x0FF0 to 0x0FFF	—	(Disabled)	—	—

15.2 Port 1

Port 1 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95630H Series Hardware Manual”.

15.2.1 Port 1 configuration

Port 1 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 1 data register (PDR1)
- Port 1 direction register (DDR1)
- Port 1 pull-up register (PUL1)

15.2.2 Block diagrams of port 1

- P10/PPG10/CMP0_O pin

  This pin has the following peripheral functions:
  - 8/16-bit PPG ch. 1 output pin (PPG10)
  - Comparator digital output pin (CMP0_O)

- P11/PPG11 pin

  This pin has the following peripheral function:
  - 8/16-bit PPG ch. 1 output pin (PPG11)

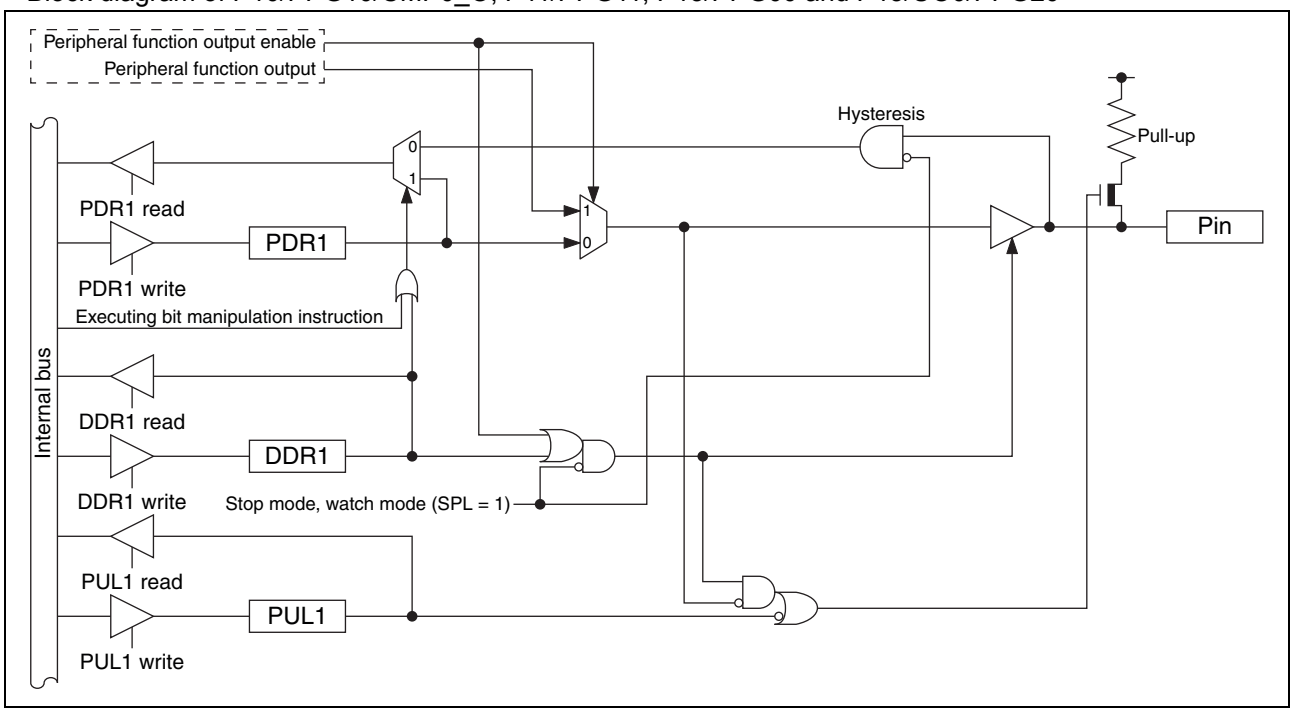
- P13/PPG00 pin

  This pin has the following peripheral function:
  - 8/16-bit PPG ch. 0 output pin (PPG00)

- P15/UO0/PPG20 pin

  This pin has the following peripheral functions:
  - UART/SIO ch. 0 data output pin (UO0)
  - 8/16-bit PPG ch. 2 output pin (PPG20)

- Block diagram of P10/PPG10/CMP0_O, P11/PPG11, P13/PPG00 and P15/UO0/PPG20



16. Interrupt Source Table

Interrupt source	Interrupt request number	Vector table address		Interrupt level setting register		Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower	Register	Bit	
External interrupt ch. 0	IRQ00	0xFFFA	0xFFFB	ILR0	L00 [1:0]	High
External interrupt ch. 4						
External interrupt ch. 1	IRQ01	0xFFF8	0xFFF9	ILR0	L01 [1:0]	
External interrupt ch. 5						
External interrupt ch. 2	IRQ02	0xFFF6	0xFFF7	ILR0	L02 [1:0]	
External interrupt ch. 6						
External interrupt ch. 3	IRQ03	0xFFF4	0xFFF5	ILR0	L03 [1:0]	
External interrupt ch. 7						
UART/SIO ch. 0	IRQ04	0xFFF2	0xFFF3	ILR1	L04 [1:0]	
MPG (DTTI)						
8/16-bit composite timer ch. 0 (lower)	IRQ05	0xFFF0	0xFFF1	ILR1	L05 [1:0]	
8/16-bit composite timer ch. 0 (upper)	IRQ06	0xFFEE	0xFFEF	ILR1	L06 [1:0]	
LIN-UART (reception)	IRQ07	0xFFEC	0xFFED	ILR1	L07 [1:0]	
LIN-UART (transmission)	IRQ08	0xFFEA	0xFFEB	ILR2	L08 [1:0]	
8/16-bit PPG ch. 1 (lower)	IRQ09	0xFFE8	0xFFE9	ILR2	L09 [1:0]	
8/16-bit PPG ch. 1 (upper)	IRQ10	0xFFE6	0xFFE7	ILR2	L10 [1:0]	
8/16-bit PPG ch. 2 (upper)	IRQ11	0xFFE4	0xFFE5	ILR2	L11 [1:0]	
8/16-bit PPG ch. 0 (upper)	IRQ12	0xFFE2	0xFFE3	ILR3	L12 [1:0]	
8/16-bit PPG ch. 0 (lower)	IRQ13	0xFFE0	0xFFE1	ILR3	L13 [1:0]	
8/16-bit composite timer ch. 1 (upper)	IRQ14	0xFFDE	0xFFDF	ILR3	L14 [1:0]	
8/16-bit PPG ch. 2 (lower)	IRQ15	0xFFDC	0xFFDD	ILR3	L15 [1:0]	
16-bit reload timer ch. 1	IRQ16	0xFFDA	0xFFDB	ILR4	L16 [1:0]	
MPG (write timing/compare clear)						
I²C bus interface						
16-bit PPG timer ch. 1	IRQ17	0xFFD8	0xFFD9	ILR4	L17 [1:0]	
MPG (position detection/compare interrupt)						
8/10-bit A/D converter	IRQ18	0xFFD6	0xFFD7	ILR4	L18 [1:0]	
Time-base timer	IRQ19	0xFFD4	0xFFD5	ILR4	L19 [1:0]	
Watch prescaler	IRQ20	0xFFD2	0xFFD3	ILR5	L20 [1:0]	
Comparator						
External interrupt ch. 8	IRQ21	0xFFD0	0xFFD1	ILR5	L21 [1:0]	
External interrupt ch. 9						
8/16-bit composite timer ch. 1 (lower)	IRQ22	0xFFCE	0xFFCF	ILR5	L22 [1:0]	
Flash memory	IRQ23	0xFFCC	0xFFCD	ILR5	L23 [1:0]	Low

18.3 DC Characteristics

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = –40 °C to +85°C)

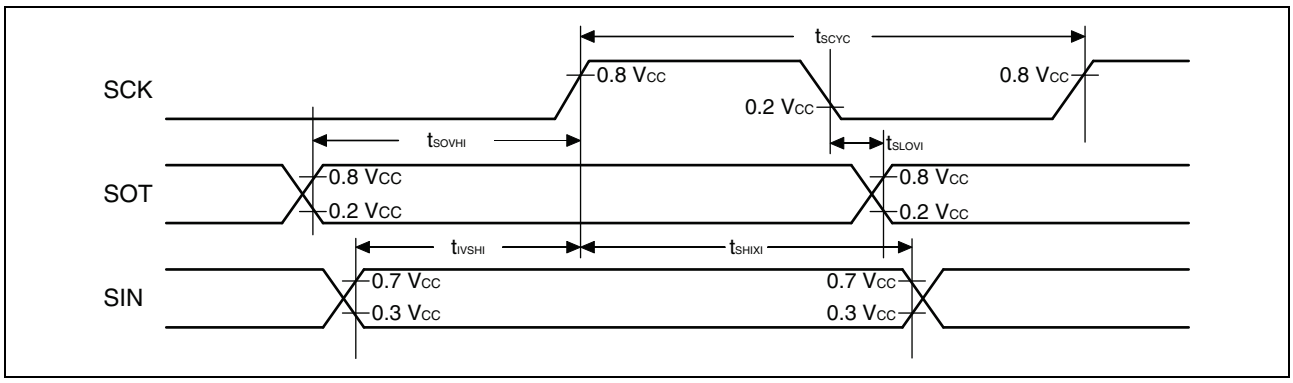
Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IHI}	P04, P16, P60, P61	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	CMOS input level
	V_{IHS}	P00 to P07, P10 to P17, P60 to P67, PF0, PF1, PG1, PG2	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
	V_{IHM}	PF2	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
"L" level input voltage	V_{ILI}	P04, P16, P60, P61	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	CMOS input level
	V_{ILS}	P00 to P07, P10 to P17, P60 to P67, PF0, PF1, PG1, PG2	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	Hysteresis input
	V_{ILM}	PF2	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	Hysteresis input
Open-drain output application voltage	V_D	P12, P60, P61, PF2	—	V_{SS} – 0.3	—	Vss + 5.5	V	
"H" level output voltage	V_{OH1}	Output pins other than P12, P62 to P67, PF2	I_{OH} = –4 mA	V_{CC} – 0.5	—	—	V	
	V_{OH2}	P62 to P67	I_{OH} = –8 mA	V_{CC} – 0.5	—	—	V	
"L" level output voltage	V_{OL1}	Output pins other than P62 to P67	I_{OL} = 4 mA	—	—	0.4	V	
	V_{OL2}	P62 to P67	I_{OL} = 12 mA	—	—	0.4	V	
Input leak current (Hi-Z output leak current)	I_{LI}	All input pins	0.0 V < V_I < V_{CC}	–5	—	+5	µA	When the internal pull-up resistor is disabled
Internal pull-up resistor	R_{PULL}	P00 to P07, P10, P11, P13 to P17, P62 to P67, PG1, PG2	V_I = 0 V	25	50	100	kΩ	When the internal pull-up resistor is enabled
Input capacitance	C_{IN}	Other than V_{CC} and V_{SS}	f = 1 MHz	—	5	15	pF	

18.4 AC Characteristics

18.4.1 Clock Timing

(V_{CC} = 2.4 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{CH}	X0, X1	—	1	—	16.25	MHz	When the main oscillation circuit is used
		X0	X1: open	1	—	12	MHz	When the main external clock is used
		X0, X1	*	1	—	32.5	MHz	
	F_{CRH}	—	—	3.92	4	4.08	MHz	Operating conditions • The main CR clock is used. • 0°C ≤ T_A ≤ +70°C
				3.8	4	4.2	MHz	Operating conditions • The main CR clock is used. • – 40 °C ≤ T_A < 0 °C, + 70 °C < T_A ≤ + 85 °C
	F_{MCRPLL}	—	—	7.84	8	8.16	MHz	Operating conditions • PLL multiplication rate: 2 • 0°C ≤ T_A ≤ +70°C
				7.6	8	8.4	MHz	Operating conditions • PLL multiplication rate: 2 • – 40 °C ≤ T_A < 0 °C, + 70 °C < T_A ≤ + 85 °C
				9.8	10	10.2	MHz	Operating conditions • PLL multiplication rate: 2.5 • 0°C ≤ T_A ≤ +70°C
				9.5	10	10.5	MHz	Operating conditions • PLL multiplication rate: 2.5 • – 40 °C ≤ T_A < 0 °C, + 70 °C < T_A ≤ + 85 °C
				11.76	12	12.24	MHz	Operating conditions • PLL multiplication rate: 3 • 0°C ≤ T_A ≤ +70°C
				11.4	12	12.6	MHz	Operating conditions • PLL multiplication rate: 3 • – 40 °C ≤ T_A < 0 °C, + 70 °C < T_A ≤ + 85 °C
				15.68	16	16.32	MHz	Operating conditions • PLL multiplication rate: 4 • 0°C ≤ T_A ≤ +70°C
				15.2	16	16.8	MHz	Operating conditions • PLL multiplication rate: 4 • – 40 °C ≤ T_A < 0 °C, + 70 °C < T_A ≤ + 85 °C
	F_{CL}	X0A, X1A	—	—	32.768	—	kHz	When the suboscillation circuit is used
				—	32.768	—	kHz	When the sub-external clock is used
	F_{CRL}	—	—	50	100	150	kHz	When the sub-CR clock is used



18.4.7 Low-voltage Detection

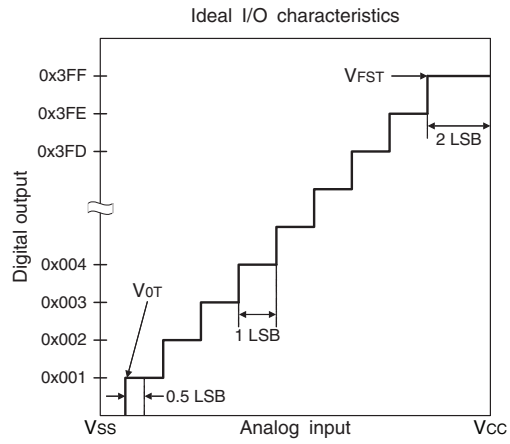
(V_{SS} = 0.0 V, T_A = –40°C to +85°C)

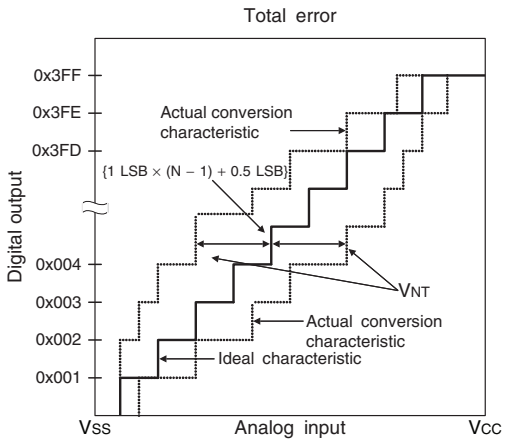
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Release voltage*	V_{DL+}	2.52	2.7	2.88	V	At power supply rise
		2.61	2.8	2.99		
		2.89	3.1	3.31		
		3.08	3.3	3.52		
Detection voltage*	V_{DL-}	2.43	2.6	2.77	V	At power supply fall
		2.52	2.7	2.88		
		2.80	3	3.20		
		2.99	3.2	3.41		
Hysteresis width	V_{HYS}	—	—	100	mV	
Power supply start voltage	V_{off}	—	—	2.3	V	
Power supply end voltage	V_{on}	4.9	—	—	V	
Power supply voltage change time (at power supply rise)	t_r	650	—	—	µs	Slope of power supply that the reset release signal generates within the rating (V_{DL+})
Power supply voltage change time (at power supply fall)	t_f	650	—	—	µs	Slope of power supply that the reset detection signal generates within the rating (V_{DL-})
Reset release delay time	t_{d1}	—	—	30	µs	
Reset detection delay time	t_{d2}	—	—	30	µs	
LVD reset threshold voltage transition stabilization time	t_{stb}	10	—	—	µs	

*: The release voltage and the detection voltage can be selected by using the LVD reset voltage selection ID register (LVDR) in the low-voltage detection reset circuit. For details of the LVDR register, refer to “CHAPTER 16 LOW-VOLTAGE DETECTION RESET CIRCUIT” in “New 8FX MB95630H Series Hardware Manual”.

18.5.3 Definitions of A/D Converter Terms

- Resolution
  It indicates the level of analog variation that can be distinguished by the A/D converter.
  When the number of bits is 10, analog voltage can be divided into 2^{10} = 1024.
- Linearity error (unit: LSB)
  It indicates how much an actual conversion value deviates from the straight line connecting the zero transition point ("0000000000" ← → "0000000001") of a device to the full-scale transition point ("1111111111" ← → "1111111110") of the same device.
- Differential linear error (unit: LSB)
  It indicates how much the input voltage required to change the output code by 1 LSB deviates from an ideal value.
- Total error (unit: LSB)
  It indicates the difference between an actual value and a theoretical value. The error can be caused by a zero transition error, a full-scale transition errors, a linearity error, a quantum error, or noise.





$$1\ \text{LSB} = \frac{V_{CC} - V_{SS}}{1024}\ \text{V}$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ \text{LSB}$$

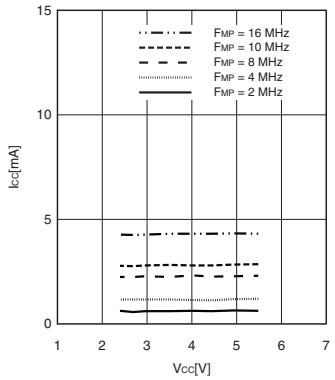
N : A/D converter digital output value

V_{NT} : Voltage at which the digital output transits from 0x(N – 1) to 0xN

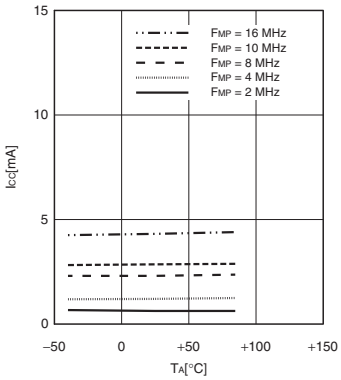
19. Sample Characteristics

- Power supply current temperature characteristics

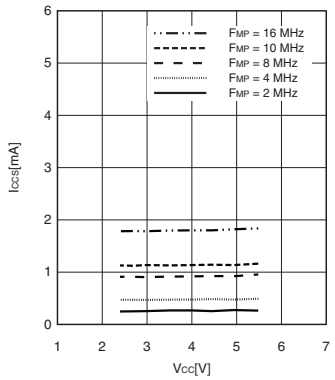
I_{CC} – V_{CC}
T_A = +25°C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



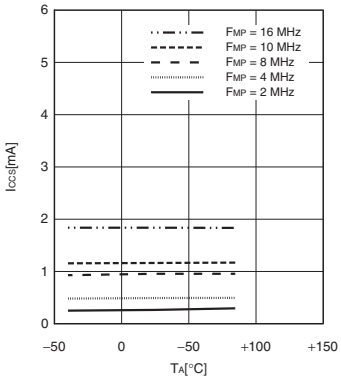
I_{CC} – T_A
V_{CC} = 5.5 V, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



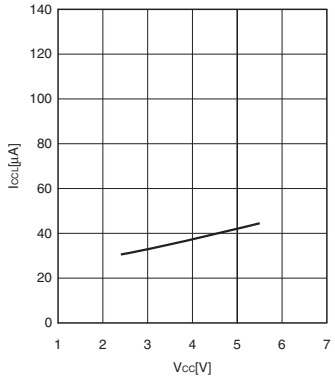
I_{CCS} – V_{CC}
T_A = +25°C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



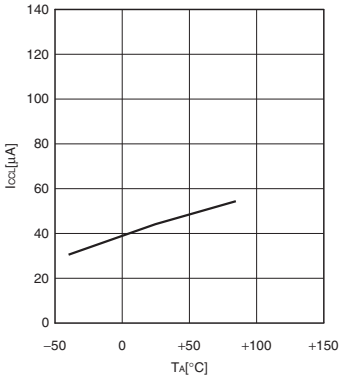
I_{CCS} – T_A
V_{CC} = 5.5 V, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



I_{CCL} – V_{CC}
T_A = +25°C, F_{MPL} = 16 kHz (divided by 2)
Subclock mode with the external clock operating



I_{CCL} – T_A
V_{CC} = 5.5 V, F_{MPL} = 16 kHz (divided by 2)
Subclock mode with the external clock operating



23. Major Changes In This Edition

Spansion Publication Number: DS702-00009

Page	Section	Details
22	■ PIN CONNECTION • C pin	Corrected the following statement. The bypass capacitor for the V_{CC} pin must have a capacitance larger than C_S. → The decoupling capacitor for the V_{CC} pin must have a capacitance equal to or larger than the capacitance of C_S.
66	■ ELECTRICAL CHARACTERISTICS 2. Recommended Operating Conditions	Corrected the following statement in remark *2. The bypass capacitor for the V_{CC} pin must have a capacitance larger than C_S. → The decoupling capacitor for the V_{CC} pin must have a capacitance equal to or larger than the capacitance of C_S.
71	4. AC Characteristics (1) Clock Timing	Corrected the pin names of the parameter “Input clock rising time and falling time”. X0 → X0, X0A X0, X1 → X0, X1, X0A, X1A

NOTE: Please see “Document History” about later revised information.