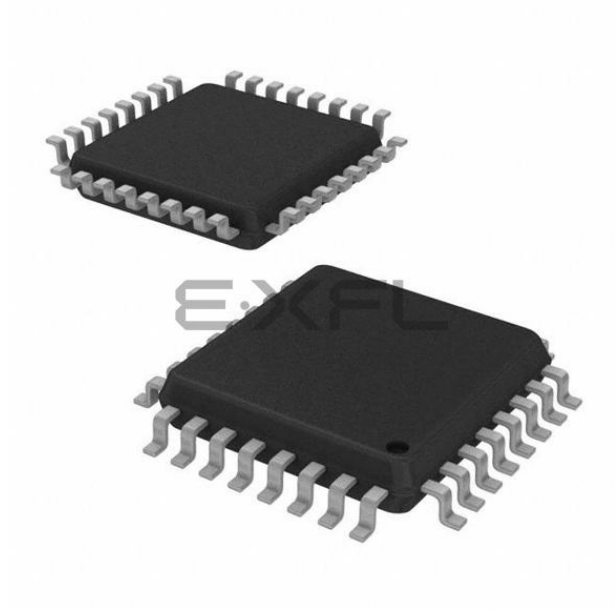

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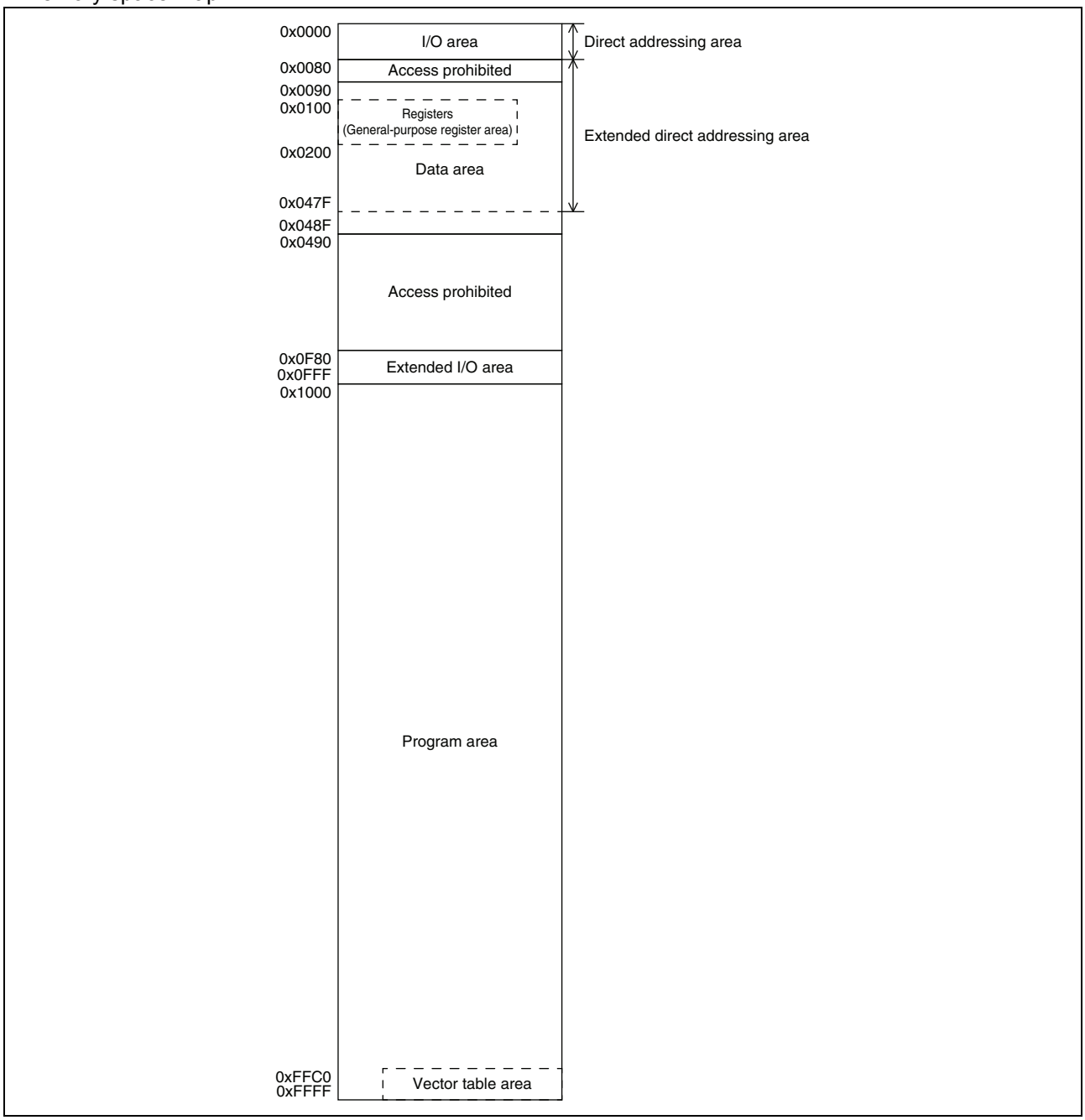
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SIO, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	28
Program Memory Size	20KB (20K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f634hpmc-g-une2

- Memory space map

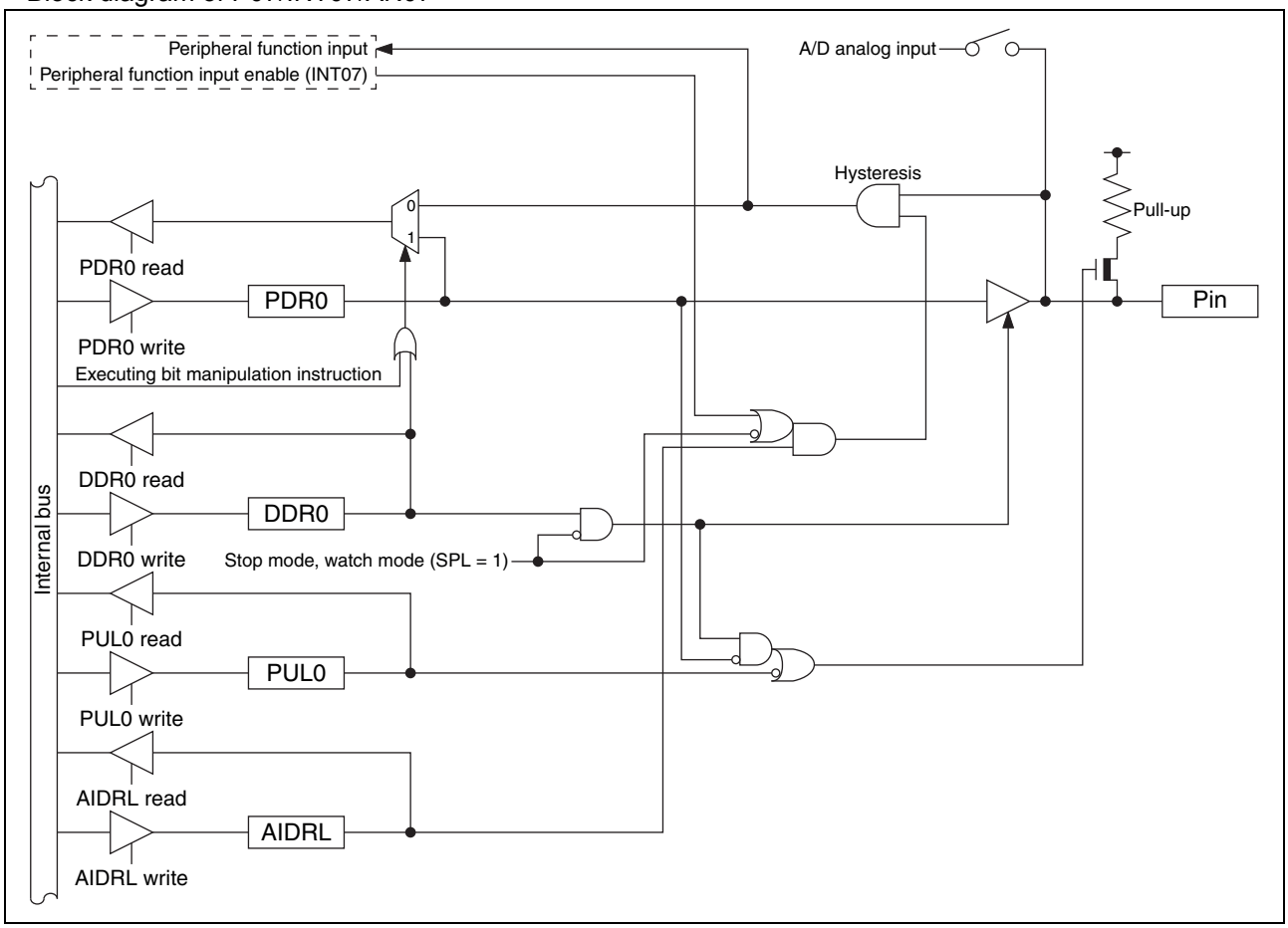


Address	Register abbreviation	Register name	R/W	Initial value
0x005A	RDR0	UART/SIO serial input data register	R	0b00000000
0x005B to 0x005F	—	(Disabled)	—	—
0x0060	IBCR00	I²C bus control register 0 ch. 0	R/W	0b00000000
0x0061	IBCR10	I²C bus control register 1 ch. 0	R/W	0b00000000
0x0062	IBSR0	I²C bus status register ch. 0	R/W	0b00000000
0x0063	IDDR0	I²C data register ch. 0	R/W	0b00000000
0x0064	IAAR0	I²C address register ch. 0	R/W	0b00000000
0x0065	ICCR0	I²C clock control register ch. 0	R/W	0b00000000
0x0066	OPCUR	16-bit MPG output control register (upper)	R/W	0b00000000
0x0067	OPCLR	16-bit MPG output control register (lower)	R/W	0b00000000
0x0068	IPCUR	16-bit MPG input control register (upper)	R/W	0b00000000
0x0069	IPCLR	16-bit MPG input control register (lower)	R/W	0b00000000
0x006A	NCCR	16-bit MPG noise cancellation control register	R/W	0b00000000
0x006B	TCSR	16-bit MPG timer control status register	R/W	0b00000000
0x006C	ADC1	8/10-bit A/D converter control register 1	R/W	0b00000000
0x006D	ADC2	8/10-bit A/D converter control register 2	R/W	0b00000000
0x006E	ADDH	8/10-bit A/D converter data register (upper)	R/W	0b00000000
0x006F	ADDL	8/10-bit A/D converter data register (lower)	R/W	0b00000000
0x0070	—	(Disabled)	—	—
0x0071	FSR2	Flash memory status register 2	R/W	0b00000000
0x0072	FSR	Flash memory status register	R/W	0b000X0000
0x0073	SWRE0	Flash memory sector write control register 0	R/W	0b00000000
0x0074	FSR3	Flash memory status register 3	R	0b000XXXXX
0x0075	FSR4	Flash memory status register 4	R/W	0b00000000
0x0076	WREN	Wild register address compare enable register	R/W	0b00000000
0x0077	WROR	Wild register data test setting register	R/W	0b00000000
0x0078	—	Mirror of register bank pointer (RP) and direct bank pointer (DP)	—	—
0x0079	ILR0	Interrupt level setting register 0	R/W	0b11111111
0x007A	ILR1	Interrupt level setting register 1	R/W	0b11111111
0x007B	ILR2	Interrupt level setting register 2	R/W	0b11111111
0x007C	ILR3	Interrupt level setting register 3	R/W	0b11111111
0x007D	ILR4	Interrupt level setting register 4	R/W	0b11111111
0x007E	ILR5	Interrupt level setting register 5	R/W	0b11111111
0x007F	—	(Disabled)	—	—

Address	Register abbreviation	Register name	R/W	Initial value
0x0FCE	OPDBRH5	16-bit MPG output data buffer register (upper) ch. 5	R/W	0b00000000
0x0FCF	OPDBRL5	16-bit MPG output data buffer register (lower) ch. 5	R/W	0b00000000
0x0FD0	OPDBRH6	16-bit MPG output data buffer register (upper) ch. 6	R/W	0b00000000
0x0FD1	OPDBRL6	16-bit MPG output data buffer register (lower) ch. 6	R/W	0b00000000
0x0FD2	OPDBRH7	16-bit MPG output data buffer register (upper) ch. 7	R/W	0b00000000
0x0FD3	OPDBRL7	16-bit MPG output data buffer register (lower) ch. 7	R/W	0b00000000
0x0FD4	OPDBRH8	16-bit MPG output data buffer register (upper) ch. 8	R/W	0b00000000
0x0FD5	OPDBRL8	16-bit MPG output data buffer register (lower) ch. 8	R/W	0b00000000
0x0FD6	OPDBRH9	16-bit MPG output data buffer register (upper) ch. 9	R/W	0b00000000
0x0FD7	OPDBRL9	16-bit MPG output data buffer register (lower) ch. 9	R/W	0b00000000
0x0FD8	OPDBRHA	16-bit MPG output data buffer register (upper) ch. A	R/W	0b00000000
0x0FD9	OPDBRLA	16-bit MPG output data buffer register (lower) ch. A	R/W	0b00000000
0x0FDA	OPDBRHB	16-bit MPG output data buffer register (upper) ch. B	R/W	0b00000000
0x0FDB	OPDBRLB	16-bit MPG output data buffer register (lower) ch. B	R/W	0b00000000
0x0FDC	OPDUR	16-bit MPG output data register (upper)	R	0b0000XXXX
0x0FDD	OPDLR	16-bit MPG output data register (lower)	R	0bXXXXXXXX
0x0FDE	CPCUR	16-bit MPG compare clear register (upper)	R/W	0bXXXXXXXX
0x0FDF	CPCLR	16-bit MPG compare clear register (lower)	R/W	0bXXXXXXXX
0x0FE0, 0x0FE1	—	(Disabled)	—	—
0x0FE2	TMBUR	16-bit MPG timer buffer register (upper)	R	0bXXXXXXXX
0x0FE3	TMBLR	16-bit MPG timer buffer register (lower)	R	0bXXXXXXXX
0x0FE4	CRTH	Main CR clock trimming register (upper)	R/W	0b000XXXXX
0x0FE5	CRTL	Main CR clock trimming register (lower)	R/W	0b000XXXXX
0x0FE6	—	(Disabled)	—	—
0x0FE7	CRTDA	Main CR clock temperature dependent adjustment register	R/W	0b000XXXXX
0x0FE8	SYSC	System configuration register	R/W	0b11000011
0x0FE9	CMCR	Clock monitoring control register	R/W	0b00000000
0x0FEA	CMDR	Clock monitoring data register	R	0b00000000
0x0FEB	WDTH	Watchdog timer selection ID register (upper)	R	0bXXXXXXXX
0x0FEC	WDTL	Watchdog timer selection ID register (lower)	R	0bXXXXXXXX
0x0FED, 0x0FEE	—	(Disabled)	—	—
0x0FEF	WICR	Interrupt pin selection circuit control register	R/W	0b01000000
0x0FF0 to 0x0FFF	—	(Disabled)	—	—

- P07/INT07/AN07 pin
  This pin has the following peripheral functions:
  - External interrupt circuit input pin (INT07)
  - 8/10-bit A/D converter analog input pin (AN07)

- Block diagram of P07/INT07/AN07



15.2 Port 1

Port 1 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95630H Series Hardware Manual”.

15.2.1 Port 1 configuration

Port 1 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 1 data register (PDR1)
- Port 1 direction register (DDR1)
- Port 1 pull-up register (PUL1)

15.2.2 Block diagrams of port 1

- P10/PPG10/CMP0_O pin

  This pin has the following peripheral functions:
  - 8/16-bit PPG ch. 1 output pin (PPG10)
  - Comparator digital output pin (CMP0_O)

- P11/PPG11 pin

  This pin has the following peripheral function:
  - 8/16-bit PPG ch. 1 output pin (PPG11)

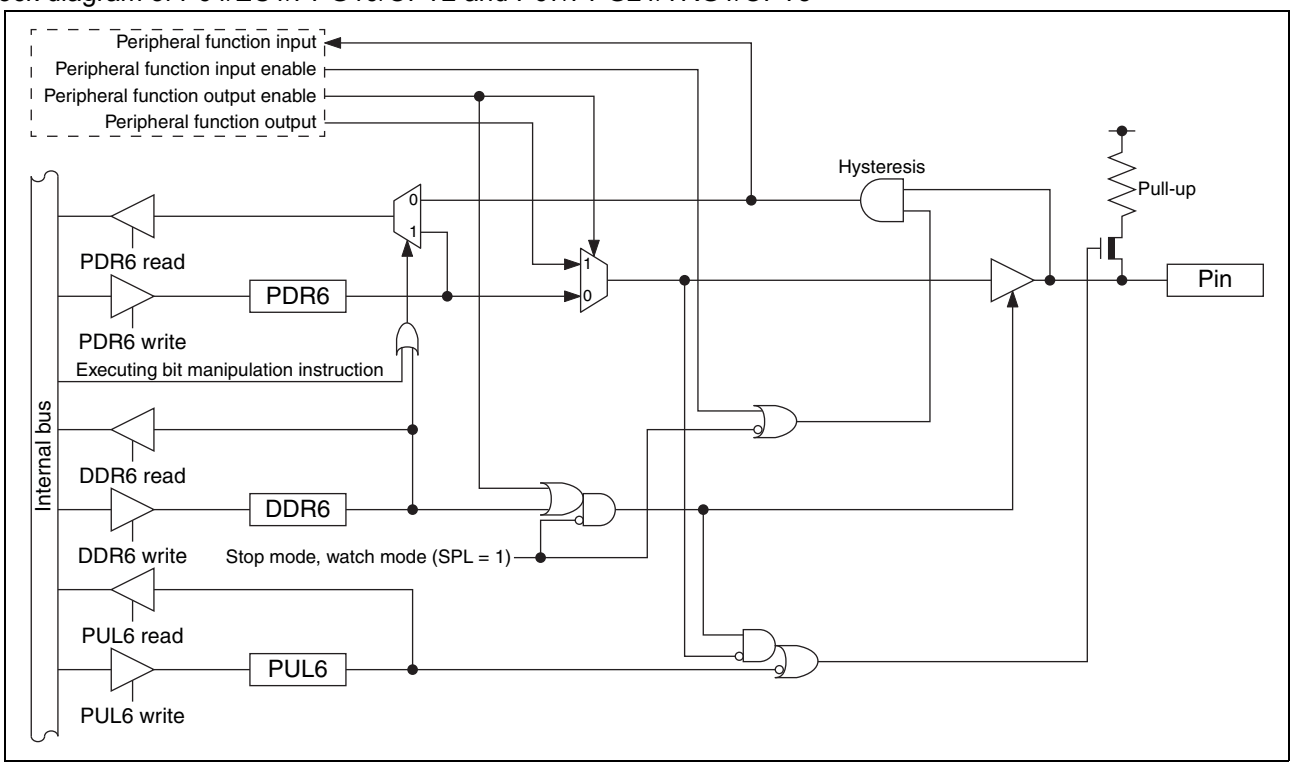
- P13/PPG00 pin

  This pin has the following peripheral function:
  - 8/16-bit PPG ch. 0 output pin (PPG00)

- P15/UO0/PPG20 pin

  This pin has the following peripheral functions:
  - UART/SIO ch. 0 data output pin (UO0)
  - 8/16-bit PPG ch. 2 output pin (PPG20)

• Block diagram of P64/EC1/PPG10/OPT2 and P67/PPG21/TRG1/OPT5



15.3.3 Port 6 registers

• Port 6 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR6	0	Pin state is “L” level.	PDR6 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR6 value is “1”.	As output port, outputs “H” level.*
DDR6	0	Port input enabled		
	1	Port output enabled		
PUL6	0	Pull-up disabled		
	1	Pull-up enabled		

*: If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

• Correspondence between registers and pins for port 6

	Correspondence between related register bits and pins							
Pin name	**P67**	**P66**	**P65**	**P64**	**P63**	**P62**	**P61**	**P60**
PDR6	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DDR6								
PUL6							-	-

15.4 Port F

Port F is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95630H Series Hardware Manual”.

15.4.1 Port F configuration

Port F is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port F data register (PDRF)
- Port F direction register (DDRF)

15.4.2 Block diagrams of port F

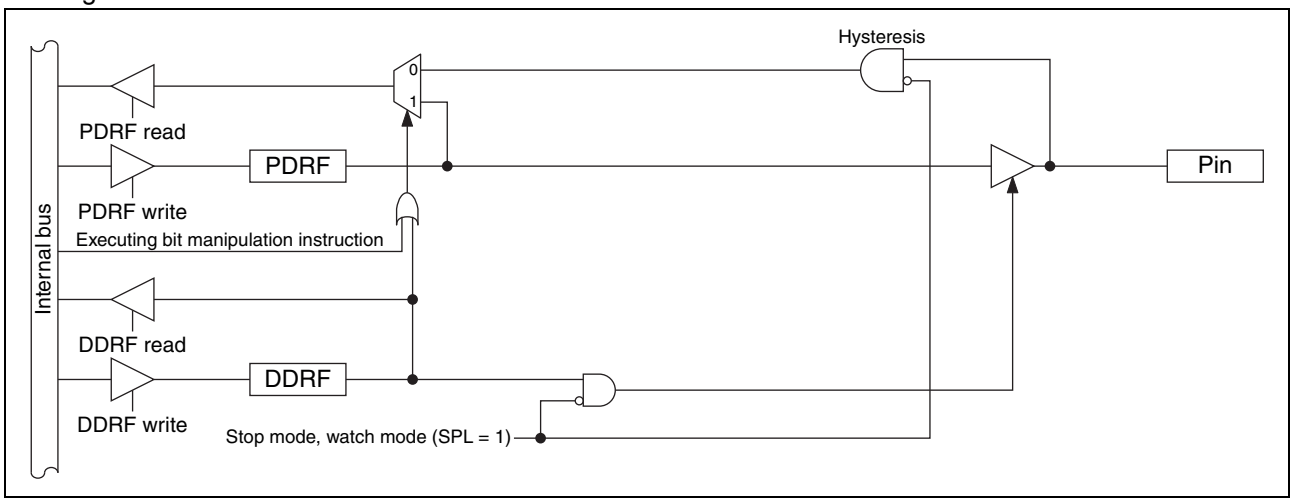
- PF0/X0 pin

  This pin has the following peripheral function:
  - Main clock input oscillation pin (X0)

- PF1/X1 pin

  This pin has the following peripheral function:
  - Main clock I/O oscillation pin (X1)

- Block diagram of PF0/X0 and PF1/X1



Pin name	Normal operation	Sleep mode	Stop mode		Watch mode		On reset
			SPL=0	SPL=1	SPL=0	SPL=1	
P14/UCK0/ PPG01	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*2 (However, an external interrupt can be input when the external interrupt request is enabled.)	- Hi-Z (However, the setting of the pull-up control is effective.) - Input blocked*2 (However, an external interrupt can be input when the external interrupt request is enabled.)	- Previous state kept - Input blocked*2 (However, an external interrupt can be input when the external interrupt request is enabled.)	- Hi-Z (However, the setting of the pull-up control is effective.) - Input blocked*2 (However, an external interrupt can be input when the external interrupt request is enabled.)	- Hi-Z - Input enabled*1 (However, it does not function.)
P15/UO0/ PPG20	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*2	- Hi-Z (However, the setting of the pull-up control is effective.) - Input blocked*2	- Previous state kept - Input blocked*2	- Hi-Z (However, the setting of the pull-up control is effective.) - Input blocked*2	- Hi-Z - Input enabled*1 (However, it does not function.)
P16/UI0/ PPG21	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*2 (However, an external interrupt can be input when the external interrupt request is enabled.)	- Hi-Z (However, the setting of the pull-up control is effective.) - Input blocked*2 (However, an external interrupt can be input when the external interrupt request is enabled.)	- Previous state kept - Input blocked*2 (However, an external interrupt can be input when the external interrupt request is enabled.)	- Hi-Z (However, the setting of the pull-up control is effective.) - Input blocked*2 (However, an external interrupt can be input when the external interrupt request is enabled.)	- Hi-Z - Input enabled*1 (However, it does not function.)
P17/TO1/ SNI0	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*2	- Hi-Z (However, the setting of the pull-up control is effective.) - Input blocked*2	- Previous state kept - Input blocked*2	- Hi-Z (However, the setting of the pull-up control is effective.) - Input blocked*2	- Hi-Z - Input enabled*1 (However, it does not function.)
P00/INT00/ AN00/ CMP0_P	I/O port/ peripheral function I/O/ analog input	I/O port/ peripheral function I/O/ analog input	- Previous state kept - Input blocked*2 (However, an external interrupt can be input when the external interrupt request is enabled.)	- Hi-Z (However, the setting of the pull-up control is effective.) - Input blocked*2 (However, an external interrupt can be input when the external interrupt request is enabled.)	- Previous state kept - Input blocked*2 (However, an external interrupt can be input when the external interrupt request is enabled.)	- Hi-Z (However, the setting of the pull-up control is effective.) - Input blocked*2 (However, an external interrupt can be input when the external interrupt request is enabled.)	- Hi-Z - Input blocked*2
P01/INT01/ AN01/ CMP0_N							
P02/INT02/ AN02/SCK							
P03/INT03/ AN03/SOT							

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = –40 °C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ*1	Max*2		
Power supply current*3	I_V	V_{CC}	Current consumption of the comparator	—	60	160	µA	
	I_{LVD}		Current consumption of the low-voltage detection circuit	—	4	7	µA	
	I_{CRH}		Current consumption of the main CR oscillator	—	240	320	µA	
	I_{CRL}		Current consumption of the sub-CR oscillator oscillating at 100 kHz	—	7	20	µA	
	I_{NSTBY}		Current consumption difference between normal standby mode and deep standby mode T_A = +25°C	—	20	30	µA	

*1: V_{CC} = 5.0 V, T_A = +25°C

*2: V_{CC} = 5.5 V, T_A = +85°C (unless otherwise specified)

*3:
- The power supply current is determined by the external clock. When the low-voltage detection circuit is selected, the power supply current is the sum of adding the current consumption of the low-voltage detection circuit (I_{LVD}) to one of the values from I_{CC} to I_{CCH}. In addition, when both the low-voltage detection option and the CR oscillator are selected, the power supply current is the sum of adding up the current consumption of the low-voltage detection circuit (I_{LVD}), the current consumption of the CR oscillators (I_{CRH}, I_{CRL}) and a specified value. In on-chip debug mode, the CR oscillator (I_{CRH}) and the low-voltage detection circuit are always in operation, and current consumption therefore increases accordingly.
- See “4. AC Characteristics Clock Timing” for F_{CH}, F_{CL}, F_{CRH} and F_{MCRPLL}.
- See “4. AC Characteristics Source Clock/Machine Clock” for F_{MP} and F_{MPL}.
- The power supply current value in standby mode is measured in deep standby mode. The current consumption in normal standby is higher than that in deep standby mode. The power supply current value in normal standby can be found by adding the current consumption difference between normal standby mode and deep standby mode (I_{NSTBY}) to the power supply current value in deep standby mode. For details of normal standby and deep standby mode, refer to “CHAPTER 3 CLOCK CONTROLLER” in “New 8FX MB95630H Series Hardware Manual”.

18.4 AC Characteristics

18.4.1 Clock Timing

(V_{CC} = 2.4 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

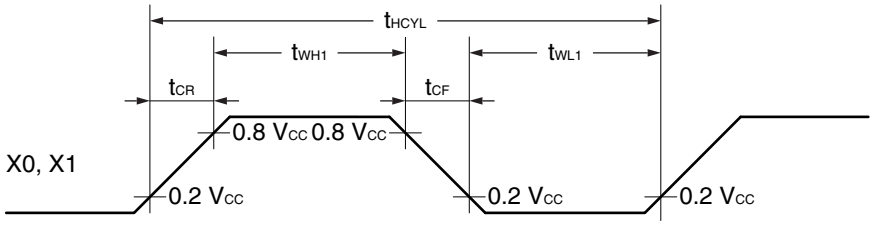
Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{CH}	X0, X1	—	1	—	16.25	MHz	When the main oscillation circuit is used
		X0	X1: open	1	—	12	MHz	When the main external clock is used
		X0, X1	*	1	—	32.5	MHz	
	F_{CRH}	—	—	3.92	4	4.08	MHz	Operating conditions • The main CR clock is used. • 0°C ≤ T_A ≤ +70°C
				3.8	4	4.2	MHz	Operating conditions • The main CR clock is used. • – 40 °C ≤ T_A < 0 °C, + 70 °C < T_A ≤ + 85 °C
	F_{MCRPLL}	—	—	7.84	8	8.16	MHz	Operating conditions • PLL multiplication rate: 2 • 0°C ≤ T_A ≤ +70°C
				7.6	8	8.4	MHz	Operating conditions • PLL multiplication rate: 2 • – 40 °C ≤ T_A < 0 °C, + 70 °C < T_A ≤ + 85 °C
				9.8	10	10.2	MHz	Operating conditions • PLL multiplication rate: 2.5 • 0°C ≤ T_A ≤ +70°C
				9.5	10	10.5	MHz	Operating conditions • PLL multiplication rate: 2.5 • – 40 °C ≤ T_A < 0 °C, + 70 °C < T_A ≤ + 85 °C
				11.76	12	12.24	MHz	Operating conditions • PLL multiplication rate: 3 • 0°C ≤ T_A ≤ +70°C
				11.4	12	12.6	MHz	Operating conditions • PLL multiplication rate: 3 • – 40 °C ≤ T_A < 0 °C, + 70 °C < T_A ≤ + 85 °C
				15.68	16	16.32	MHz	Operating conditions • PLL multiplication rate: 4 • 0°C ≤ T_A ≤ +70°C
				15.2	16	16.8	MHz	Operating conditions • PLL multiplication rate: 4 • – 40 °C ≤ T_A < 0 °C, + 70 °C < T_A ≤ + 85 °C
	F_{CL}	X0A, X1A	—	—	32.768	—	kHz	When the suboscillation circuit is used
				—	32.768	—	kHz	When the sub-external clock is used
	F_{CRL}	—	—	50	100	150	kHz	When the sub-CR clock is used

(V_{CC} = 2.4 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock cycle time	t_{HCYL}	X0, X1	—	61.5	—	1000	ns	When the main oscillation circuit is used
		X0	X1: open	83.4	—	1000	ns	When an external clock is used
		X0, X1	*	30.8	—	1000	ns	
	t_{LCYL}	X0A, X1A	—	—	30.5	—	µs	When the subclock is used
Input clock pulse width	t_{WH1}, t_{WL1}	X0	X1: open	33.4	—	—	ns	When an external clock is used, the duty ratio should range between 40% and 60%.
		X0, X1	*	12.4	—	—	ns	
	t_{WH2}, t_{WL2}	X0A	—	—	15.2	—	µs	
Input clock rising time and falling time	t_{CR}, t_{CF}	X0, X0A	X1: open	—	—	5	ns	When an external clock is used
		X0, X1, X0A, X1A	*	—	—	5	ns	
CR oscillation start time	t_{CRHWK}	—	—	—	—	50	µs	When the main CR clock is used
	t_{CRLWK}	—	—	—	—	30	µs	When the sub-CR clock is used
PLL oscillation start time	$t_{MCRPLLWK}$	—	—	—	—	100	µs	When the main CR PLL clock is used

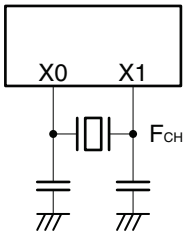
*: The external clock signal is input to X0 and the inverted external clock signal to X1.

- Input waveform generated when an external clock (main clock) is used

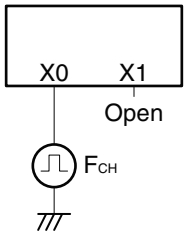


- Figure of main clock input port external connection

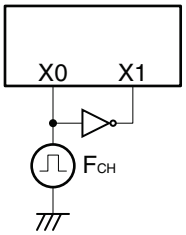
When a crystal oscillator or a ceramic oscillator is used



When an external clock is used (X1 is open)



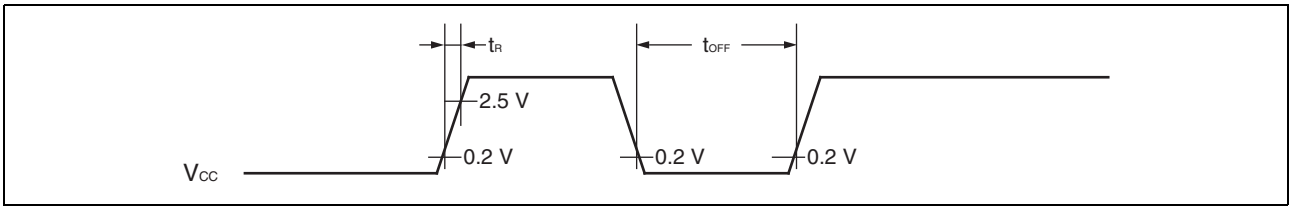
When an external clock is used



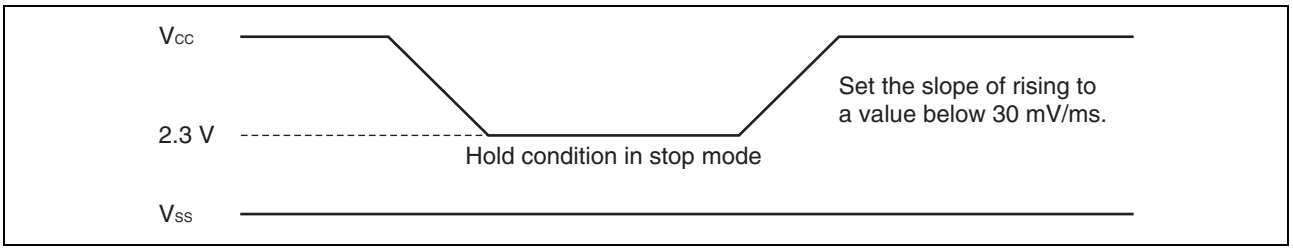
18.4.4 Power-on Reset

(V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_R	—	—	50	ms	
Power supply cutoff time	t_{OFF}	—	1	—	ms	Wait time until power-on



Note: A sudden change of power supply voltage may activate the power-on reset function. When changing the power supply voltage during the operation, set the slope of rising to a value below within 30 mV/ms as shown below.

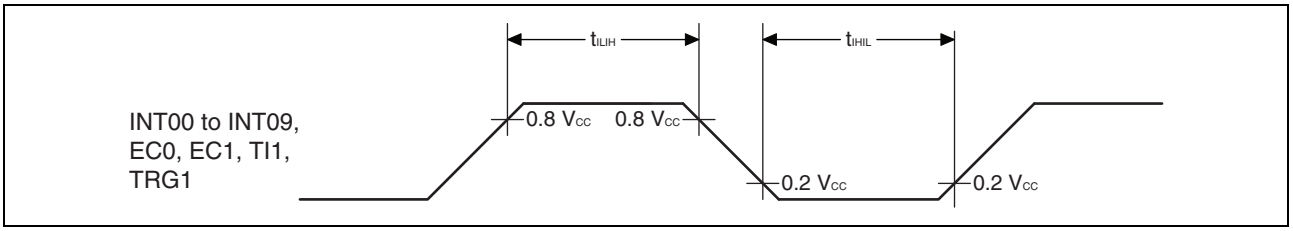


18.4.5 Peripheral Input Timing

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Peripheral input “H” pulse width	t_{ILIH}	INT00 to INT09, EC0, EC1, TI1, TRG1	2 t_{MCLK}*	—	ns
Peripheral input “L” pulse width	t_{IHIL}		2 t_{MCLK}*	—	ns

*: See “Source Clock/Machine Clock” for t_{MCLK}.



18.4.6 LIN-UART Timing

Sampling is executed at the rising edge of the sampling clock*1, and serial clock delay is disabled*2. (ESCR register : SCES bit = 0, ECCR register : SCDE bit = 0)

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

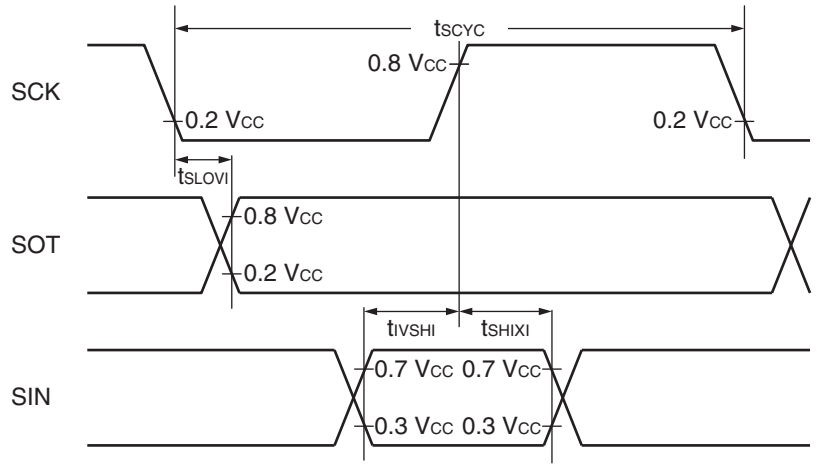
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK↓ → SOT delay time	t_{SLOVI}	SCK, SOT		–50	+50	ns
Valid SIN → SCK↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3 + 80	—	ns
SCK↑ → valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK	External clock operation output pin: C_L = 80 pF + 1 TTL	3 t_{MCLK}*3–t_R	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK		t_{MCLK}*3 + 10	—	ns
SCK↓ → SOT delay time	t_{SLOVE}	SCK, SOT		—	2 t_{MCLK}*3 + 60	ns
Valid SIN → SCK↑	t_{IVSHE}	SCK, SIN		30	—	ns
SCK↑ → valid SIN hold time	t_{SHIXE}	SCK, SIN		t_{MCLK}*3 + 30	—	ns
SCK falling time	t_F	SCK		—	10	ns
SCK rising time	t_R	SCK		—	10	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See “Source Clock/Machine Clock” for t_{MCLK}.

- Internal shift clock mode

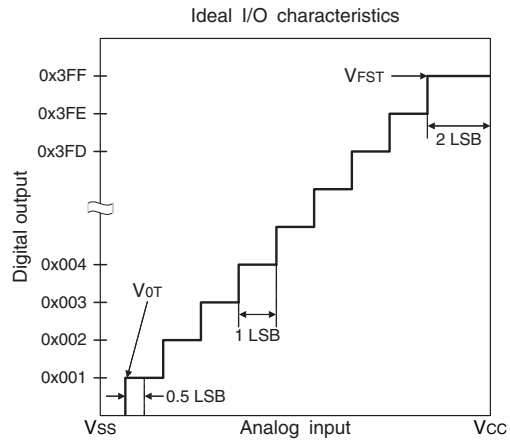


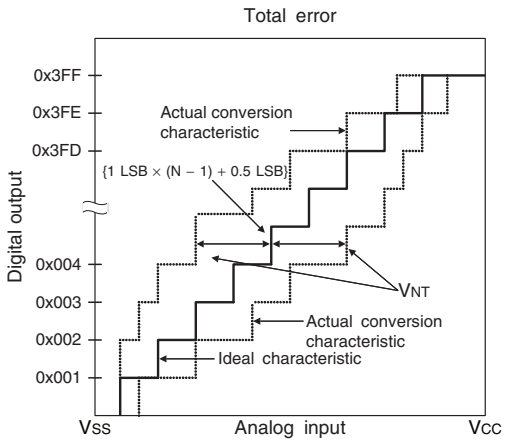
(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value*2		Unit	Remarks
				Min	Max		
SCL clock “L” width	t_{LOW}	SCL	R = 1.7 kΩ, C = 50 pF*1	$(2 + nm/2)t_{MCLK} - 20$	—	ns	Master mode
SCL clock “H” width	t_{HIGH}	SCL		$(nm/2)t_{MCLK} - 20$	$(nm/2)t_{MCLK} + 20$	ns	Master mode
START condition hold time	$t_{HD;STA}$	SCL, SDA		$(-1 + nm/2)t_{MCLK} - 20$	$(-1 + nm)t_{MCLK} + 20$	ns	Master mode Maximum value is applied when m, n = 1, 8. Otherwise, the minimum value is applied.
STOP condition setup time	$t_{SU;STO}$	SCL, SDA		$(1 + nm/2)t_{MCLK} - 20$	$(1 + nm/2)t_{MCLK} + 20$	ns	Master mode
START condition setup time	$t_{SU;STA}$	SCL, SDA		$(1 + nm/2)t_{MCLK} - 20$	$(1 + nm/2)t_{MCLK} + 20$	ns	Master mode
Bus free time between STOP condition and START condition	t_{BUF}	SCL, SDA		$(2\ nm + 4)\ t_{MCLK} - 20$	—	ns	
Data hold time	$t_{HD;DAT}$	SCL, SDA		$3\ t_{MCLK} - 20$	—	ns	Master mode
Data setup time	$t_{SU;DAT}$	SCL, SDA		$(-2 + nm/2)\ t_{MCLK} - 20$	$(-1 + nm/2)\ t_{MCLK} + 20$	ns	Master mode It is assumed that “L” of SCL is not extended. The minimum value is applied to the first bit of continuous data. Otherwise, the maximum value is applied.
Setup time between clearing interrupt and SCL rising	$t_{SU;INT}$	SCL		$(nm/2)\ t_{MCLK} - 20$	$(1 + nm/2)\ t_{MCLK} + 20$	ns	The minimum value is applied to the interrupt at the ninth SCL↓. The maximum value is applied to the interrupt at the eighth SCL↓.
SCL clock “L” width	t_{LOW}	SCL		$4\ t_{MCLK} - 20$	—	ns	At reception
SCL clock “H” width	t_{HIGH}	SCL		$4\ t_{MCLK} - 20$	—	ns	At reception

18.5.3 Definitions of A/D Converter Terms

- Resolution
  It indicates the level of analog variation that can be distinguished by the A/D converter.
  When the number of bits is 10, analog voltage can be divided into 2^{10} = 1024.
- Linearity error (unit: LSB)
  It indicates how much an actual conversion value deviates from the straight line connecting the zero transition point ("0000000000" ← → "0000000001") of a device to the full-scale transition point ("1111111111" ← → "1111111110") of the same device.
- Differential linear error (unit: LSB)
  It indicates how much the input voltage required to change the output code by 1 LSB deviates from an ideal value.
- Total error (unit: LSB)
  It indicates the difference between an actual value and a theoretical value. The error can be caused by a zero transition error, a full-scale transition errors, a linearity error, a quantum error, or noise.





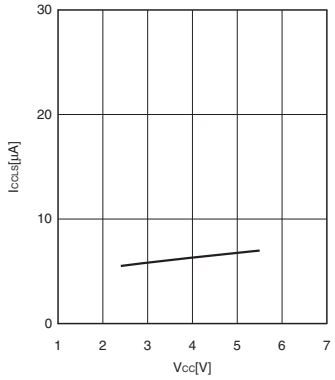
$$1\ \text{LSB} = \frac{V_{CC} - V_{SS}}{1024}\ \text{V}$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ \text{LSB}$$

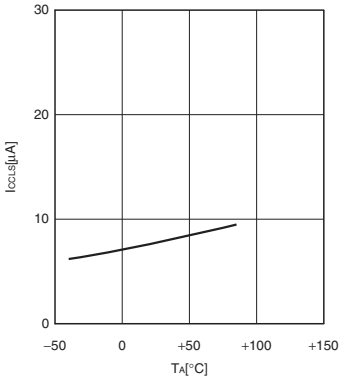
N : A/D converter digital output value

V_{NT} : Voltage at which the digital output transits from 0x(N – 1) to 0xN

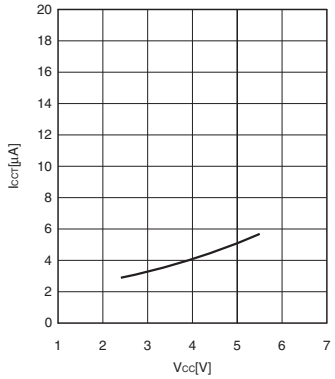
I_{CCLS} – V_{CC}
T_A = +25°C, F_{MPL} = 16 kHz (divided by 2)
Subsleep mode with the external clock operating



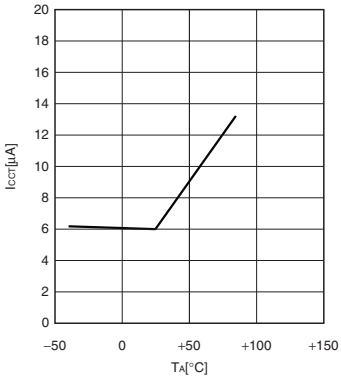
I_{CCLS} – T_A
V_{CC} = 5.5 V, F_{MPL} = 16 kHz (divided by 2)
Subsleep mode with the external clock operating



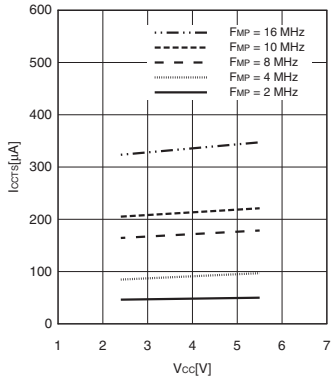
I_{CCT} – V_{CC}
T_A = +25°C, F_{MPL} = 16 kHz (divided by 2)
Watch mode with the external clock operating



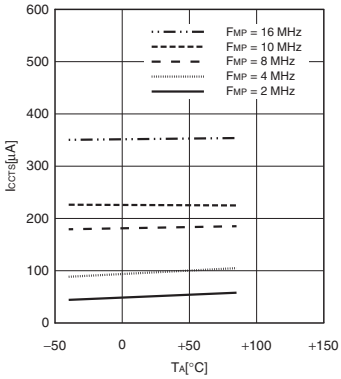
I_{CCT} – T_A
V_{CC} = 5.5 V, F_{MPL} = 16 kHz (divided by 2)
Watch mode with the external clock operating



I_{CCTS} – V_{CC}
T_A = +25°C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Time-base timer mode with the external clock operating

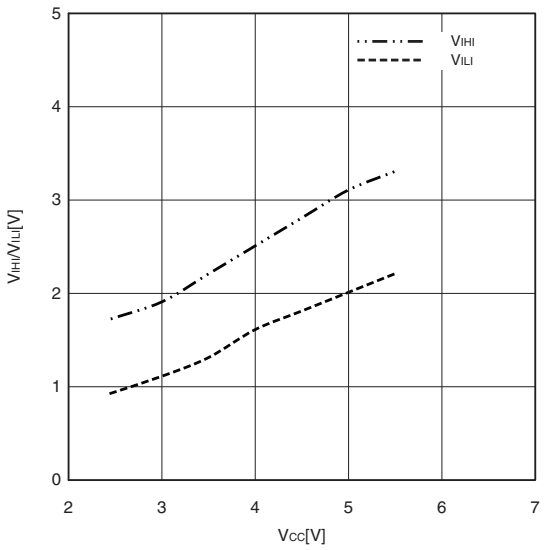


I_{CCTS} – T_A
V_{CC} = 5.5 V, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Time-base timer mode with the external clock operating

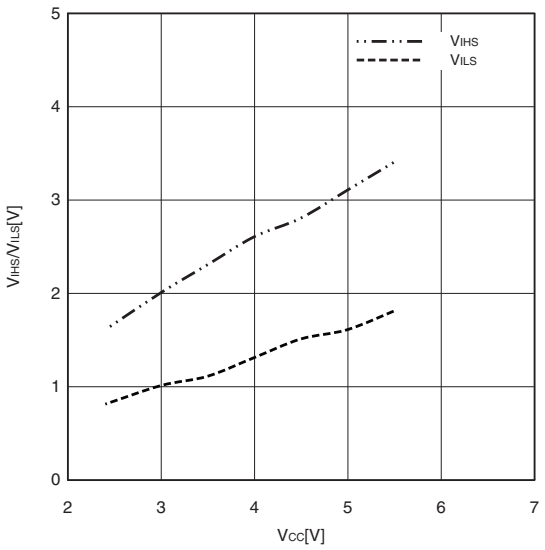


- Input voltage characteristics

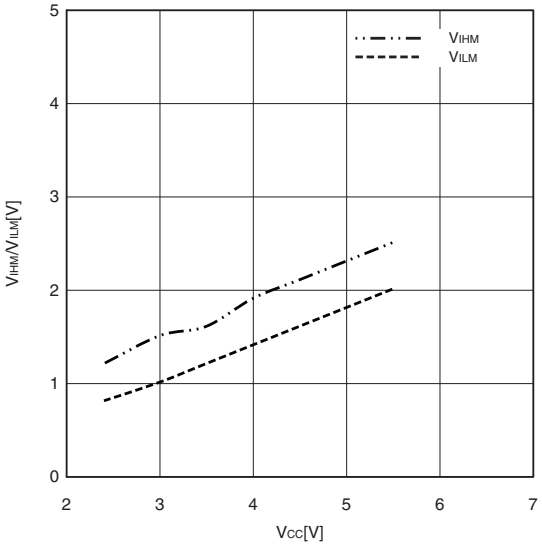
V_{IHI} – V_{CC} and V_{ILI} – V_{CC}
T_A = +25°C



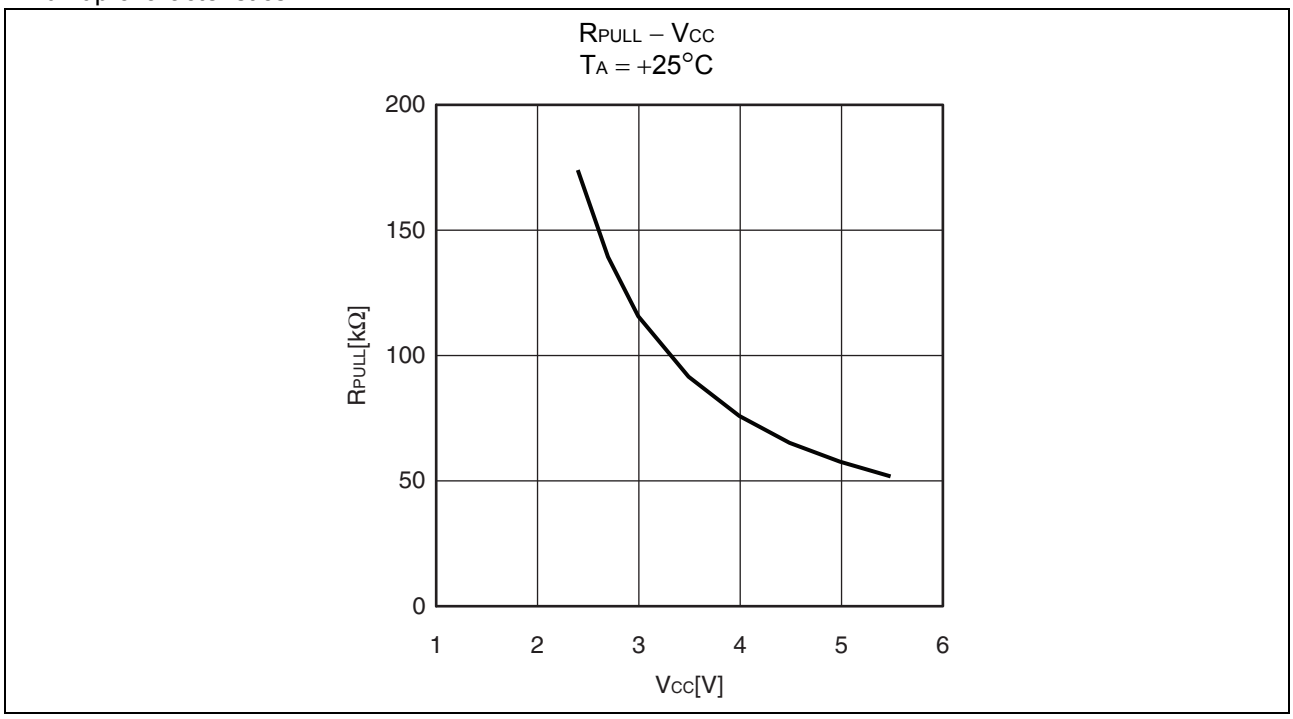
V_{IHS} – V_{CC} and V_{ILS} – V_{CC}
T_A = +25°C



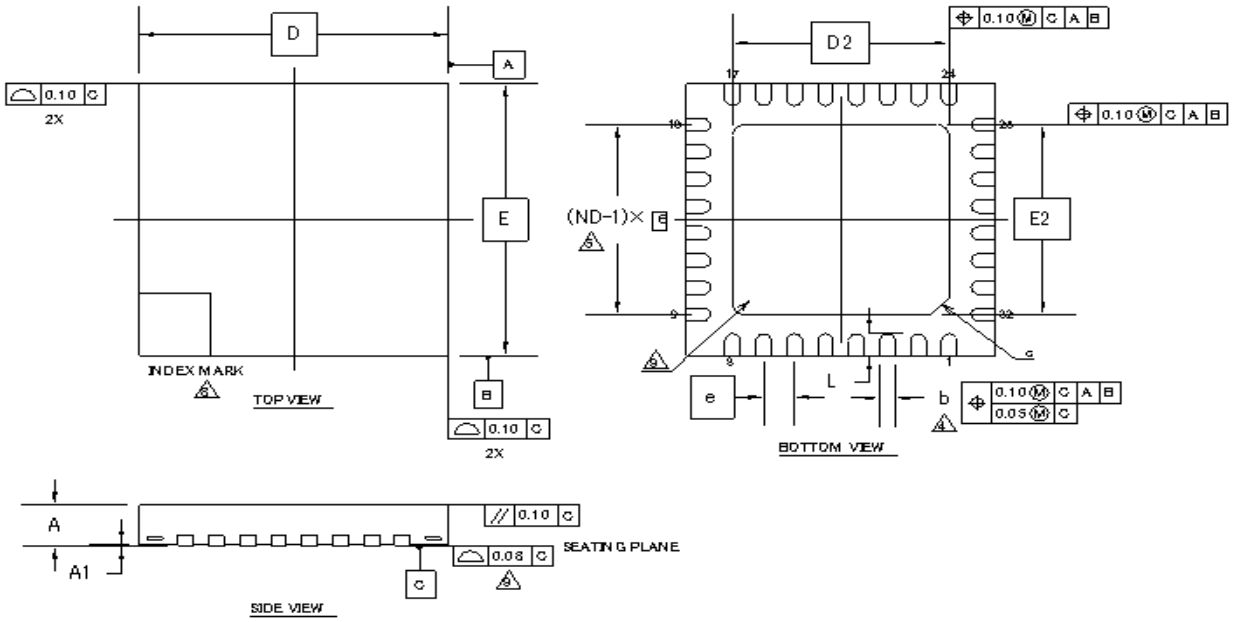
V_{IHM} – V_{CC} and V_{ILM} – V_{CC}
T_A = +25°C



- Pull-up characteristics



Package Type	Package Code
QFN 32	WNP032



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	——	——	0.80
A_1	0.00	——	0.05
D		5.00 BSC	
E		5.00 BSC	
b	0.18	0.25	0.30
D_2		3.50 BSC	
E_2		3.50 BSC	
e		0.50 BSC	
c		0.30 REF	
L	0.35	0.40	0.45

NOTE

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING CONFORMS TO ASME Y14.5-1994.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND REFER TO THE NUMBER OF TERMINALS ON D OR E SIDE.
6. MAX. PACKAGE WARPAGE IS 0.05mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LOCATED WITHIN INDICATED ZONE.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. JEDEC SPECIFICATION NO. REF: N/A

PACKAGE OUTLINE, 32 LEAD QFN
5.00X5.00X0.8 MM WNP032 3.5X3.5 MM EPAD (SAWN) REV**

002-15160 **

Document History Page

Document Title: MB95630H Series, New 8FX 8-bit Microcontrollers Document Number: 002-04627				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	-	AKIH	06/07/2013	Migrated to Cypress and assigned document number 002-04627. No change to document contents or format.
*A	5193921	AKIH	03/29/2016	Updated to Cypress template Added “MB95F636KPMC-G-UNE2” in “Ordering Information”
*B	5443796	HTER	02/06/2017	Changed three package codes as the following from “FPT-32P-M30” to “LQB032” from “LCC-32P-M19” to “WNP032” from “DIP-32P-M06” to “PDS032” in chapter: 1.Product Line-up (Page 5) 2.Packages And Corresponding Products (Page 5) 4.Pin Assignment (Page 6, 7) 5.Pin Functions (Page 11) 21.Ordering Information (Page 97) 28.Package Dimensions (Page 98 to 100). Added three Part numbers - MB95F632KPMC-G-UNE2 - MB95F633KPMC-G-UNE2 - MB95F634KPMC-G-UNE2 in chapter 21.Ordering Information (Page 97). Deleted four Part numbers - MB95F632KPMC-G-SNE2 - MB95F633KPMC-G-SNE2 - MB95F634KPMC-G-SNE2 - MB95F636KPMC-G-SNE2 in chapter 21.Ordering Information (Page 97).
*C	5746267	AESATP12	05/23/2017	Updated logo and copyright.
*D	5895915	HUAL	09/27/2017	Added Part number “MB95F633HPMC-G-UNERE2” and Packing information Modified from “MB95F634HPMC-G-SNE2” to “MB95F634HPMC-G-UNE2” in 21.Ordering Information (Page 97)