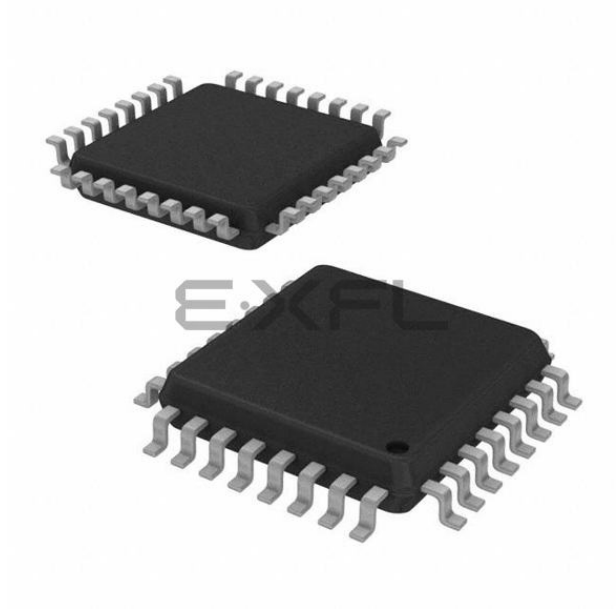


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SIO, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	29
Program Memory Size	20KB (20K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f634kpmc-g-sne2

<table>
<tr><th>Part number
Parameter</th><th>MB95F632H</th><th>MB95F633H</th><th>MB95F634H</th><th>MB95F636H</th><th>MB95F632K</th><th>MB95F633K</th><th>MB95F634K</th><th>MB95F636K</th></tr>
<tr><td>Flash memory</td><td colspan="8">• It supports automatic programming (Embedded Algorithm), and program/erase/erase-suspend/erase-resume commands.
• It has a flag indicating the completion of the operation of Embedded Algorithm.
• Flash security feature for protecting the content of the Flash memory
<table><tr><td>Number of program/erase cycles</td><td>1000</td><td>10000</td><td>100000</td></tr><tr><td>Data retention time</td><td>20 years</td><td>10 years</td><td>5 years</td></tr></table></td></tr>
<tr><td>Standby mode</td><td colspan="8">There are four standby modes as follows:
• Stop mode
• Sleep mode
• Watch mode
• Time-base timer mode
In standby mode, two further options can be selected: normal standby mode and deep standby mode.</td></tr>
<tr><td>Package</td><td colspan="8">LQB032
PDS032
WNP032</td></tr>
</table>

2. Packages And Corresponding Products

Part number / Package	MB95F632H	MB95F633H	MB95F634H	MB95F636H	MB95F632K	MB95F633K	MB95F634K	MB95F636K
LQB032	O	O	O	O	O	O	O	O
PDS032	O	O	O	O	O	O	O	O
WNP032	O	O	O	O	O	O	O	O

O: Available

3. Differences Among Products And Notes On Product Selection

- Current consumption
  When using the on-chip debug function, take account of the current consumption of Flash memory program/erase.
  For details of current consumption, see “Electrical Characteristics”.

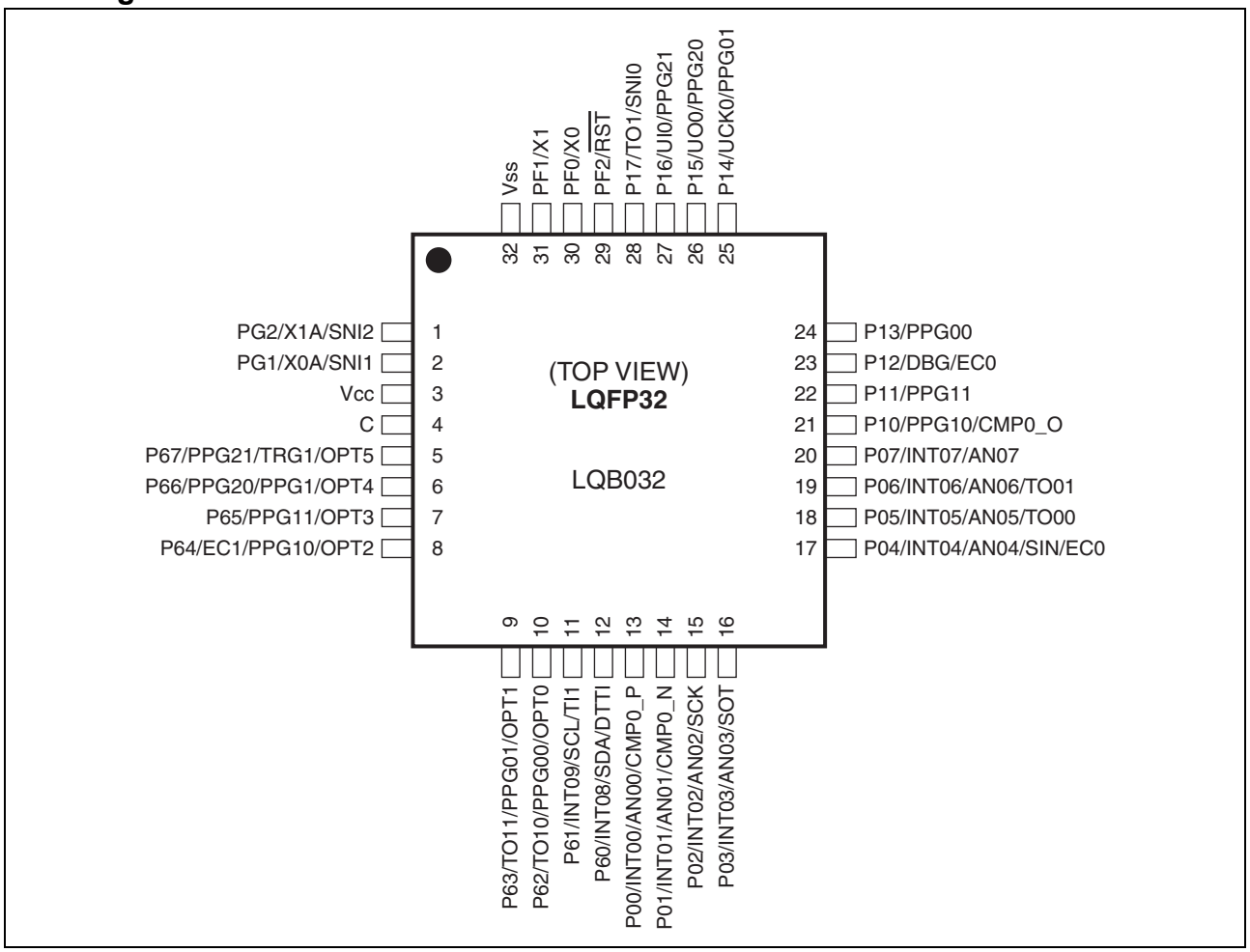
- Package
  For details of information on each package, see “Packages And Corresponding Products” and “Package Dimension”.

- Operating voltage
  The operating voltage varies, depending on whether the on-chip debug function is used or not.
  For details of operating voltage, see “Electrical Characteristics”.

- On-chip debug function

The on-chip debug function requires that Vcc, Vss and one serial wire be connected to an evaluation tool. For details of the connection method, refer to “CHAPTER 25 EXAMPLE OF SERIAL PROGRAMMING CONNECTION” in “New 8FX MB95630H Series Hardware Manual”.

4. Pin Assignment



5. Pin Functions

Pin no.		Pin name	I/O circuit type*4	Function	I/O type			
LQFP32*1, QFN32*2	SH-DIP32*3				Input	Output	OD*5	PU*6
1	5	PG2	C	General-purpose I/O port	Hysteresis	CMOS	—	O
		X1A		Subclock I/O oscillation pin				
		SNI2		Trigger input pin for the position detection function of the MPG waveform sequencer				
2	6	PG1	C	General-purpose I/O port	Hysteresis	CMOS	—	O
		X0A		Subclock input oscillation pin				
		SNI1		Trigger input pin for the position detection function of the MPG waveform sequencer				
3	7	V_{CC}	—	Power supply pin	—	—	—	—
4	8	C	—	Decoupling capacitor connection pin	—	—	—	—
5	9	P67	D	General-purpose I/O port High-current pin	Hysteresis	CMOS	—	O
		PPG21		8/16-bit PPG ch. 2 output pin				
		TRG1		16-bit PPG timer ch. 1 trigger input pin				
		OPT5		MPG waveform sequencer output pin				
6	10	P66	D	General-purpose I/O port High-current pin	Hysteresis	CMOS	—	O
		PPG20		8/16-bit PPG ch. 2 output pin				
		PPG1		16-bit PPG timer ch. 1 output pin				
		OPT4		MPG waveform sequencer output pin				
7	11	P65	D	General-purpose I/O port High-current pin	Hysteresis	CMOS	—	O
		PPG11		8/16-bit PPG ch. 1 output pin				
		OPT3		MPG waveform sequencer output pin				
8	12	P64	D	General-purpose I/O port High-current pin	Hysteresis	CMOS	—	O
		EC1		8/16-bit composite timer ch. 1 clock input pin				
		PPG10		8/16-bit PPG ch. 1 output pin				
		OPT2		MPG waveform sequencer output pin				

7.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

(1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

(2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

(3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

(4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

(5) Smoke, Flame

CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

8. Notes On Device Handling

- Preventing latch-ups
  When using the device, ensure that the voltage applied does not exceed the maximum voltage rating.
  In a CMOS IC, if a voltage higher than V_{CC} or a voltage lower than V_{SS} is applied to an input/output pin that is neither a medium-withstand voltage pin nor a high-withstand voltage pin, or if a voltage out of the rating range of power supply voltage mentioned in “18.1 Absolute Maximum Ratings” of “Electrical Characteristics” is applied to the V_{CC} pin or the V_{SS} pin, a latch-up may occur.
  When a latch-up occurs, power supply current increases significantly, which may cause a component to be thermally destroyed.

- Stabilizing supply voltage
  Supply voltage must be stabilized.
  A malfunction may occur when power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the V_{CC} power supply voltage.
  As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in V_{CC} ripple (p-p value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard V_{CC} value, and the transient fluctuation rate does not exceed 0.1 V/ms at a momentary fluctuation such as switching the power supply.

- Notes on using the external clock
  When an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from sub-clock mode or stop mode.

15.2.3 Port 1 registers

- Port 1 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR1	0	Pin state is “L” level.	PDR1 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR1 value is “1”.	As output port, outputs “H” level.*
DDR1	0	Port input enabled		
	1	Port output enabled		
PUL1	0	Pull-up disabled		
	1	Pull-up enabled		

*: If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

- Correspondence between registers and pins for port 1

	Correspondence between related register bits and pins							
Pin name	P17	P16	P15	P14	P13	P12	P11	P10
PDR1	bit7	bit6	bit5	bit4	bit3	bit2*	bit1	bit0
DDR1								
PUL1								

*: Though P12 has no pull-up function, bit2 in the PUL1 register can still be accessed. The operation of P12 is not affected by the setting of bit2 in the PUL1 register.

15.2.4 Port 1 operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDR1 register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDR1 register to external pins.
  - If data is written to the PDR1 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDR1 register returns the PDR1 register value.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDR1 register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDR1 register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDR1 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR1 register, the PDR1 register value is returned.

- Operation as a peripheral function output pin
  - A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
  - The pin value can be read from the PDR1 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR1 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR1 register, the PDR1 register value is returned.

- Operation as a peripheral function input pin
  - To set a pin as an input port, set the bit in the DDR1 register corresponding to the input pin of a peripheral function

to “0”.
- Reading the PDR1 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR1 register, the PDR1 register value is returned.

- Operation at reset
  If the CPU is reset, all bits in the DDR1 register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR1 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open. However, if the interrupt input of P14/UCK0 and P16/UI0 is enabled by the external interrupt control register ch. 0 (EIC00) of the external interrupt circuit and the interrupt pin selection circuit control register (WICR) of the interrupt pin selection circuit, the input is enabled and is not blocked.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

- Operation of the pull-up register
  Setting the bit in the PUL1 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL1 register.

15.3 Port 6

Port 6 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95630H Series Hardware Manual”.

15.3.1 Port 6 configuration

Port 6 is made up of the following elements.
- General-purpose I/O pins/peripheral function I/O pins
- Port 6 data register (PDR6)
- Port 6 direction register (DDR6)
- Port 6 pull-up register (PUL6)

15.3.2 Block diagrams of port 6

- P60/INT08/SDA/DTTI pin
  This pin has the following peripheral functions:
  - External interrupt circuit input pin (INT08)
  - I²C bus interface ch. 0 data I/O pin (SDA)
  - MPG waveform sequencer input pin (DTTI)

- P61/INT09/SCL/TI1 pin
  This pin has the following peripheral functions:
  - External interrupt circuit input pin (INT09)
  - I²C bus interface ch. 0 clock I/O pin (SCL)
  - 16-bit reload timer ch. 1 input pin (TI1)

17. Pin States In Each Mode

Pin name	Normal operation	Sleep mode	Stop mode		Watch mode		On reset
			SPL=0	SPL=1	SPL=0	SPL=1	
PF0/X0	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*4	I/O port*4	- Previous state kept - Input blocked*2*4	- Hi-Z - Input blocked*2*4	- Previous state kept - Input blocked*2*4	- Hi-Z - Input blocked*2*4	- Hi-Z - Input enabled*1 (However, it does not function.)
PF1/X1	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*4	I/O port*4	- Previous state kept - Input blocked*2*4	- Hi-Z - Input blocked*2*4	- Previous state kept - Input blocked*2*4	- Hi-Z - Input blocked*2*4	- Hi-Z - Input enabled*1 (However, it does not function.)
PG1/X0A/ SNI1	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*4/ peripheral function I/O	I/O port*4/ peripheral function I/O	- Previous state kept - Input blocked*2*4	- Hi-Z (However, the setting of the pull-up control is effective.) - Input blocked*2*4	- Previous state kept - Input blocked*2*4	- Hi-Z (However, the setting of the pull-up control is effective.) - Input blocked*2*4	- Hi-Z - Input enabled*1 (However, it does not function.)
PG2/X1A/ SNI2	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*4/ peripheral function I/O	I/O port*4/ peripheral function I/O	- Previous state kept - Input blocked*2*4	- Hi-Z (However, the setting of the pull-up control is effective.) - Input blocked*2*4	- Previous state kept - Input blocked*2*4	- Hi-Z (However, the setting of the pull-up control is effective.) - Input blocked*2*4	- Hi-Z - Input enabled*1 (However, it does not function.)
PF2/$\overline{\text{RST}}$	I/O port	Reset input	Reset input	Reset input	Reset input	Reset input	Reset input*3
P60/INT08/ SDA/DTTI	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*2 (However, an external interrupt can be input when the external interrupt request is enabled.)	- Hi-Z - Input blocked*2 (However, an external interrupt can be input when the external interrupt request is enabled.)	- Previous state kept - Input blocked*2 (However, an external interrupt can be input when the external interrupt request is enabled.)	- Hi-Z - Input blocked*2 (However, an external interrupt can be input when the external interrupt request is enabled.)	- Hi-Z - Input enabled*1 (However, it does not function.)
P61/INT09/ SCL/TI1							
P62/TO10/ PPG00/ OPT0	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*2	- Hi-Z (However, the setting of the pull-up control is effective.) - Input blocked*2	- Previous state kept - Input blocked*2	- Hi-Z (However, the setting of the pull-up control is effective.) - Input blocked*2	- Hi-Z - Input enabled*1 (However, it does not function.)
P63/TO11/ PPG01/ OPT1							

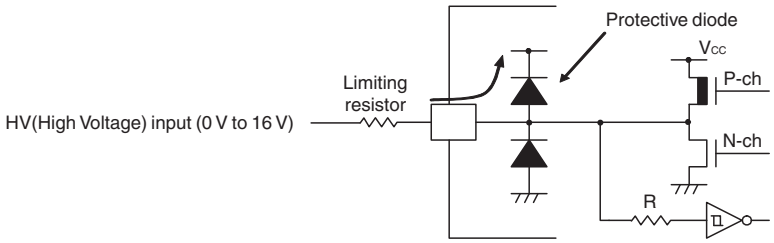
18. Electrical Characteristics

18.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} – 0.3	V_{SS} + 6	V	
Input voltage*1	V_I	V_{SS} – 0.3	V_{SS} + 6	V	*2
Output voltage*1	V_O	V_{SS} – 0.3	V_{SS} + 6	V	*2
Maximum clamp current	I_{CLAMP}	–2	+2	mA	Applicable to specific pins*3
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	—	20	mA	Applicable to specific pins*3
“L” level maximum output current	I_{OL}	—	15	mA	
“L” level average current	I_{OLAV1}	—	4	mA	Other than P62 to P67 Average output current = operating current × operating ratio (1 pin)
	I_{OLAV2}		12		P62 to P67 Average output current = operating current × operating ratio (1 pin)
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	37	mA	Total average output current = operating current × operating ratio (Total number of pins)
“H” level maximum output current	I_{OH}	—	–15	mA	
“H” level average current	I_{OHAV1}	—	–4	mA	Other than P62 to P67 Average output current = operating current × operating ratio (1 pin)
	I_{OHAV2}		–8		P62 to P67 Average output current = operating current × operating ratio (1 pin)
“H” level total maximum output current	ΣI_{OH}	—	–100	mA	
“H” level total average output current	ΣI_{OHAV}	—	–47	mA	Total average output current = operating current × operating ratio (Total number of pins)
Power consumption	P_d	—	320	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	T_{stg}	–55	+150	°C	

*1: These parameters are based on the condition that V_{SS} is 0.0 V.
*2: V_I and V_O must not exceed V_{CC} + 0.3 V. V_I must not exceed the rated voltage. However, if the maximum current to/from an input is limited by means of an external component, the I_{CLAMP} rating is used instead of the V_I rating.
*3: Specific pins: P00 to P07, P10, P11, P13 to P17, P62 to P67, PF0, PF1, PG1, PG2

- Use under recommended operating conditions.
- Use with DC voltage (current).
- The HV (High Voltage) signal is an input signal exceeding the V_{CC} voltage. Always connect a limiting resistor between the HV (High Voltage) signal and the microcontroller before applying the HV (High Voltage) signal.
- The value of the limiting resistor should be set to a value at which the current to be input to the microcontroller pin when the HV (High Voltage) signal is input is below the standard value, irrespective of whether the current is transient current or stationary current.
- When the microcontroller drive current is low, such as in low power consumption modes, the HV (High Voltage) input potential may pass through the protective diode to increase the potential of the V_{CC} pin, affecting other devices.
- If the HV (High Voltage) signal is input when the microcontroller power supply is off (not fixed at 0 V), since power is supplied from the pins, incomplete operations may be executed.
- If the HV (High Voltage) input is input after power-on, since power is supplied from the pins, the voltage of power supply may not be sufficient to enable a power-on reset.
- Do not leave the HV (High Voltage) input pin unconnected.
- Example of a recommended circuit:
  - Input/Output equivalent circuit



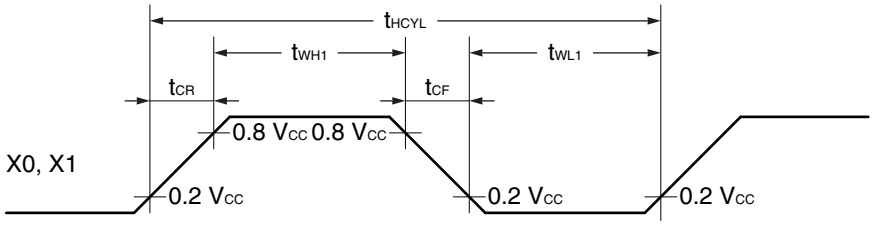
WARNING: Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings.
Do not exceed any of these ratings.

(V_{CC} = 2.4 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock cycle time	t_{HCYL}	X0, X1	—	61.5	—	1000	ns	When the main oscillation circuit is used
		X0	X1: open	83.4	—	1000	ns	When an external clock is used
		X0, X1	*	30.8	—	1000	ns	
	t_{LCYL}	X0A, X1A	—	—	30.5	—	µs	When the subclock is used
Input clock pulse width	t_{WH1}, t_{WL1}	X0	X1: open	33.4	—	—	ns	When an external clock is used, the duty ratio should range between 40% and 60%.
		X0, X1	*	12.4	—	—	ns	
	t_{WH2}, t_{WL2}	X0A	—	—	15.2	—	µs	
Input clock rising time and falling time	t_{CR}, t_{CF}	X0, X0A	X1: open	—	—	5	ns	When an external clock is used
		X0, X1, X0A, X1A	*	—	—	5	ns	
CR oscillation start time	t_{CRHWK}	—	—	—	—	50	µs	When the main CR clock is used
	t_{CRLWK}	—	—	—	—	30	µs	When the sub-CR clock is used
PLL oscillation start time	$t_{MCRPLLWK}$	—	—	—	—	100	µs	When the main CR PLL clock is used

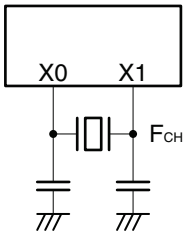
*: The external clock signal is input to X0 and the inverted external clock signal to X1.

- Input waveform generated when an external clock (main clock) is used

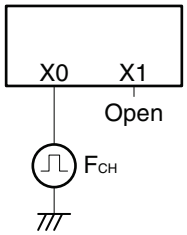


- Figure of main clock input port external connection

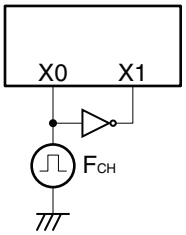
When a crystal oscillator or a ceramic oscillator is used



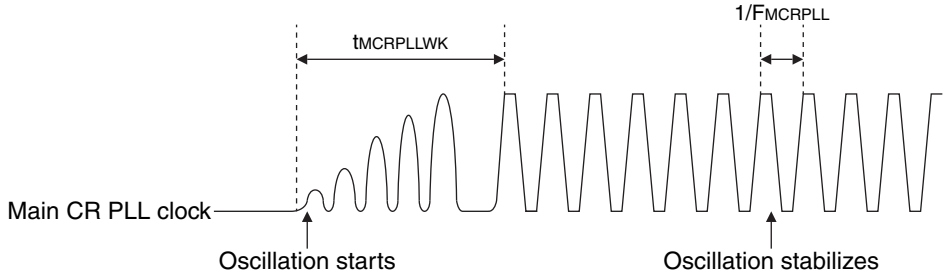
When an external clock is used (X1 is open)



When an external clock is used



- Input waveform generated when an internal clock (main CR PLL clock) is used



18.4.2 Source Clock/Machine Clock

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Source clock cycle time*1	t_{SCLK}	—	61.5	—	2000	ns	When the main external clock is used Min: F_{CH} = 32.5 MHz, divided by 2 Max: F_{CH} = 1 MHz, divided by 2
			62.5	—	250	ns	When the main CR clock is used Min: F_{CRH} = 4 MHz, multiplied by 4 Max: F_{CRH} = 4 MHz, no division
			—	61	—	µs	When the suboscillation clock is used F_{CL} = 32.768 kHz, divided by 2
			—	20	—	µs	When the sub-CR clock is used F_{CL} = 100 kHz, divided by 2
Source clock frequency	F_{SP}	—	0.5	—	16.25	MHz	When the main oscillation clock is used
			—	4	—	MHz	When the main CR clock is used
	F_{SPL}		—	16.384	—	kHz	When the suboscillation clock is used
			—	50	—	kHz	When the sub-CR clock is used F_{CRL} = 100 kHz, divided by 2
Machine clock cycle time*2 (minimum instruction execution time)	t_{MCLK}	—	61.5	—	32000	ns	When the main oscillation clock is used Min: F_{SP} = 16.25 MHz, no division Max: F_{SP} = 0.5 MHz, divided by 16
			250	—	4000	ns	When the main CR clock is used Min: F_{SP} = 4 MHz, no division Max: F_{SP} = 4 MHz, divided by 16
			61	—	976.5	µs	When the suboscillation clock is used Min: F_{SPL} = 16.384 kHz, no division Max: F_{SPL} = 16.384 kHz, divided by 16
			20	—	320	µs	When the sub-CR clock is used Min: F_{SPL} = 50 kHz, no division Max: F_{SPL} = 50 kHz, divided by 16

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Machine clock frequency	F_{MP}	—	0.031	—	16.25	MHz	When the main oscillation clock is used
			0.25	—	16	MHz	When the main CR clock is used
	F_{MPL}		1.024	—	16.384	kHz	When the suboscillation clock is used
			3.125	—	50	kHz	When the sub-CR clock is used F_{CRL} = 100 kHz

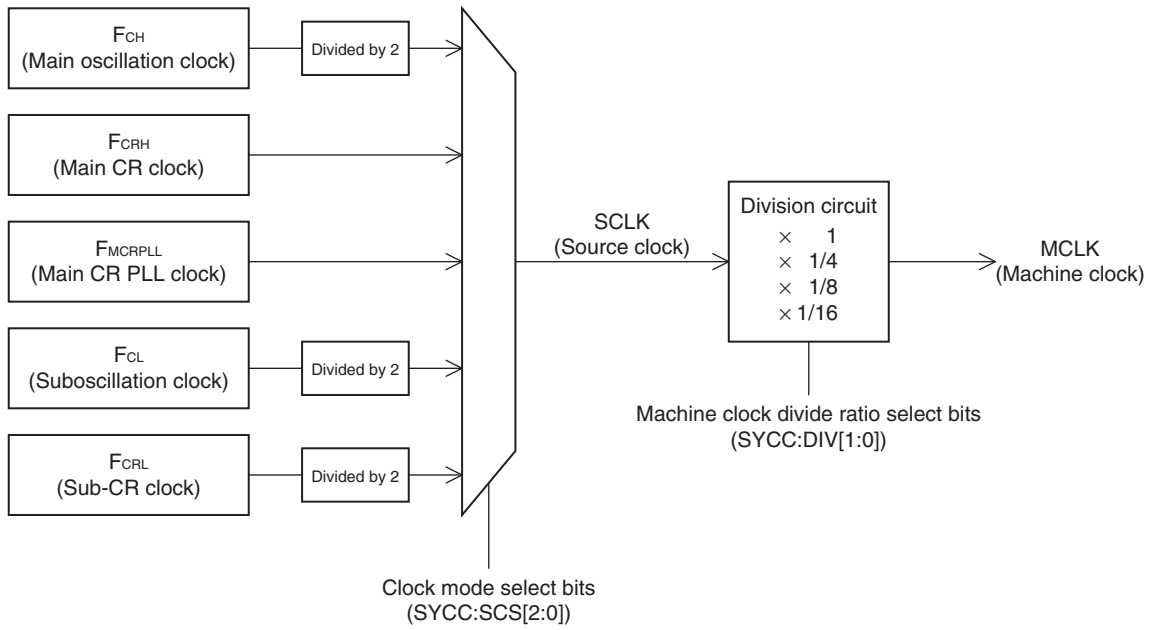
*1: This is the clock before it is divided according to the division ratio set by the machine clock division ratio select bits (SYCC:DIV[1:0]). This source clock is divided to become a machine clock according to the division ratio set by the machine clock division ratio select bits (SYCC:DIV[1:0]). In addition, a source clock can be selected from the following.

- Main clock divided by 2
- Main CR clock
- PLL multiplication of main CR clock (Select a multiplication rate from 2, 2.5, 3 and 4.)
- Subclock divided by 2
- Sub-CR clock divided by 2

*2: This is the operating clock of the microcontroller. A machine clock can be selected from the following.

- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

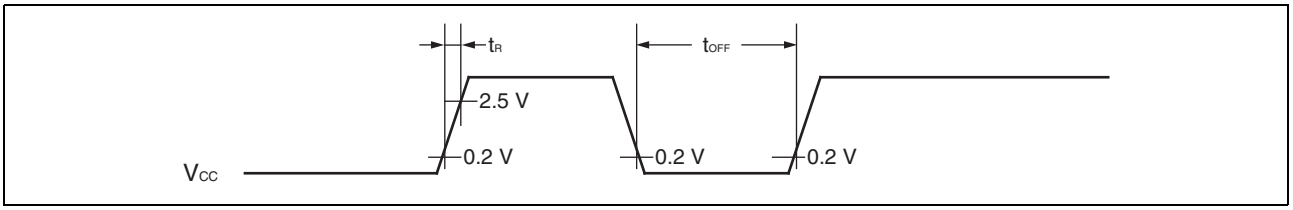
- Schematic diagram of the clock generation block



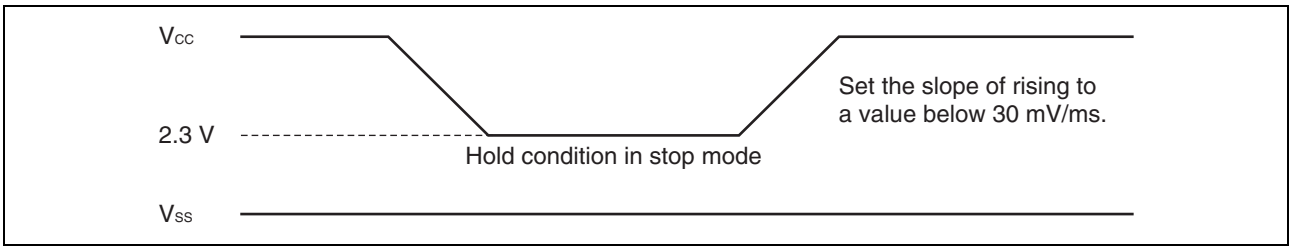
18.4.4 Power-on Reset

(V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_R	—	—	50	ms	
Power supply cutoff time	t_{OFF}	—	1	—	ms	Wait time until power-on



Note: A sudden change of power supply voltage may activate the power-on reset function. When changing the power supply voltage during the operation, set the slope of rising to a value below within 30 mV/ms as shown below.

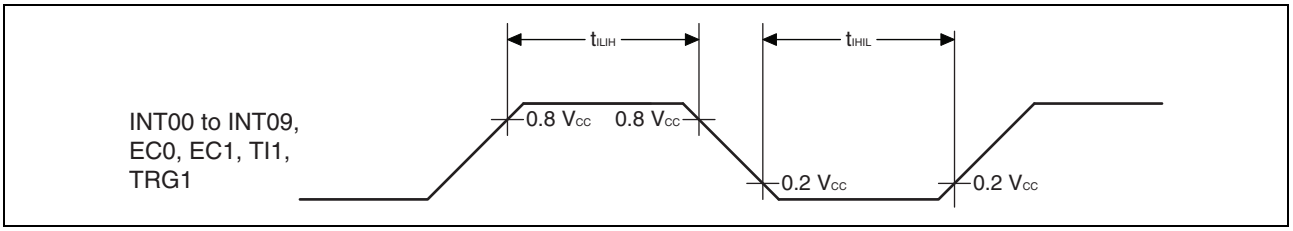


18.4.5 Peripheral Input Timing

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Peripheral input “H” pulse width	t_{ILIH}	INT00 to INT09, EC0, EC1, TI1, TRG1	2 t_{MCLK}*	—	ns
Peripheral input “L” pulse width	t_{IHIL}		2 t_{MCLK}*	—	ns

*: See “Source Clock/Machine Clock” for t_{MCLK}.



18.5 A/D Converter

18.5.1 A/D Converter Electrical Characteristics

(V_{CC} = 2.7 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

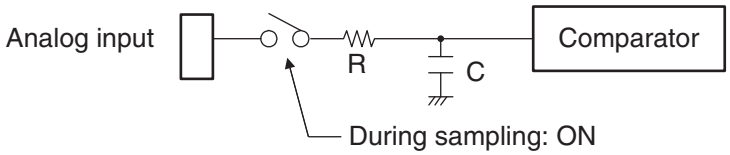
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error		–3	—	+3	LSB	
Linearity error		–2.5	—	+2.5	LSB	
Differential linearity error		–1.9	—	+1.9	LSB	
Zero transition voltage	V_{0T}	V_{SS} – 1.5 LSB	V_{SS} + 0.5 LSB	V_{SS} + 2.5 LSB	V	
Full-scale transition voltage	V_{FST}	V_{CC} – 4.5 LSB	V_{CC} – 2 LSB	V_{CC} + 0.5 LSB	V	
Compare time	—	3	—	10	µs	2.7 V ≤ V_{CC} ≤ 5.5 V
Sampling time	—	0.941	—	∞	µs	2.7 V ≤ V_{CC} ≤ 5.5 V, with external impedance < 3.3 kΩ and external capacitance = 10 pF
Analog input current	I_{AIN}	–0.3	—	+0.3	µA	
Analog input voltage	V_{AIN}	V_{SS}	—	V_{CC}	V	

18.5.2 Notes on Using A/D Converter

- External impedance of analog input and its sampling time

  The A/D converter of the MB95630H Series has a sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the capacitor of the internal sample and hold circuit is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, considering the relationship between the external impedance and minimum sampling time, either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. In addition, if sufficient sampling time cannot be secured, connect a capacitor of about 0.1 µF to the analog input pin.

- Analog input equivalent circuit



V_{CC}	R	C
4.5 V ≤ V_{CC} ≤ 5.5 V	1.45 kΩ (Max)	14.89 pF (Max)
2.7 V ≤ V_{CC} < 4.5 V	2.7 kΩ (Max)	14.89 pF (Max)

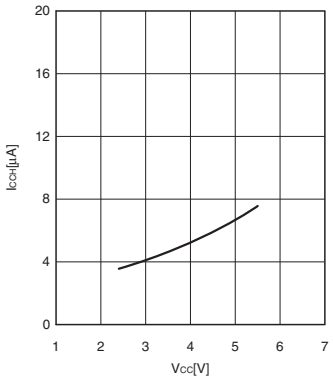
Note: The values are reference values.

18.6 Flash Memory Program/Erase Characteristics

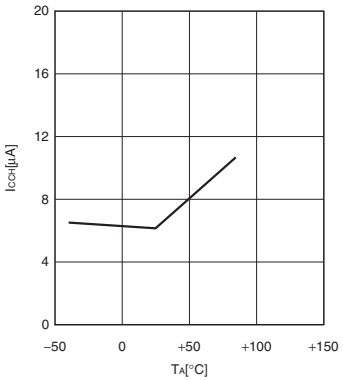
Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time (2 Kbyte sector)	—	0.3*1	1.6*2	s	The time of writing “0x00” prior to erasure is excluded.
Sector erase time (32 Kbyte sector)	—	0.6*1	3.1*2	s	The time of writing “0x00” prior to erasure is excluded.
Byte writing time	—	17	272	µs	System-level overhead is excluded.
Program/erase cycle	100000	—	—	cycle	
Power supply voltage at program/erase	2.4	—	5.5	V	
Flash memory data retention time	20*3	—	—	year	Average T_A = +85°C Number of program/erase cycles: 1000 or below
	10*3	—	—		Average T_A = +85°C Number of program/erase cycles: 1001 to 10000 inclusive
	5*3	—	—		Average T_A = +85°C Number of program/erase cycles: 10001 or above

*1: V_{CC} = 5.5 V, T_A = +25°C, 0 cycle
*2: V_{CC} = 2.4 V, T_A = +85°C, 100000 cycles
*3: These values were converted from the result of a technology reliability assessment. (These values were converted from the result of a high temperature accelerated test using the Arrhenius equation with the average temperature being +85°C.)

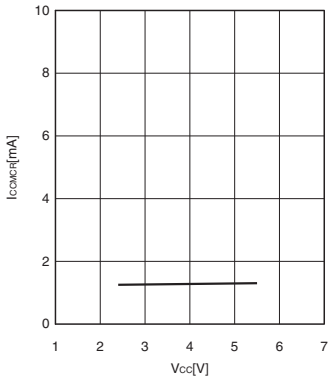
I_{CCH} – V_{CC}
T_A = +25°C, F_{MPL} = (stop)
Substop mode with the external clock stopping



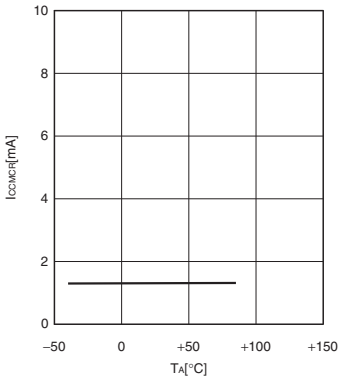
I_{CCH} – T_A
V_{CC} = 5.5 V, F_{MPL} = (stop)
Substop mode with the external clock stopping



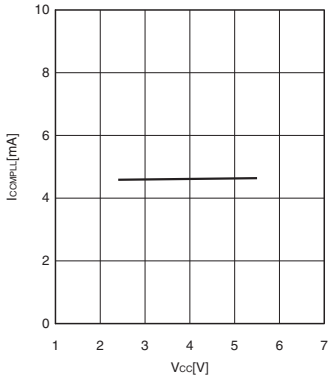
I_{CCMCR} – V_{CC}
T_A = +25°C, F_{MP} = 4 MHz (no division)
Main CR clock mode



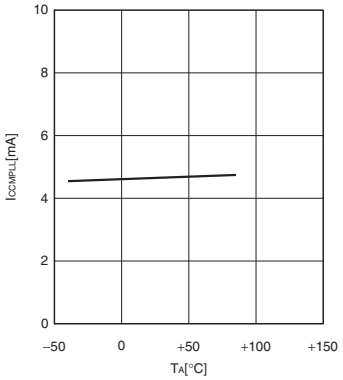
I_{CCMCR} – T_A
V_{CC} = 5.5 V, F_{MP} = 4 MHz (no division)
Main CR clock mode



I_{CCMPLL} – V_{CC}
T_A = +25°C, F_{MP} = 16 MHz (PLL multiplication rate: 4)
Main CR PLL clock mode



I_{CCMPLL} – T_A
V_{CC} = 5.5 V, F_{MP} = 16 MHz (PLL multiplication rate: 4)
Main CR PLL clock mode



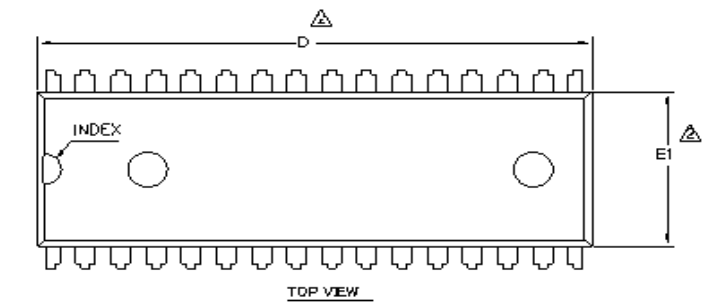
20. Mask Options

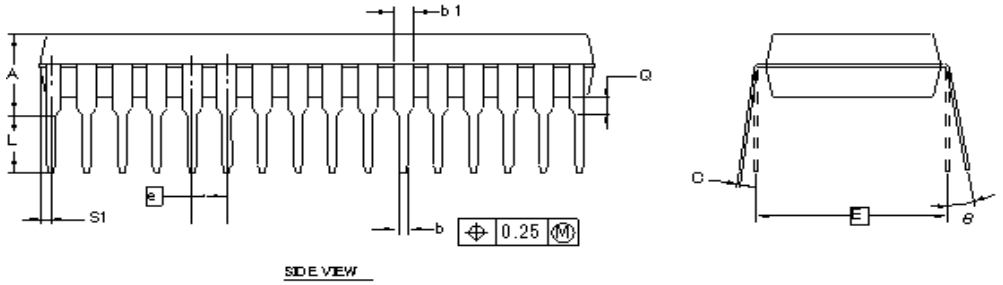
No.	Part number	MB95F632H MB95F633H MB95F634H MB95F636H	MB95F632K MB95F633K MB95F634K MB95F636K
	Selectable/Fixed	Fixed	
1	Low-voltage detection reset	Without low-voltage detection reset	With low-voltage detection reset
2	Reset	With dedicated reset input	Without dedicated reset input

21. Ordering Information

Part number	Package	Packing
MB95F632HPMC-G-SNE2 MB95F632KPMC-G-UNE2 MB95F633HPMC-G-SNE2 MB95F633KPMC-G-UNE2 MB95F634HPMC-G-UNE2 MB95F634KPMC-G-UNE2 MB95F636HPMC-G-SNE2 MB95F636KPMC-G-UNE2	32-pin plastic LQFP (LQB032)	Tray
MB95F633HPMC-G-UNERE2		Reel
MB95F632HP-G-SH-SNE2 MB95F632KP-G-SH-SNE2 MB95F633HP-G-SH-SNE2 MB95F633KP-G-SH-SNE2 MB95F634HP-G-SH-SNE2 MB95F634KP-G-SH-SNE2 MB95F636HP-G-SH-SNE2 MB95F636KP-G-SH-SNE2	32-pin plastic SH-DIP (PDS032)	Tube
MB95F632HWQN-G-SNE1 MB95F632KWQN-G-SNE1 MB95F633HWQN-G-SNE1 MB95F633KWQN-G-SNE1 MB95F634HWQN-G-SNE1 MB95F634KWQN-G-SNE1 MB95F636HWQN-G-SNE1 MB95F636KWQN-G-SNE1	32-pin plastic QFN (WNP032)	Tray

Package Type	Package Code
SDIP 32	PDS032





SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	4.50	4.70	5.40
L	3.00	3.30	3.50
D	27.70	28.00	28.20
E	10.16 BSC		
E1	8.64	8.89	9.14
θ	0°	——	15°
c	0.20	0.27	0.30
b	0.36	0.48	0.56
b1	0.82	1.02	1.32
e	1.778 BSC		
S1	——	——	1.27
Q	0.51	——	——

NOTES
1. ALL DIMENSIONS ARE IN MILLIMETER.
2. DIMENSIONS NOT INCLUDE RESIN REMAINING.
3. TERMINAL WIDTH AND TERMINAL THICKNESS INCLUDE PLATING THICKNESS.
4. JEDEC SPECIFICATION NO. REF : N/A

PACKAGE OUTLINE, 32 LEAD PDIP
28.00X8.89X4.19 MM PDS032 REV**

002-16908 **

23. Major Changes In This Edition

Spansion Publication Number: DS702-00009

Page	Section	Details
22	■ PIN CONNECTION • C pin	Corrected the following statement. The bypass capacitor for the V_{CC} pin must have a capacitance larger than C_S. → The decoupling capacitor for the V_{CC} pin must have a capacitance equal to or larger than the capacitance of C_S.
66	■ ELECTRICAL CHARACTERISTICS 2. Recommended Operating Conditions	Corrected the following statement in remark *2. The bypass capacitor for the V_{CC} pin must have a capacitance larger than C_S. → The decoupling capacitor for the V_{CC} pin must have a capacitance equal to or larger than the capacitance of C_S.
71	4. AC Characteristics (1) Clock Timing	Corrected the pin names of the parameter “Input clock rising time and falling time”. X0 → X0, X0A X0, X1 → X0, X1, X0A, X1A

NOTE: Please see “Document History” about later revised information.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless/RF	cypress.com/wireless

PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP| PSoC 6

Cypress Developer Community

Forums | WICED IOT Forums | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support