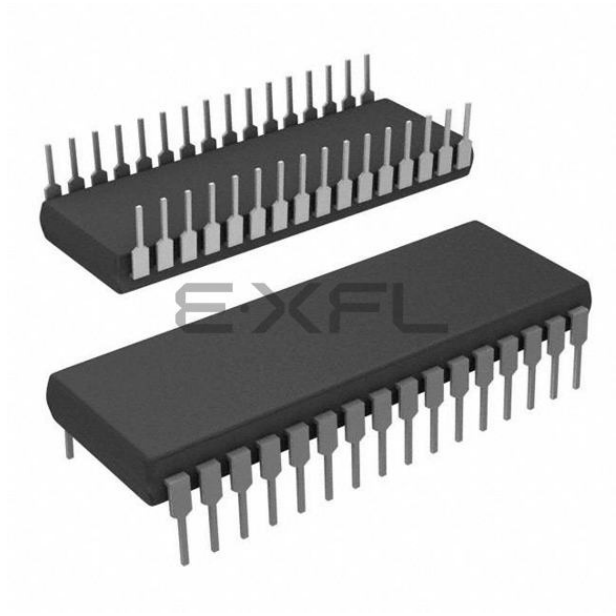
Infineon Technologies - MB95F636HP-G-SH-SNE2 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SIO, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	28
Program Memory Size	36KB (36K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	32-SDIP (0.400", 10.16mm)
Supplier Device Package	32-SDIP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f636hp-g-sh-sne2

Part number / Parameter	MB95F632H	MB95F633H	MB95F634H	MB95F636H	MB95F632K	MB95F633K	MB95F634K	MB95F636K
External interrupt	10 channels							
	• Interrupt by edge detection (The rising edge, falling edge, and both edges can be selected.) • It can be used to wake up the device from different standby modes.							
On-chip debug	• 1-wire serial control • It supports serial writing (asynchronous mode).							
UART/SIO	1 channel							
	• Data transfer with UART/SIO is enabled. • It has a full duplex double buffer, variable data length (5/6/7/8 bits), an internal baud rate generator and an error detection function. • It uses the NRZ type transfer format. • LSB-first data transfer and MSB-first data transfer are available to use. • Both clock asynchronous (UART) serial data transfer and clock synchronous (SIO) serial data transfer are enabled.							
I^2C bus interface	1 channel							
	• Master/slave transmission and reception • It has the following functions: bus error function, arbitration function, transfer direction detection function, wake-up function, and functions of generating and detecting repeated START conditions.							
8/16-bit PPG	3 channels							
	• Each channel can be used as an “8-bit timer × 2 channels” or a “16-bit timer × 1 channel”. • The counter operating clock can be selected from eight clock sources.							
16-bit PPG timer	1 channel							
	• PWM mode and one-shot mode are available to use. • The counter operating clock can be selected from eight clock sources. • It supports external trigger start. • It can work independently or together with the multi-pulse generator.							
16-bit reload timer	1 channel							
	• Two clock modes and two counter operating modes are available to use. • It can output square wave. • Count clock: it can be selected from internal clocks (seven types) and external clocks. • Two counter operating modes: reload mode and one-shot mode • It can work independently or together with the multi-pulse generator.							
Multi-pulse generator (for DC motor control)	• 16-bit PPG timer: 1 channel • 16-bit reload timer operations: toggle output, one-shot output • Event counter: 1 channel • Waveform sequencer (including a 16-bit timer equipped with a buffer and a compare clear function)							
Watch prescaler	Eight different time intervals can be selected.							
Comparator	1 channel							

<table>
<tr><th>Part number
Parameter</th><th>MB95F632H</th><th>MB95F633H</th><th>MB95F634H</th><th>MB95F636H</th><th>MB95F632K</th><th>MB95F633K</th><th>MB95F634K</th><th>MB95F636K</th></tr>
<tr><td>Flash memory</td><td colspan="8">• It supports automatic programming (Embedded Algorithm), and program/erase/erase-suspend/erase-resume commands.
• It has a flag indicating the completion of the operation of Embedded Algorithm.
• Flash security feature for protecting the content of the Flash memory
<table><tr><td>Number of program/erase cycles</td><td>1000</td><td>10000</td><td>100000</td></tr><tr><td>Data retention time</td><td>20 years</td><td>10 years</td><td>5 years</td></tr></table></td></tr>
<tr><td>Standby mode</td><td colspan="8">There are four standby modes as follows:
• Stop mode
• Sleep mode
• Watch mode
• Time-base timer mode
In standby mode, two further options can be selected: normal standby mode and deep standby mode.</td></tr>
<tr><td>Package</td><td colspan="8">LQB032
PDS032
WNP032</td></tr>
</table>

2. Packages And Corresponding Products

Part number / Package	MB95F632H	MB95F633H	MB95F634H	MB95F636H	MB95F632K	MB95F633K	MB95F634K	MB95F636K
LQB032	O	O	O	O	O	O	O	O
PDS032	O	O	O	O	O	O	O	O
WNP032	O	O	O	O	O	O	O	O

O: Available

3. Differences Among Products And Notes On Product Selection

- Current consumption
  When using the on-chip debug function, take account of the current consumption of Flash memory program/erase.
  For details of current consumption, see “Electrical Characteristics”.

- Package
  For details of information on each package, see “Packages And Corresponding Products” and “Package Dimension”.

- Operating voltage
  The operating voltage varies, depending on whether the on-chip debug function is used or not.
  For details of operating voltage, see “Electrical Characteristics”.

- On-chip debug function

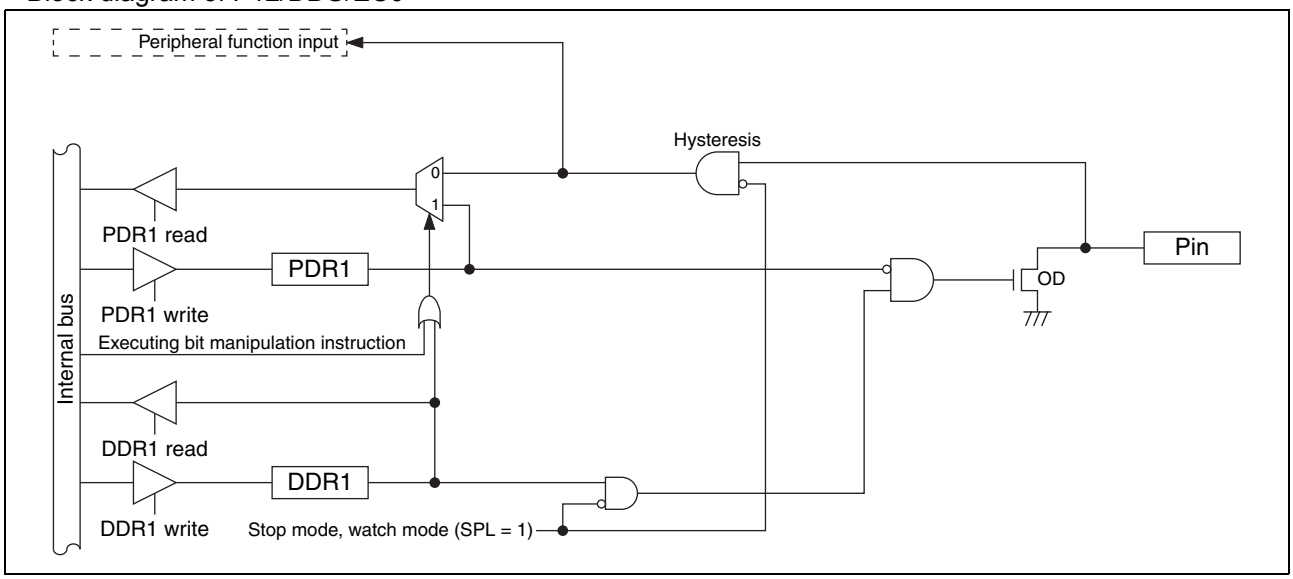
Pin no.		Pin name	I/O circuit type*4	Function	I/O type			
LQFP32*1, QFN32*2	SH-DIP32*3				Input	Output	OD*5	PU*6
15	19	P02	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		INT02		External interrupt input pin				
		AN02		8/10-bit A/D converter analog input pin				
		SCK		LIN-UART clock I/O pin				
16	20	P03	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		INT03		External interrupt input pin				
		AN03		8/10-bit A/D converter analog input pin				
		SOT		LIN-UART data output pin				
17	21	P04	F	General-purpose I/O port	CMOS/ analog	CMOS	—	O
		INT04		External interrupt input pin				
		AN04		8/10-bit A/D converter analog input pin				
		SIN		LIN-UART data input pin				
		EC0		8/16-bit composite timer ch. 0 clock input pin				
18	22	P05	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		INT05		External interrupt input pin				
		AN05		8/10-bit A/D converter analog input pin				
		TO00		8/16-bit composite timer ch. 0 output pin				
19	23	P06	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		INT06		External interrupt input pin				
		AN06		8/10-bit A/D converter analog input pin				
		TO01		8/16-bit composite timer ch. 0 output pin				
20	24	P07	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		INT07		External interrupt input pin				
		AN07		8/10-bit A/D converter analog input pin				
21	25	P10	G	General-purpose I/O port	Hysteresis	CMOS	—	O
		PPG10		8/16-bit PPG ch. 1 output pin				
		CMP0_O		Comparator digital output pin				

Address	Register abbreviation	Register name	R/W	Initial value
0x005A	RDR0	UART/SIO serial input data register	R	0b00000000
0x005B to 0x005F	—	(Disabled)	—	—
0x0060	IBCR00	I²C bus control register 0 ch. 0	R/W	0b00000000
0x0061	IBCR10	I²C bus control register 1 ch. 0	R/W	0b00000000
0x0062	IBSR0	I²C bus status register ch. 0	R/W	0b00000000
0x0063	IDDR0	I²C data register ch. 0	R/W	0b00000000
0x0064	IAAR0	I²C address register ch. 0	R/W	0b00000000
0x0065	ICCR0	I²C clock control register ch. 0	R/W	0b00000000
0x0066	OPCUR	16-bit MPG output control register (upper)	R/W	0b00000000
0x0067	OPCLR	16-bit MPG output control register (lower)	R/W	0b00000000
0x0068	IPCUR	16-bit MPG input control register (upper)	R/W	0b00000000
0x0069	IPCLR	16-bit MPG input control register (lower)	R/W	0b00000000
0x006A	NCCR	16-bit MPG noise cancellation control register	R/W	0b00000000
0x006B	TCSR	16-bit MPG timer control status register	R/W	0b00000000
0x006C	ADC1	8/10-bit A/D converter control register 1	R/W	0b00000000
0x006D	ADC2	8/10-bit A/D converter control register 2	R/W	0b00000000
0x006E	ADDH	8/10-bit A/D converter data register (upper)	R/W	0b00000000
0x006F	ADDL	8/10-bit A/D converter data register (lower)	R/W	0b00000000
0x0070	—	(Disabled)	—	—
0x0071	FSR2	Flash memory status register 2	R/W	0b00000000
0x0072	FSR	Flash memory status register	R/W	0b000X0000
0x0073	SWRE0	Flash memory sector write control register 0	R/W	0b00000000
0x0074	FSR3	Flash memory status register 3	R	0b000XXXXX
0x0075	FSR4	Flash memory status register 4	R/W	0b00000000
0x0076	WREN	Wild register address compare enable register	R/W	0b00000000
0x0077	WROR	Wild register data test setting register	R/W	0b00000000
0x0078	—	Mirror of register bank pointer (RP) and direct bank pointer (DP)	—	—
0x0079	ILR0	Interrupt level setting register 0	R/W	0b11111111
0x007A	ILR1	Interrupt level setting register 1	R/W	0b11111111
0x007B	ILR2	Interrupt level setting register 2	R/W	0b11111111
0x007C	ILR3	Interrupt level setting register 3	R/W	0b11111111
0x007D	ILR4	Interrupt level setting register 4	R/W	0b11111111
0x007E	ILR5	Interrupt level setting register 5	R/W	0b11111111
0x007F	—	(Disabled)	—	—

Address	Register abbreviation	Register name	R/W	Initial value
0x0FCE	OPDBRH5	16-bit MPG output data buffer register (upper) ch. 5	R/W	0b00000000
0x0FCF	OPDBRL5	16-bit MPG output data buffer register (lower) ch. 5	R/W	0b00000000
0x0FD0	OPDBRH6	16-bit MPG output data buffer register (upper) ch. 6	R/W	0b00000000
0x0FD1	OPDBRL6	16-bit MPG output data buffer register (lower) ch. 6	R/W	0b00000000
0x0FD2	OPDBRH7	16-bit MPG output data buffer register (upper) ch. 7	R/W	0b00000000
0x0FD3	OPDBRL7	16-bit MPG output data buffer register (lower) ch. 7	R/W	0b00000000
0x0FD4	OPDBRH8	16-bit MPG output data buffer register (upper) ch. 8	R/W	0b00000000
0x0FD5	OPDBRL8	16-bit MPG output data buffer register (lower) ch. 8	R/W	0b00000000
0x0FD6	OPDBRH9	16-bit MPG output data buffer register (upper) ch. 9	R/W	0b00000000
0x0FD7	OPDBRL9	16-bit MPG output data buffer register (lower) ch. 9	R/W	0b00000000
0x0FD8	OPDBRHA	16-bit MPG output data buffer register (upper) ch. A	R/W	0b00000000
0x0FD9	OPDBRLA	16-bit MPG output data buffer register (lower) ch. A	R/W	0b00000000
0x0FDA	OPDBRHB	16-bit MPG output data buffer register (upper) ch. B	R/W	0b00000000
0x0FDB	OPDBRLB	16-bit MPG output data buffer register (lower) ch. B	R/W	0b00000000
0x0FDC	OPDUR	16-bit MPG output data register (upper)	R	0b0000XXXX
0x0FDD	OPDLR	16-bit MPG output data register (lower)	R	0bXXXXXXXX
0x0FDE	CPCUR	16-bit MPG compare clear register (upper)	R/W	0bXXXXXXXX
0x0FDF	CPCLR	16-bit MPG compare clear register (lower)	R/W	0bXXXXXXXX
0x0FE0, 0x0FE1	—	(Disabled)	—	—
0x0FE2	TMBUR	16-bit MPG timer buffer register (upper)	R	0bXXXXXXXX
0x0FE3	TMBLR	16-bit MPG timer buffer register (lower)	R	0bXXXXXXXX
0x0FE4	CRTH	Main CR clock trimming register (upper)	R/W	0b000XXXXX
0x0FE5	CRTL	Main CR clock trimming register (lower)	R/W	0b000XXXXX
0x0FE6	—	(Disabled)	—	—
0x0FE7	CRTDA	Main CR clock temperature dependent adjustment register	R/W	0b000XXXXX
0x0FE8	SYSC	System configuration register	R/W	0b11000011
0x0FE9	CMCR	Clock monitoring control register	R/W	0b00000000
0x0FEA	CMDR	Clock monitoring data register	R	0b00000000
0x0FEB	WDTH	Watchdog timer selection ID register (upper)	R	0bXXXXXXXX
0x0FEC	WDTL	Watchdog timer selection ID register (lower)	R	0bXXXXXXXX
0x0FED, 0x0FEE	—	(Disabled)	—	—
0x0FEF	WICR	Interrupt pin selection circuit control register	R/W	0b01000000
0x0FF0 to 0x0FFF	—	(Disabled)	—	—

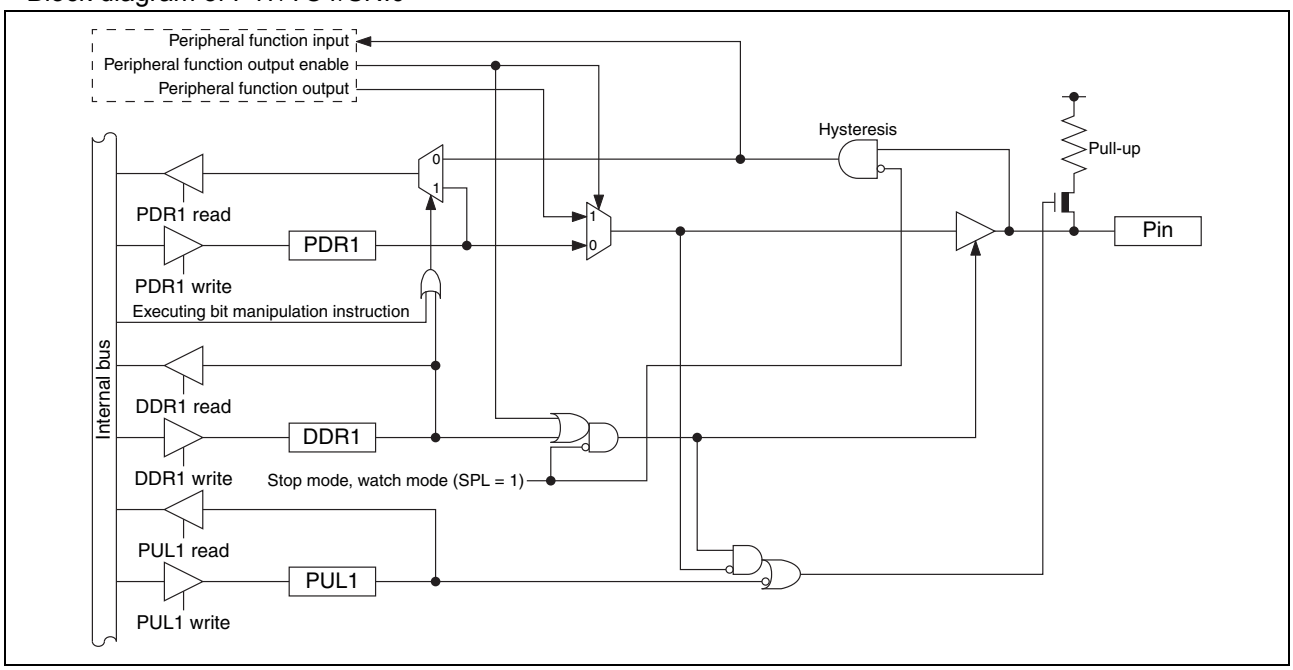
- P12/DBG/EC0 pin
  This pin has the following peripheral functions:
  - DBG input pin (DBG)
  - 8/16-bit composite timer ch. 0 clock input pin (EC0)

- Block diagram of P12/DBG/EC0



- P14/UCK0/PPG01 pin
  This pin has the following peripheral functions:
  - UART/SIO ch. 0 clock I/O pin (UCK0)
  - 8/16-bit PPG ch. 0 output pin (PPG01)

- Block diagram of P17/TO1/SNI0



to “0”.
- Reading the PDR1 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR1 register, the PDR1 register value is returned.

- Operation at reset
  If the CPU is reset, all bits in the DDR1 register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR1 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open. However, if the interrupt input of P14/UCK0 and P16/UI0 is enabled by the external interrupt control register ch. 0 (EIC00) of the external interrupt circuit and the interrupt pin selection circuit control register (WICR) of the interrupt pin selection circuit, the input is enabled and is not blocked.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

- Operation of the pull-up register
  Setting the bit in the PUL1 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL1 register.

15.3 Port 6

Port 6 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95630H Series Hardware Manual”.

15.3.1 Port 6 configuration

Port 6 is made up of the following elements.
- General-purpose I/O pins/peripheral function I/O pins
- Port 6 data register (PDR6)
- Port 6 direction register (DDR6)
- Port 6 pull-up register (PUL6)

15.3.2 Block diagrams of port 6

- P60/INT08/SDA/DTTI pin
  This pin has the following peripheral functions:
  - External interrupt circuit input pin (INT08)
  - I²C bus interface ch. 0 data I/O pin (SDA)
  - MPG waveform sequencer input pin (DTTI)

- P61/INT09/SCL/TI1 pin
  This pin has the following peripheral functions:
  - External interrupt circuit input pin (INT09)
  - I²C bus interface ch. 0 clock I/O pin (SCL)
  - 16-bit reload timer ch. 1 input pin (TI1)

15.4 Port F

Port F is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95630H Series Hardware Manual”.

15.4.1 Port F configuration

Port F is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port F data register (PDRF)
- Port F direction register (DDRF)

15.4.2 Block diagrams of port F

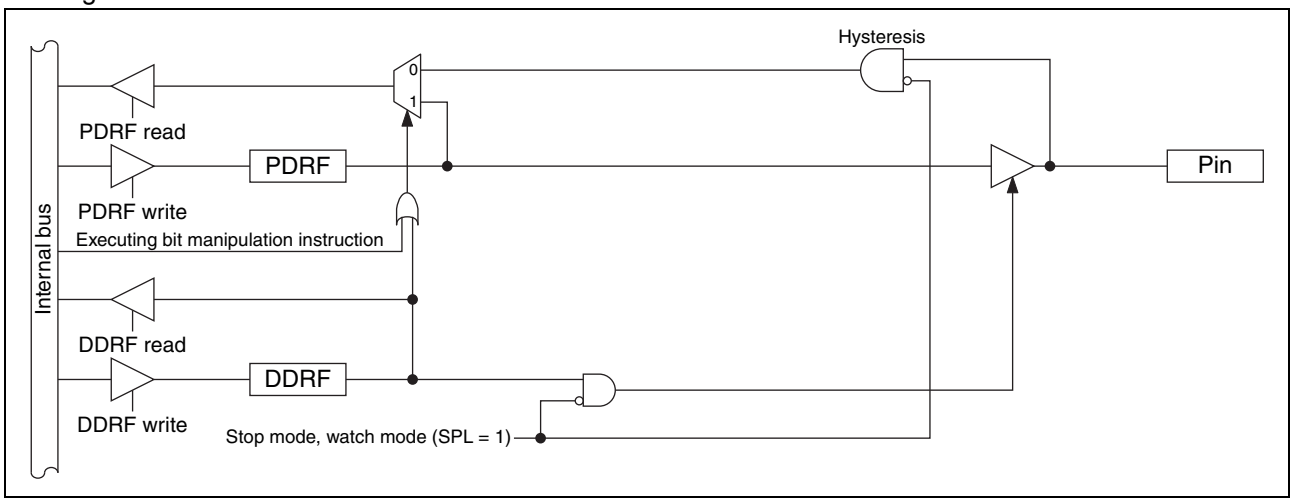
- PF0/X0 pin

  This pin has the following peripheral function:
  - Main clock input oscillation pin (X0)

- PF1/X1 pin

  This pin has the following peripheral function:
  - Main clock I/O oscillation pin (X1)

- Block diagram of PF0/X0 and PF1/X1



- Operation as an input port
  - A pin becomes an input port if the bit in the DDRF register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDRF register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDRF register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRF register, the PDRF register value is returned.

- Operation at reset
  If the CPU is reset, all bits in the DDRF register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRF register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

15.5 Port G

Port G is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95630H Series Hardware Manual”.

15.5.1 Port G configuration

Port G is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port G data register (PDRG)
- Port G direction register (DDRG)
- Port G pull-up register (PULG)

15.5.2 Block diagram of port G

- PG1/X0A/SNI1 pin
  This pin has the following peripheral functions:
  - Subclock input oscillation pin (X0A)
  - Trigger input pin for the position detection function of the MPG waveform sequencer (SNI1)

- PG2/X1A/SNI2 pin
  This pin has the following peripheral functions:
  - Subclock I/O oscillation pin (X1A)
  - Trigger input pin for the position detection function of the MPG waveform sequencer (SNI2)

17. Pin States In Each Mode

Pin name	Normal operation	Sleep mode	Stop mode		Watch mode		On reset
			SPL=0	SPL=1	SPL=0	SPL=1	
PF0/X0	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*4	I/O port*4	- Previous state kept - Input blocked*2*4	- Hi-Z - Input blocked*2*4	- Previous state kept - Input blocked*2*4	- Hi-Z - Input blocked*2*4	- Hi-Z - Input enabled*1 (However, it does not function.)
PF1/X1	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*4	I/O port*4	- Previous state kept - Input blocked*2*4	- Hi-Z - Input blocked*2*4	- Previous state kept - Input blocked*2*4	- Hi-Z - Input blocked*2*4	- Hi-Z - Input enabled*1 (However, it does not function.)
PG1/X0A/ SNI1	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*4/ peripheral function I/O	I/O port*4/ peripheral function I/O	- Previous state kept - Input blocked*2*4	- Hi-Z (However, the setting of the pull-up control is effective.) - Input blocked*2*4	- Previous state kept - Input blocked*2*4	- Hi-Z (However, the setting of the pull-up control is effective.) - Input blocked*2*4	- Hi-Z - Input enabled*1 (However, it does not function.)
PG2/X1A/ SNI2	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*4/ peripheral function I/O	I/O port*4/ peripheral function I/O	- Previous state kept - Input blocked*2*4	- Hi-Z (However, the setting of the pull-up control is effective.) - Input blocked*2*4	- Previous state kept - Input blocked*2*4	- Hi-Z (However, the setting of the pull-up control is effective.) - Input blocked*2*4	- Hi-Z - Input enabled*1 (However, it does not function.)
PF2/$\overline{\text{RST}}$	I/O port	Reset input	Reset input	Reset input	Reset input	Reset input	Reset input*3
P60/INT08/ SDA/DTTI	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*2 (However, an external interrupt can be input when the external interrupt request is enabled.)	- Hi-Z - Input blocked*2 (However, an external interrupt can be input when the external interrupt request is enabled.)	- Previous state kept - Input blocked*2 (However, an external interrupt can be input when the external interrupt request is enabled.)	- Hi-Z - Input blocked*2 (However, an external interrupt can be input when the external interrupt request is enabled.)	- Hi-Z - Input enabled*1 (However, it does not function.)
P61/INT09/ SCL/TI1							
P62/TO10/ PPG00/ OPT0	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*2	- Hi-Z (However, the setting of the pull-up control is effective.) - Input blocked*2	- Previous state kept - Input blocked*2	- Hi-Z (However, the setting of the pull-up control is effective.) - Input blocked*2	- Hi-Z - Input enabled*1 (However, it does not function.)
P63/TO11/ PPG01/ OPT1							

18. Electrical Characteristics

18.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} – 0.3	V_{SS} + 6	V	
Input voltage*1	V_I	V_{SS} – 0.3	V_{SS} + 6	V	*2
Output voltage*1	V_O	V_{SS} – 0.3	V_{SS} + 6	V	*2
Maximum clamp current	I_{CLAMP}	–2	+2	mA	Applicable to specific pins*3
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	—	20	mA	Applicable to specific pins*3
“L” level maximum output current	I_{OL}	—	15	mA	
“L” level average current	I_{OLAV1}	—	4	mA	Other than P62 to P67 Average output current = operating current × operating ratio (1 pin)
	I_{OLAV2}		12		P62 to P67 Average output current = operating current × operating ratio (1 pin)
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	37	mA	Total average output current = operating current × operating ratio (Total number of pins)
“H” level maximum output current	I_{OH}	—	–15	mA	
“H” level average current	I_{OHAV1}	—	–4	mA	Other than P62 to P67 Average output current = operating current × operating ratio (1 pin)
	I_{OHAV2}		–8		P62 to P67 Average output current = operating current × operating ratio (1 pin)
“H” level total maximum output current	ΣI_{OH}	—	–100	mA	
“H” level total average output current	ΣI_{OHAV}	—	–47	mA	Total average output current = operating current × operating ratio (Total number of pins)
Power consumption	P_d	—	320	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	T_{stg}	–55	+150	°C	

*1: These parameters are based on the condition that V_{SS} is 0.0 V.
*2: V_I and V_O must not exceed V_{CC} + 0.3 V. V_I must not exceed the rated voltage. However, if the maximum current to/from an input is limited by means of an external component, the I_{CLAMP} rating is used instead of the V_I rating.
*3: Specific pins: P00 to P07, P10, P11, P13 to P17, P62 to P67, PF0, PF1, PG1, PG2

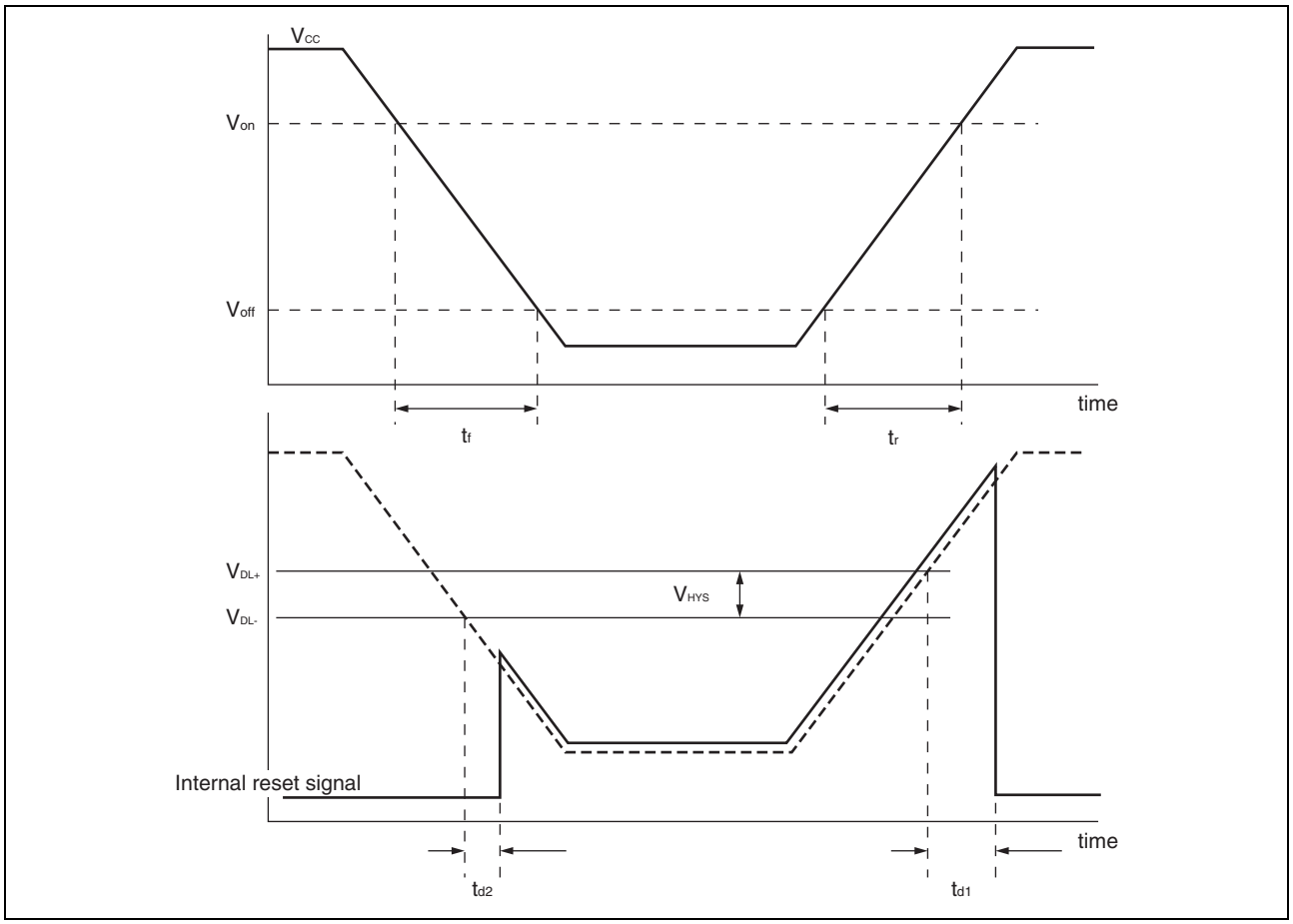
(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = –40 °C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ*1	Max*2		
Power supply current*3	I_V	V_{CC}	Current consumption of the comparator	—	60	160	µA	
	I_{LVD}		Current consumption of the low-voltage detection circuit	—	4	7	µA	
	I_{CRH}		Current consumption of the main CR oscillator	—	240	320	µA	
	I_{CRL}		Current consumption of the sub-CR oscillator oscillating at 100 kHz	—	7	20	µA	
	I_{NSTBY}		Current consumption difference between normal standby mode and deep standby mode T_A = +25°C	—	20	30	µA	

*1: V_{CC} = 5.0 V, T_A = +25°C

*2: V_{CC} = 5.5 V, T_A = +85°C (unless otherwise specified)

*3:
- The power supply current is determined by the external clock. When the low-voltage detection circuit is selected, the power supply current is the sum of adding the current consumption of the low-voltage detection circuit (I_{LVD}) to one of the values from I_{CC} to I_{CCH}. In addition, when both the low-voltage detection option and the CR oscillator are selected, the power supply current is the sum of adding up the current consumption of the low-voltage detection circuit (I_{LVD}), the current consumption of the CR oscillators (I_{CRH}, I_{CRL}) and a specified value. In on-chip debug mode, the CR oscillator (I_{CRH}) and the low-voltage detection circuit are always in operation, and current consumption therefore increases accordingly.
- See “4. AC Characteristics Clock Timing” for F_{CH}, F_{CL}, F_{CRH} and F_{MCRPLL}.
- See “4. AC Characteristics Source Clock/Machine Clock” for F_{MP} and F_{MPL}.
- The power supply current value in standby mode is measured in deep standby mode. The current consumption in normal standby is higher than that in deep standby mode. The power supply current value in normal standby can be found by adding the current consumption difference between normal standby mode and deep standby mode (I_{NSTBY}) to the power supply current value in deep standby mode. For details of normal standby and deep standby mode, refer to “CHAPTER 3 CLOCK CONTROLLER” in “New 8FX MB95630H Series Hardware Manual”.


V_{CC}
V_{on}
V_{off}
time
t_f
t_r
V_{DL+}
V_{DL-}
V_{HYS}
Internal reset signal
time
t_{d2}
t_{d1}

18.4.8 I²C Bus Interface Timing

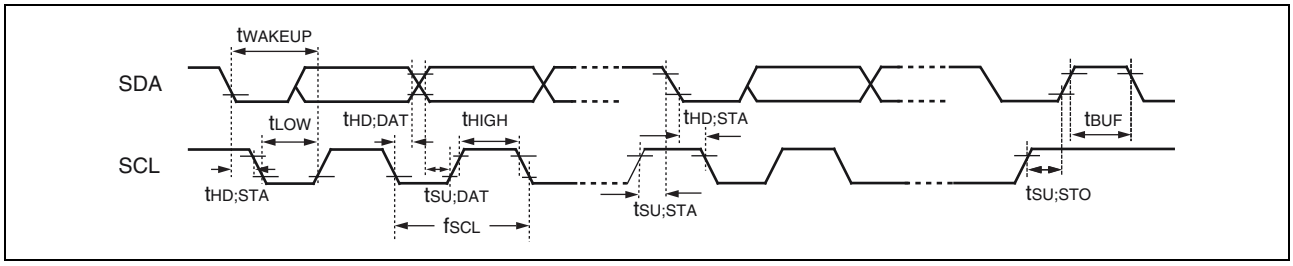
(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value				Unit
				Standard-mode		Fast-mode		
				Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	SCL	R = 1.7 kΩ, C = 50 pF*1	0	100	0	400	kHz
(Repeated) START condition hold time SDA ↓ → SCL ↓	$t_{HD;STA}$	SCL, SDA		4.0	—	0.6	—	µs
SCL clock “L” width	t_{LOW}	SCL		4.7	—	1.3	—	µs
SCL clock “H” width	t_{HIGH}	SCL		4.0	—	0.6	—	µs
(Repeated) START condition setup time SCL ↑ → SDA ↓	$t_{SU;STA}$	SCL, SDA		4.7	—	0.6	—	µs
Data hold time SCL ↓ → SDA ↓↑	$t_{HD;DAT}$	SCL, SDA		0	3.45*2	0	0.9*3	µs
Data setup time SDA ↓↑ → SCL ↑	$t_{SU;DAT}$	SCL, SDA		0.25	—	0.1	—	µs
STOP condition setup time SCL ↑ → SDA ↑	$t_{SU;STO}$	SCL, SDA		4	—	0.6	—	µs
Bus free time between STOP condition and START condition	t_{BUF}	SCL, SDA		4.7	—	1.3	—	µs

*1: R represents the pull-up resistor of the SCL and SDA lines, and C the load capacitor of the SCL and SDA lines.

*2: The maximum $t_{HD;DAT}$ in the Standard-mode is applicable only when the time during which the device is holding the SCL signal at “L” (t_{LOW}) does not extend.

*3: A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, provided that the condition of $t_{SU;DAT}$ ≥ 250 ns is fulfilled.



(Continued)

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value*2		Unit	Remarks
				Min	Max		
START condition detection	$t_{HD;STA}$	SCL, SDA	R = 1.7 kΩ, C = 50 pF*1	2 t_{MCLK} – 20	—	ns	No START condition is detected when 1 t_{MCLK} is used at reception.
STOP condition detection	$t_{SU;STO}$	SCL, SDA		2 t_{MCLK} – 20	—	ns	No STOP condition is detected when 1 t_{MCLK} is used at reception.
RESTART condition detection condition	$t_{SU;STA}$	SCL, SDA		2 t_{MCLK} – 20	—	ns	No RESTART condition is detected when 1 t_{MCLK} is used at reception.
Bus free time	t_{BUF}	SCL, SDA		2 t_{MCLK} – 20	—	ns	At reception
Data hold time	$t_{HD;DAT}$	SCL, SDA		2 t_{MCLK} – 20	—	ns	At slave transmission mode
Data setup time	$t_{SU;DAT}$	SCL, SDA		t_{LOW} – 3 t_{MCLK} – 20	—	ns	At slave transmission mode
Data hold time	$t_{HD;DAT}$	SCL, SDA		0	—	ns	At reception
Data setup time	$t_{SU;DAT}$	SCL, SDA		t_{MCLK} – 20	—	ns	At reception
SDA↓ → SCL↑ (with wakeup function in use)	t_{WAKEUP}	SCL, SDA		Oscillation stabilization wait time +2 t_{MCLK} – 20	—	ns	

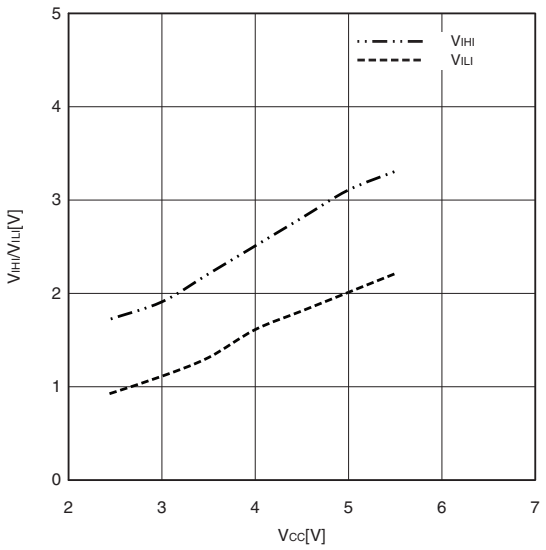
*1: R represents the pull-up resistor of the SCL and SDA lines, and C the load capacitor of the SCL and SDA lines.

*2: • See “Source Clock/Machine Clock” for t_{MCLK}.

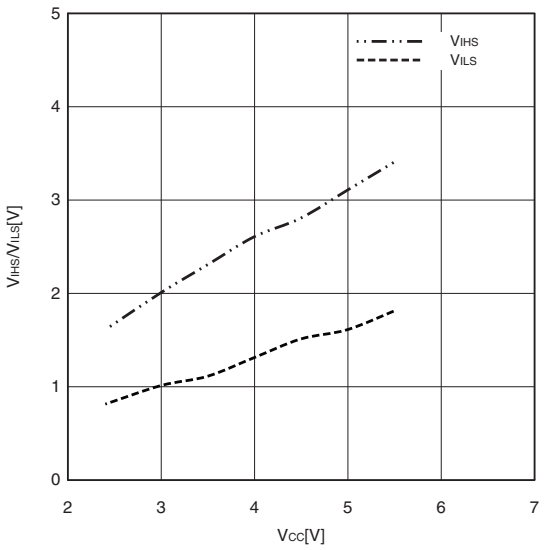
- m represents the CS[4:3] bits in the I²C clock control register ch. 0 (ICCR0).
- n represents the CS[2:0] bits in the I²C clock control register ch. 0 (ICCR0).
- The actual timing of the I²C bus interface is determined by the values of m and n set by the machine clock (t_{MCLK}) and the CS[4:0] bits in the ICCR0 register.
- Standard-mode:
  m and n can be set to values in the following range: 0.9 MHz < t_{MCLK} (machine clock) < 16.25 MHz.
  The usable frequencies of the machine clock are determined by the settings of m and n as shown below.
  (m, n) = (1, 8) : 0.9 MHz < t_{MCLK} ≤ 1 MHz
  (m, n) = (1, 22), (5, 4), (6, 4), (7, 4), (8, 4) : 0.9 MHz < t_{MCLK} ≤ 2 MHz
  (m, n) = (1, 38), (5, 8), (6, 8), (7, 8), (8, 8) : 0.9 MHz < t_{MCLK} ≤ 4 MHz
  (m, n) = (1, 98), (5, 22), (6, 22), (7, 22) : 0.9 MHz < t_{MCLK} ≤ 10 MHz
  (m, n) = (8, 22) : 0.9 MHz < t_{MCLK} ≤ 16.25 MHz
- Fast-mode:
  m and n can be set to values in the following range: 3.3 MHz < t_{MCLK} (machine clock) < 16.25 MHz.
  The usable frequencies of the machine clock are determined by the settings of m and n as shown below.
  (m, n) = (1, 8) : 3.3 MHz < t_{MCLK} ≤ 4 MHz
  (m, n) = (1, 22), (5, 4) : 3.3 MHz < t_{MCLK} ≤ 8 MHz
  (m, n) = (1, 38), (6, 4), (7, 4), (8, 4) : 3.3 MHz < t_{MCLK} ≤ 10 MHz
  (m, n) = (5, 8) : 3.3 MHz < t_{MCLK} ≤ 16.25 MHz

- Input voltage characteristics

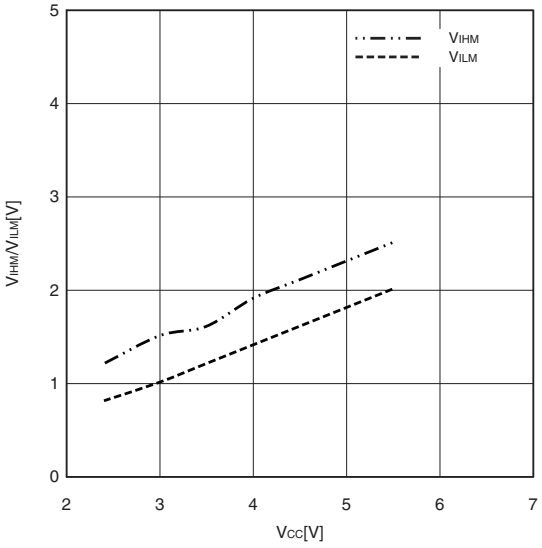
V_{IHI} – V_{CC} and V_{ILI} – V_{CC}
T_A = +25°C



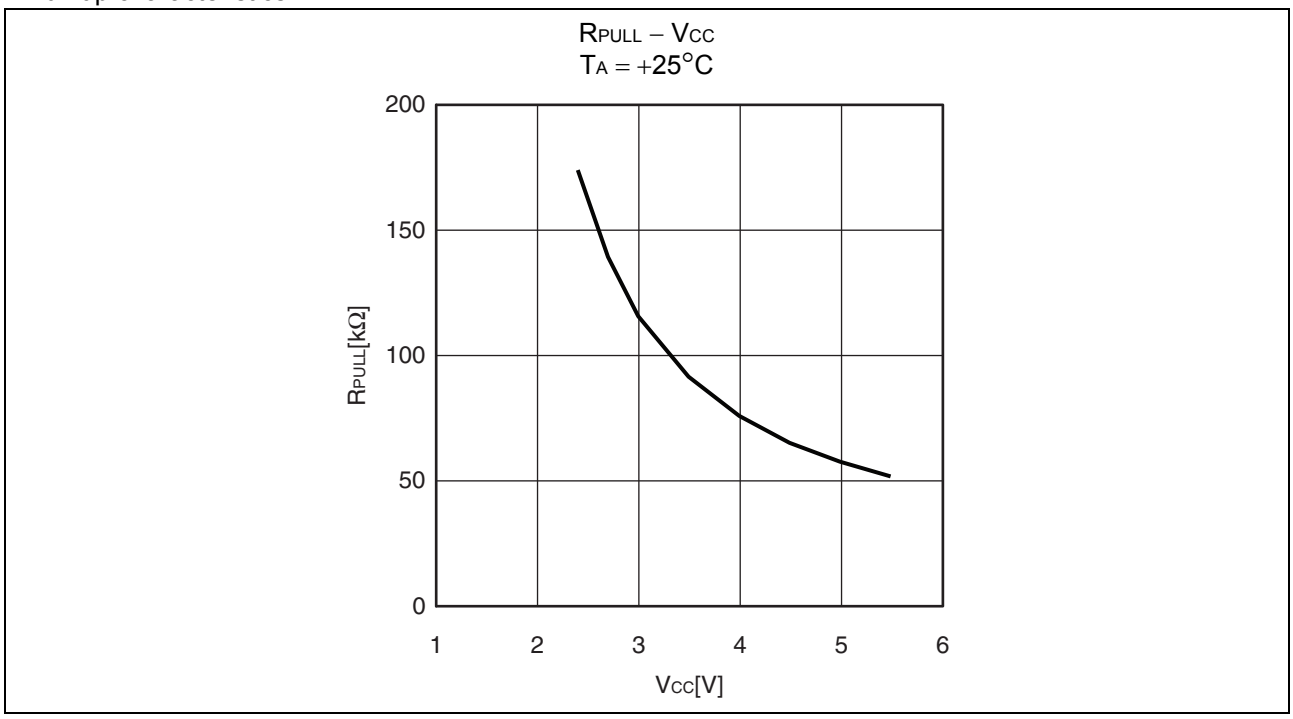
V_{IHS} – V_{CC} and V_{ILS} – V_{CC}
T_A = +25°C



V_{IHM} – V_{CC} and V_{ILM} – V_{CC}
T_A = +25°C

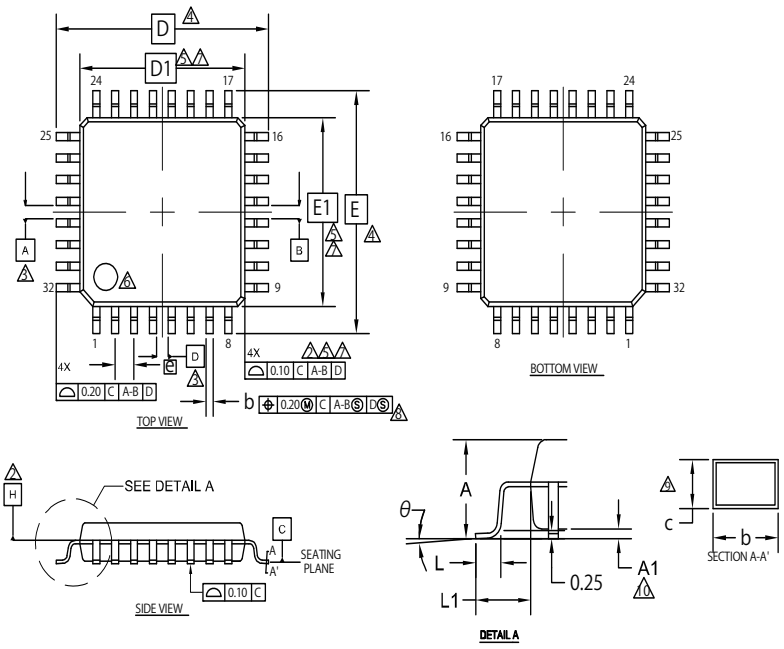


- Pull-up characteristics



22. Package Dimension

Package Type	Package Code
LQFP 32	LQB032



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
b	0.32	0.35	0.43
c	0.13	—	0.18
D		9.00 BSC	
D1		7.00 BSC	
e		0.80 BSC	
E		9.00 BSC	
E1		7.00 BSC	
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13879 **

PACKAGE OUTLINE, 32 LEAD LQFP
7.0X7.0X1.6 MM LQB032 REV*.*

Document History Page

Document Title: MB95630H Series, New 8FX 8-bit Microcontrollers Document Number: 002-04627				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	-	AKIH	06/07/2013	Migrated to Cypress and assigned document number 002-04627. No change to document contents or format.
*A	5193921	AKIH	03/29/2016	Updated to Cypress template Added “MB95F636KPMC-G-UNE2” in “Ordering Information”
*B	5443796	HTER	02/06/2017	Changed three package codes as the following from “FPT-32P-M30” to “LQB032” from “LCC-32P-M19” to “WNP032” from “DIP-32P-M06” to “PDS032” in chapter: 1.Product Line-up (Page 5) 2.Packages And Corresponding Products (Page 5) 4.Pin Assignment (Page 6, 7) 5.Pin Functions (Page 11) 21.Ordering Information (Page 97) 28.Package Dimensions (Page 98 to 100). Added three Part numbers - MB95F632KPMC-G-UNE2 - MB95F633KPMC-G-UNE2 - MB95F634KPMC-G-UNE2 in chapter 21.Ordering Information (Page 97). Deleted four Part numbers - MB95F632KPMC-G-SNE2 - MB95F633KPMC-G-SNE2 - MB95F634KPMC-G-SNE2 - MB95F636KPMC-G-SNE2 in chapter 21.Ordering Information (Page 97).
*C	5746267	AESATP12	05/23/2017	Updated logo and copyright.
*D	5895915	HUAL	09/27/2017	Added Part number “MB95F633HPMC-G-UNERE2” and Packing information Modified from “MB95F634HPMC-G-SNE2” to “MB95F634HPMC-G-UNE2” in 21.Ordering Information (Page 97)