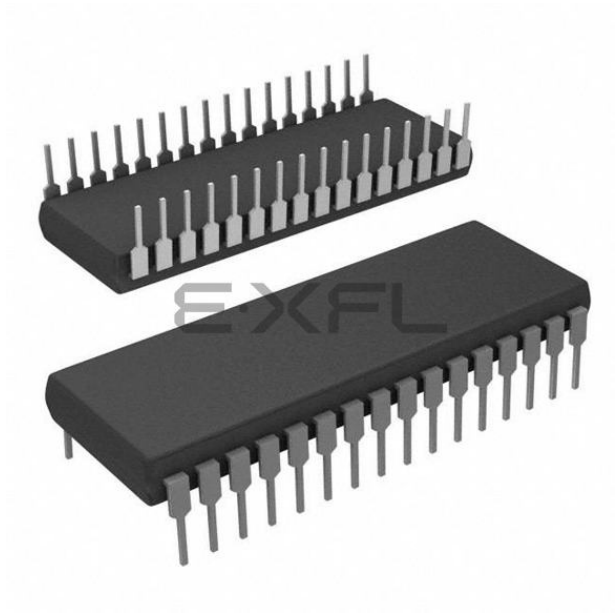
Infineon Technologies - MB95F636KP-G-SH-SNE2 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SIO, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	29
Program Memory Size	36KB (36K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	32-SDIP (0.400", 10.16mm)
Supplier Device Package	32-SDIP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f636kp-g-sh-sne2

MB95630H Series

New 8FX 8-bit Microcontrollers

The MB95630H Series is a series of general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers of this series contain a variety of peripheral functions.

Features

- F²MC-8FX CPU core
  - Instruction set optimized for controllers
    - Multiplication and division instructions
    - 16-bit arithmetic operations
    - Bit test branch instructions
    - Bit manipulation instructions, etc.
- Clock
  - Selectable main clock source
    - Main oscillation clock (up to 16.25 MHz, maximum machine clock frequency: 8.125 MHz)
    - External clock (up to 32.5 MHz, maximum machine clock frequency: 16.25 MHz)
    - Main CR clock (4 MHz ±2%)
    - Main CR PLL clock
      - The main CR PLL clock frequency becomes 8 MHz ±2% when the PLL multiplication rate is 2.
      - The main CR PLL clock frequency becomes 10 MHz ±2% when the PLL multiplication rate is 2.5.
      - The main CR PLL clock frequency becomes 12 MHz ±2% when the PLL multiplication rate is 3.
      - The main CR PLL clock frequency becomes 16 MHz ±2% when the PLL multiplication rate is 4.
  - Selectable subclock source
    - Suboscillation clock (32.768 kHz)
    - External clock (32.768 kHz)
    - Sub-CR clock (Typ: 100 kHz, Min: 50 kHz, Max: 150 kHz)
- Timer
  - 8/16-bit composite timer × 2 channels
  - 8/16-bit PPG × 3 channels
  - 16-bit PPG timer × 1 channel (can work independently or together with the multi-pulse generator)
  - 16-bit reload timer × 1 channel (can work independently or together with the multi-pulse generator)
  - Time-base timer × 1 channel
  - Watch prescaler × 1 channel
- UART/SIO × 1 channel
  - Full duplex double buffer
  - Capable of clock asynchronous (UART) serial data transfer and clock synchronous (SIO) serial data transfer
- I²C bus interface × 1 channel
  - Built-in wake-up function
- Multi-pulse generator (MPG) (for DC motor control) × 1 channel
  - 16-bit reload timer × 1 channel
  - 16-bit PPG timer × 1 channel
  - Waveform sequencer (including a 16-bit timer equipped with a buffer and a compare clear function)
- LIN-UART
  - Full duplex double buffer
  - Capable of clock asynchronous serial data transfer and clock synchronous serial data transfer
- External interrupt × 10 channels
  - Interrupt by edge detection (rising edge, falling edge, and both edges can be selected)
  - Can be used to wake up the device from different low power consumption (standby) modes
- 8/10-bit A/D converter × 8 channels
  - 8-bit or 10-bit resolution can be selected.
- Low power consumption (standby) modes
  - There are four standby modes as follows:
    - Stop mode
    - Sleep mode
    - Watch mode
    - Time-base timer mode
  - In standby mode, two further options can be selected: normal standby mode and deep standby mode.
- I/O port
  - MB95F632H/F633H/F634H/F636H (number of I/O ports: 28)
    - General-purpose I/O ports (CMOS I/O): 25
    - General-purpose I/O ports (N-ch open drain): 3
  - MB95F632K/F633K/F634K/F636K (number of I/O ports: 29)
    - General-purpose I/O ports (CMOS I/O): 25
    - General-purpose I/O ports (N-ch open drain): 4
- On-chip debug
  - 1-wire serial control
  - Serial writing supported (asynchronous mode)
- Hardware/software watchdog timer
  - Built-in hardware watchdog timer
  - Built-in software watchdog timer
- Power-on reset
  - A power-on reset is generated when the power is switched on.
- Low-voltage detection reset circuit (only available on MB95F632K/F633K/F634K/F636K)
  - Built-in low-voltage detection function (The combination of detection voltage and release voltage can be selected from four options.)
- Comparator
- Clock supervisor counter
  - Built-in clock supervisor counter
- Dual operation Flash memory
  - The program/erase operation and the read operation can be executed in different banks (upper bank/lower bank) simultaneously.
- Flash memory security function
  - Protects the content of the Flash memory.

<table>
<tr><th>Part number
Parameter</th><th>MB95F632H</th><th>MB95F633H</th><th>MB95F634H</th><th>MB95F636H</th><th>MB95F632K</th><th>MB95F633K</th><th>MB95F634K</th><th>MB95F636K</th></tr>
<tr><td>Flash memory</td><td colspan="8">• It supports automatic programming (Embedded Algorithm), and program/erase/erase-suspend/erase-resume commands.
• It has a flag indicating the completion of the operation of Embedded Algorithm.
• Flash security feature for protecting the content of the Flash memory
<table><tr><td>Number of program/erase cycles</td><td>1000</td><td>10000</td><td>100000</td></tr><tr><td>Data retention time</td><td>20 years</td><td>10 years</td><td>5 years</td></tr></table></td></tr>
<tr><td>Standby mode</td><td colspan="8">There are four standby modes as follows:
• Stop mode
• Sleep mode
• Watch mode
• Time-base timer mode
In standby mode, two further options can be selected: normal standby mode and deep standby mode.</td></tr>
<tr><td>Package</td><td colspan="8">LQB032
PDS032
WNP032</td></tr>
</table>

2. Packages And Corresponding Products

Part number / Package	MB95F632H	MB95F633H	MB95F634H	MB95F636H	MB95F632K	MB95F633K	MB95F634K	MB95F636K
LQB032	O	O	O	O	O	O	O	O
PDS032	O	O	O	O	O	O	O	O
WNP032	O	O	O	O	O	O	O	O

O: Available

3. Differences Among Products And Notes On Product Selection

- Current consumption
  When using the on-chip debug function, take account of the current consumption of Flash memory program/erase.
  For details of current consumption, see “Electrical Characteristics”.

- Package
  For details of information on each package, see “Packages And Corresponding Products” and “Package Dimension”.

- Operating voltage
  The operating voltage varies, depending on whether the on-chip debug function is used or not.
  For details of operating voltage, see “Electrical Characteristics”.

- On-chip debug function

7.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

(1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

(2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

(3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

(4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

(5) Smoke, Flame

CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

8. Notes On Device Handling

- Preventing latch-ups
  When using the device, ensure that the voltage applied does not exceed the maximum voltage rating.
  In a CMOS IC, if a voltage higher than V_{CC} or a voltage lower than V_{SS} is applied to an input/output pin that is neither a medium-withstand voltage pin nor a high-withstand voltage pin, or if a voltage out of the rating range of power supply voltage mentioned in “18.1 Absolute Maximum Ratings” of “Electrical Characteristics” is applied to the V_{CC} pin or the V_{SS} pin, a latch-up may occur.
  When a latch-up occurs, power supply current increases significantly, which may cause a component to be thermally destroyed.

- Stabilizing supply voltage
  Supply voltage must be stabilized.
  A malfunction may occur when power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the V_{CC} power supply voltage.
  As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in V_{CC} ripple (p-p value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard V_{CC} value, and the transient fluctuation rate does not exceed 0.1 V/ms at a momentary fluctuation such as switching the power supply.

- Notes on using the external clock
  When an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from sub-clock mode or stop mode.

9. Pin Connection

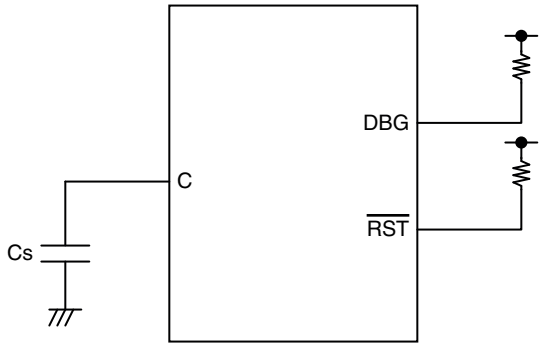
- Treatment of unused pins
  If an unused input pin is left unconnected, a component may be permanently damaged due to malfunctions or latch-ups. Always pull up or pull down an unused input pin through a resistor of at least 2 kΩ. Set an unused input/output pin to the output state and leave it unconnected, or set it to the input state and treat it the same as an unused input pin. If there is an unused output pin, leave it unconnected.

- Power supply pins
  To reduce unnecessary electro-magnetic emission, prevent malfunctions of strobe signals due to an increase in the ground level, and conform to the total output current standard, always connect the V_{CC} pin and the V_{SS} pin to the power supply and ground outside the device. In addition, connect the current supply source to the V_{CC} pin and the V_{SS} pin with low impedance.
  It is also advisable to connect a ceramic capacitor of approximately 0.1 µF as a bypass capacitor between the V_{CC} pin and the V_{SS} pin at a location close to this device.

- DBG pin
  Connect the DBG pin to an external pull-up resistor of 2 kΩ or above.
  After power-on, ensure that the DBG pin does not stay at “L” level until the reset output is released.
  The DBG pin becomes a communication pin in debug mode. Since the actual pull-up resistance depends on the tool used and the interconnection length, refer to the tool document when selecting a pull-up resistor.

- $\overline{RST}$ pin
  Connect the $\overline{RST}$ pin to an external pull-up resistor of 2 kΩ or above.
  To prevent the device from unintentionally entering the reset mode due to noise, minimize the interconnection length between a pull-up resistor and the $\overline{RST}$ pin and that between a pull-up resistor and the V_{CC} pin when designing the layout of the printed circuit board.
  The PF2/$\overline{RST}$ pin functions as the reset input/output pin after power-on. In addition, the reset output of the PF2/$\overline{RST}$ pin can be enabled by the RSTOE bit in the SYSC register, and the reset input function and the general-purpose I/O function can be selected by the RSTEN bit in the SYSC register.
- C pin
  Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The decoupling capacitor for the V_{CC} pin must have a capacitance equal to or larger than the capacitance of C_S. For the connection to a decoupling capacitor C_S, see the diagram below. To prevent the device from unintentionally entering a mode to which the device is not set to transit due to noise, minimize the distance between the C pin and C_S and the distance between C_S and the V_{SS} pin when designing the layout of a printed circuit board.

- DBG/$\overline{RST}$/C pins connection diagram



- Note on serial communication
  In serial communication, reception of wrong data may occur due to noise or other causes. Therefore, design a printed

13. Areas For Specific Applications

The general-purpose register area and vector table area are used for the specific applications.

- General-purpose register area (Addresses: 0x0100 to 0x01FF*1)
  - This area contains the auxiliary registers used for 8-bit arithmetic operations, transfer, etc.
  - As this area forms part of the RAM area, it can also be used as conventional RAM.
  - When the area is used as general-purpose registers, general-purpose register addressing enables high-speed access with short instructions.

- Non-volatile register data area (Addresses: 0xFFBB to 0xFFBF)
  - The area from 0xFFBB to 0xFFBF is used to store data of the non-volatile register. For details, refer to “CHAPTER 26 NON-VOLATILE REGISTER (NVR) INTERFACE” in “New 8FX MB95630H Series Hardware Manual”.

- Vector table area (Addresses: 0xFFC0 to 0xFFFF)
  - This area is used as the vector table for vector call instructions (CALLV), interrupts, and resets.
  - The top of the Flash memory area is allocated to the vector table area. The start address of a service routine is set to an address in the vector table in the form of data.

  “Interrupt Source Table” lists the vector table addresses corresponding to vector call instructions, interrupts, and resets.
  For details, refer to “CHAPTER 4 RESET”, “CHAPTER 5 INTERRUPTS” and “A.2 Special Instruction ■ Special Instruction ● CALLV #vct” in “New 8FX MB95630H Series Hardware Manual”.

- Direct bank pointer and access area

Direct bank pointer (DP[2:0])	Operand-specified dir	Access area
0bXXX (It does not affect mapping.)	0x0000 to 0x007F	0x0000 to 0x007F
0b000 (Initial value)	0x0090 to 0x00FF	0x0090 to 0x00FF
0b001	0x0080 to 0x00FF	0x0100 to 0x017F
0b010		0x0180 to 0x01FF*1
0b011		0x0200 to 0x027F
0b100		0x0280 to 0x02FF*2
0b101		0x0300 to 0x037F
0b110		0x0380 to 0x03FF
0b111		0x0400 to 0x047F

*1: Due to the memory size limit, the available access area is up to “0x018F” in MB95F632H/F632K.
*2: Due to the memory size limit, the available access area is up to “0x028F” in MB95F633H/F633K.

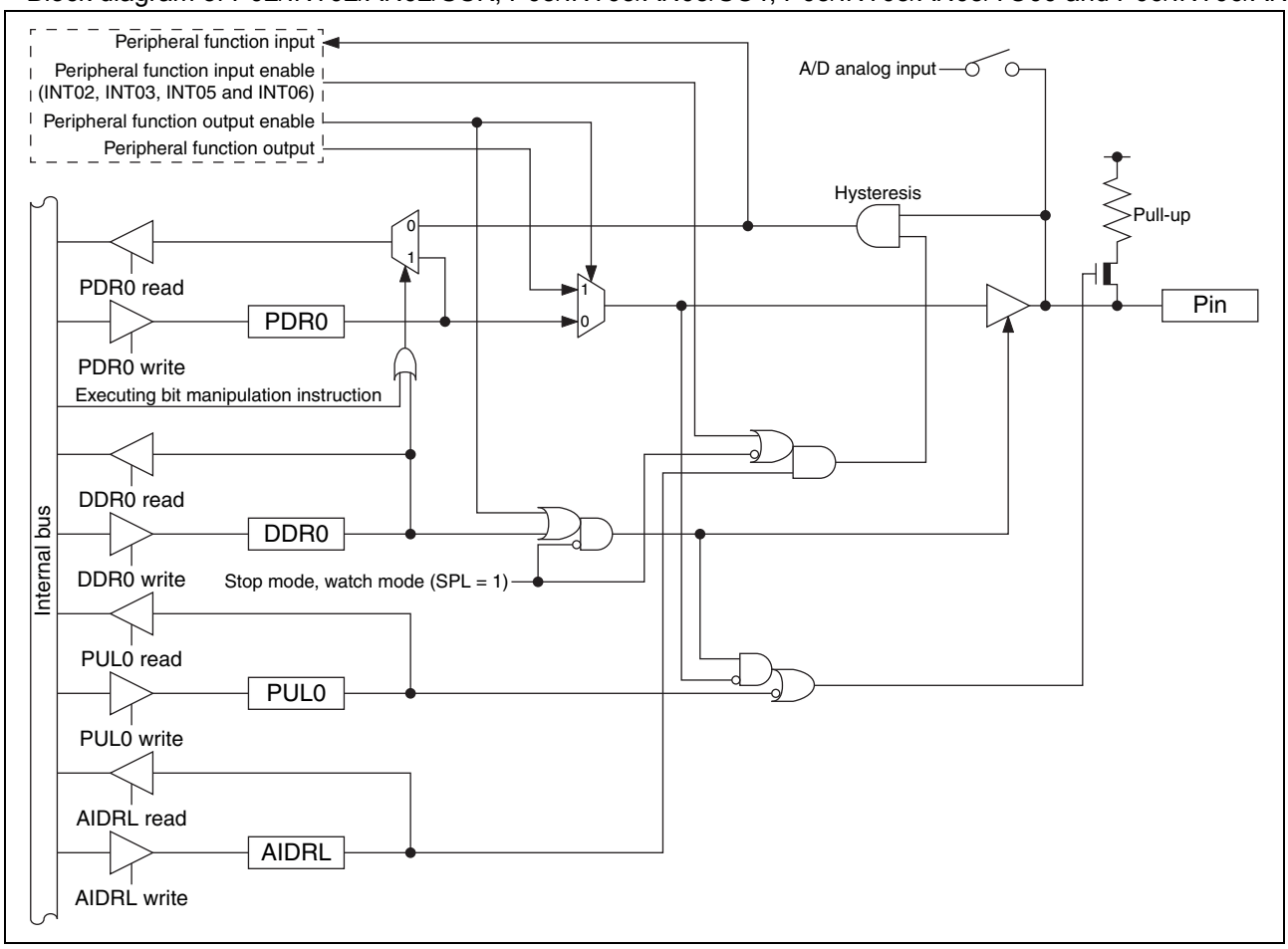
- P02/INT02/AN02/SCK pin
  This pin has the following peripheral functions:
  - External interrupt circuit input pin (INT02)
  - 8/10-bit A/D converter analog input pin (AN02)
  - LIN-UART clock I/O pin (SCK)

- P03/INT03/AN03/SOT pin
  This pin has the following peripheral functions:
  - External interrupt circuit input pin (INT03)
  - 8/10-bit A/D converter analog input pin (AN03)
  - LIN-UART data output pin (SOT)

- P05/INT05/AN05/TO00 pin
  This pin has the following peripheral functions:
  - External interrupt circuit input pin (INT05)
  - 8/10-bit A/D converter analog input pin (AN05)
  - 8/16-bit composite timer ch. 0 output pin (TO00)

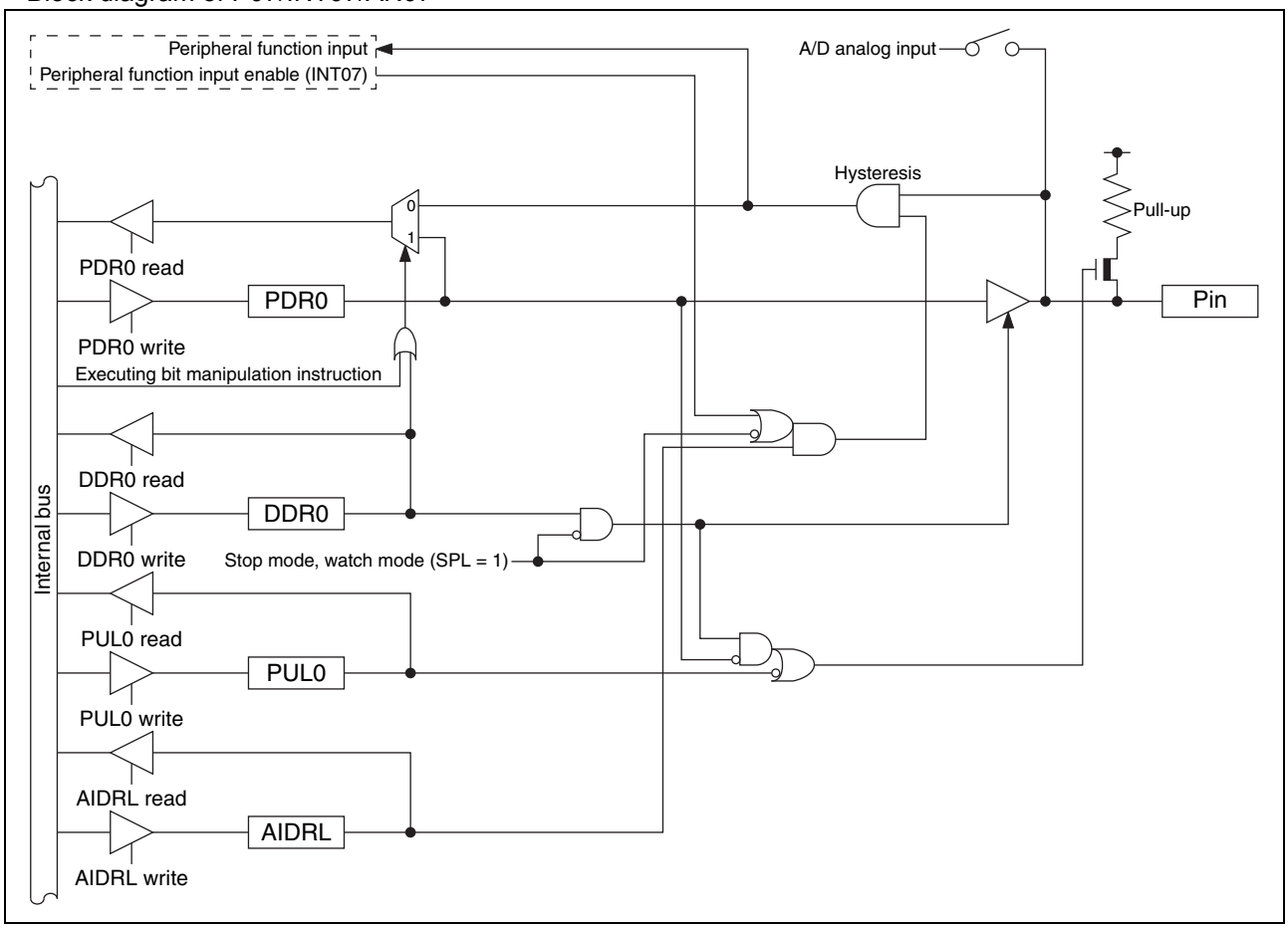
- P06/INT06/AN06/TO01 pin
  This pin has the following peripheral functions:
  - External interrupt circuit input pin (INT06)
  - 8/10-bit A/D converter analog input pin (AN06)
  - 8/16-bit composite timer ch. 0 output pin (TO01)

- Block diagram of P02/INT02/AN02/SCK, P03/INT03/AN03/SOT, P05/INT05/AN05/TO00 and P06/INT06/AN06/TO01

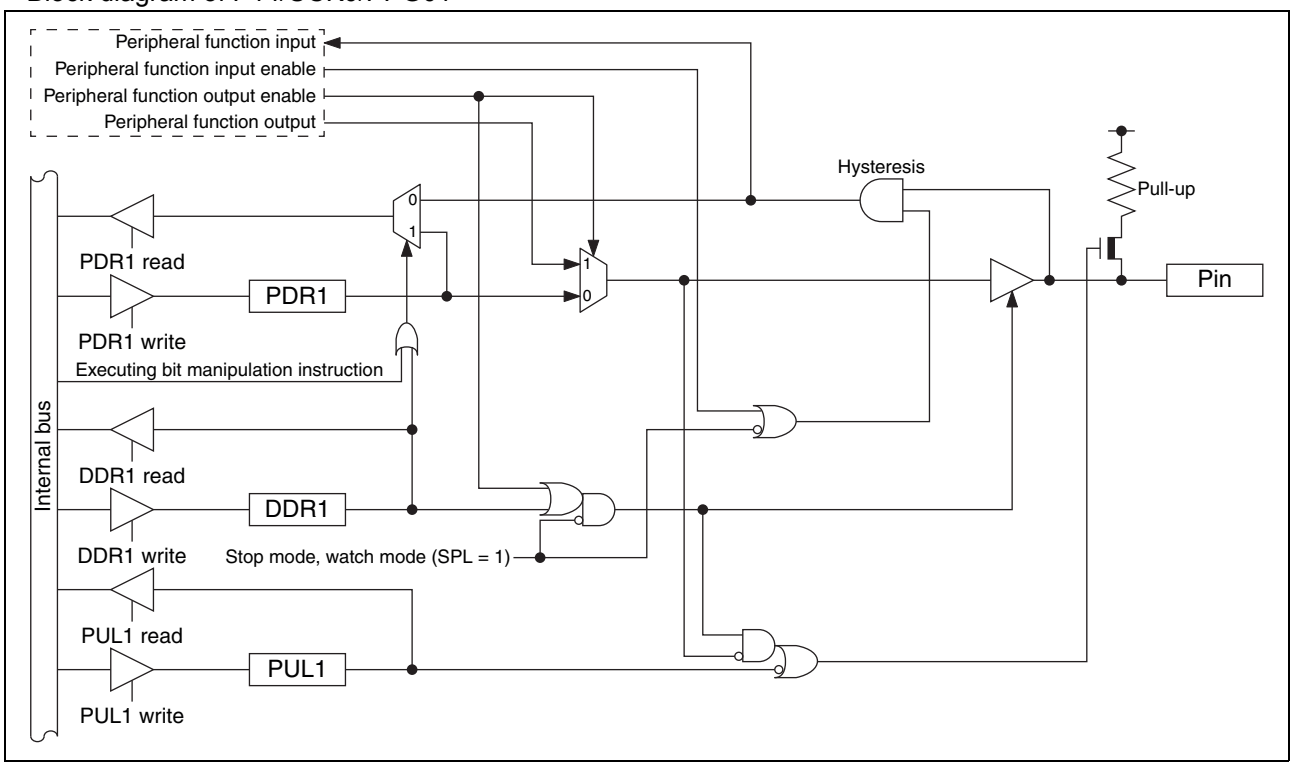


- P07/INT07/AN07 pin
  This pin has the following peripheral functions:
  - External interrupt circuit input pin (INT07)
  - 8/10-bit A/D converter analog input pin (AN07)

- Block diagram of P07/INT07/AN07



- Block diagram of P14/UCK0/PPG01



15.4 Port F

Port F is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95630H Series Hardware Manual”.

15.4.1 Port F configuration

Port F is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port F data register (PDRF)
- Port F direction register (DDRF)

15.4.2 Block diagrams of port F

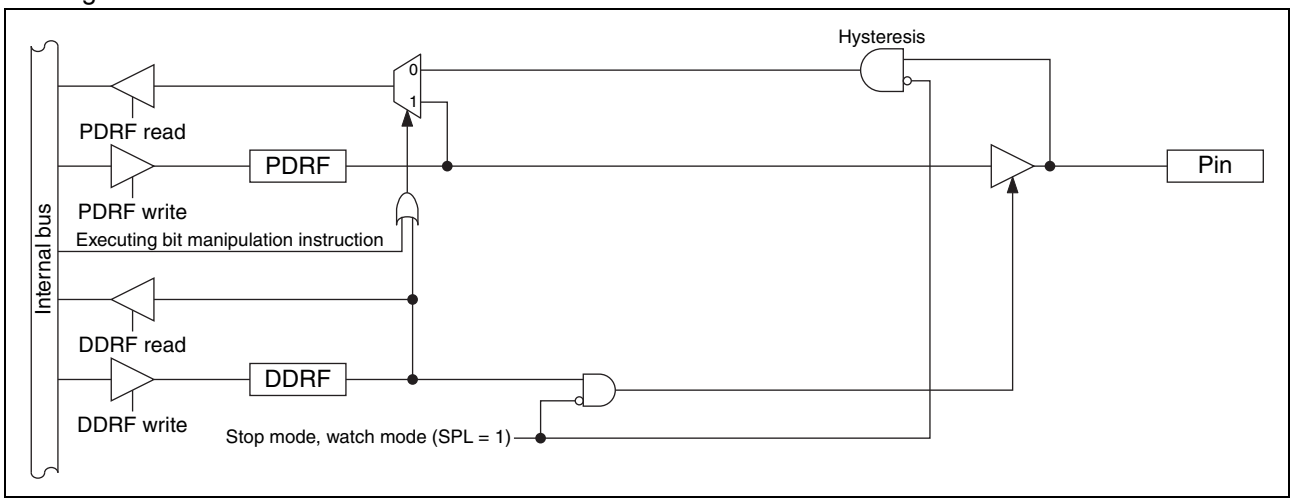
- PF0/X0 pin

  This pin has the following peripheral function:
  - Main clock input oscillation pin (X0)

- PF1/X1 pin

  This pin has the following peripheral function:
  - Main clock I/O oscillation pin (X1)

- Block diagram of PF0/X0 and PF1/X1



- Operation as an input port
  - A pin becomes an input port if the bit in the DDRF register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDRF register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDRF register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRF register, the PDRF register value is returned.

- Operation at reset
  If the CPU is reset, all bits in the DDRF register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRF register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

15.5 Port G

Port G is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95630H Series Hardware Manual”.

15.5.1 Port G configuration

Port G is made up of the following elements.

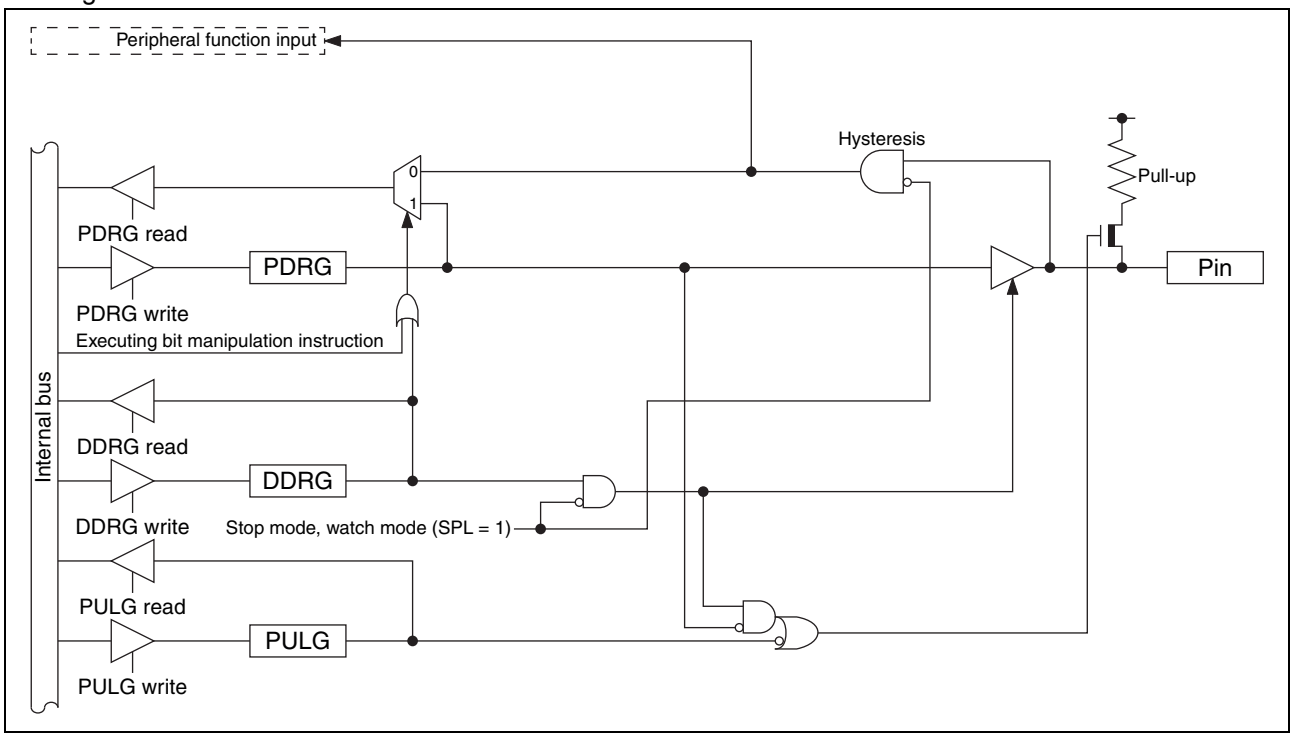
- General-purpose I/O pins/peripheral function I/O pins
- Port G data register (PDRG)
- Port G direction register (DDRG)
- Port G pull-up register (PULG)

15.5.2 Block diagram of port G

- PG1/X0A/SNI1 pin
  This pin has the following peripheral functions:
  - Subclock input oscillation pin (X0A)
  - Trigger input pin for the position detection function of the MPG waveform sequencer (SNI1)

- PG2/X1A/SNI2 pin
  This pin has the following peripheral functions:
  - Subclock I/O oscillation pin (X1A)
  - Trigger input pin for the position detection function of the MPG waveform sequencer (SNI2)

- Block diagram of PG1/X0A/SNI1 and PG2/X1A/SNI2



15.5.3 Port G registers

- Port G register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDRG	0	Pin state is “L” level.	PDRG value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDRG value is “1”.	As output port, outputs “H” level.
DDRG	0	Port input enabled		
	1	Port output enabled		
PULG	0	Pull-up disabled		
	1	Pull-up enabled		

- Correspondence between registers and pins for port G

	Correspondence between related register bits and pins							
Pin name	**-**	**-**	**-**	**-**	**-**	**PG2**	**PG1**	**-**
PDRG	-	-	-	-	-	bit2	bit1	-
DDRG								
PULG								

15.5.4 Port G operations

- Operation as an output port
  - A pin becomes an output port if the bit in the DDRG register corresponding to that pin is set to “1”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - When a pin is used as an output port, it outputs the value of the PDRG register to external pins.

  - If data is written to the PDRG register, the value is stored in the output latch and is output to the pin set as an output port as it is.
  - Reading the PDRG register returns the PDRG register value.

- Operation as an input port
  - A pin becomes an input port if the bit in the DDRG register corresponding to that pin is set to “0”.
  - For a pin shared with other peripheral functions, disable the output of such peripheral functions.
  - If data is written to the PDRG register, the value is stored in the output latch but is not output to the pin set as an input port.
  - Reading the PDRG register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRG register, the PDRG register value is returned.

- Operation as a peripheral function input pin
  - To set a pin as an input port, set the bit in the DDRG register corresponding to the input pin of a peripheral function to “0”.
  - Reading the PDRG register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDRG register, the PDRG register value is returned.

- Operation at reset
  If the CPU is reset, all bits in the DDRG register are initialized to “0” and port input is enabled.

- Operation in stop mode and watch mode
  - If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRG register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
  - If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

- Operation of the pull-up register
  Setting the bit in the PULG register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PULG register.

17. Pin States In Each Mode

Pin name	Normal operation	Sleep mode	Stop mode		Watch mode		On reset
			SPL=0	SPL=1	SPL=0	SPL=1	
PF0/X0	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*4	I/O port*4	- Previous state kept - Input blocked*2*4	- Hi-Z - Input blocked*2*4	- Previous state kept - Input blocked*2*4	- Hi-Z - Input blocked*2*4	- Hi-Z - Input enabled*1 (However, it does not function.)
PF1/X1	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*4	I/O port*4	- Previous state kept - Input blocked*2*4	- Hi-Z - Input blocked*2*4	- Previous state kept - Input blocked*2*4	- Hi-Z - Input blocked*2*4	- Hi-Z - Input enabled*1 (However, it does not function.)
PG1/X0A/ SNI1	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*4/ peripheral function I/O	I/O port*4/ peripheral function I/O	- Previous state kept - Input blocked*2*4	- Hi-Z (However, the setting of the pull-up control is effective.) - Input blocked*2*4	- Previous state kept - Input blocked*2*4	- Hi-Z (However, the setting of the pull-up control is effective.) - Input blocked*2*4	- Hi-Z - Input enabled*1 (However, it does not function.)
PG2/X1A/ SNI2	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*4/ peripheral function I/O	I/O port*4/ peripheral function I/O	- Previous state kept - Input blocked*2*4	- Hi-Z (However, the setting of the pull-up control is effective.) - Input blocked*2*4	- Previous state kept - Input blocked*2*4	- Hi-Z (However, the setting of the pull-up control is effective.) - Input blocked*2*4	- Hi-Z - Input enabled*1 (However, it does not function.)
PF2/$\overline{\text{RST}}$	I/O port	Reset input	Reset input	Reset input	Reset input	Reset input	Reset input*3
P60/INT08/ SDA/DTTI	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*2 (However, an external interrupt can be input when the external interrupt request is enabled.)	- Hi-Z - Input blocked*2 (However, an external interrupt can be input when the external interrupt request is enabled.)	- Previous state kept - Input blocked*2 (However, an external interrupt can be input when the external interrupt request is enabled.)	- Hi-Z - Input blocked*2 (However, an external interrupt can be input when the external interrupt request is enabled.)	- Hi-Z - Input enabled*1 (However, it does not function.)
P61/INT09/ SCL/TI1							
P62/TO10/ PPG00/ OPT0	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*2	- Hi-Z (However, the setting of the pull-up control is effective.) - Input blocked*2	- Previous state kept - Input blocked*2	- Hi-Z (However, the setting of the pull-up control is effective.) - Input blocked*2	- Hi-Z - Input enabled*1 (However, it does not function.)
P63/TO11/ PPG01/ OPT1							

Pin name	Normal operation	Sleep mode	Stop mode		Watch mode		On reset
			SPL=0	SPL=1	SPL=0	SPL=1	
P64/EC1/ PPG10/ OPT2	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*2 (However, an external interrupt can be input when the external interrupt request is enabled.)	- Hi-Z (However, the setting of the pull-up control is effective.) - Input blocked*2 (However, an external interrupt can be input when the external interrupt request is enabled.)	- Previous state kept - Input blocked*2 (However, an external interrupt can be input when the external interrupt request is enabled.)	- Hi-Z (However, the setting of the pull-up control is effective.) - Input blocked*2 (However, an external interrupt can be input when the external interrupt request is enabled.)	- Hi-Z - Input enabled*1 (However, it does not function.)
P65/PPG11/ OPT3 P66/PPG1/ PPG20/ OPT4	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*2	- Hi-Z (However, the setting of the pull-up control is effective.) - Input blocked*2	- Previous state kept - Input blocked*2	- Hi-Z (However, the setting of the pull-up control is effective.) - Input blocked*2	- Hi-Z - Input enabled*1 (However, it does not function.)
P67/TRG1/ PPG21/ OPT5	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*2 (However, an external interrupt can be input when the external interrupt request is enabled.)	- Hi-Z (However, the setting of the pull-up control is effective.) - Input blocked*2 (However, an external interrupt can be input when the external interrupt request is enabled.)	- Previous state kept - Input blocked*2 (However, an external interrupt can be input when the external interrupt request is enabled.)	- Hi-Z (However, the setting of the pull-up control is effective.) - Input blocked*2 (However, an external interrupt can be input when the external interrupt request is enabled.)	- Hi-Z - Input enabled*1 (However, it does not function.)
P10/PPG10/ CMP0_O P11/PPG11	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*2	- Hi-Z (However, the setting of the pull-up control is effective.) - Input blocked*2	- Previous state kept - Input blocked*2	- Hi-Z (However, the setting of the pull-up control is effective.) - Input blocked*2	- Hi-Z - Input enabled*1 (However, it does not function.)
P12/DBG/ EC0	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*2	- Hi-Z - Input blocked*2	- Previous state kept - Input blocked*2	- Hi-Z - Input blocked*2	- Hi-Z - Input enabled*1 (However, it does not function.)
P13/PPG00	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	- Previous state kept - Input blocked*2	- Hi-Z (However, the setting of the pull-up control is effective.) - Input blocked*2	- Previous state kept - Input blocked*2	- Hi-Z (However, the setting of the pull-up control is effective.) - Input blocked*2	- Hi-Z - Input enabled*1 (However, it does not function.)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Machine clock frequency	F_{MP}	—	0.031	—	16.25	MHz	When the main oscillation clock is used
			0.25	—	16	MHz	When the main CR clock is used
	F_{MPL}		1.024	—	16.384	kHz	When the suboscillation clock is used
			3.125	—	50	kHz	When the sub-CR clock is used F_{CRL} = 100 kHz

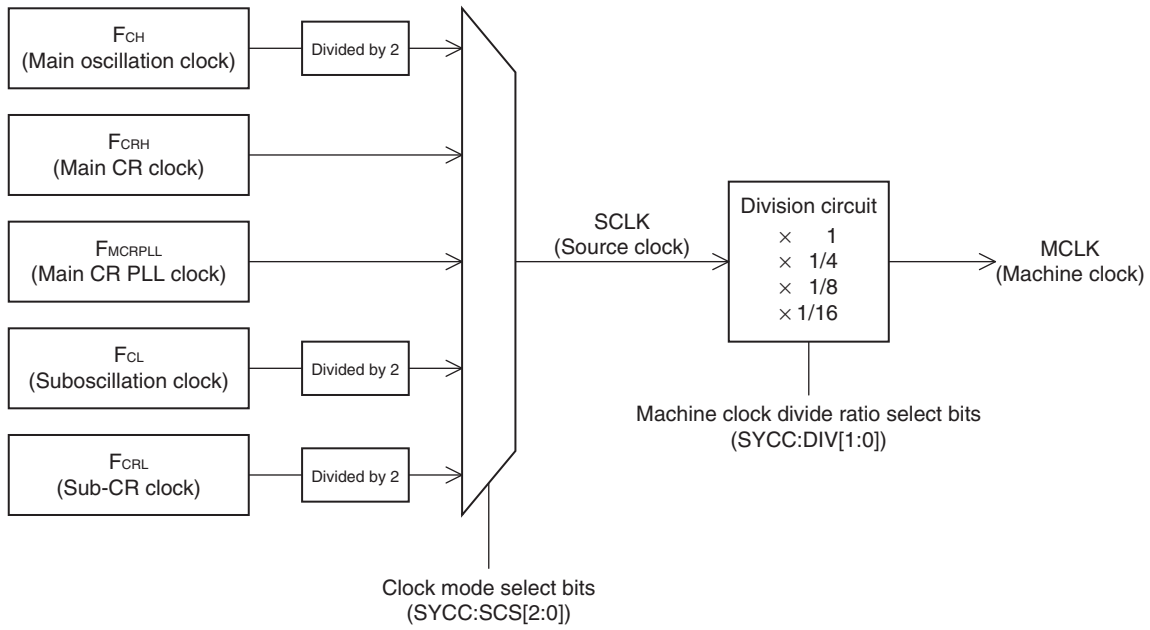
*1: This is the clock before it is divided according to the division ratio set by the machine clock division ratio select bits (SYCC:DIV[1:0]). This source clock is divided to become a machine clock according to the division ratio set by the machine clock division ratio select bits (SYCC:DIV[1:0]). In addition, a source clock can be selected from the following.

- Main clock divided by 2
- Main CR clock
- PLL multiplication of main CR clock (Select a multiplication rate from 2, 2.5, 3 and 4.)
- Subclock divided by 2
- Sub-CR clock divided by 2

*2: This is the operating clock of the microcontroller. A machine clock can be selected from the following.

- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

- Schematic diagram of the clock generation block

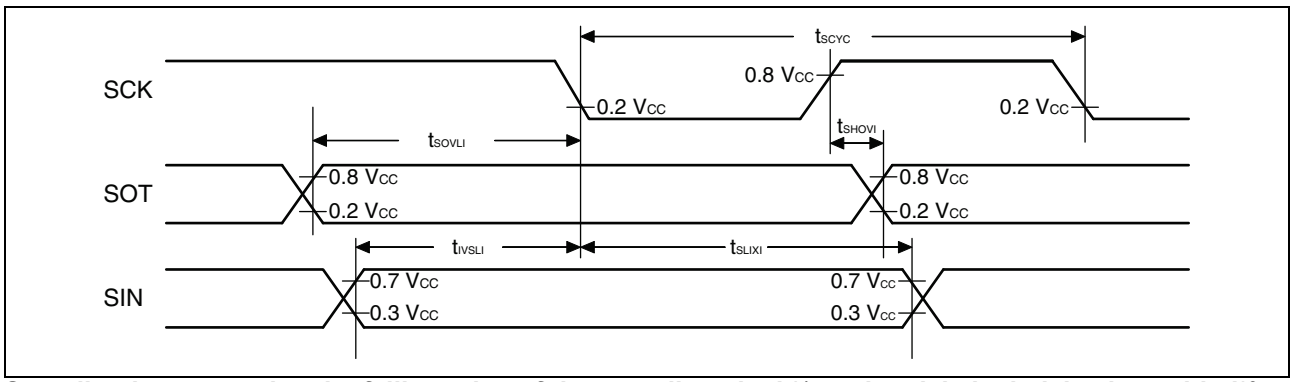


Sampling is executed at the rising edge of the sampling clock*1, and serial clock delay is enabled*2.
(ESCR register : SCES bit = 0, ECCR register : SCDE bit = 1)

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK↑ → SOT delay time	t_{SHOVI}	SCK, SOT		−50	+50	ns
Valid SIN → SCK↓	t_{IVSLI}	SCK, SIN		t_{MCLK}*3 + 80	—	ns
SCK↓→ valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
SOT → SCK↓delay time	t_{SOVLI}	SCK, SOT		3t_{MCLK}*3 − 70	—	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.
*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.
*3: See “Source Clock/Machine Clock” for t_{MCLK}.



Sampling is executed at the falling edge of the sampling clock*1, and serial clock delay is enabled*2.
(ESCR register : SCES bit = 1, ECCR register : SCDE bit = 1)

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK↓ → SOT delay time	t_{SLOVI}	SCK, SOT		−50	+50	ns
Valid SIN → SCK↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3 + 80	—	ns
SCK↑ → valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
SOT → SCK↑delay time	t_{SOVHI}	SCK, SOT		3t_{MCLK}*3 − 70	—	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.
*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.
*3: See “Source Clock/Machine Clock” for t_{MCLK}.

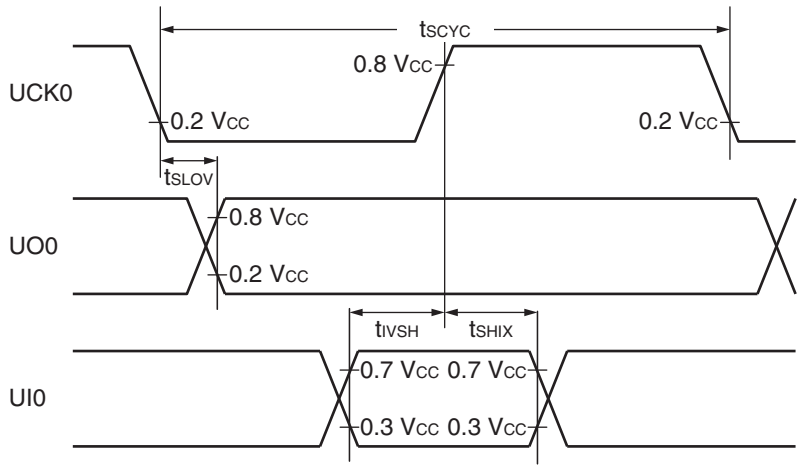
18.4.9 UART/SIO, Serial I/O Timing

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = −40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	UCK0	Internal clock operation	4 t_{MCLK}*	—	ns
UCK ↓ → UO time	t_{SLOV}	UCK0, UO0		−190	+190	ns
Valid UI → UCK ↑	t_{IVSH}	UCK0, UI0		2 t_{MCLK}*	—	ns
UCK ↑ → valid UI hold time	t_{SHIX}	UCK0, UI0		2 t_{MCLK}*	—	ns
Serial clock “H” pulse width	t_{SHSL}	UCK0	External clock operation	4 t_{MCLK}*	—	ns
Serial clock “L” pulse width	t_{SLSH}	UCK0		4 t_{MCLK}*	—	ns
UCK ↓ → UO time	t_{SLOV}	UCK0, UO0		—	190	ns
Valid UI → UCK ↑	t_{IVSH}	UCK0, UI0		2 t_{MCLK}*	—	ns
UCK ↑ → valid UI hold time	t_{SHIX}	UCK0, UI0		2 t_{MCLK}*	—	ns

*: See “Source Clock/Machine Clock” for t_{MCLK}.

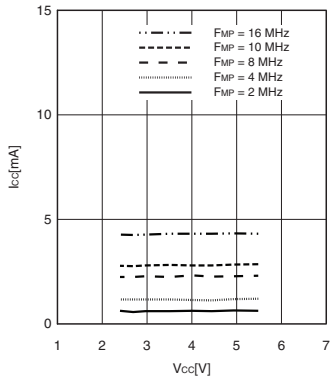
- Internal shift clock mode



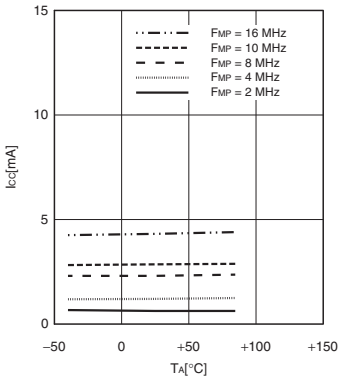
19. Sample Characteristics

- Power supply current temperature characteristics

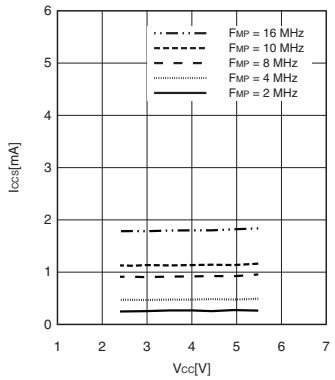
I_{CC} – V_{CC}
T_A = +25°C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



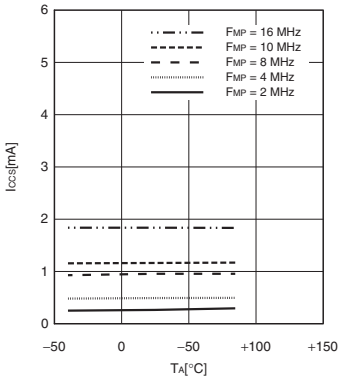
I_{CC} – T_A
V_{CC} = 5.5 V, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



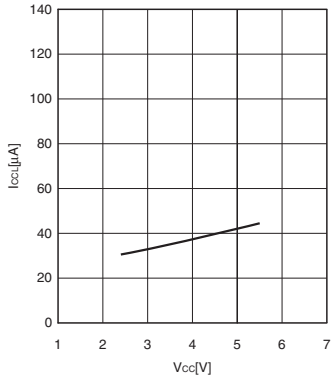
I_{CCS} – V_{CC}
T_A = +25°C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



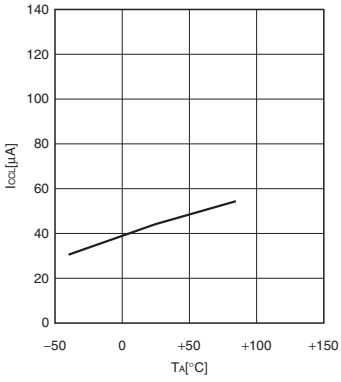
I_{CCS} – T_A
V_{CC} = 5.5 V, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



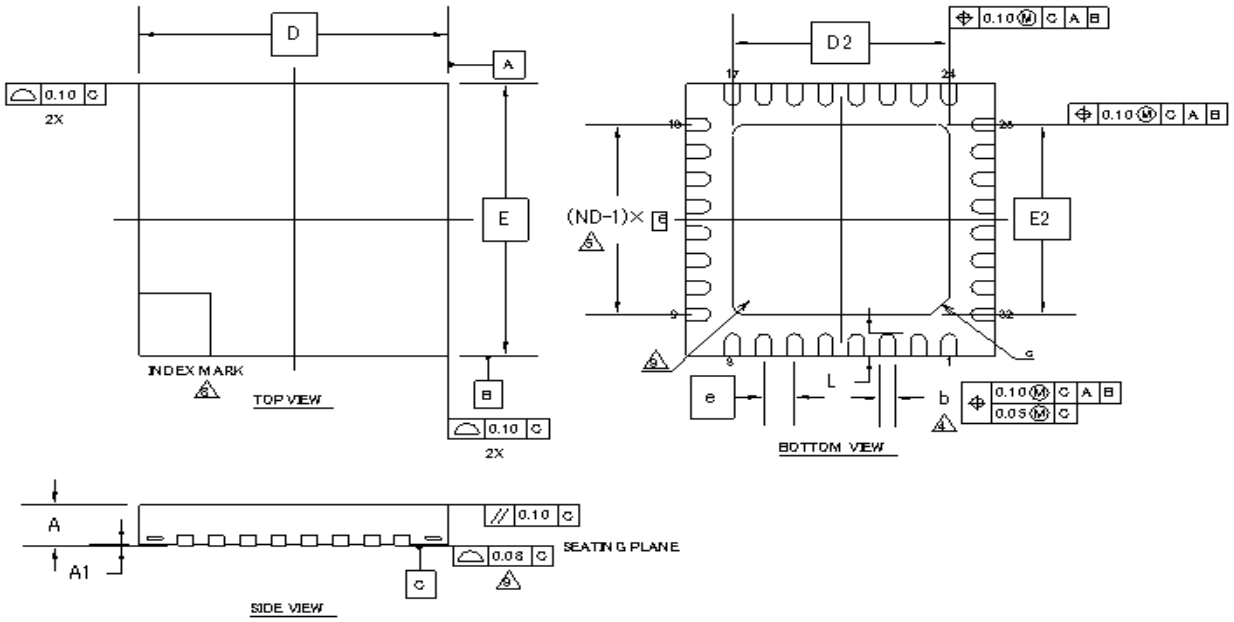
I_{CCL} – V_{CC}
T_A = +25°C, F_{MPL} = 16 kHz (divided by 2)
Subclock mode with the external clock operating



I_{CCL} – T_A
V_{CC} = 5.5 V, F_{MPL} = 16 kHz (divided by 2)
Subclock mode with the external clock operating



Package Type	Package Code
QFN 32	WNP032



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	——	——	0.80
A_1	0.00	——	0.05
D		5.00 BSC	
E		5.00 BSC	
b	0.18	0.25	0.30
D_2		3.50 BSC	
E_2		3.50 BSC	
e		0.50 BSC	
c		0.30 REF	
L	0.35	0.40	0.45

NOTE

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING CONFORMS TO ASME Y14.5-1994.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND REFER TO THE NUMBER OF TERMINALS ON D OR E SIDE.
6. MAX. PACKAGE WARPAGE IS 0.05mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LOCATED WITHIN INDICATED ZONE.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. JEDEC SPECIFICATION NO. REF: N/A

PACKAGE OUTLINE, 32 LEAD QFN
5.00X5.00X0.8 MM WNP032 3.5X3.5 MM EPAD (SAWN) REV**

002-15160 **