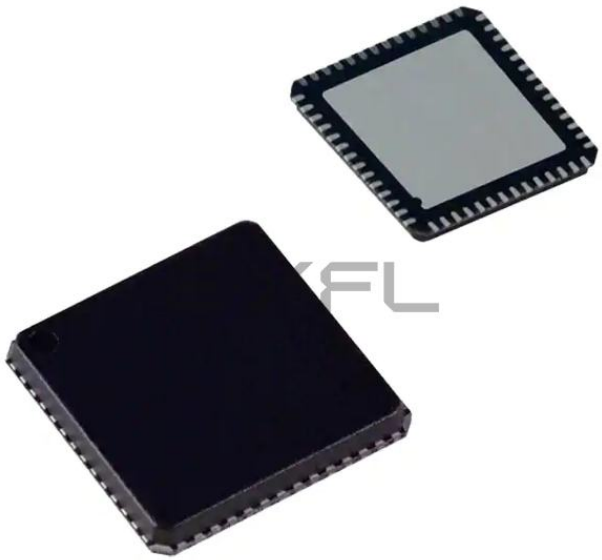

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8052
Core Size	8-Bit
Speed	12.58MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	PSM, Temp Sensor, WDT
Number of I/O	34
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	640 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 7x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	56-VFQFN Exposed Pad, CSP
Supplier Device Package	56-LFCSP-VQ (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc816bcp

SPECIFICATIONS[1] (AV_{DD} = 2.7 V to 3.6 V or 4.75 V to 5.25 V, DV_{DD} = 2.7 V to 3.6 V or 4.75 V to 5.25 V, REFIN(+) = 2.5 V; REFIN(–) = AGND; AGND = DGND = 0 V; XTAL1/XTAL2 = 32.768 kHz Crystal; all specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	ADuC816BS	Unit	Test Conditions/Comments
ADC SPECIFICATIONS			
Conversion Rate	5.4	Hz min	On Both Channels
	105	Hz max	Programmable in 0.732 ms Increments
Primary ADC			
No Missing Codes[2]	16	Bits min	20 Hz Update Rate
Resolution	13	Bits p-p typ	Range = ±20 mV, 20 Hz Update Rate
	16	Bits p-p typ	Range = ±2.56 V, 20 Hz Update Rate p-p Resolution at this Range/Update Rate Setting Is Limited Only by the Number of Bits Available from ADC
Output Noise	See Table IX and X in ADC Description		Output Noise Varies with Selected Update Rate and Gain Range
Integral Nonlinearity	±1	LSB max	
Offset Error	±3	µV typ	
Offset Error Drift	±10	nV/°C typ	
Full-Scale Error[3]	±10	µV typ	Range = ±20 mV to ±640 mV
	0.5	LSB typ	Range = ±1.28 V to ±2.56 V
Gain Error Drift[4]	±0.5	ppm/°C typ	
ADC Range Matching	±0.5	LSB typ	AIN = 18 mV
Power Supply Rejection (PSR)	95	dBs typ	AIN = 7.8 mV, Range = ±20 mV
	80	dBs typ	AIN = 1 V, Range = ±2.56 V
Common-Mode DC Rejection			
On AIN	95	dBs typ	At DC, AIN = 7.8 mV, Range = ±20 mV
	90	dBs typ	At DC, AIN = 1 V, Range = ±2.56 V
On REFIN	90	dBs typ	At DC, AIN = 1 V, Range = ±2.56 V
Common-Mode 50 Hz/60 Hz Rejection[2]			20 Hz Update Rate
On AIN	95	dBs typ	50 Hz/60 Hz ±1 Hz, AIN = 7.8 mV, Range = ±20 mV
	90	dBs typ	50 Hz/60 Hz ±1 Hz, AIN = 1 V, Range = ±2.56 V
On REFIN	90	dBs typ	50 Hz/60 Hz ±1 Hz, AIN = 1 V, Range = ±2.56 V
Normal Mode 50 Hz/60 Hz Rejection[2]			
On AIN	60	dBs typ	50 Hz/60 Hz ±1 Hz, 20 Hz Update Rate
On REFIN	60	dBs typ	50 Hz/60 Hz ±1 Hz, 20 Hz Update Rate
Auxiliary ADC			
No Missing Codes[2]	16	Bits min	
Resolution	16	Bits p-p typ	Range = ±2.5 V, 20 Hz Update Rate
Output Noise	See Table XI in ADC Description		Output Noise Varies with Selected Update Rate
Integral Nonlinearity	±1	LSB max	
Offset Error	–2	LSB typ	
Offset Error Drift	1	µV/°C typ	
Full-Scale Error[5]	–2.5	LSB typ	
Gain Error Drift[4]	±0.5	ppm/°C typ	
Power Supply Rejection (PSR)	80	dBs typ	AIN = 1 V, 20 Hz Update Rate
Normal Mode 50 Hz/60 Hz Rejection[2]			
On AIN	60	dBs typ	50 Hz/60 Hz ±1 Hz
On REFIN	60	dBs typ	50 Hz/60 Hz ±1 Hz, 20 Hz Update Rate
DAC PERFORMANCE			
DC Specifications[6]			
Resolution	12	Bits	
Relative Accuracy	±3	LSB typ	
Differential Nonlinearity	–1	LSB max	Guaranteed 12-Bit Monotonic
Offset Error	±50	mV max	
Gain Error[7]	±1	% max	AV_{DD} Range
	±1	% typ	V_{REF} Range
AC Specifications[2, 6]			
Voltage Output Settling Time	15	µs typ	Settling Time to 1 LSB of Final Value
Digital-to-Analog Glitch Energy	10	nVs typ	1 LSB Change at Major Carry

Parameter		12.58 MHz Core_Clk Min	12.58 MHz Core_Clk Max	Variable Core_Clk Min	Variable Core_Clk Max	Unit	Figure
EXTERNAL PROGRAM MEMORY							
t_{LHLL}	ALE Pulsewidth	119		$2t_{CORE} - 40$		ns	3
t_{AVLL}	Address Valid to ALE Low	39		$t_{CORE} - 40$		ns	3
t_{LLAX}	Address Hold after ALE Low	49		$t_{CORE} - 30$		ns	3
t_{LLIV}	ALE Low to Valid Instruction In		218		$4t_{CORE} - 100$	ns	3
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	49		$t_{CORE} - 30$		ns	3
t_{PLPH}	$\overline{PSEN}$ Pulsewidth	193		$3t_{CORE} - 45$		ns	3
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		133		$3t_{CORE} - 105$	ns	3
t_{PXIX}	Input Instruction Hold after $\overline{PSEN}$	0		0		ns	3
t_{PXIZ}	Input Instruction Float after $\overline{PSEN}$		54		$t_{CORE} - 25$	ns	3
t_{AVIV}	Address to Valid Instruction In		292		$5t_{CORE} - 105$	ns	3
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		25		25	ns	3
t_{PHAX}	Address Hold after $\overline{PSEN}$ High	0		0		ns	3

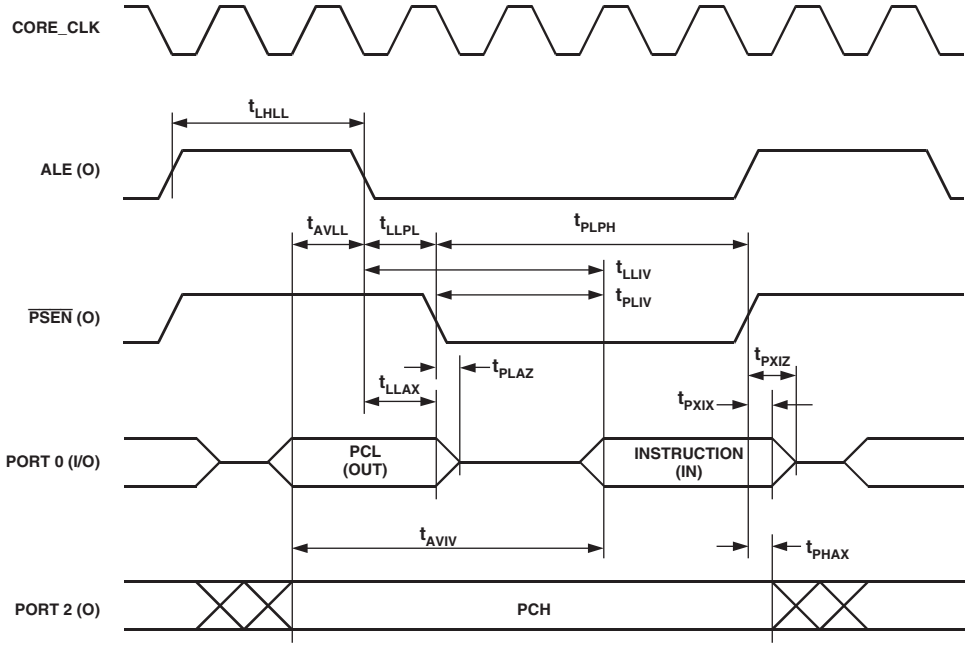


Figure 3. External Program Memory Read Cycle

Parameter		12.58 MHz Core_Clk Min	Max	Variable Core_Clk Min	Max	Unit	Figure
EXTERNAL DATA MEMORY WRITE CYCLE							
t_{WLWH}	$\overline{WR}$ Pulsewidth	377		$6t_{CORE} - 100$		ns	5
t_{AVLL}	Address Valid after ALE Low	39		$t_{CORE} - 40$		ns	5
t_{LLAX}	Address Hold after ALE Low	44		$t_{CORE} - 35$		ns	5
t_{LLWL}	ALE Low to $\overline{WR}$ Low	188	288	$3t_{CORE} - 50$	$3t_{CORE} + 50$	ns	5
t_{AVWL}	Address Valid to $\overline{WR}$ Low	188		$4t_{CORE} - 130$		ns	5
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	29		$t_{CORE} - 50$		ns	5
t_{QVWH}	Data Setup before $\overline{WR}$	406		$7t_{CORE} - 150$		ns	5
t_{WHQX}	Data and Address Hold after $\overline{WR}$	29		$t_{CORE} - 50$		ns	5
t_{WHLH}	$\overline{WR}$ High to ALE High	39	119	$t_{CORE} - 40$	$t_{CORE} + 40$	ns	5

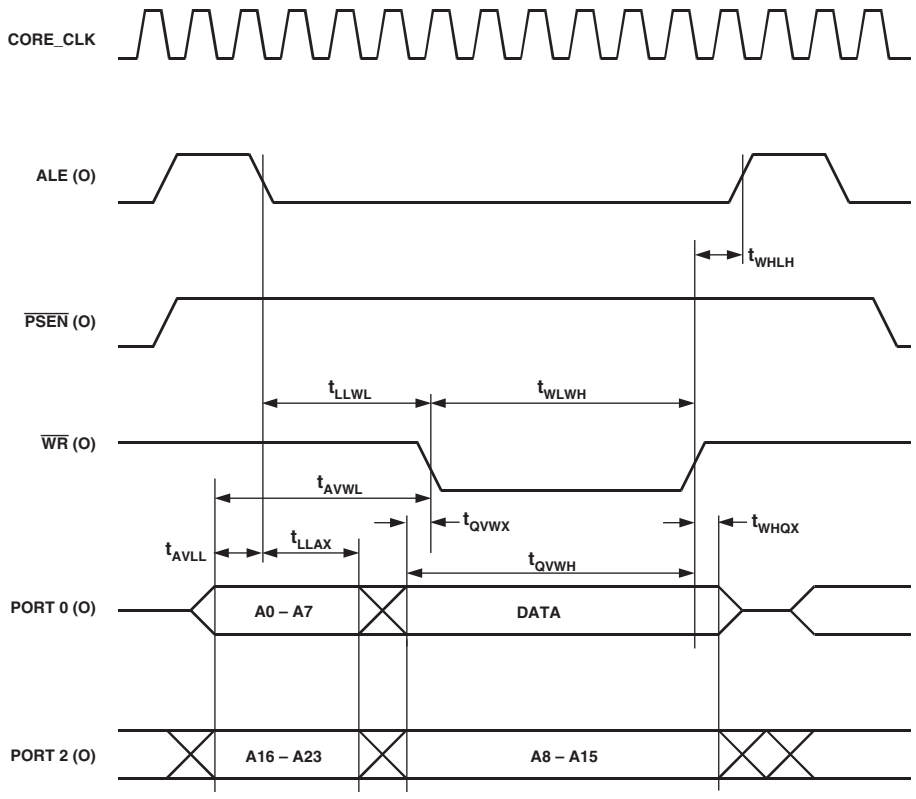


Figure 5. External Data Memory Write Cycle

Parameter		Min	Typ	Max	Unit	Figure
SPI MASTER MODE TIMING (CPHA = 0)						
t_{SL}	SCLOCK Low Pulsewidth*		630		ns	9
t_{SH}	SCLOCK High Pulsewidth*		630		ns	9
t_{DAV}	Data Output Valid after SCLOCK Edge			50	ns	9
t_{DOSU}	Data Output Setup before SCLOCK Edge			150	ns	9
t_{DSU}	Data Input Setup Time before SCLOCK Edge	100			ns	9
t_{DHD}	Data Input Hold Time after SCLOCK Edge	100			ns	9
t_{DF}	Data Output Fall Time		10	25	ns	9
t_{DR}	Data Output Rise Time		10	25	ns	9
t_{SR}	SCLOCK Rise Time		10	25	ns	9
t_{SF}	SCLOCK Fall Time		10	25	ns	9

*Characterized under the following conditions:
a. Core clock divider bits CD2, CD1 and CD0 bits in PLLCON SFR set to 0, 1, and 1 respectively, i.e., core clock frequency = 1.57 MHz and
b. SPI bit-rate selection bits SPR1 and SPR0 bits in SPICON SFR set to 0 and 0 respectively.

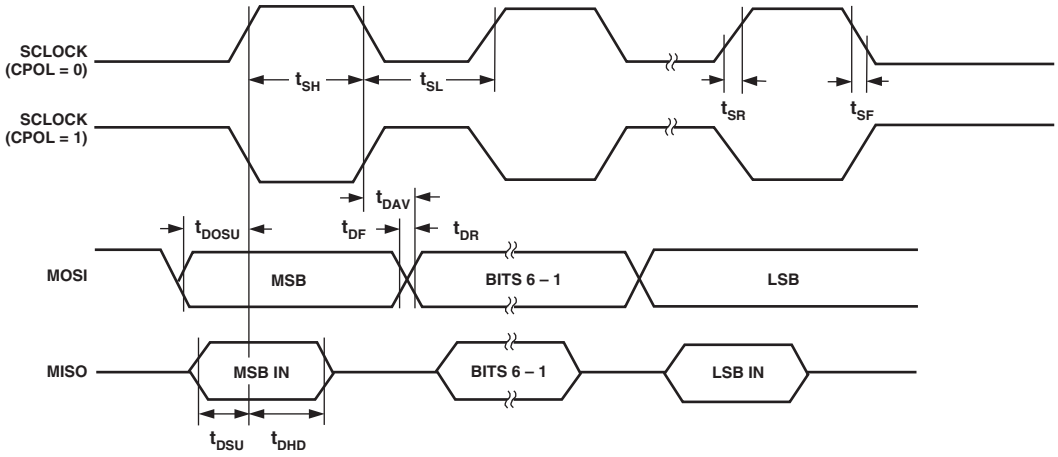


Figure 9. SPI Master Mode Timing (CPHA = 0)

Parameter		Min	Typ	Max	Unit	Figure
SPI SLAVE MODE TIMING (CPHA = 1)						
t_{SS}	$\overline{SS}$ to SCLOCK Edge	0			ns	10
t_{SL}	SCLOCK Low Pulsewidth		330		ns	10
t_{SH}	SCLOCK High Pulsewidth		330		ns	10
t_{DAV}	Data Output Valid after SCLOCK Edge			50	ns	10
t_{DSU}	Data Input Setup Time before SCLOCK Edge	100			ns	10
t_{DHD}	Data Input Hold Time after SCLOCK Edge	100			ns	10
t_{DF}	Data Output Fall Time		10	25	ns	10
t_{DR}	Data Output Rise Time		10	25	ns	10
t_{SR}	SCLOCK Rise Time		10	25	ns	10
t_{SF}	SCLOCK Fall Time		10	25	ns	10
t_{SFS}	$\overline{SS}$ High after SCLOCK Edge	0			ns	10

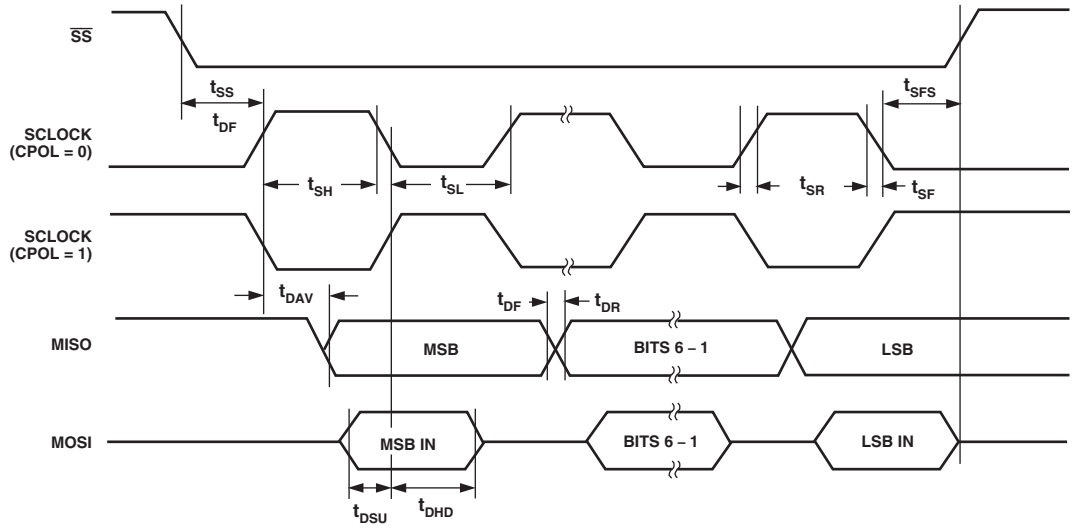
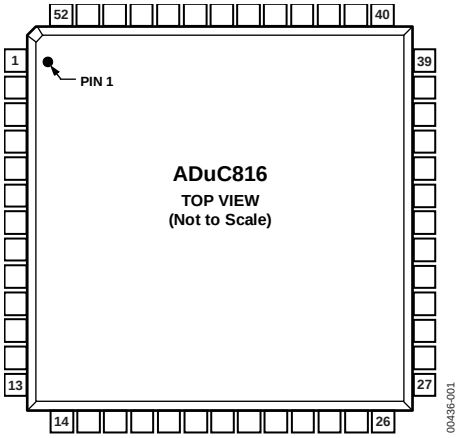
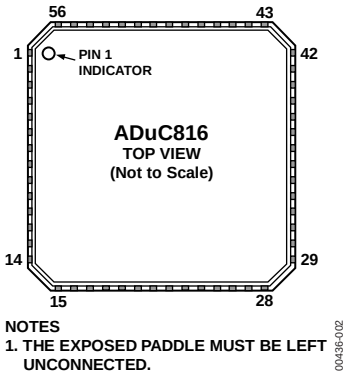


Figure 10. SPI Slave Mode Timing (CPHA = 1)

PIN FUNCTION DESCRIPTIONS



56-Lead MQFP



56-Lead LFCSP

PIN FUNCTION DESCRIPTIONS

Pin No. 52-Lead MQFP	Pin No. 56-Lead CSP	Mnemonic	Type[1]	Description
1, 2	56, 1	P1.0/P1.1	I/O	P1.0 and P1.1 can function as digital inputs or digital outputs and have a pull-up configuration as described for Port 3. P1.0 and P1.1 have an increased current drive sink capability of 10 mA.
		P1.0/T2	I/O	P1.0 and P1.1 also have various secondary functions as described below. P1.0 can be used to provide a clock input to Timer 2. When enabled, Counter 2 is incremented in response to a negative transition on the T2 input pin.
		P1.1/T2EX	I/O	P1.1 can also be used to provide a control input to Timer 2.When enabled, a negative transition on the T2EX input pin will cause a Timer 2 capture or reload event.
3–4,	2–3,	P1.2–P1.7	I	Port 1.2 to Port 1.7 have no digital output driver; they can function as a digital input
9–12	11–14	P1.2/DAC/IEXC1	I/O	for which 0 must be written to the port bit. As a digital input, these pins must be driven high or low externally. These pins also have the following analog functionality: The voltage output from the DAC or one or both current sources (200 μA or 2 × 200 μA) can be configured to appear at this pin.
		P1.3/AIN5/IEXC2	I/O	Auxiliary ADC input or one or both current sources can be configured at this pin.
		P1.4/AIN1	I	Primary ADC, Positive Analog Input
		P1.5/AIN2	I	Primary ADC, Negative Analog Input
		P1.6/AIN3	I	Auxiliary ADC Input or Muxed Primary ADC, Positive Analog Input
		P1.7/AIN4/DAC	I/O	Auxiliary ADC Input or Muxed Primary ADC, Negative Analog Input. The voltage output from the DAC can also be configured to appear at this pin.
5	4, 5	AV_{DD}	S	Analog Supply Voltage, 3 V or 5 V
6	6, 7, 8	AGND	S	Analog Ground. Ground reference pin for the analog circuitry.
7	9	REFIN(–)	I	Reference Input, Negative Terminal
8	10	REFIN(+)	I	Reference Input, Positive Terminal
13	15	$\overline{SS}$	I	Slave Select Input for the SPI Interface. A weak pull-up is present on this pin.
14	16	MISO	I/O	Master Input/Slave Output for the SPI Interface. A weak pull-up is present on this input pin
15	17	RESET	I	Reset Input. A high level on this pin for 16 core clock cycles while the oscillator is running resets the device. There is an internal weak pull-down and a Schmitt trigger input stage on this pin.
16–19,	18–21,	P3.0–P3.7	I/O	P3.0–P3.7 are bidirectional port pins with internal pull-up resistors. Port 3 pins that
22–25	24–27	P3.0/RXD	I/O	have 1s written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, Port 3 pins being pulled externally low will source current because of the internal pull-up resistors.When driving a 0-to-1 output transition, a strong pull-up is active for two core clock periods of the instruction cycle. Port 3 pins also have various secondary functions including: Receiver Data for UART Serial Port
		P3.1/TXD	I/O	Transmitter Data for UART Serial Port
		P3.2/$\overline{INT0}$	I/O	External Interrupt 0.This pin can also be used as a gate control input to Timer 0.
		P3.3/$\overline{INT1}$	I/O	External Interrupt 1.This pin can also be used as a gate control input to Timer 1.
		P3.4/T0	I/O	Timer/Counter 0 External Input.
		P3.5/T1	I/O	Timer/Counter 1 External Input
		P3.6/$\overline{WR}$	I/O	External Data Memory Write Strobe. Latches the data byte from Port 0 into an external data memory.
		P3.7/$\overline{RD}$	I/O	External Data Memory Read Strobe. Enables the data from an external data memory to Port 0.

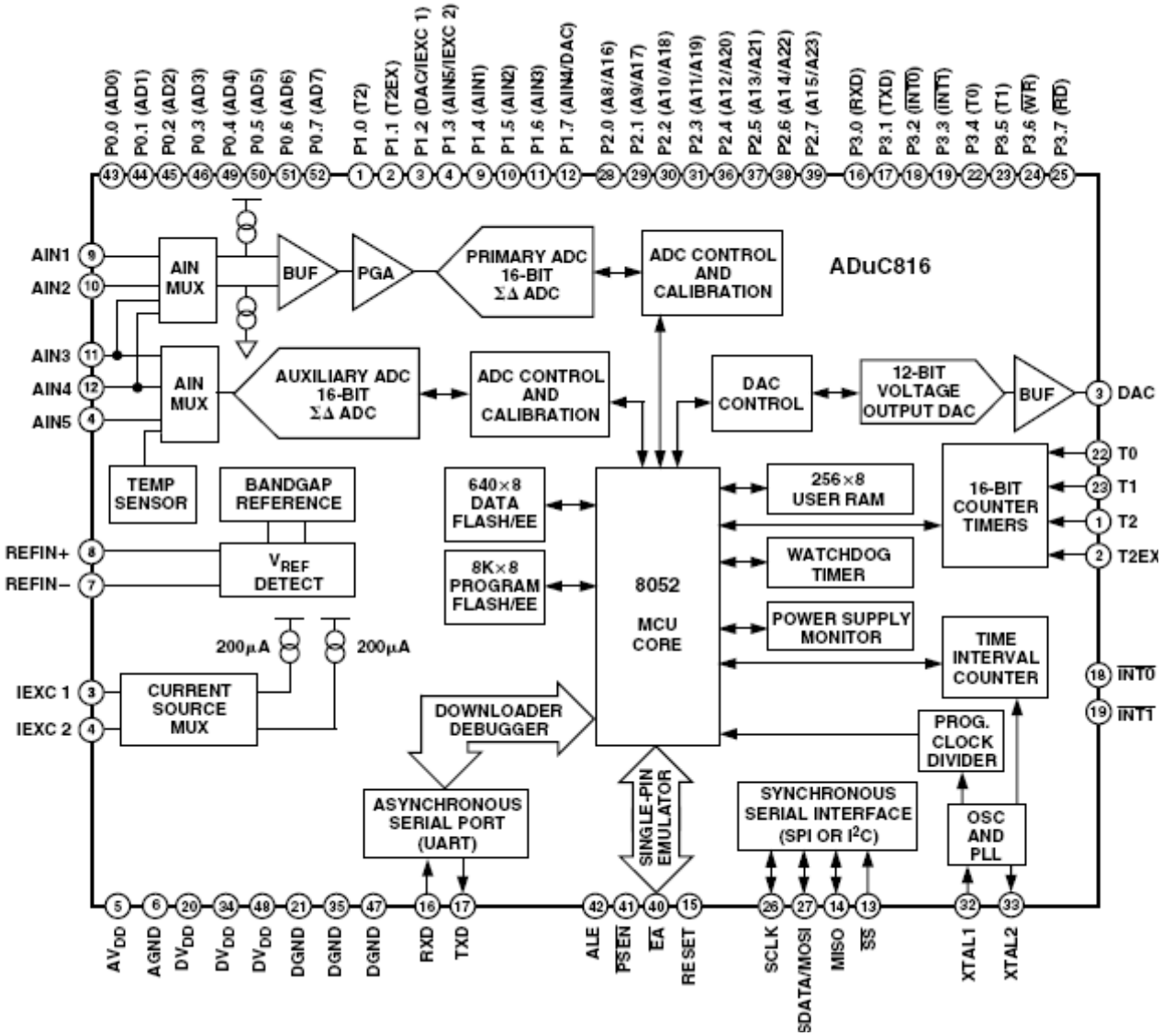


Figure 12. 52-MQFP Block Diagram

MEMORY ORGANIZATION

As with all 8051-compatible devices, the ADuC816 has separate address spaces for Program and Data memory as shown in Figure 13 and Figure 14.

If the user applies power or resets the device while the $\overline{EA}$ pin is pulled low, the part will execute code from the external program space, otherwise the part defaults to code execution from its internal 8 Kbyte Flash/EE program memory. This internal code space can be downloaded via the UART serial port while the device is in-circuit.

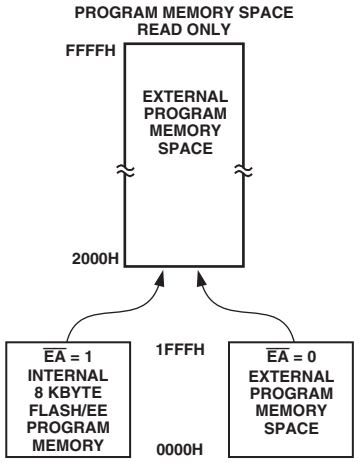


Figure 13. Program Memory Map

The data memory address space consists of internal and external memory space. The internal memory space is divided into four physically separate and distinct blocks, namely the lower 128 bytes of RAM, the upper 128 bytes of RAM, the 128 bytes of special function register (SFR) area, and a 640-byte Flash/EE Data memory. While the upper 128 bytes of RAM, and the SFR area share the same address locations, they are accessed through different address modes.

The lower 128 bytes of data memory can be accessed through direct or indirect addressing, the upper 128 bytes of RAM can be accessed through indirect addressing, and the SFR area is accessed through direct addressing.

Also, as shown in Figure 13, the additional 640 Bytes of Flash/EE Data Memory are available to the user and can be accessed indirectly via a group of control registers mapped into the Special Function Register (SFR) area. Access to the Flash/EE Data Memory is discussed in detail later as part of the Flash/EE Memory section in this data sheet.

The external data memory area can be expanded up to 16 MBytes. This is an enhancement of the 64 KByte external data memory space available on standard 8051-compatible cores.

The external data memory is discussed in more detail in the ADuC816 Hardware Design Considerations section.

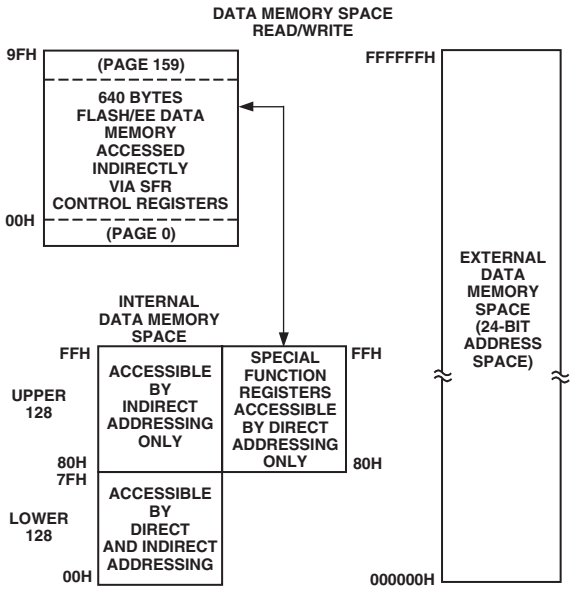


Figure 14. Data Memory Map

The lower 128 bytes of internal data memory are mapped as shown in Figure 15. The lowest 32 bytes are grouped into four banks of eight registers addressed as R0 through R7. The next 16 bytes (128 bits), locations 20Hex through 2FHex above the register banks, form a block of directly addressable bit locations at bit addresses 00H through 7FH. The stack can be located anywhere in the internal memory address space, and the stack depth can be expanded up to 256 bytes.

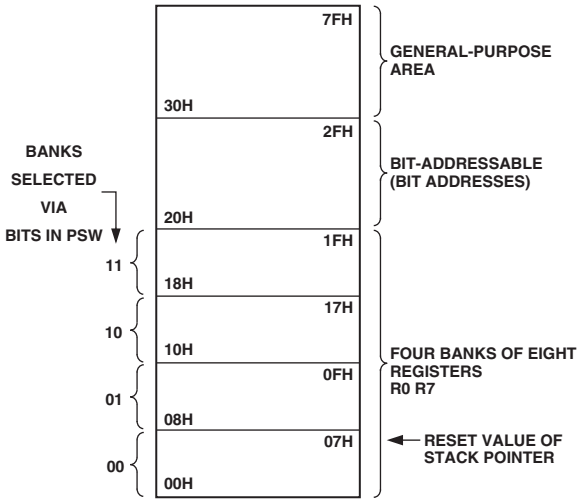


Figure 15. Lower 128 Bytes of Internal Data Memory

mended. Deriving the reference input voltage across an external resistor, as shown in Figure 52, will mean that the reference input sees a significant external source impedance. External decoupling on the REFIN(+) and REFIN(–) pins would not be recommended in this type of circuit configuration.

Reference Detect

The ADuC816 includes on-chip circuitry to detect if the part has a valid reference for conversions or calibrations. If the voltage between the external REFIN(+) and REFIN(–) pins goes below 0.3 V or either the REFIN(+) or REFIN(–) inputs is open circuit, the ADuC816 detects that it no longer has a valid reference. In this case, the NOXREF bit of the ADCSTAT SFR is set to a 1. If the ADuC816 is performing normal conversions and the NOXREF bit becomes active, the conversion results revert to all 1s. Therefore, it is not necessary to continuously monitor the status of the NOXREF bit when performing conversions. It is only necessary to verify its status if the conversion result read from the ADC Data Register is all 1s.

If the ADuC816 is performing either an offset or gain calibration and the NOXREF bit becomes active, the updating of the respective calibration registers is inhibited to avoid loading incorrect coefficients to these registers, and the appropriate ERR0 or ERR1 bits in the ADCSTAT SFR are set. If the user is concerned about verifying that a valid reference is in place every time a calibration is performed, the status of the ERR0 or ERR1 bit should be checked at the end of the calibration cycle.

Sigma-Delta Modulator

A sigma-delta ADC generally consists of two main blocks, an analog modulator and a digital filter. In the case of the ADuC816 ADCs, the analog modulators consist of a difference amplifier, an integrator block, a comparator, and a feedback DAC as illustrated in Figure 20.

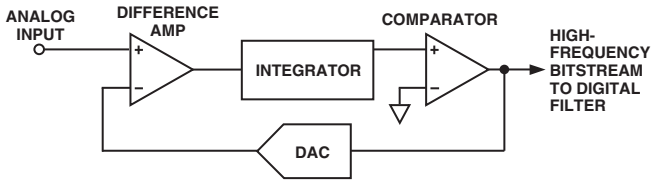


Figure 20. Sigma-Delta Modulator Simplified Block Diagram

In operation, the analog signal sample is fed to the difference amplifier along with the output of the feedback DAC. The difference between these two signals is integrated and fed to the comparator. The output of the comparator provides the input to the feedback DAC so the system functions as a negative feedback loop that tries to minimize the difference signal. The digital data that represents the analog input voltage is contained in the duty cycle of the pulse train appearing at the output of the comparator. This duty cycle data can be recovered as a data word using a subsequent digital filter stage. The sampling frequency of the modulator loop is many times higher than the bandwidth of the input signal. The integrator in the modulator shapes the quantization noise (which results from the analog-to-digital conversion) so that the noise is pushed toward one-half of the modulator frequency.

Digital Filter

The output of the sigma-delta modulator feeds directly into the digital filter. The digital filter then band-limits the response to a frequency significantly lower than one-half of the modulator frequency. In this manner, the 1-bit output of the comparator is translated into a band-limited, low noise output from the ADuC816 ADCs.

The ADuC816 filter is a low-pass, $Sinc^3$ or $(sinx/x)^3$ filter whose primary function is to remove the quantization noise introduced at the modulator. The cutoff frequency and decimated output data rate of the filter are programmable via the SF (Sinc Filter) SFR as described in Table VII.

Figure 21 shows the frequency response of the ADC channel at the default SF word of 69 dec or 45 hex, yielding an overall output update rate of just under 20 Hz.

It should be noted that this frequency response allows frequency components higher than the ADC Nyquist frequency to pass through the ADC, in some cases without significant attenuation. These components may, therefore, be aliased and appear in-band after the sampling process.

It should also be noted that rejection of mains-related frequency components, i.e., 50 Hz and 60 Hz, is seen to be at level of >65 dB at 50 Hz and >100 dB at 60 Hz. This confirms the data sheet specifications for 50 Hz/60 Hz Normal Mode Rejection (NMR) at a 20 Hz update rate.

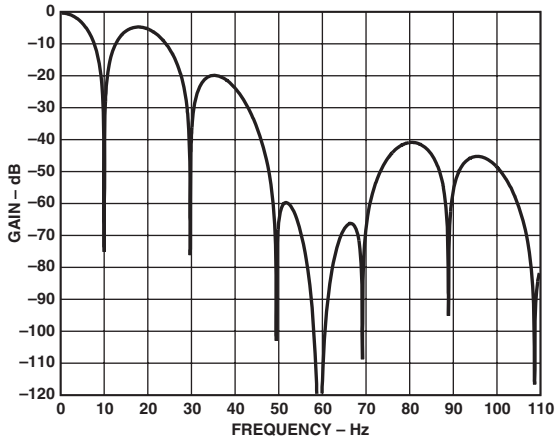


Figure 21. Filter Response, SF = 69 dec

The response of the filter, however, will change with SF word as can be seen in Figure 22, which shows >90 dB NMR at 50 Hz and >70 dB NMR at 60 Hz when SF = 255 dec.

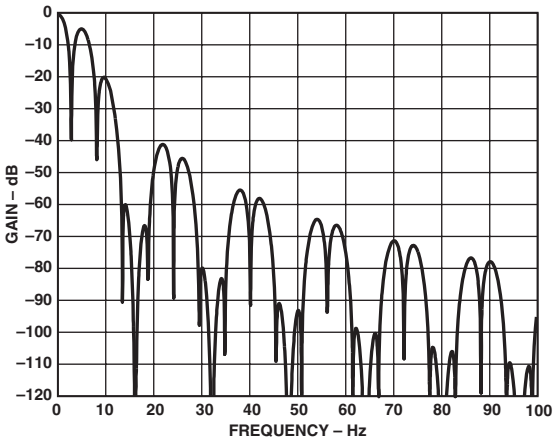


Figure 22. Filter Response, SF = 255 dec

Figures 23 and 24 show the NMR for 50 Hz and 60 Hz across the full range of SF word, i.e., SF = 13 dec to SF = 255 dec.

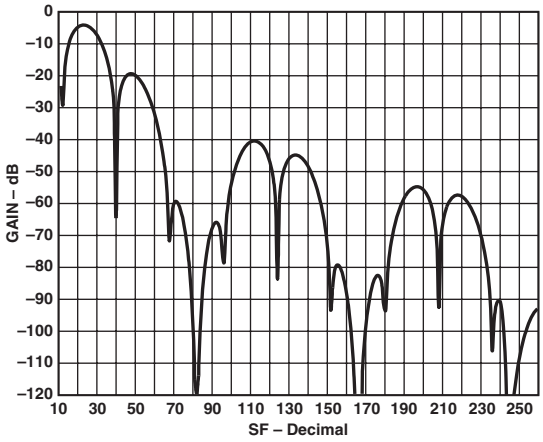


Figure 23. 50 Hz Normal Mode Rejection vs. SF

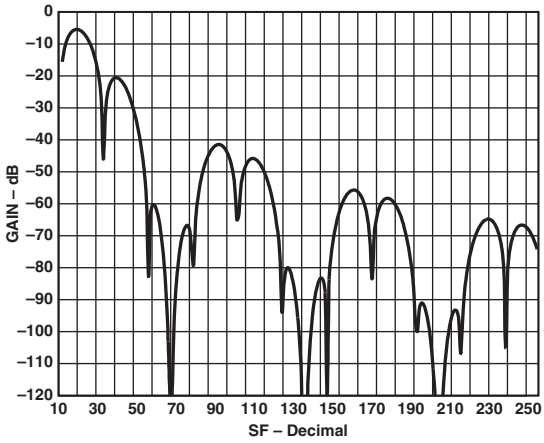


Figure 24. 60 Hz Normal Mode Rejection vs. SF

ADC Chopping

Both ADCs on the ADuC816 implement a chopping scheme whereby the ADC repeatability reverses its inputs. The decimated digital output words from the $Sinc^3$ filters therefore have a positive offset and negative offset term included.

As a result, a final summing stage is included in each ADC so that each output word from the filter is summed and averaged with the previous filter output to produce a new valid output result to be written to the ADC data SFRs. In this way, while the ADC throughput or update rate is as discussed earlier and illustrated in Table VII, the full settling time through the ADC (or the time to a first conversion result), will actually be given by $2 \times t_{ADC}$.

The chopping scheme incorporated in the ADuC816 ADC results in excellent dc offset and offset drift specifications and is extremely beneficial in applications where drift, noise rejection, and optimum EMI rejection are important factors.

Calibration

The ADuC816 provides four calibration modes that can be programmed via the mode bits in the ADCMODE SFR detailed in Table IV. In fact, every ADuC816 has already been factory calibrated. The resultant Offset and Gain calibration coefficients for both the primary and auxiliary ADCs are stored on-chip in manufacturing-specific Flash/EE memory locations. At power-on, these factory calibration coefficients are automatically downloaded to the calibration registers in the ADuC816 SFR space. Each ADC (primary and auxiliary) has dedicated calibration SFRs, these have been described earlier as part of the general ADC SFR description. However, the factory calibration values in the ADC calibration SFRs will be overwritten if any one of the four calibration options are initiated and that ADC is enabled via the ADC enable bits in ADCMODE.

Even though an internal offset calibration mode is described below, it should be recognized that both ADCs are chopped. This chopping scheme inherently minimizes offset and means that an internal offset calibration should never be required. Also, because factory 5 V/25°C gain calibration coefficients are automatically present at power-on, an internal full-scale calibration will only be required if the part is being operated at 3 V or at temperatures significantly different from 25°C.

The ADuC816 offers "internal" or "system" calibration facilities. For full calibration to occur on the selected ADC, the calibration logic must record the modulator output for two different input conditions. These are "zero-scale" and "full-scale" points. These points are derived by performing a conversion on the different input voltages provided to the input of the modulator during calibration. The result of the "zero-scale" calibration conversion is stored in the Offset Calibration Registers for the appropriate ADC. The result of the "full-scale" calibration conversion is stored in the Gain Calibration Registers for the appropriate ADC. With these readings, the calibration logic can calculate the offset and the gain slope for the input-to-output transfer function of the converter.

During an "internal" zero-scale or full-scale calibration, the respective "zero" input and "full-scale" input are automatically connected to the ADC input pins internally to the device. A "system" calibration, however, expects the system zero-scale and system full-scale voltages to be applied to the external ADC pins before the calibration mode is initiated. In this way external ADC errors are taken into account and minimized as a result of system calibration. It should also be noted that to optimize calibration accuracy, all ADuC816 ADC calibrations are carried out automatically at the slowest update rate.

Internally in the ADuC816, the coefficients are normalized before being used to scale the words coming out of the digital filter. The offset calibration coefficient is subtracted from the result prior to the multiplication by the gain coefficient. All ADuC816 ADC specifications will only apply after a zero-scale and full-scale calibration at the operating point (supply voltage/temperature) of interest.

From an operational point of view, a calibration should be treated like another ADC conversion. A zero-scale calibration (if required) should always be carried out before a full-scale calibration. System software should monitor the relevant ADC RDY0/1 bit in the ADCSTAT SFR to determine end of calibration via a polling sequence or interrupt driven routine.

Using the Flash/EE Program Memory

The 8 Kbyte Flash/EE Program Memory array is mapped into the lower 8 Kbytes of the 64 Kbytes program space addressable by the ADuC816, and is used to hold user code in typical applications.

The program memory Flash/EE memory arrays can be programmed in one of two modes, namely:

Serial Downloading (In-Circuit Programming)

As part of its factory boot code, the ADuC816 facilitates serial code download via the standard UART serial port. Serial download mode is automatically entered on power-up if the external pin, $\overline{PSEN}$, is pulled low through an external resistor as shown in Figure 27. Once in this mode, the user can download code to the program memory array while the device is sited in its target application hardware. A PC serial download executable is provided as part of the ADuC816 QuickStart development system. The Serial Download protocol is detailed in a MicroConverter Applications Note uC004 available from the ADI MicroConverter Website at www.analog.com/microconverter.

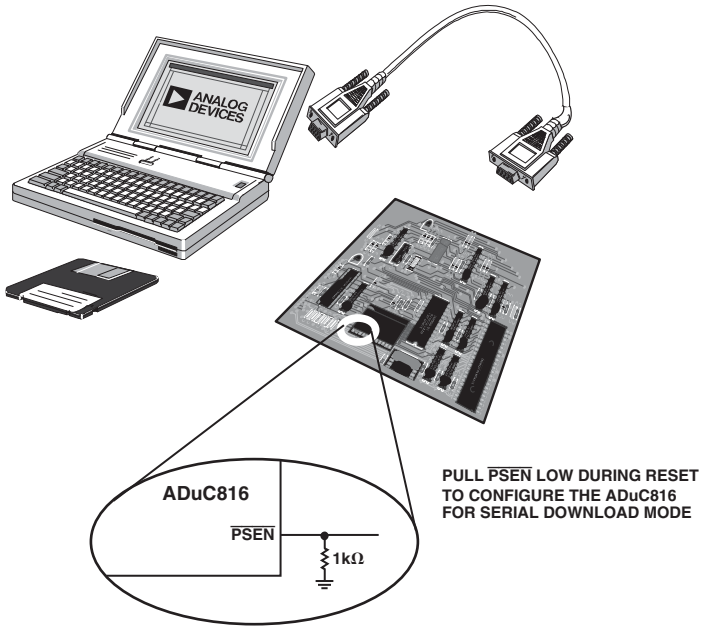


Figure 27. Flash/EE Memory Serial Download Mode Programming

Parallel Programming

The parallel programming mode is fully compatible with conventional third party Flash or EEPROM device programmers. A block diagram of the external pin configuration required to support parallel programming is shown in Figure 28. In this mode, Ports 0, 1, and 2 operate as the external data and address bus interface, ALE operates as the Write Enable strobe, and Port 3 is used as a general configuration port that configures the device for various program and erase operations during parallel programming.

The high voltage (12 V) supply required for Flash/EE programming is generated using on-chip charge pumps to supply the high voltage program lines.

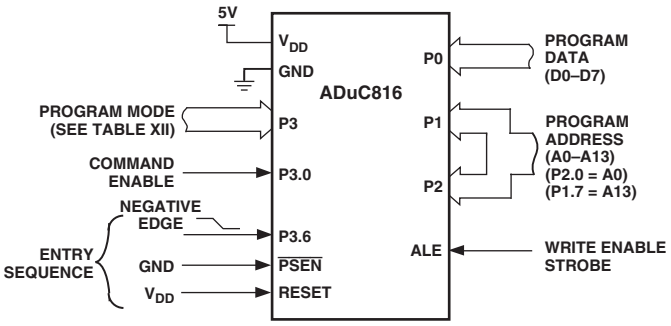


Figure 28. Flash/EE Memory Parallel Programming

Table XII. Flash/EE Memory Parallel Programming Modes

Port 3 Pins							Programming
0.7	0.6	0.5	0.4	0.3	0.2	0.1	Mode
X	X	X	X	0	0	0	Erase Flash/EE Program, Data, and Security Modes
X	X	X	X	0	0	1	Read Device Signature/ID
X	X	X	1	0	1	0	Program Code Byte
X	X	X	0	0	1	0	Program Data Byte
X	X	X	1	0	1	1	Read Code Byte
X	X	X	0	0	1	1	Read Data Byte
X	X	X	X	1	0	0	Program Security Modes
X	X	X	X	1	0	1	Read/Verify Security Modes
All Other Codes							Redundant

Flash/EE Program Memory Security

The ADuC816 facilitates three modes of Flash/EE program memory security. These modes can be independently activated, restricting access to the internal code space. These security modes can be enabled as part of the user interface available on all ADuC816 serial or parallel programming tools referenced on the MicroConverter web page at www.analog.com/microconverter. The security modes available on the ADuC816 are described as follows:

Lock Mode

This mode locks code in memory, disabling parallel programming of the program memory although reading the memory in parallel mode is still allowed. This mode is deactivated by initiating a "code-erase" command in serial download or parallel programming modes.

Secure Mode

This mode locks code in memory, disabling parallel programming (program and verify/read commands) as well as disabling the execution of a "MOVC" instruction from external memory, which is attempting to read the op codes from internal memory. This mode is deactivated by initiating a "code-erase" command in serial download or parallel programming modes.

USER INTERFACE TO OTHER ON-CHIP ADuC816 PERIPHERALS

The following section gives a brief overview of the various peripherals also available on-chip. A summary of the SFRs used to control and configure these peripherals is also given.

DAC

The ADuC816 incorporates a 12-bit, voltage output DAC on-chip. It has a rail-to-rail voltage output buffer capable of driving 10 kΩ/100 pF. It has two selectable ranges, 0 V to V_{REF} (the internal bandgap 2.5 V reference) and 0 V to AV_{DD}. It can operate in 12-bit or 8-bit mode. The DAC has a control register, DACCON, and two data registers, DACH/L. The DAC output can be programmed to appear at Pin 3 or Pin 12. It should be noted that in 12-bit mode, the DAC voltage output will be updated as soon as the DACL data SFR has been written; therefore, the DAC data registers should be updated as DACH first followed by DACL.

DACCON	**DAC Control Register**
SFR Address	FDH
Power-On Default Value	00H
Bit Addressable	No

---	---	---	**DACPIN**	**DAC8**	**DACRN**	**$\overline{\text{DACCLR}}$**	**DACEN**

Table XIV. DACCON SFR Bit Designations

Bit	Name	Description
7	---	Reserved for Future Use.
6	---	Reserved for Future Use.
5	---	Reserved for Future Use.
4	DACPIN	DAC Output Pin Select. *Set* by the user to direct the DAC output to Pin 12 (P1.7/AIN4/DAC). *Cleared* by user to direct the DAC output to Pin 3 (P1.2/DAC/IEXC1).
3	DAC8	DAC 8-bit Mode Bit. *Set* by user to enable 8-bit DAC operation. In this mode the 8-bits in DACL SFR are routed to the 8 MSBs of the DAC and the 4 LSBs of the DAC are set to zero. *Cleared* by user to operate the DAC in its normal 12-bit mode of operation.
2	DACRN	DAC Output Range Bit. *Set* by user to configure DAC range of 0 – AV_{DD}. *Cleared* by user to configure DAC range of 0 – 2.5 V.
1	$\overline{\text{DACCLR}}$	DAC Clear Bit. *Set* to "1" by user to enable normal DAC operation. *Cleared* to "0" by user to reset DAC data registers DACl/H to zero.
0	DACEN	DAC Enable Bit. *Set* to "1" by user to enable normal DAC operation. *Cleared* to "0" by user to power-down the DAC.

DACH/L	**DAC Data Registers**	
Function	DAC Data Registers, written by user to update the DAC output.	
SFR Address	DACL (DAC Data Low Byte)	–>FBH
	DACH (DAC Data High Byte)	–>FCH
Power-On Default Value	00H	–>Both Registers
Bit Addressable	No	–>Both Registers

The 12-bit DAC data should be written into DACH/L right-justified such that DACL contains the lower eight bits, and the lower nibble of DACH contains the upper four bits.

Watchdog Timer

The purpose of the watchdog timer is to generate a device reset or interrupt within a reasonable amount of time if the ADuC816 enters an erroneous state, possibly due to a programming error, electrical noise, or RFI. The Watchdog function can be disabled by clearing the WDE (Watchdog Enable) bit in the Watchdog Control (WDCON) SFR. When enabled; the watchdog circuit will generate a system reset or interrupt (WDS) if the user program fails to set the watchdog (WDE) bit within a predetermined amount of time (see PRE3–0 bits in WDCON). The watchdog timer itself is a 16-bit counter that is clocked at 32.768 kHz. The watchdog time-out interval can be adjusted via the PRE3–0 bits in WDCON. Full Control and Status of the watchdog timer function can be controlled via the watchdog timer control SFR (WDCON). The WDCON SFR can only be written by user software if the double write sequence described in WDWR below is initiated on every write access to the WDCON SFR.

WDCON	**Watchdog Timer Control Register**
SFR Address	C0H
Power-On Default Value	10H
Bit Addressable	Yes

PRE3	PRE2	PRE1	PRE0	WDIR	WDS	WDE	WDWR

Table XVII. WDCON SFR Bit Designations

Bit	Name	Description
7	PRE3	Watchdog Timer Prescale Bits.
6	PRE2	The Watchdog timeout period is given by the equation: $t_{WD} = (2^{PRE} \times (2^9/f_{PLL}))$
5	PRE1	($0 \le PRE \le 7$; f_{PLL} = 32.768 kHz)
4	PRE0	PRE3 PRE2 PRE1 PRE0 Timout Period (ms) Action 0 0 0 0 15.6 Reset or Interrupt 0 0 0 1 31.2 Reset or Interrupt 0 0 1 0 62.5 Reset or Interrupt 0 0 1 1 125 Reset or Interrupt 0 1 0 0 250 Reset or Interrupt 0 1 0 1 500 Reset or Interrupt 0 1 1 0 1000 Reset or Interrupt 0 1 1 1 2000 Reset or Interrupt 1 0 0 0 0.0 Immediate Reset PRE3–0 > 1001 Reserved
3	WDIR	Watchdog Interrupt Response Enable Bit. If this bit is set by the user, the watchdog will generate an interrupt response instead of a system reset when the watchdog timeout period has expired. This interrupt is not disabled by the CLR EA instruction and it is also a fixed, high-priority interrupt. If the watchdog is not being used to monitor the system, it can alternatively be used as a timer. The prescaler is used to set the timeout period in which an interrupt will be generated. (See also Note 1, Table XXXIV in the Interrupt System section.)
2	WDS	Watchdog Status Bit. *Set* by the Watchdog Controller to indicate that a watchdog timeout has occurred. *Cleared* by writing a "0" or by an external hardware reset. It is not cleared by a watchdog reset.
1	WDE	Watchdog Enable Bit. *Set* by user to enable the watchdog and clear its counters. If this bit is not set by the user within the watchdog timeout period, the watchdog will generate a reset or interrupt, depending on WDIR. *Cleared* under the following conditions, User writes "0," Watchdog Reset (WDIR = "0"); Hardware Reset; PSM Interrupt.

0	WDWR	Watchdog Write Enable Bit.
		To write data into the WDCON SFR involves a double instruction sequence. The WDWR bit must be set and the very next instruction must be a write instruction to the WDCON SFR.
		e.g., `CLR EA ; disable interrupts while writing to WDT`
		`SETB WDWR ; allow write to WDCON`
		`MOV WDCON, #72h ; enable WDT for 2.0s timeout`
		`SET B EA ; enable interrupts again (if rqd)`

Power Supply Monitor

As its name suggests, the Power Supply Monitor, once enabled, monitors both supplies (AVDD or DVDD) on the ADuC816. It will indicate when any of the supply pins drop below one of four user-selectable voltage trip points from 2.63 V to 4.63 V. For correct operation of the Power Supply Monitor function, AV_{DD} must be equal to or greater than 2.7 V. Monitor function is controlled via the PSMCON SFR. If enabled via the IEIP2 SFR, the monitor will interrupt the core using the PSMI bit in the PSMCON SFR. This bit will not be cleared until the failing power supply has returned above the trip point for at least 250 ms. This monitor function allows the user to save working registers to avoid possible data loss due to the low supply condition, and also ensures that normal code execution will not resume until a safe supply level has been well established. The supply monitor is also protected against spurious glitches triggering the interrupt circuit.

PSMCON **Power Supply Monitor Control Register**

SFR Address DFH
Power-On Default Value DEH
Bit Addressable No

CMPD	CMPA	PSMI	TPD1	TPD0	TPA1	TPA0	PSMEN

Table XVIII. PSMCON SFR Bit Designations

Bit	Name	Description
7	CMPD	DVDD Comparator Bit. This is a read-only bit and directly reflects the state of the DVDD comparator. Read "1" indicates the DVDD supply is above its selected trip point. Read "0" indicates the DVDD supply is below its selected trip point.
6	CMPA	AVDD Comparator Bit. This is a read-only bit and directly reflects the state of the AVDD comparator. Read "1" indicates the AVDD supply is above its selected trip point. Read "0" indicates the AVDD supply is below its selected trip point.
5	PSMI	Power Supply Monitor Interrupt Bit. This bit will be set high by the MicroConverter if either CMPA or CMPD are low, indicating low analog or digital supply. The PSMI bit can be used to interrupt the processor. Once CMPD and/or CMPA return (and remain) high, a 250 ms counter is started. When this counter times out, the PSMI interrupt is cleared. PSMI can also be written by the user. However, if either comparator output is low, it is not possible for the user to clear PSMI.
4	TPD1	DVDD Trip Point Selection Bits.
3	TPD0	These bits select the DVDD trip-point voltage as follows: TPD1 TPD0 Selected DVDD Trip Point (V) 0 0 4.63 0 1 3.08 1 0 2.93 1 1 2.63
2	TPA1	AVDD Trip Point Selection Bits.
1	TPA0	These bits select the AVDD trip-point voltage as follows: TPA1 TPA0 Selected AVDD Trip Point (V) 0 0 4.63 0 1 3.08 1 0 2.93 1 1 2.63
0	PSMEN	Power Supply Monitor Enable Bit. *Set* to "1" by the user to enable the Power Supply Monitor Circuit. *Cleared* to "0" by the user to disable the Power Supply Monitor Circuit.

8051-COMPATIBLE ON-CHIP PERIPHERALS

This section gives a brief overview of the various secondary peripheral circuits are also available to the user on-chip. These remaining functions are fully 8051-compatible and are controlled via standard 8051 SFR bit definitions.

Parallel I/O Ports 0–3

The ADuC816 uses four input/output ports to exchange data with external devices. In addition to performing general-purpose I/O, some ports are capable of external memory operations; others are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

Port 0 is an 8-bit open drain bidirectional I/O port that is directly controlled via the Port 0 SFR (SFR address = 80 hex). Port 0 pins that have 1s written to them via the Port 0 SFR will be configured as open drain and will therefore float. In that state, Port 0 pins can be used as high impedance inputs. An external pull-up resistor will be required on Port 0 outputs to force a valid logic high level externally. Port 0 is also the multiplexed low-order address and data bus during accesses to external program or data memory. In this application it uses strong internal pull-ups when emitting 1s.

Port 1 is also an 8-bit port directly controlled via the P1 SFR (SFR address = 90 hex). The Port 1 pins are divided into two distinct pin groupings.

P1.0 and P1.1 pins on Port 1 are bidirectional digital I/O pins with internal pull-ups. If P1.0 and P1.1 have 1s written to them via the P1 SFR, these pins are pulled high by the internal pull-up resistors. In this state they can also be used as inputs; as input pins being externally pulled low, they will source current because of the internal pull-ups. With 0s written to them, both these pins will drive a logic low output voltage (VOL) and will be capable of sinking 10 mA compared to the standard 1.6 mA sink capability on the other port pins. These pins also have various secondary functions described in Table XXI.

Table XXI. Port 1, Alternate Pin Functions

Pin	Alternate Function
P1.0	T2 (Timer/Counter 2 External Input)
P1.1	T2EX (Timer/Counter 2 Capture/Reload Trigger)

The remaining Port 1 pins (P1.2–P1.7) can only be configured as Analog Input (ADC), Analog Output (DAC) or Digital Input pins. By (power-on) default these pins are configured as Analog Inputs, i.e., "1" written in the corresponding Port 1 register bit. To configure any of these pins as digital inputs, the user should write a "0" to these port bits to configure the corresponding pin as a high impedance digital input.

Port 2 is a bidirectional port with internal pull-up resistors directly controlled via the P2 SFR (SFR address = A0 hex). Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors and, in that state, they can be used as inputs. As inputs, Port 2 pins being pulled externally low will source current because of the internal pull-up resistors. Port 2 emits the high order address bytes during fetches from external program memory and middle and high order address bytes during accesses to the 16-bit external data memory space.

Port 3 is a bidirectional port with internal pull-ups directly controlled via the P2 SFR (SFR address = B0 hex). Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and in that state they can be used as inputs. As inputs, Port 3 pins being pulled externally low will source current because of the internal pull-ups. Port 3 pins also have various secondary functions described in Table XXII.

Table XXII. Port 3, Alternate Pin Functions

Pin	Alternate Function
P3.0	RXD (UART Input Pin) (or Serial Data I/O in Mode 0)
P3.1	TXD (UART Output Pin) (or Serial Clock Output in Mode 0)
P3.2	$\overline{\text{INT0}}$ (External Interrupt 0)
P3.3	$\overline{\text{INT1}}$ (External Interrupt 1)
P3.4	T0 (Timer/Counter 0 External Input)
P3.5	T1 (Timer/Counter 1 External Input)
P3.6	$\overline{\text{WR}}$ (External Data Memory Write Strobe)
P3.7	$\overline{\text{RD}}$ (External Data Memory Read Strobe)

The alternate functions of P1.0, P1.1, and Port 3 pins can only be activated if the corresponding bit latch in the P1 and P3 SFRs contains a 1. Otherwise, the port pin is stuck at 0.

Timers/Counters

The ADuC816 has three 16-bit Timer/Counters: Timer 0, Timer 1, and Timer 2. The Timer/Counter hardware has been included on-chip to relieve the processor core of the overhead inherent in implementing timer/counter functionality in software. Each Timer/Counter consists of two 8-bit registers THx and TLx (x = 0, 1 and 2). All three can be configured to operate either as timers or event counters.

In "Timer" function, the TLx register is incremented every machine cycle. Thus one can think of it as counting machine cycles. Since a machine cycle consists of 12 core clock periods, the maximum count rate is 1/12 of the core clock frequency.

In "Counter" function, the TLx register is incremented by a 1-to-0 transition at its corresponding external input pin, T0, T1, or T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since it takes two machine cycles (16 core clock periods) to recognize a 1-to-0 transition, the maximum count rate is 1/16 of the core clock frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it must be held for a minimum of one full machine cycle. Remember that the core clock frequency is programmed via the CD0–2 selection bits in the PLLCON SFR.

TCON: Timer/Counter 0 and 1 Control Register

SFR Address 88H
Power-On Default Value 00H
Bit Addressable Yes

TF1	TR1	TF0	TR0	IE1[1]	IT1[1]	IE0[1]	IT0[1]

NOTE
[1]These bits are not used in the control of timer/counter 0 and 1, but are used instead in the control and monitoring of the external $\overline{INT0}$ and $\overline{INT1}$ interrupt pins.

Table XXIV. TCON SFR Bit Designations

Bit	Name	Description
7	TF1	Timer 1 Overflow Flag. *Set* by hardware on a timer/counter 1 overflow. *Cleared* by hardware when the Program Counter (PC) vectors to the interrupt service routine.
6	TR1	Timer 1 Run Control Bit. *Set* by user to turn on timer/counter 1. *Cleared* by user to turn off timer/counter 1.
5	TF0	Timer 0 Overflow Flag. *Set* by hardware on a timer/counter 0 overflow. *Cleared* by hardware when the PC vectors to the interrupt service routine.
4	TR0	Timer 0 Run Control Bit. *Set* by user to turn on timer/counter 0. *Cleared* by user to turn off timer/counter 0.
3	IE1	External Interrupt 1 ($\overline{INT1}$) Flag. *Set* by hardware by a falling edge or zero level being applied to external interrupt pin $\overline{INT1}$, depending on bit IT1 state. *Cleared* by hardware when the when the PC vectors to the interrupt service routine only if the interrupt was transition-activated. If level-activated, the external requesting source controls the request flag, rather than the on-chip hardware.
2	IT1	External Interrupt 1 (IE1) Trigger Type. *Set* by software to specify edge-sensitive detection (i.e., 1-to-0 transition). *Cleared* by software to specify level-sensitive detection (i.e., zero level).
1	IE0	External Interrupt 0 ($\overline{INT0}$) Flag. *Set* by hardware by a falling edge or zero level being applied to external interrupt pin $\overline{INT0}$, depending on bit IT0 state. *Cleared* by hardware when the PC vectors to the interrupt service routine only if the interrupt was transition-activated. If level-activated, the external requesting source controls the request flag, rather than the on-chip hardware.
0	IT0	External Interrupt 0 (IE0) Trigger Type. *Set* by software to specify edge-sensitive detection (i.e., 1-to-0 transition). *Cleared* by software to specify level-sensitive detection (i.e., zero level).

Timer/Counter 0 and 1 Data Registers

Each timer consists of two 8-bit registers. These can be used as independent registers or combined to be a single 16-bit register depending on the timer mode configuration.

TH0 and TL0

Timer 0 high byte and low byte.
SFR Address = 8Chex, 8Ahex respectively.

TH1 and TL1

Timer 1 high byte and low byte.
SFR Address = 8Dhex, 8Bhex respectively.

Timer/Counter 2 Operating Modes

The following paragraphs describe the operating modes for timer/counter 2. The operating modes are selected by bits in the T2CON SFR as shown in Table XXVI.

Table XXVI. TIMECON SFR Bit Designations

RCLK (or) TCLK	CAP2	TR2	MODE
0	0	1	16-Bit Autoreload
0	1	1	16-Bit Capture
1	X	1	Baud Rate
X	X	0	OFF

16-Bit Autoreload Mode

In "Autoreload" mode, there are two options, which are selected by bit EXEN2 in T2CON. If EXEN2 = 0, then when Timer 2 rolls over it not only sets TF2 but also causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2L and RCAP2H, which are preset by software. If EXEN2 = 1, then Timer 2 still performs the above, but with the added feature that a 1-to-0 transition at external input T2EX will also trigger the 16-bit reload and set EXF2. The autoreload mode is illustrated in Figure 37 below.

16-Bit Capture Mode

In the "Capture" mode, there are again two options, which are selected by bit EXEN2 in T2CON. If EXEN2 = 0, then Timer 2 is a 16-bit timer or counter which, upon overflowing, sets bit TF2, the Timer 2 overflow bit, which can be used to generate an interrupt. If EXEN2 = 1, then Timer 2 still performs the above, but a l-to-0 transition on external input T2EX causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into registers RCAP2L and RCAP2H, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set, and EXF2, like TF2, can generate an interrupt. The Capture Mode is illustrated in Figure 38.

The baud rate generator mode is selected by RCLK = 1 and/or TCLK = 1.

In either case if Timer 2 is being used to generate the baud rate, the TF2 interrupt flag will not occur. Hence Timer 2 interrupts will not occur so they do not have to be disabled. In this mode the EXF2 flag, however, can still cause interrupts and this can be used as a third external interrupt.

Baud rate generation will be described as part of the UART serial port operation in the following pages.

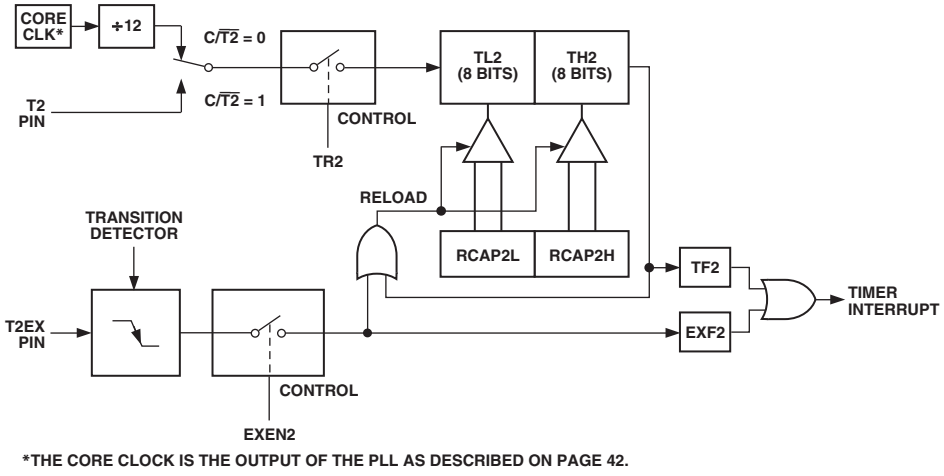


Figure 37. Timer/Counter 2, 16-Bit Autoreload Mode

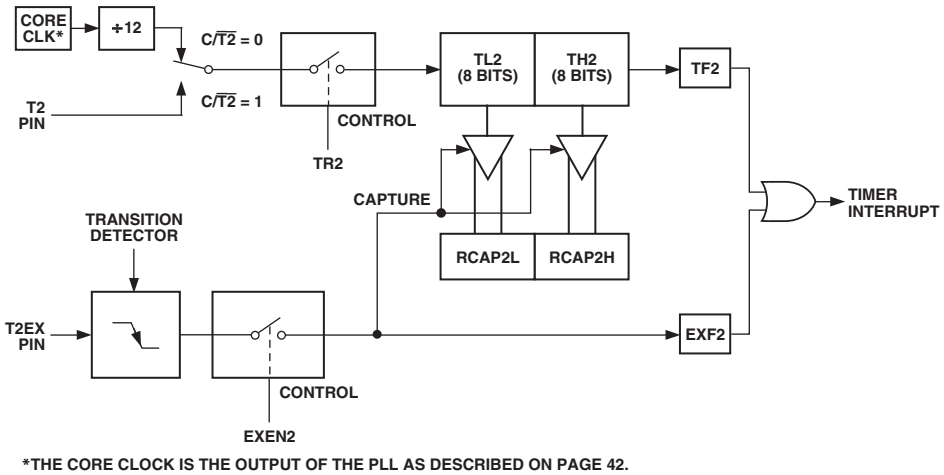


Figure 38. Timer/Counter 2, 16-Bit Capture Mode

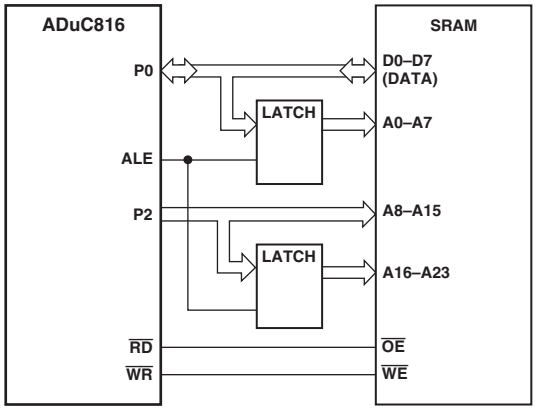


Figure 45. External Data Memory Interface (16 M Bytes Address Space)

In either implementation, Port 0 (P0) serves as a multiplexed address/data bus. It emits the low byte of the data pointer (DPL) as an address, which is latched by a pulse of ALE prior to data being placed on the bus by the ADuC816 (write operation) or the SRAM (read operation). Port 2 (P2) provides the data pointer page byte (DPP) to be latched by ALE, followed by the data pointer high byte (DPH). If no latch is connected to P2, DPP is ignored by the SRAM, and the 8051 standard of 64 Kbyte external data memory access is maintained.

Detailed timing diagrams of external program and data memory read and write access can be found in the timing specification sections of this data sheet.

Power-On Reset Operation

External POR (power-on reset) circuitry must be implemented to drive the RESET pin of the ADuC816. The circuit must hold the RESET pin asserted (high) whenever the power supply (DV_{DD}) is below 2.5 V. Furthermore, V_{DD} must remain above 2.5 V for at least 10 ms before the RESET signal is deasserted (low) by which time the power supply must have reached at least a 2.7 V level. The external POR circuit must be operational down to 1.2 V or less. The timing diagram of Figure 46 illustrates this functionality under three separate events: power-up, brownout, and power-down. Notice that when RESET is asserted (high) it tracks the voltage on DV_{DD}.

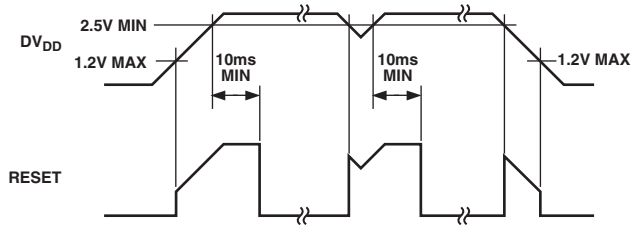


Figure 46. External POR Timing

The best way to implement an external POR function to meet the above requirements involves the use of a dedicated POR chip, such as the ADM809/ADM810 SOT-23 packaged PORs from Analog Devices. Recommended connection diagrams for both active-high ADM810 and active-low ADM809 PORs are shown in Figure 47 and Figure 48, respectively.

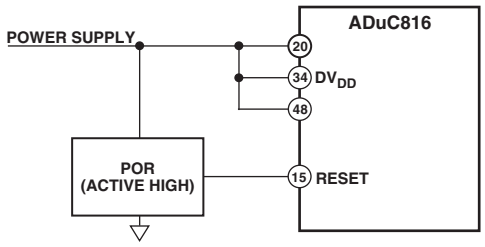


Figure 47. External Active High POR Circuit

Some active-low POR chips, such as the ADM809 can be used with a manual push-button as an additional reset source as illustrated by the dashed line connection in Figure 48.

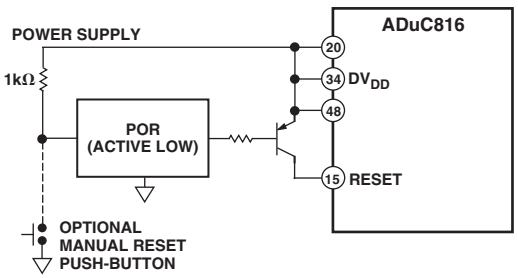


Figure 48. External Active Low POR Circuit

Power Supplies

The ADuC816's operational power supply voltage range is 2.7 V to 5.25 V. Although the guaranteed data sheet specifications are given only for power supplies within 2.7 V to 3.6 V or +5% of the nominal 5 V level, the chip will function equally well at any power supply level between 2.7 V and 5.25 V.

Separate analog and digital power supply pins (AV_{DD} and DV_{DD} respectively) allow AV_{DD} to be kept relatively free of noisy digital signals often present on the system DVDD line. In this mode the part can also operate with split supplies; that is, using different voltage supply levels for each supply. For example, this means that the system can be designed to operate with a DV_{DD} voltage level of 3 V while the AV_{DD} level can be at 5 V or vice-versa if required. A typical split supply configuration is shown in Figure 49.

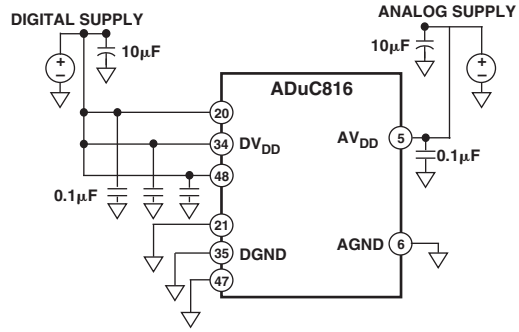


Figure 49. External Dual Supply Connections

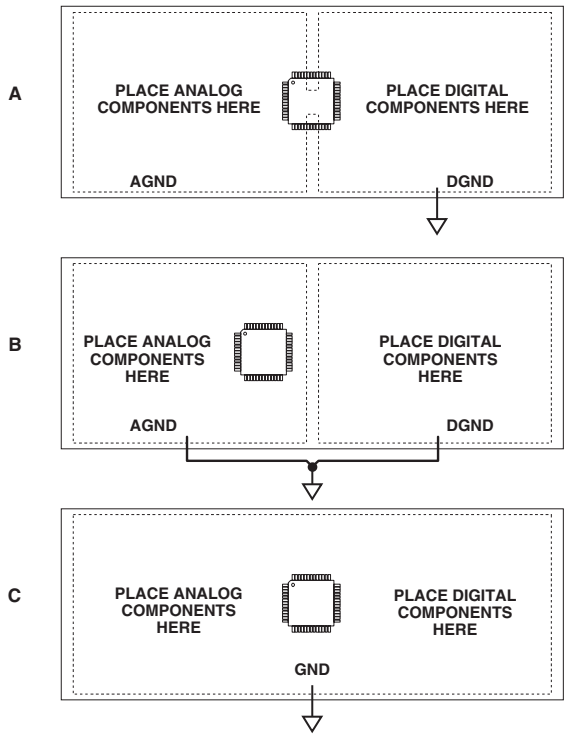


Figure 51. System Grounding Schemes

In all of these scenarios, and in more complicated real-life applications, keep in mind the flow of current from the supplies and back to ground. Make sure the return paths for all currents are as close as possible to the paths the currents took to reach their destinations. For example, do not power components on the analog side of Figure 51b with DV_{DD} since that would force return currents from DV_{DD} to flow through AGND. Also, try to avoid digital currents flowing under analog circuitry, which could happen if the user placed a noisy digital chip on the left half of the board in Figure 51c. Whenever possible, avoid large discontinuities in the ground plane(s) (such as are formed by a long trace on the same layer), since they force return signals to travel a longer path. And of course, make all connections to the ground plane directly, with little or no trace separating the pin from its via to ground.

If the user plans to connect fast logic signals (rise/fall time < 5 ns) to any of the ADuC816's digital inputs, add a series resistor to each relevant line to keep rise and fall times longer than 5 ns at the ADuC816 input pins. A value of 100 Ω or 200 Ω is usually sufficient to prevent high-speed signals from coupling capacitively into the ADuC816 and affecting the accuracy of ADC conversions.

ADuC816 System Self-Identification

In some hardware designs it may be an advantage for the software running on the ADuC816 target to identify the host MicroConverter. For example, code running on the ADuC816 may be used at future date to run on an ADuC816 MicroConverter host and the code may be required to operate differently.

The CHIPID SFR is a read-only register located at SFR address C2 hex. The top nibble of this byte is set to "1" to designate an ADuC824 host. For an ADuC824 host, the CHIPID SFR will contain the value "0" in the upper nibble.

OTHER HARDWARE CONSIDERATIONS

To facilitate in-circuit programming, plus in-circuit debug and emulation options, users will want to implement some simple connection points in their hardware that will allow easy access to download, debug, and emulation modes.

In-Circuit Serial Download Access

Nearly all ADuC816 designs will want to take advantage of the in-circuit reprogrammability of the chip. This is accomplished by a connection to the ADuC816's UART, which requires an external RS-232 chip for level translation if downloading code from a PC. Basic configuration of an RS-232 connection is illustrated in Figure 52 with a simple ADM202-based circuit. If users would rather not design an RS-232 chip onto a board, refer to the application note "uC006–A 4-Wire UART-to-PC Interface"[1] for a simple (and zero-cost-per-board) method of gaining in-circuit serial download access to the ADuC816.

NOTE
[1]Application note uC006 is available at www.analog.com/microconverter

In addition to the basic UART connections, users will also need a way to trigger the chip into download mode. This is accomplished via a 1 kΩ pull-down resistor that can be jumpered onto the $\overline{\text{PSEN}}$ pin, as shown in Figure 52. To get the ADuC816 into download mode, simply connect this jumper and power-cycle the device (or manually reset the device, if a manual reset button is available) and it will be ready to receive a new program serially. With the jumper removed, the device will come up in normal mode (and run the program) whenever power is cycled or RESET is toggled.

Note that $\overline{\text{PSEN}}$ is normally an output (as described in the External Memory Interface section) and it is sampled as an input only on the falling edge of RESET (i.e., at power-up or upon an external manual reset). Note also that if any external circuitry unintentionally pulls $\overline{\text{PSEN}}$ low during power-up or reset events, it could cause the chip to enter download mode and therefore fail to begin user code execution as it should. To prevent this, ensure that no external signals are capable of pulling the $\overline{\text{PSEN}}$ pin low, except for the external $\overline{\text{PSEN}}$ jumper itself.

Embedded Serial Port Debugger

From a hardware perspective, entry to serial port debug mode is identical to the serial download entry sequence described above. In fact, both serial download and serial port debug modes can be thought of as essentially one mode of operation used in two different ways.

Note that the serial port debugger is fully contained on the ADuC816 device, (unlike "ROM monitor" type debuggers) and therefore no external memory is needed to enable in-system debug sessions.

Single-Pin Emulation Mode

Also built into the ADuC816 is a dedicated controller for single-pin in-circuit emulation (ICE) using standard production ADuC816 devices. In this mode, emulation access is gained by connection to a single pin, the $\overline{\text{EA}}$ pin. Normally, this pin is hardwired either high or low to select execution from internal or external program memory space, as described earlier. To enable single-pin emulation mode, however, users will need to pull the $\overline{\text{EA}}$ pin high through a 1 kΩ resistor as shown in Figure 52. The emulator will then connect to the 2-pin header also shown in Figure 52. To be compatible with the standard connector that

REVISION HISTORY

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