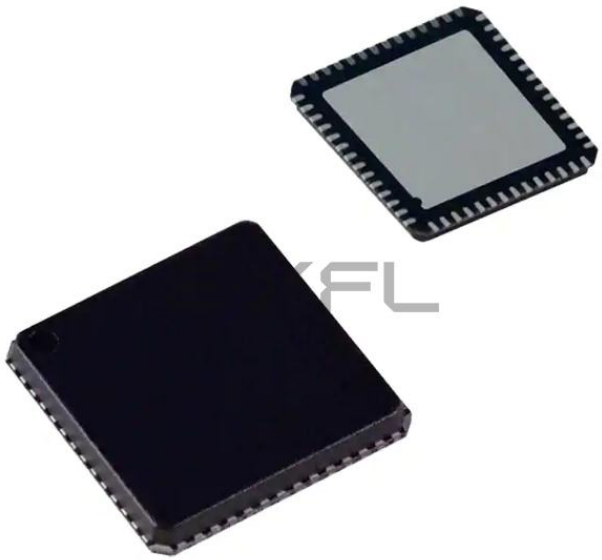

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Details	
Product Status	Active
Core Processor	8052
Core Size	8-Bit
Speed	12.58MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	PSM, Temp Sensor, WDT
Number of I/O	34
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	640 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 7x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	56-VFQFN Exposed Pad, CSP
Supplier Device Package	56-LFCSP-VQ (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc816bcpz

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SPECIFICATIONS[1] (AV_{DD} = 2.7 V to 3.6 V or 4.75 V to 5.25 V, DV_{DD} = 2.7 V to 3.6 V or 4.75 V to 5.25 V, REFIN(+) = 2.5 V; REFIN(–) = AGND; AGND = DGND = 0 V; XTAL1/XTAL2 = 32.768 kHz Crystal; all specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	ADuC816BS	Unit	Test Conditions/Comments
ADC SPECIFICATIONS			
Conversion Rate	5.4	Hz min	On Both Channels
	105	Hz max	Programmable in 0.732 ms Increments
Primary ADC			
No Missing Codes[2]	16	Bits min	20 Hz Update Rate
Resolution	13	Bits p-p typ	Range = ±20 mV, 20 Hz Update Rate
	16	Bits p-p typ	Range = ±2.56 V, 20 Hz Update Rate p-p Resolution at this Range/Update Rate Setting Is Limited Only by the Number of Bits Available from ADC
Output Noise	See Table IX and X in ADC Description		Output Noise Varies with Selected Update Rate and Gain Range
Integral Nonlinearity	±1	LSB max	
Offset Error	±3	µV typ	
Offset Error Drift	±10	nV/°C typ	
Full-Scale Error[3]	±10	µV typ	Range = ±20 mV to ±640 mV
	0.5	LSB typ	Range = ±1.28 V to ±2.56 V
Gain Error Drift[4]	±0.5	ppm/°C typ	
ADC Range Matching	±0.5	LSB typ	AIN = 18 mV
Power Supply Rejection (PSR)	95	dBs typ	AIN = 7.8 mV, Range = ±20 mV
	80	dBs typ	AIN = 1 V, Range = ±2.56 V
Common-Mode DC Rejection			
On AIN	95	dBs typ	At DC, AIN = 7.8 mV, Range = ±20 mV
	90	dBs typ	At DC, AIN = 1 V, Range = ±2.56 V
On REFIN	90	dBs typ	At DC, AIN = 1 V, Range = ±2.56 V
Common-Mode 50 Hz/60 Hz Rejection[2]			20 Hz Update Rate
On AIN	95	dBs typ	50 Hz/60 Hz ±1 Hz, AIN = 7.8 mV, Range = ±20 mV
	90	dBs typ	50 Hz/60 Hz ±1 Hz, AIN = 1 V, Range = ±2.56 V
On REFIN	90	dBs typ	50 Hz/60 Hz ±1 Hz, AIN = 1 V, Range = ±2.56 V
Normal Mode 50 Hz/60 Hz Rejection[2]			
On AIN	60	dBs typ	50 Hz/60 Hz ±1 Hz, 20 Hz Update Rate
On REFIN	60	dBs typ	50 Hz/60 Hz ±1 Hz, 20 Hz Update Rate
Auxiliary ADC			
No Missing Codes[2]	16	Bits min	
Resolution	16	Bits p-p typ	Range = ±2.5 V, 20 Hz Update Rate
Output Noise	See Table XI in ADC Description		Output Noise Varies with Selected Update Rate
Integral Nonlinearity	±1	LSB max	
Offset Error	–2	LSB typ	
Offset Error Drift	1	µV/°C typ	
Full-Scale Error[5]	–2.5	LSB typ	
Gain Error Drift[4]	±0.5	ppm/°C typ	
Power Supply Rejection (PSR)	80	dBs typ	AIN = 1 V, 20 Hz Update Rate
Normal Mode 50 Hz/60 Hz Rejection[2]			
On AIN	60	dBs typ	50 Hz/60 Hz ±1 Hz
On REFIN	60	dBs typ	50 Hz/60 Hz ±1 Hz, 20 Hz Update Rate
DAC PERFORMANCE			
DC Specifications[6]			
Resolution	12	Bits	
Relative Accuracy	±3	LSB typ	
Differential Nonlinearity	–1	LSB max	Guaranteed 12-Bit Monotonic
Offset Error	±50	mV max	
Gain Error[7]	±1	% max	AV_{DD} Range
	±1	% typ	V_{REF} Range
AC Specifications[2, 6]			
Voltage Output Settling Time	15	µs typ	Settling Time to 1 LSB of Final Value
Digital-to-Analog Glitch Energy	10	nVs typ	1 LSB Change at Major Carry

Parameter	ADuC816BS	Unit	Test Conditions/Comments
POWER REQUIREMENTS (continued)			
Power Supply Currents Normal Mode[16, 17]			
DV_{DD} Current	4	mA max	DV_{DD} = 4.75 V to 5.25 V, Core CLK = 1.57 MHz
	2.1	mA max	DV_{DD} = 2.7 V to 3.6 V, Core CLK = 1.57 MHz
AV_{DD} Current	170	μA max	AV_{DD} = 5.25 V, Core CLK = 1.57 MHz
DV_{DD} Current	15	mA max	DV_{DD} = 4.75 V to 5.25 V, Core CLK = 12.58 MHz
	8	mA max	DV_{DD} = 2.7 V to 3.6 V, Core CLK = 12.58 MHz
AV_{DD} Current	170	μA max	AV_{DD} = 5.25 V, Core CLK = 12.58 MHz
Power Supply Currents Idle Mode[16, 17]			
DV_{DD} Current	1.2	mA max	DV_{DD} = 4.75 V to 5.25 V, Core CLK = 1.57 MHz
	750	μA typ	DV_{DD} = 2.7 V to 3.6 V, Core CLK = 1.57 MHz
AV_{DD} Current	140	μA typ	Measured @ AV_{DD} = 5.25 V, Core CLK = 1.57 MHz
DV_{DD} Current	2	mA typ	DV_{DD} = 4.75 V to 5.25 V, Core CLK = 12.58 MHz
	1	mA typ	DV_{DD} = 2.7 V to 3.6 V, Core CLK = 12.58 MHz
AV_{DD} Current	140	μA typ	Measured at AV_{DD} = 5.25 V, Core CLK = 12.58 MHz
Power Supply Currents Power-Down Mode[16, 17]			Core CLK = 1.57 MHz or 12.58 MHz
DV_{DD} Current	50	μA max	DV_{DD} = 4.75 V to 5.25 V, Osc. On, TIC On
	20	μA max	DV_{DD} = 2.7 V to 3.6 V, Osc. On, TIC On
AV_{DD} Current	1	μA max	Measured at AV_{DD} = 5.25 V, Osc. On or Osc. Off
DV_{DD} Current	20	μA max	DV_{DD} = 4.75 V to 5.25 V, Osc. Off
	5	μA typ	DV_{DD} = 2.7 V to 3.6 V, Osc. Off
Typical Additional Power Supply Currents (AI_{DD} and DI_{DD})			Core CLK = 1.57 MHz, AV_{DD} = DV_{DD} = 5 V
PSM Peripheral	50	μA typ	
Primary ADC	1	mA typ	
Auxiliary ADC	500	μA typ	
DAC	150	μA typ	
Dual Current Sources	400	μA typ	

NOTES

[1]Temperature Range –40°C to +85°C.

[2]These numbers are not production tested but are guaranteed by Design and/or Characterization data on production release.

[3]The primary ADC is factory-calibrated at 25°C with AV_{DD} = DV_{DD} = 5 V yielding this full-scale error. If user power supply or temperature conditions are significantly different from these, an Internal Full-Scale Calibration will restore this error to this level.

[4]Gain Error Drift is a span drift. To calculate Full-Scale Error Drift, add the Offset Error Drift to the Gain Error Drift times the full-scale input.

[5]The auxiliary ADC is factory-calibrated at 25°C with AV_{DD} = DV_{DD} = 5 V yielding this full-scale error of –2.5 LSB. A system zero-scale and full-scale calibration will remove this error altogether.

[6]DAC linearity and AC Specifications are calculated using:
reduced code range of 48 to 4095, 0 to V_{REF}
reduced code range of 48 to 3995, 0 to V_{DD}.

[7]Gain Error is a measure of the span error of the DAC.

[8]In general terms, the bipolar input voltage range to the primary ADC is given by $Range_{ADC} = \pm(V_{REF}\ 2^{RN})/125$, where:
V_{REF} = REFIN(+) to REFIN(–) voltage and V_{REF} = 1.25 V when internal ADC V_{REF} is selected.
RN = decimal equivalent of RN2, RN1, RN0, e.g., V_{REF} = 2.5 V and RN2, RN1, RN0 = 1, 1, 0 the $Range_{ADC} = \pm 1.28$ V.
In unipolar mode the effective range is 0 V to 1.28 V in our example.

[9]1.25 V is used as the reference voltage to the ADC when internal V_{REF} is selected via XREF0 and XREF1 bits in ADC0CON and ADC1CON respectively.

[10]In bipolar mode, the Auxiliary ADC can only be driven to a minimum of A_{GND} – 30 mV as indicated by the Auxiliary ADC absolute AIN voltage limits. The bipolar range is still $-V_{REF}$ to $+V_{REF}$; however, the negative voltage is limited to –30 mV.

[11]Pins configured in I²C-compatible mode or SPI mode, pins configured as digital inputs during this test.

[12]Pins configured in I²C-compatible mode only.

[13]Flash/EE Memory Reliability Characteristics apply to both the Flash/EE program memory and Flash/EE data memory.

[14]Endurance is qualified to 100 Kcycles as per JEDEC Std. 22 method A117 and measured at –40°C, +25°C and +85°C, typical endurance at 25°C is 700 Kcycles.

[15]Retention lifetime equivalent at junction temperature (T_J) = 55°C as per JEDEC Std. 22, Method A117. Retention lifetime based on an activation energy of 0.6eV will derate with junction temperature as shown in Figure 27 in the Flash/EE Memory description section of this data sheet.

[16]Power Supply current consumption is measured in Normal, Idle, and Power-Down Modes under the following conditions:
Normal Mode: Reset = 0.4 V, Digital I/O pins = open circuit, Core Clk changed via CD bits in PLLCON, Core Executing internal software loop.
Idle Mode: Reset = 0.4 V, Digital I/O pins = open circuit, Core Clk changed via CD bits in PLLCON, PCON.0 = 1, Core Execution suspended in idle mode.
Power-Down Mode: Reset = 0.4 V, All P0 pins and P1.2–P1.7 pins = 0.4 V, All other digital I/O pins are open circuit, Core Clk changed via CD bits in PLLCON, PCON.1 = 1, Core Execution suspended in power-down mode, OSC turned ON or OFF via OSC_PD bit (PLLCON.7) in PLLCON SFR.

[17]DV_{DD} power supply current will typically increase by 3 mA (3 V operation) and 10 mA (5 V operation) during a Flash/EE memory program or erase cycle.

Specifications subject to change without notice

TIMING SPECIFICATIONS[1, 2, 3] (AV_{DD} = 2.7 V to 3.6 V or 4.75 V to 5.25 V, DV_{DD} = 2.7 V to 3.6 V or 4.75 V to 5.25 V; all specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter		32.768 kHz External Crystal Min	Typ	Max	Unit	Figure
CLOCK INPUT (External Clock Driven XTAL1)						
t_{CK}	XTAL1 Period		30.52		µs	1
t_{CKL}	XTAL1 Width Low		15.16		µs	1
t_{CKH}	XTAL1 Width High		15.16		µs	1
t_{CKR}	XTAL1 Rise Time		20		ns	1
t_{CKF}	XTAL1 Fall Time		20		ns	1
$1/t_{CORE}$	ADuC816 Core Clock Frequency[4]	0.098		12.58	MHz	
t_{CORE}	ADuC816 Core Clock Period[5]		0.636		µs	
t_{CYC}	ADuC816 Machine Cycle Time[6]	0.95	7.6	122.45	µs	

NOTES

[1]AC inputs during testing are driven at DV_{DD} – 0.5 V for a Logic 1, and 0.45 V for a Logic 0. Timing measurements are made at V_{IH} min for a Logic 1, and V_{IL} max for a Logic 0 as shown in Figure 2.

[2]For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs as shown in Figure 2.

[3]C_{LOAD} for Port0, ALE, $\overline{PSEN}$ outputs = 100 pF; C_{LOAD} for all other outputs = 80 pF unless otherwise noted.

[4]ADuC816 internal PLL locks onto a multiple (384 times) the external crystal frequency of 32.768 kHz to provide a Stable 12.583 MHz internal clock for the system. The core can operate at this frequency or at a binary submultiple called Core_Clk, selected via the PLLCON SFR.

[5]This number is measured at the default Core_Clk operating frequency of 1.57 MHz.

[6]ADuC816 Machine Cycle Time is nominally defined as 12/Core_CLK.

Specifications subject to change without notice.

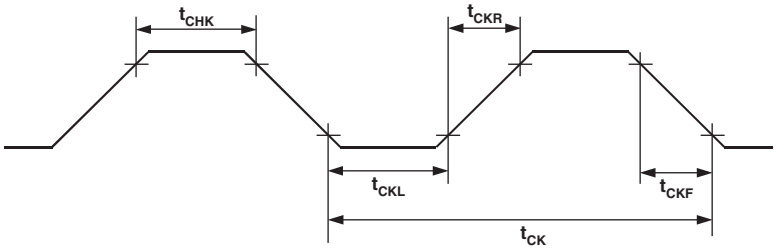

Figure 1. XTAL1 Input

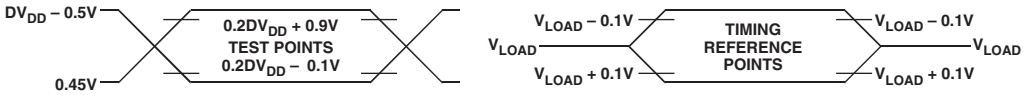

Figure 2. Timing Waveform Characteristics

Parameter		12.58 MHz Core_Clk Min	Max	Variable Core_Clk Min	Max	Unit	Figure
EXTERNAL DATA MEMORY WRITE CYCLE							
t_{WLWH}	$\overline{WR}$ Pulsewidth	377		$6t_{CORE} - 100$		ns	5
t_{AVLL}	Address Valid after ALE Low	39		$t_{CORE} - 40$		ns	5
t_{LLAX}	Address Hold after ALE Low	44		$t_{CORE} - 35$		ns	5
t_{LLWL}	ALE Low to $\overline{WR}$ Low	188	288	$3t_{CORE} - 50$	$3t_{CORE} + 50$	ns	5
t_{AVWL}	Address Valid to $\overline{WR}$ Low	188		$4t_{CORE} - 130$		ns	5
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	29		$t_{CORE} - 50$		ns	5
t_{QVWH}	Data Setup before $\overline{WR}$	406		$7t_{CORE} - 150$		ns	5
t_{WHQX}	Data and Address Hold after $\overline{WR}$	29		$t_{CORE} - 50$		ns	5
t_{WHLH}	$\overline{WR}$ High to ALE High	39	119	$t_{CORE} - 40$	$t_{CORE} + 40$	ns	5

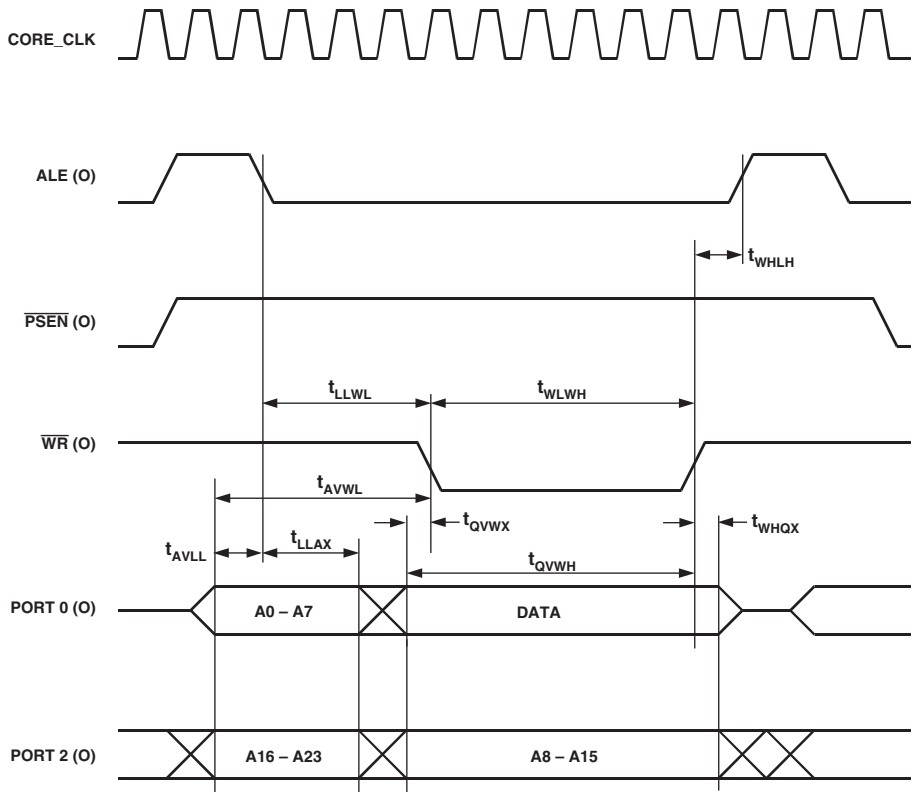

Figure 5. External Data Memory Write Cycle

Parameter		12.58 MHz Core_Clk Min	Typ	Max	Variable Core_Clk Min	Typ	Max	Unit	Figure
UART TIMING (Shift Register Mode)									
t_{XLXL}	Serial Port Clock Cycle Time		0.95			$2t_{CORE}$		µs	6
t_{QVXH}	Output Data Setup to Clock	662			$10t_{CORE} - 133$			ns	6
t_{DVXH}	Input Data Setup to Clock	292			$2t_{CORE} + 133$			ns	6
t_{XHDX}	Input Data Hold after Clock	0			0			ns	
t_{XHQX}	Output Data Hold after Clock	42			$2t_{CORE} - 117$			ns	6

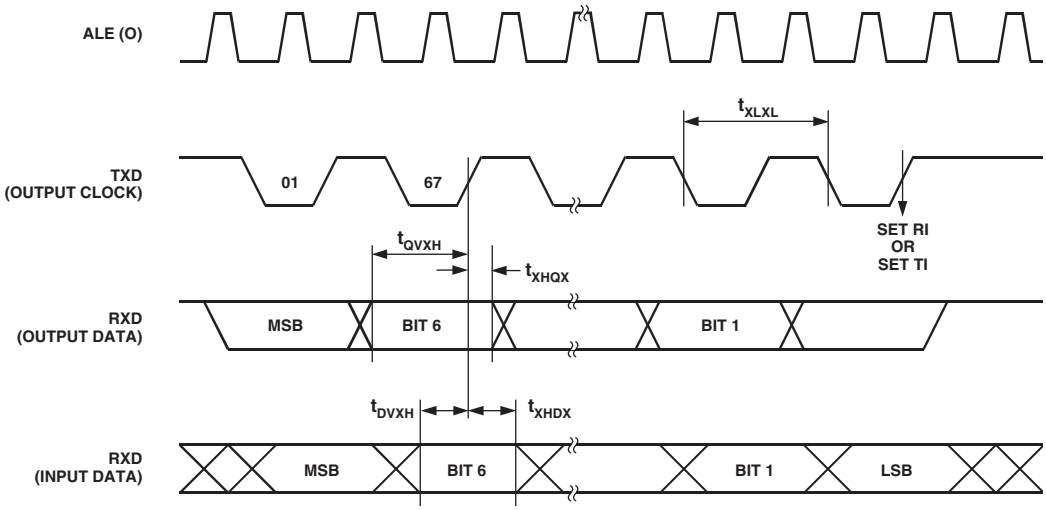

Figure 6. UART Timing in Shift Register Mode

Parameter		Min	Max	Unit	Figure
I^2C-COMPATIBLE INTERFACE TIMING					
t_L	SCLOCK Low Pulsewidth	4.7		μs	7
t_H	SCLOCK High Pulsewidth	4.0		μs	7
t_{SHD}	Start Condition Hold Time	0.6		μs	7
t_{DSU}	Data Setup Time	100		μs	7
t_{DHD}	Data Hold Time		0.9	μs	7
t_{RSU}	Setup Time for Repeated Start	0.6		μs	7
t_{PSU}	Stop Condition Setup Time	0.6		μs	7
t_{BUF}	Bus Free Time between a STOP Condition and a START Condition	1.3		μs	7
t_R	Rise Time of Both SCLOCK and SDATA		300	ns	7
t_F	Fall Time of Both SCLOCK and SDATA		300	ns	7
t_{SUP}*	Pulsewidth of Spike Suppressed		50	ns	7

*Input filtering on both the SCLOCK and SDATA inputs suppresses noise spikes less than 50 ns.

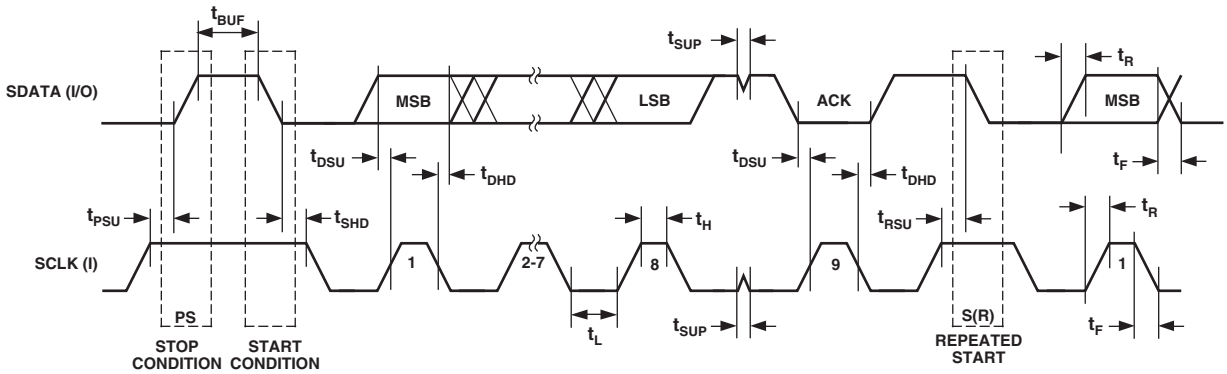

Figure 7. I^2C-Compatible Interface Timing

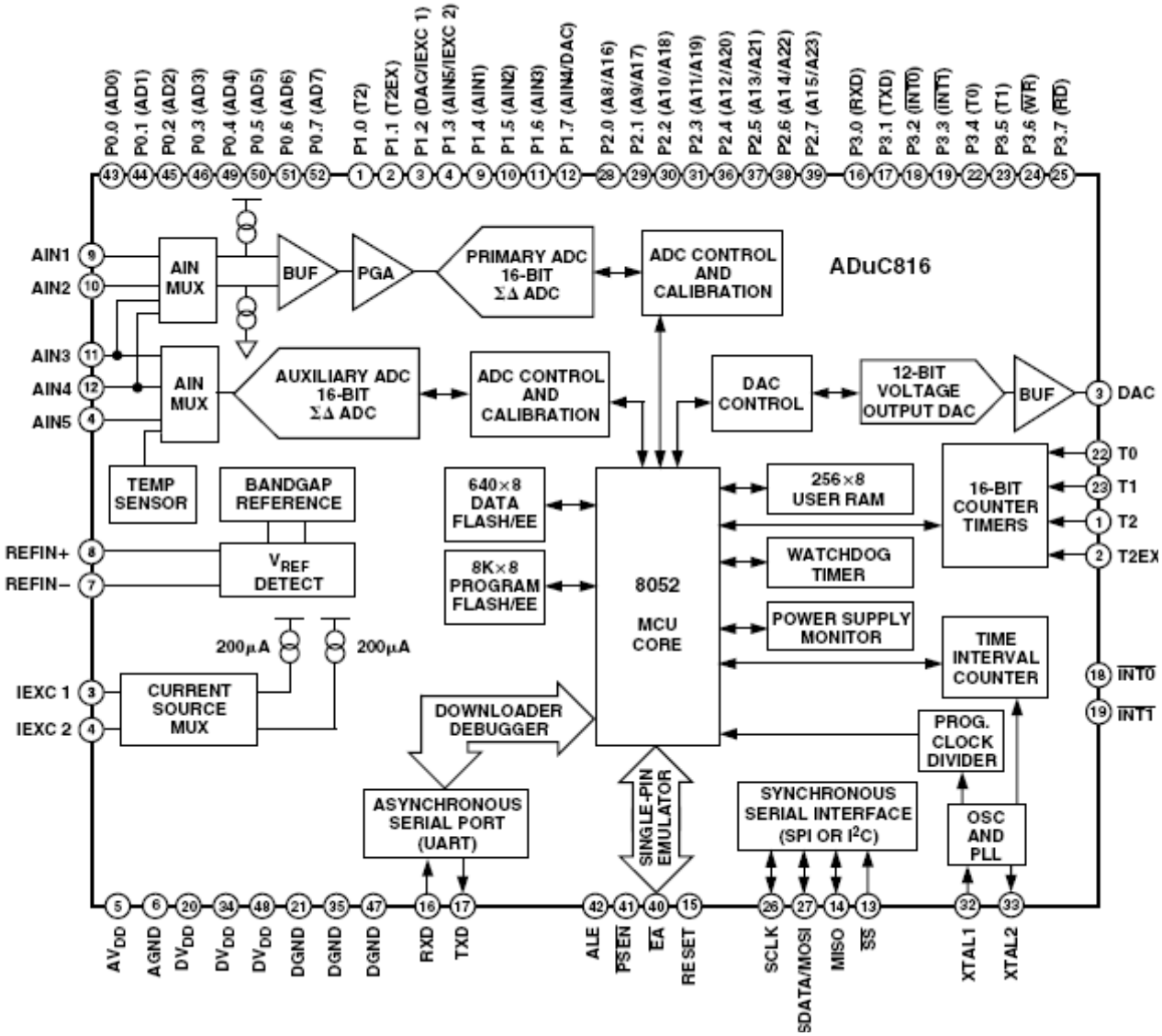

Figure 12. 52-MQFP Block Diagram

Reset initializes the stack pointer to location 07 hex and increments it once to start from locations 08 hex which is also the first register (R0) of register bank 1. Thus, if one is going to use more than one register bank, the stack pointer should be initialized to an area of RAM not used for data storage.

The SFR space is mapped to the upper 128 bytes of internal data memory space and accessed by direct addressing only. It provides an interface between the CPU and all on-chip peripherals. A block diagram showing the programming model of the ADuC816 via the SFR area is shown in Figure 16. A complete SFR map is shown in Figure 17.

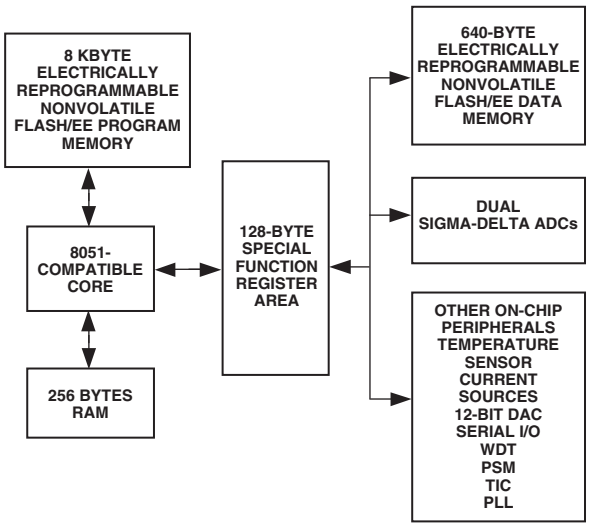

Figure 16. Programming Model

OVERVIEW OF MCU-RELATED SFRS

Accumulator SFR

ACC is the Accumulator register and is used for math operations including addition, subtraction, integer multiplication and division, and Boolean bit manipulations. The mnemonics for accumulator-specific instructions refer to the Accumulator as A.

B SFR

The B register is used with the ACC for multiplication and division operations. For other instructions it can be treated as a general-purpose scratchpad register.

Stack Pointer SFR

The SP register is the stack pointer and is used to hold an internal RAM address that is called the *"top of the stack."* The SP register is incremented before data is stored during PUSH and CALL executions. While the Stack may reside anywhere in on-chip RAM, the SP register is initialized to 07H after a reset. This causes the stack to begin at location 08H.

Data Pointer

The Data Pointer is made up of three 8-bit registers, named DPP (page byte), DPH (high byte) and DPL (low byte). These are used to provide memory addresses for internal and external code access and external data access. It may be manipulated as a 16-bit register (DPTR = DPH, DPL), although INC DPTR instructions will automatically carry over to DPP, or as three independent 8-bit registers (DPP, DPH, DPL).

Program Status Word SFR

The PSW register is the Program Status Word which contains several bits reflecting the current status of the CPU as detailed in Table I.

SFR Address	D0H
Power ON Default Value	00H
Bit Addressable	Yes

CY	AC	F0	RS1	RS0	OV	F1	P

Table I. PSW SFR Bit Designations

Bit	Name	Description		
7	CY	Carry Flag		
6	AC	Auxiliary Carry Flag		
5	F0	General-Purpose Flag		
4	RS1	Register Bank Select Bits		
3	RS0	RS1	RS0	Selected Bank
		0	0	0
		0	1	1
		1	0	2
		1	1	3
2	OV	Overflow Flag		
1	F1	General-Purpose Flag		
0	P	Parity Bit		

Power Control SFR

The Power Control (PCON) register contains bits for power-saving options and general-purpose status flags as shown in Table II.

SFR Address	87H
Power ON Default Value	00H
Bit Addressable	No

SMOD	SERIPD	INT0PD	ALEOFF	GF1	GF0	PD	IDL

Table II. PCON SFR Bit Designations

Bit	Name	Description
7	SMOD	Double UART Baud Rate
6	SERIPD	I^2C/SPI Power-Down Interrupt Enable
5	INT0PD	$\overline{INT0}$ Power-Down Interrupt Enable
4	ALEOFF	Disable ALE Output
3	GF1	General-Purpose Flag Bit
2	GF0	General-Purpose Flag Bit
1	PD	Power-Down Mode Enable
0	IDL	Idle Mode Enable

ADC1CON (Auxiliary ADC Control Register)

Used to configure the Auxiliary ADC for channel selection, external Ref enable and unipolar or bipolar coding. It should be noted that the Auxiliary ADC only operates on a fixed input range of $\pm V_{REF}$.

SFR Address D3H
Power-On Default Value 00H
Bit Addressable No

---	XREF1	ACH1	ACH0	UNI1	---	---	---

Table VI. ADC1CON SFR Bit Designations

Bit	Name	Description
7	---	Reserved for Future Use.
6	XREF1	Auxiliary ADC External Reference Bit. *Set* by user to enable the Auxiliary ADC to use the external reference via REFIN(+)/REFIN(–). *Cleared* by user to enable the Auxiliary ADC to use the internal bandgap reference.
5	ACH1	Auxiliary ADC Channel Selection Bits.
4	ACH0	Written by the user to select the single-ended input pins used to drive the Auxiliary ADC as follows: ACH1 ACH0 Positive Input Negative Input 0 0 AIN3 AGND 0 1 AIN4 AGND 1 0 Temp Sensor* AGND (Temp. Sensor routed to the ADC input) 1 1 AIN5 AGND
3	UNI1	Auxiliary ADC Unipolar Bit. *Set* by user to enable unipolar coding, i.e., zero input will result in 0000 hex output. *Cleared* by user to enable bipolar coding, zero input will result in 8000 hex output.
2	---	Reserved for Future Use.
1	---	Reserved for Future Use.
0	---	Reserved for Future Use.

*NOTES
1. When the temperature sensor is selected, user code must select internal reference via XREF1 bit above and clear the UNI1 bit (ADC1CON.3) to select bipolar coding.
2. The temperature sensor is factory calibrated to yield conversion results 8000H at 0°C.
3. A +1°C change in temperature will result in a +1 LSB change in the ADC1H register ADC conversion result.

SF (Sinc Filter Register)

The number in this register sets the decimation factor and thus the output update rate for the Primary and Auxiliary ADCs. This SFR cannot be written by user software while either ADC is active. The update rate applies to both Primary and Auxiliary ADCs and is calculated as follows:

$$f_{ADC} = \frac{1}{3} \cdot \frac{1}{8.SF} \cdot f_{MOD}$$

Where: f_{ADC} = ADC Output Update Rate
f_{MOD} = Modulator Clock Frequency = 32.768 kHz
SF = Decimal Value of SF Register

The allowable range for SF is 0Dhex to FFhex. Examples of SF values and corresponding conversion update rate (f_{ADC}) and conversion time (t_{ADC}) are shown in Table VII, the power-on default value for the SF register is 45 hex, resulting in a default ADC update rate of just under 20 Hz. Both ADC inputs are chopped to minimize offset errors, which means that the settling time for a single conversion or the time to a first conversion result in continuous conversion mode is $2 \times t_{ADC}$. As mentioned earlier, all calibration cycles will be carried out automatically with a maximum, i.e., FFhex, SF value to ensure optimum calibration performance. Once a calibration cycle has completed, the value in the SF register will be that programmed by user software.

Table VII. SF SFR Bit Designations

SF(dec)	SF(hex)	f_{ADC}(Hz)	t_{ADC}(ms)
13	0D	105.3	9.52
69	45	19.79	50.34
255	FF	5.35	186.77

ICON (Current Sources Control Register)
Used to control and configure the various excitation and burnout current source options available on-chip.

SFR Address D5H
Power-On Default Value 00H
Bit Addressable No

---	BO	ADC1IC	ADC0IC	I2PIN	I1PIN	I2EN	I1EN

Table VIII. ICON SFR Bit Designations

Bit	Name	Description
7	---	Reserved for Future Use.
6	BO	Burnout Current Enable Bit. *Set* by user to enable both transducer burnout current sources in the primary ADC signal paths. *Cleared* by user to disable both transducer burnout current sources.
5	ADC1IC	Auxiliary ADC Current Correction Bit. *Set* by user to allow scaling of the Auxiliary ADC by an internal current source calibration word.
4	ADC0IC	Primary ADC Current Correction Bit. *Set* by user to allow scaling of the Primary ADC by an internal current source calibration word.
3	I2PIN*	Current Source-2 Pin Select Bit. *Set* by user to enable current source-2 (200 μA) to external Pin 3 (P1.2/DAC/IEXC1). *Cleared* by user to enable current source-2 (200 μA) to external Pin 4 (P1.3/AIN5/IEXC2).
2	I1PIN*	Current Source-1 Pin Select Bit. *Set* by user to enable current source-1 (200 μA) to external Pin 4 (P1.3/AIN5/IEXC2). *Cleared* by user to enable current source-1 (200 μA) to external Pin 3 (P1.2/DAC/IEXC1).
1	I2EN	Current Source-2 Enable Bit. *Set* by user to turn on excitation current source-2 (200 μA). *Cleared* by user to turn off excitation current source-2 (200 μA).
0	I1EN	Current Source-1 Enable Bit. *Set* by user to turn on excitation current source-1 (200 μA). *Cleared* by user to turn off excitation current source-1 (200 μA).

*Both current sources can be enabled to the same external pin, yielding a 400 μA current source.

ADC0H/ADC0M (Primary ADC Conversion Result Registers)
These two 8-bit registers hold the 16-bit conversion result from the Primary ADC.

SFR Address	ADC0H	High Data Byte	DBH
	ADC0M	Middle Data Byte	DAH
Power-On Default Value	00H	Both Registers	
Bit Addressable	No	Both Registers	

ADC1H/ADC1L (Auxiliary ADC Conversion Result Registers)
These two 8-bit registers hold the 16-bit conversion result from the Auxiliary ADC.

SFR Address	ADC1H	High Data Byte	DDH
	ADC1L	Low Data Byte	DCH
Power-On Default Value	00H	Both Registers	
Bit Addressable	No	Both Registers	

Auxiliary ADC

The Auxiliary ADC is intended to convert supplementary inputs such as those from a cold junction diode or thermistor. This ADC is not buffered and has a fixed input range of 0 V to 2.5 V (assuming an external 2.5 V reference). The single-ended inputs can be driven from AIN3, AIN4 or AIN5 pins or directly from the on-chip temperature sensor voltage. A block diagram of the Auxiliary ADC is shown in Figure 19.

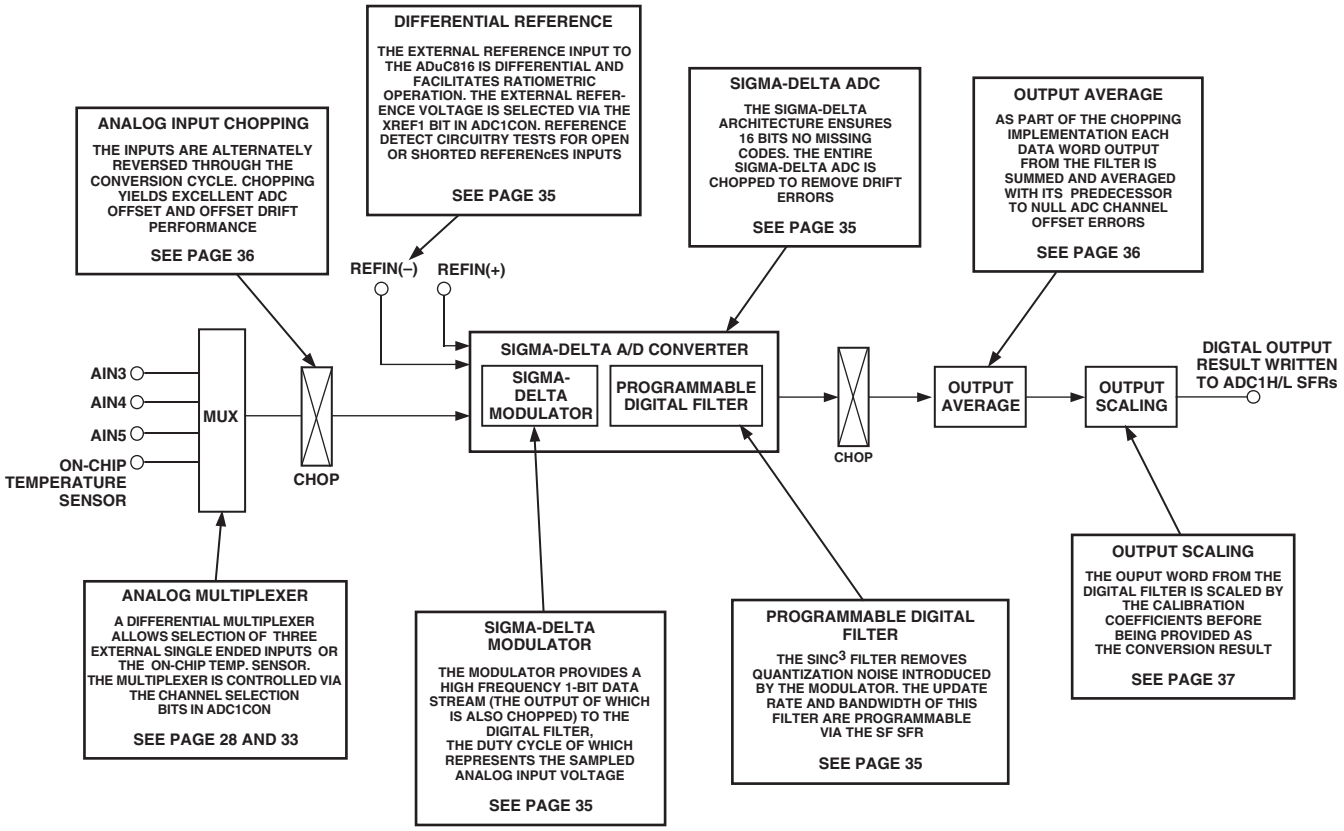

Figure 19. Auxiliary ADC Block Diagram

mended. Deriving the reference input voltage across an external resistor, as shown in Figure 52, will mean that the reference input sees a significant external source impedance. External decoupling on the REFIN(+) and REFIN(–) pins would not be recommended in this type of circuit configuration.

Reference Detect

The ADuC816 includes on-chip circuitry to detect if the part has a valid reference for conversions or calibrations. If the voltage between the external REFIN(+) and REFIN(–) pins goes below 0.3 V or either the REFIN(+) or REFIN(–) inputs is open circuit, the ADuC816 detects that it no longer has a valid reference. In this case, the NOXREF bit of the ADCSTAT SFR is set to a 1. If the ADuC816 is performing normal conversions and the NOXREF bit becomes active, the conversion results revert to all 1s. Therefore, it is not necessary to continuously monitor the status of the NOXREF bit when performing conversions. It is only necessary to verify its status if the conversion result read from the ADC Data Register is all 1s.

If the ADuC816 is performing either an offset or gain calibration and the NOXREF bit becomes active, the updating of the respective calibration registers is inhibited to avoid loading incorrect coefficients to these registers, and the appropriate ERR0 or ERR1 bits in the ADCSTAT SFR are set. If the user is concerned about verifying that a valid reference is in place every time a calibration is performed, the status of the ERR0 or ERR1 bit should be checked at the end of the calibration cycle.

Sigma-Delta Modulator

A sigma-delta ADC generally consists of two main blocks, an analog modulator and a digital filter. In the case of the ADuC816 ADCs, the analog modulators consist of a difference amplifier, an integrator block, a comparator, and a feedback DAC as illustrated in Figure 20.

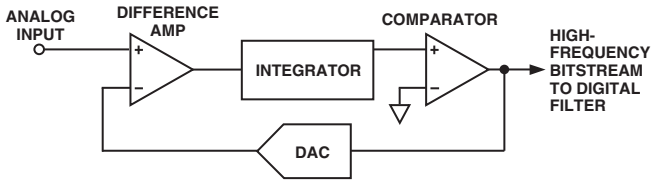

Figure 20. Sigma-Delta Modulator Simplified Block Diagram

In operation, the analog signal sample is fed to the difference amplifier along with the output of the feedback DAC. The difference between these two signals is integrated and fed to the comparator. The output of the comparator provides the input to the feedback DAC so the system functions as a negative feedback loop that tries to minimize the difference signal. The digital data that represents the analog input voltage is contained in the duty cycle of the pulse train appearing at the output of the comparator. This duty cycle data can be recovered as a data word using a subsequent digital filter stage. The sampling frequency of the modulator loop is many times higher than the bandwidth of the input signal. The integrator in the modulator shapes the quantization noise (which results from the analog-to-digital conversion) so that the noise is pushed toward one-half of the modulator frequency.

Digital Filter

The output of the sigma-delta modulator feeds directly into the digital filter. The digital filter then band-limits the response to a frequency significantly lower than one-half of the modulator frequency. In this manner, the 1-bit output of the comparator is translated into a band-limited, low noise output from the ADuC816 ADCs.

The ADuC816 filter is a low-pass, $Sinc^3$ or $(sinx/x)^3$ filter whose primary function is to remove the quantization noise introduced at the modulator. The cutoff frequency and decimated output data rate of the filter are programmable via the SF (Sinc Filter) SFR as described in Table VII.

Figure 21 shows the frequency response of the ADC channel at the default SF word of 69 dec or 45 hex, yielding an overall output update rate of just under 20 Hz.

It should be noted that this frequency response allows frequency components higher than the ADC Nyquist frequency to pass through the ADC, in some cases without significant attenuation. These components may, therefore, be aliased and appear in-band after the sampling process.

It should also be noted that rejection of mains-related frequency components, i.e., 50 Hz and 60 Hz, is seen to be at level of >65 dB at 50 Hz and >100 dB at 60 Hz. This confirms the data sheet specifications for 50 Hz/60 Hz Normal Mode Rejection (NMR) at a 20 Hz update rate.

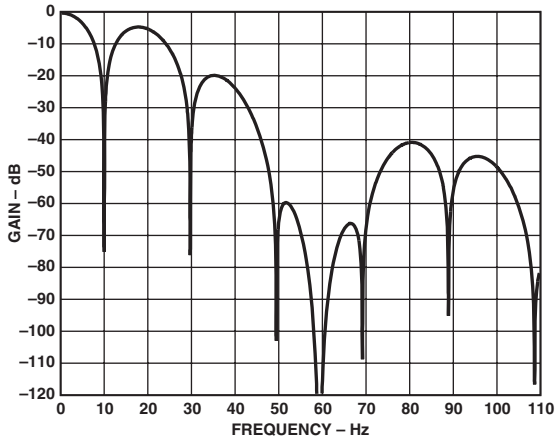

Figure 21. Filter Response, SF = 69 dec

The response of the filter, however, will change with SF word as can be seen in Figure 22, which shows >90 dB NMR at 50 Hz and >70 dB NMR at 60 Hz when SF = 255 dec.

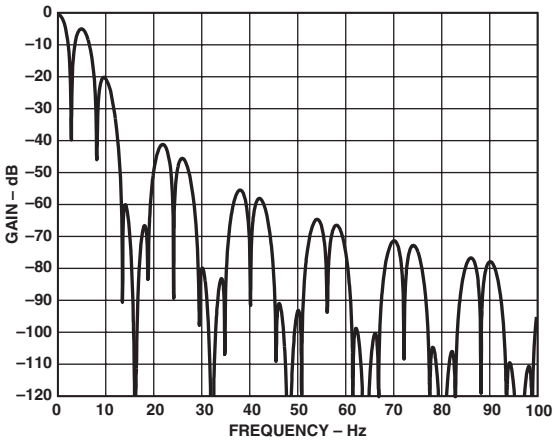

Figure 22. Filter Response, SF = 255 dec

Serial Safe Mode

This mode disables serial download capability on the device. If Serial Safe mode is activated and an attempt is made to reset the part into serial download mode, i.e., RESET asserted and deasserted with $\overline{\text{PSEN}}$ low, the part will interpret the serial download reset as a normal reset only. It will, therefore, not enter serial download mode but only execute a normal reset sequence. Serial Safe mode can only be disabled by initiating a code-erase command in parallel programming mode.

Using the Flash/EE Data Memory

The user Flash/EE data memory array consists of 640 bytes that are configured into 160 (00H to 9FH) 4-byte pages as shown in Figure 29.

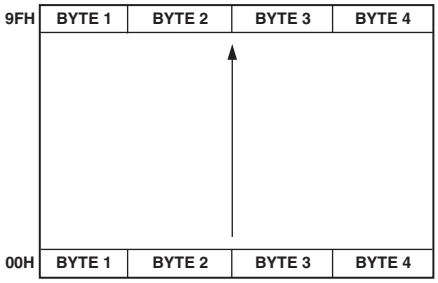

Figure 29. Flash/EE Data Memory Configuration

As with other ADuC816 user-peripheral circuits, the interface to this memory space is via a group of registers mapped in the SFR space. A group of four data registers (EDATA1–4) are used to hold 4-byte page data just accessed. EADRL is used to hold the 8-bit address of the page to be accessed. Finally, ECON is an 8-bit control register that may be written with one of five Flash/EE memory access commands to trigger various read, write, erase, and verify functions. These registers can be summarized as follows:

ECON: SFR Address: B9H
Function: Controls access to 640 Bytes Flash/EE Data Space.
Default: 00H

EADRL: SFR Address: C6H
Function: Holds the Flash/EE Data Page Address. (640 Bytes => 160 Page Addresses.)
Default: 00H

EDATA 1–4:
SFR Address: BCH to BFH respectively
Function: Holds Flash/EE Data memory page write or page read data bytes.
Default : EDATA1–2 –> 00H
EDATA3–4 –> 00H

A block diagram of the SFR interface to the Flash/EE Data Memory array is shown in Figure 30.

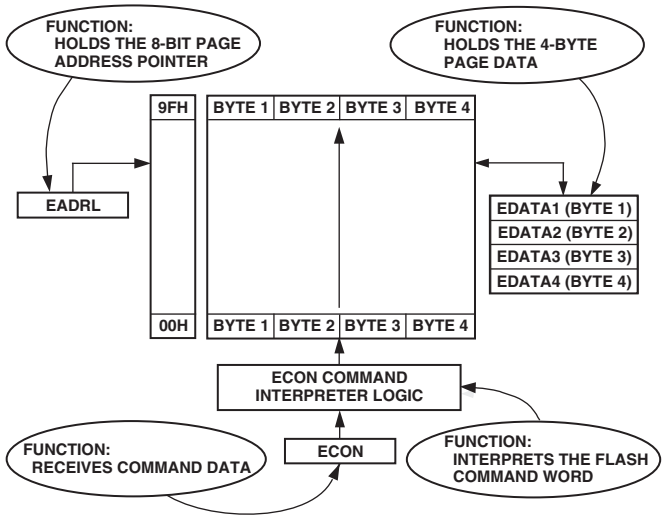

Figure 30. Flash/EE Data Memory Control and Configuration

ECON—Flash/EE Memory Control SFR

This SFR acts as a command interpreter and may be written with one of five command modes to enable various read, program and erase cycles as detailed in Table XIII:

Table XIII. ECON–Flash/EE Memory Control Register Command Modes

Command Byte	Command Mode
01H	READ COMMAND. Results in four bytes being read into EDATA1–4 from memory page address contained in EADRL.
02H	PROGRAM COMMAND. Results in four bytes (EDATA1–4) being written to memory page address in EADRL. This write command assumes the designated "write" page has been pre-erased.
03H	RESERVED FOR INTERNAL USE. 03H should not be written to the ECON SFR.
04H	VERIFY COMMAND. Allows the user to verify if data in EDATA1–4 is contained in page address designated by EADRL. A subsequent read of the ECON SFR will result in a "zero" being read if the verification is valid, a nonzero value will be read to indicate an invalid verification.
05H	ERASE COMMAND. Results in an erase of the 4-byte page designated in EADRL.
06H	ERASE-ALL COMMAND. Results in erase of the full Flash/EE Data memory 160-page (640 bytes) array.
07H to FFH	RESERVED COMMANDS. Commands reserved for future use.

Flash/EE Memory Timing
The typical program/erase times for the Flash/EE Data Memory are:

Erase Full Array (640 Bytes) – 2 ms
Erase Single Page (4 Bytes) – 2 ms
Program Page (4 Bytes) – 250 μs
Read Page (4 Bytes) – Within Single Instruction Cycle

Using the Flash/EE Memory Interface
As with all Flash/EE memory architectures, the array can be programmed in-system at a byte level, although it must be erased first; the erasure being performed in page blocks (4-byte pages in this case).

A typical access to the Flash/EE Data array will involve setting up the page address to be accessed in the EADRL SFR, configuring the EDATA1–4 with data to be programmed to the array (the EDATA SFRs will not be written for read accesses) and finally, writing the ECON command word which initiates one of the six modes shown in Table XIII.

It should be noted that a given mode of operation is initiated as soon as the command word is written to the ECON SFR. The core microcontroller operation on the ADuC816 is idled until the requested Program/Read or Erase mode is completed.

In practice, this means that even though the Flash/EE memory mode of operation is typically initiated with a two-machine cycle MOV instruction (to write to the ECON SFR), the next instruction will not be executed until the Flash/EE operation is complete (250 μs or 2 ms later). This means that the core will not respond to Interrupt requests until the Flash/EE operation is complete, although the core peripheral functions like Counter/Timers will continue to count and time as configured throughout this period.

Erase-All
Although the 640-byte User Flash/EE array is shipped from the factory pre-erased, i.e., Byte locations set to FFH, it is nonetheless good programming practice to include an erase-all routine as part of any configuration/setup code running on the ADuC816. An "ERASE-ALL" command consists of writing "06H" to the ECON SFR, which initiates an erase of all 640 byte locations in the Flash/EE array. This command coded in 8051 assembly would appear as:

```
MOV ECON, #06H    ; Erase all Command
                  ; 2 ms Duration
```

Program a Byte
In general terms, a byte in the Flash/EE array can only be programmed if it has previously been erased. To be more specific, a byte can only be programmed if it already holds the value FFH. Because of the Flash/EE architecture, this erasure must happen at a page level; therefore, a minimum of four bytes (1 page) will be erased when an erase command is initiated.

A more specific example of the Program-Byte process is shown below. In this example the user writes F3H into the second byte on Page 03H of the Flash/EE Data Memory space while preserving the other three bytes already in this page. As the user is only required to modify one of the page bytes, the full page must be first read so that this page can then be erased without the existing data being lost.

This example, coded in 8051 assembly, would appear as:

```
MOV EADRL,#03H   ; Set Page Address Pointer
MOV ECON,#01H    ; Read Page
MOV EDATA2,#0F3H ; Write New Byte
MOV ECON,#05H    ; Erase Page
MOV ECON,#02H    ; Write Page (Program Flash/EE)
```

Power Supply Monitor

As its name suggests, the Power Supply Monitor, once enabled, monitors both supplies (AVDD or DVDD) on the ADuC816. It will indicate when any of the supply pins drop below one of four user-selectable voltage trip points from 2.63 V to 4.63 V. For correct operation of the Power Supply Monitor function, AV_{DD} must be equal to or greater than 2.7 V. Monitor function is controlled via the PSMCON SFR. If enabled via the IEIP2 SFR, the monitor will interrupt the core using the PSMI bit in the PSMCON SFR. This bit will not be cleared until the failing power supply has returned above the trip point for at least 250 ms. This monitor function allows the user to save working registers to avoid possible data loss due to the low supply condition, and also ensures that normal code execution will not resume until a safe supply level has been well established. The supply monitor is also protected against spurious glitches triggering the interrupt circuit.

PSMCON **Power Supply Monitor Control Register**

SFR Address DFH
Power-On Default Value DEH
Bit Addressable No

CMPD	CMPA	PSMI	TPD1	TPD0	TPA1	TPA0	PSMEN

Table XVIII. PSMCON SFR Bit Designations

Bit	Name	Description
7	CMPD	DVDD Comparator Bit. This is a read-only bit and directly reflects the state of the DVDD comparator. Read "1" indicates the DVDD supply is above its selected trip point. Read "0" indicates the DVDD supply is below its selected trip point.
6	CMPA	AVDD Comparator Bit. This is a read-only bit and directly reflects the state of the AVDD comparator. Read "1" indicates the AVDD supply is above its selected trip point. Read "0" indicates the AVDD supply is below its selected trip point.
5	PSMI	Power Supply Monitor Interrupt Bit. This bit will be set high by the MicroConverter if either CMPA or CMPD are low, indicating low analog or digital supply. The PSMI bit can be used to interrupt the processor. Once CMPD and/or CMPA return (and remain) high, a 250 ms counter is started. When this counter times out, the PSMI interrupt is cleared. PSMI can also be written by the user. However, if either comparator output is low, it is not possible for the user to clear PSMI.
4	TPD1	DVDD Trip Point Selection Bits.
3	TPD0	These bits select the DVDD trip-point voltage as follows: TPD1 TPD0 Selected DVDD Trip Point (V) 0 0 4.63 0 1 3.08 1 0 2.93 1 1 2.63
2	TPA1	AVDD Trip Point Selection Bits.
1	TPA0	These bits select the AVDD trip-point voltage as follows: TPA1 TPA0 Selected AVDD Trip Point (V) 0 0 4.63 0 1 3.08 1 0 2.93 1 1 2.63
0	PSMEN	Power Supply Monitor Enable Bit. *Set* to "1" by the user to enable the Power Supply Monitor Circuit. *Cleared* to "0" by the user to disable the Power Supply Monitor Circuit.

8051-COMPATIBLE ON-CHIP PERIPHERALS

This section gives a brief overview of the various secondary peripheral circuits are also available to the user on-chip. These remaining functions are fully 8051-compatible and are controlled via standard 8051 SFR bit definitions.

Parallel I/O Ports 0–3

The ADuC816 uses four input/output ports to exchange data with external devices. In addition to performing general-purpose I/O, some ports are capable of external memory operations; others are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

Port 0 is an 8-bit open drain bidirectional I/O port that is directly controlled via the Port 0 SFR (SFR address = 80 hex). Port 0 pins that have 1s written to them via the Port 0 SFR will be configured as open drain and will therefore float. In that state, Port 0 pins can be used as high impedance inputs. An external pull-up resistor will be required on Port 0 outputs to force a valid logic high level externally. Port 0 is also the multiplexed low-order address and data bus during accesses to external program or data memory. In this application it uses strong internal pull-ups when emitting 1s.

Port 1 is also an 8-bit port directly controlled via the P1 SFR (SFR address = 90 hex). The Port 1 pins are divided into two distinct pin groupings.

P1.0 and P1.1 pins on Port 1 are bidirectional digital I/O pins with internal pull-ups. If P1.0 and P1.1 have 1s written to them via the P1 SFR, these pins are pulled high by the internal pull-up resistors. In this state they can also be used as inputs; as input pins being externally pulled low, they will source current because of the internal pull-ups. With 0s written to them, both these pins will drive a logic low output voltage (VOL) and will be capable of sinking 10 mA compared to the standard 1.6 mA sink capability on the other port pins. These pins also have various secondary functions described in Table XXI.

Table XXI. Port 1, Alternate Pin Functions

Pin	Alternate Function
P1.0	T2 (Timer/Counter 2 External Input)
P1.1	T2EX (Timer/Counter 2 Capture/Reload Trigger)

The remaining Port 1 pins (P1.2–P1.7) can only be configured as Analog Input (ADC), Analog Output (DAC) or Digital Input pins. By (power-on) default these pins are configured as Analog Inputs, i.e., "1" written in the corresponding Port 1 register bit. To configure any of these pins as digital inputs, the user should write a "0" to these port bits to configure the corresponding pin as a high impedance digital input.

Port 2 is a bidirectional port with internal pull-up resistors directly controlled via the P2 SFR (SFR address = A0 hex). Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors and, in that state, they can be used as inputs. As inputs, Port 2 pins being pulled externally low will source current because of the internal pull-up resistors. Port 2 emits the high order address bytes during fetches from external program memory and middle and high order address bytes during accesses to the 16-bit external data memory space.

Port 3 is a bidirectional port with internal pull-ups directly controlled via the P2 SFR (SFR address = B0 hex). Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and in that state they can be used as inputs. As inputs, Port 3 pins being pulled externally low will source current because of the internal pull-ups. Port 3 pins also have various secondary functions described in Table XXII.

Table XXII. Port 3, Alternate Pin Functions

Pin	Alternate Function
P3.0	RXD (UART Input Pin) (or Serial Data I/O in Mode 0)
P3.1	TXD (UART Output Pin) (or Serial Clock Output in Mode 0)
P3.2	$\overline{\text{INT0}}$ (External Interrupt 0)
P3.3	$\overline{\text{INT1}}$ (External Interrupt 1)
P3.4	T0 (Timer/Counter 0 External Input)
P3.5	T1 (Timer/Counter 1 External Input)
P3.6	$\overline{\text{WR}}$ (External Data Memory Write Strobe)
P3.7	$\overline{\text{RD}}$ (External Data Memory Read Strobe)

The alternate functions of P1.0, P1.1, and Port 3 pins can only be activated if the corresponding bit latch in the P1 and P3 SFRs contains a 1. Otherwise, the port pin is stuck at 0.

Timers/Counters

The ADuC816 has three 16-bit Timer/Counters: Timer 0, Timer 1, and Timer 2. The Timer/Counter hardware has been included on-chip to relieve the processor core of the overhead inherent in implementing timer/counter functionality in software. Each Timer/Counter consists of two 8-bit registers THx and TLx (x = 0, 1 and 2). All three can be configured to operate either as timers or event counters.

In "Timer" function, the TLx register is incremented every machine cycle. Thus one can think of it as counting machine cycles. Since a machine cycle consists of 12 core clock periods, the maximum count rate is 1/12 of the core clock frequency.

In "Counter" function, the TLx register is incremented by a 1-to-0 transition at its corresponding external input pin, T0, T1, or T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since it takes two machine cycles (16 core clock periods) to recognize a 1-to-0 transition, the maximum count rate is 1/16 of the core clock frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it must be held for a minimum of one full machine cycle. Remember that the core clock frequency is programmed via the CD0–2 selection bits in the PLLCON SFR.

User configuration and control of all Timer operating modes is achieved via three SFRs namely:

TMOD, TCON: Control and configuration for Timers 0 and 1.
T2CON: Control and configuration for Timer 2.

TMOD **Timer/Counter 0 and 1 Mode Register**
SFR Address 89H
Power-On Default Value 00H
Bit Addressable No

Gate	C/$\overline{T}$	M1	M0	Gate	C/$\overline{T}$	M1	M0

Table XXIII. TMOD SFR Bit Designations

Bit	Name	Description
7	Gate	Timer 1 Gating Control. *Set* by software to enable timer/counter 1 only while $\overline{INT1}$ pin is high and TR1 control bit is set. *Cleared* by software to enable timer 1 whenever TR1 control bit is set.
6	C/$\overline{T}$	Timer 1 Timer or Counter Select Bit. *Set* by software to select counter operation (input from T1 pin). *Cleared* by software to select timer operation (input from internal system clock).
5	M1	Timer 1 Mode Select Bit 1 (Used with M0 Bit).
4	M0	Timer 1 Mode Select Bit 0. M1 M0 0 0 TH1 operates as an 8-bit timer/counter. TL1 serves as 5-bit prescaler. 0 1 16-Bit Timer/Counter. TH1 and TL1 are cascaded; there is no prescaler. 1 0 8-Bit Auto-Reload Timer/Counter. TH1 holds a value which is to be reloaded into TL1 each time it overflows. 1 1 Timer/Counter 1 Stopped.
3	Gate	Timer 0 Gating Control. *Set* by software to enable timer/counter 0 only while $\overline{INT0}$ pin is high and TR0 control bit is set. *Cleared* by software to enable Timer 0 whenever TR0 control bit is set.
2	C/$\overline{T}$	Timer 0 Timer or Counter Select Bit. *Set* by software to select counter operation (input from T0 pin). *Cleared* by software to select timer operation (input from internal system clock).
1	M1	Timer 0 Mode Select Bit 1.
0	M0	Timer 0 Mode Select Bit 0. M1 M0 0 0 TH0 operates as an 8-bit timer/counter. TL0 serves as 5-bit prescaler. 0 1 16-Bit Timer/Counter. TH0 and TL0 are cascaded; there is no prescaler 1 0 8-Bit Auto-Reload Timer/Counter. TH0 holds a value which is to be reloaded into TL0 each time it overflows. 1 1 TL0 is an 8-bit timer/counter controlled by the standard timer 0 control bits. TH0 is an 8-bit timer only, controlled by Timer 1 control bits.

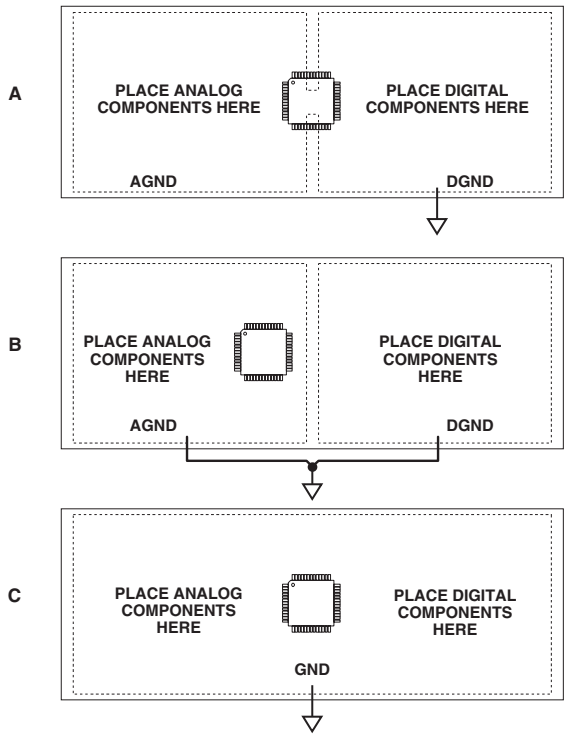

Figure 51. System Grounding Schemes

In all of these scenarios, and in more complicated real-life applications, keep in mind the flow of current from the supplies and back to ground. Make sure the return paths for all currents are as close as possible to the paths the currents took to reach their destinations. For example, do not power components on the analog side of Figure 51b with DV_{DD} since that would force return currents from DV_{DD} to flow through AGND. Also, try to avoid digital currents flowing under analog circuitry, which could happen if the user placed a noisy digital chip on the left half of the board in Figure 51c. Whenever possible, avoid large discontinuities in the ground plane(s) (such as are formed by a long trace on the same layer), since they force return signals to travel a longer path. And of course, make all connections to the ground plane directly, with little or no trace separating the pin from its via to ground.

If the user plans to connect fast logic signals (rise/fall time < 5 ns) to any of the ADuC816's digital inputs, add a series resistor to each relevant line to keep rise and fall times longer than 5 ns at the ADuC816 input pins. A value of 100 Ω or 200 Ω is usually sufficient to prevent high-speed signals from coupling capacitively into the ADuC816 and affecting the accuracy of ADC conversions.

ADuC816 System Self-Identification

In some hardware designs it may be an advantage for the software running on the ADuC816 target to identify the host MicroConverter. For example, code running on the ADuC816 may be used at future date to run on an ADuC816 MicroConverter host and the code may be required to operate differently.

The CHIPID SFR is a read-only register located at SFR address C2 hex. The top nibble of this byte is set to "1" to designate an ADuC824 host. For an ADuC824 host, the CHIPID SFR will contain the value "0" in the upper nibble.

OTHER HARDWARE CONSIDERATIONS

To facilitate in-circuit programming, plus in-circuit debug and emulation options, users will want to implement some simple connection points in their hardware that will allow easy access to download, debug, and emulation modes.

In-Circuit Serial Download Access

Nearly all ADuC816 designs will want to take advantage of the in-circuit reprogrammability of the chip. This is accomplished by a connection to the ADuC816's UART, which requires an external RS-232 chip for level translation if downloading code from a PC. Basic configuration of an RS-232 connection is illustrated in Figure 52 with a simple ADM202-based circuit. If users would rather not design an RS-232 chip onto a board, refer to the application note "uC006–A 4-Wire UART-to-PC Interface"[1] for a simple (and zero-cost-per-board) method of gaining in-circuit serial download access to the ADuC816.

NOTE
[1]Application note uC006 is available at www.analog.com/microconverter

In addition to the basic UART connections, users will also need a way to trigger the chip into download mode. This is accomplished via a 1 kΩ pull-down resistor that can be jumpered onto the $\overline{\text{PSEN}}$ pin, as shown in Figure 52. To get the ADuC816 into download mode, simply connect this jumper and power-cycle the device (or manually reset the device, if a manual reset button is available) and it will be ready to receive a new program serially. With the jumper removed, the device will come up in normal mode (and run the program) whenever power is cycled or RESET is toggled.

Note that $\overline{\text{PSEN}}$ is normally an output (as described in the External Memory Interface section) and it is sampled as an input only on the falling edge of RESET (i.e., at power-up or upon an external manual reset). Note also that if any external circuitry unintentionally pulls $\overline{\text{PSEN}}$ low during power-up or reset events, it could cause the chip to enter download mode and therefore fail to begin user code execution as it should. To prevent this, ensure that no external signals are capable of pulling the $\overline{\text{PSEN}}$ pin low, except for the external $\overline{\text{PSEN}}$ jumper itself.

Embedded Serial Port Debugger

From a hardware perspective, entry to serial port debug mode is identical to the serial download entry sequence described above. In fact, both serial download and serial port debug modes can be thought of as essentially one mode of operation used in two different ways.

Note that the serial port debugger is fully contained on the ADuC816 device, (unlike "ROM monitor" type debuggers) and therefore no external memory is needed to enable in-system debug sessions.

Single-Pin Emulation Mode

Also built into the ADuC816 is a dedicated controller for single-pin in-circuit emulation (ICE) using standard production ADuC816 devices. In this mode, emulation access is gained by connection to a single pin, the $\overline{\text{EA}}$ pin. Normally, this pin is hardwired either high or low to select execution from internal or external program memory space, as described earlier. To enable single-pin emulation mode, however, users will need to pull the $\overline{\text{EA}}$ pin high through a 1 kΩ resistor as shown in Figure 52. The emulator will then connect to the 2-pin header also shown in Figure 52. To be compatible with the standard connector that

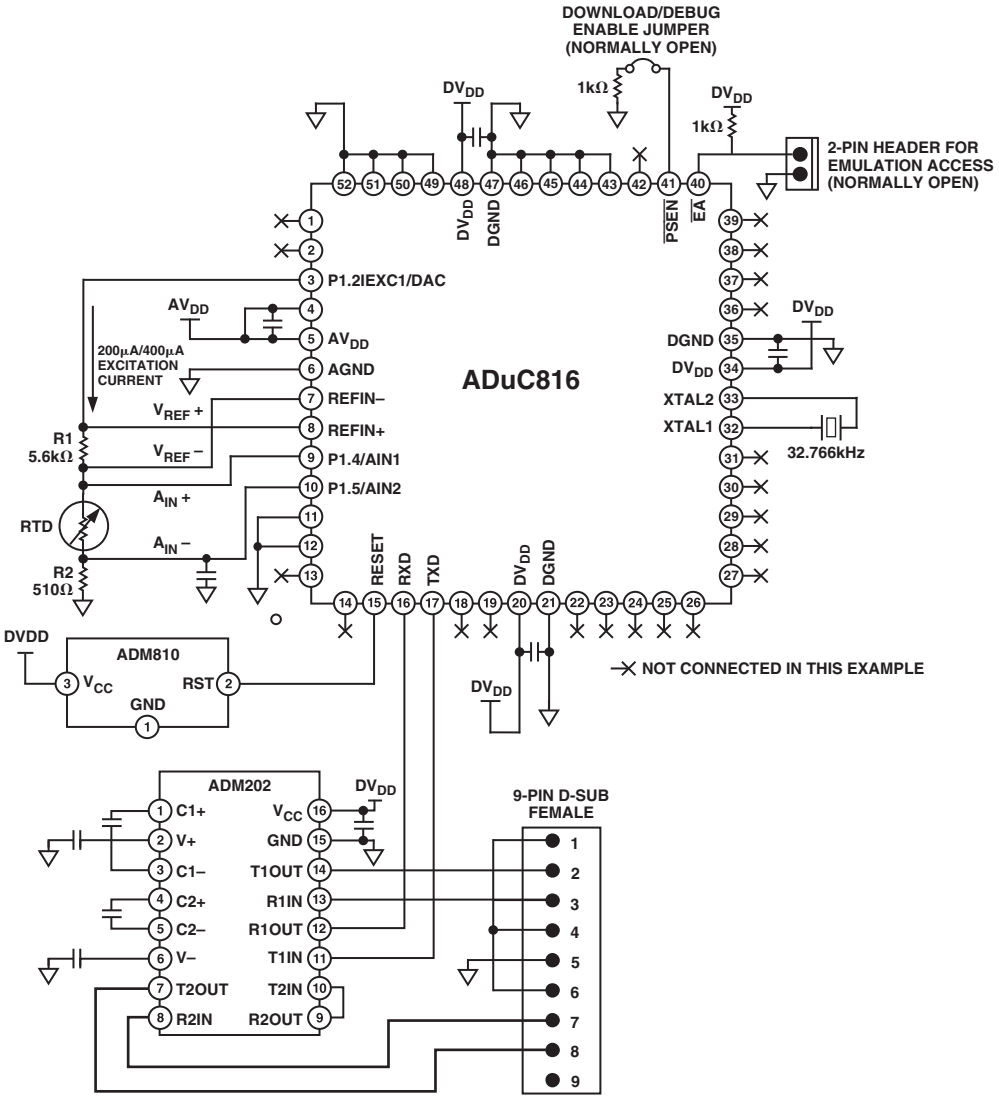

Figure 52. Typical System Configuration

comes with the single-pin emulator available from Accutron Limited (www.accutron.com), use a 2-pin 0.1-inch pitch "Friction Lock" header from Molex (www.molex.com) such as their part number 22-27-2021. Be sure to observe the polarity of this header. As represented in Figure 52, when the Friction Lock tab is at the right, the ground pin should be the lower of the two pins (when viewed from the top).

Enhanced-Hooks Emulation Mode

ADuC816 also supports enhanced-hooks emulation mode. An enhanced-hooks-based emulator is available from Metalink Corporation (www.metaice.com). No special hardware support for these emulators needs to be designed onto the board since these are "pod-style" emulators where users must replace the chip on their board with a header device that the emulator pod plugs into. The only hardware concern is then one of determining if adequate space is available for the emulator pod to fit into the system enclosure.

Typical System Configuration

A typical ADuC816 configuration is shown in Figure 52. It summarizes some of the hardware considerations discussed in the previous paragraphs.

Figure 52 also includes connections for a typical analog measurement application of the ADuC816, namely an interface to an RTD (Resistive Temperature Device). The arrangement shown is commonly referred to as a 4-wire RTD configuration.

Here, the on-chip excitation current sources are enabled to excite the sensor. An external differential reference voltage is generated by the current sourced through resistor R1. This current also flows directly through the RTD, which generates a differential voltage directly proportional to temperature. This differential voltage is routed directly to the positive and negative inputs of the primary ADC (AIN1, AIN2 respectively). A second external resistor, R2, is used to ensure that absolute analog input voltage on the negative input to the primary ADC stays within that specified for the ADuC816, i.e., AGND + 100 mV.