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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8052
Core Size	8-Bit
Speed	12.58MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	PSM, Temp Sensor, WDT
Number of I/O	34
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	640 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 7x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-QFP
Supplier Device Package	52-MQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc816bsz

Parameter	ADuC816BS	Unit	Test Conditions/Comments
TRANSDUCER BURNOUT CURRENT SOURCES			
AIN+ Current	–100	nA typ	AIN+ is the Selected Positive Input to the Primary ADC
AIN– Current	+100	nA typ	AIN– is the Selected Negative Input the Auxiliary ADC
Initial Tolerance @ 25°C Drift	±10	% typ	
Drift	0.03	%/°C typ	
EXCITATION CURRENT SOURCES			
Output Current	–200	µA typ	Available from Each Current Source
Initial Tolerance @ 25°C	±10	% typ	
Drift	200	ppm/°C typ	
Initial Current Matching @ 25°C	±1	% typ	Matching Between Both Current Sources
Drift Matching	20	ppm/°C typ	
Line Regulation (AV_{DD})	1	µA/V typ	AV_{DD} = 5 V + 5%
Load Regulation	0.1	µA/V typ	
Output Compliance	AV_{DD} – 0.6 AGND	V max min	
LOGIC INPUTS			
All Inputs Except SCLOCK, RESET, and XTAL1			
V_{INL}, Input Low Voltage	0.8	V max	DV_{DD} = 5 V
	0.4	V max	DV_{DD} = 3 V
V_{INH}, Input High Voltage	2.0	V min	
SCLOCK and RESET Only (Schmitt-Triggered Inputs)[2]			
V_{T+}	1.3/3	V min/V max	DV_{DD} = 5 V
	0.95/2.5	V min/V max	DV_{DD} = 3 V
V_{T-}	0.8/1.4	V min/V max	DV_{DD} = 5 V
	0.4/1.1	V min/V max	DV_{DD} = 3 V
$V_{T+} - V_{T-}$	0.3/0.85	V min/V max	DV_{DD} = 5 V
	0.3/0.85	V min/V max	DV_{DD} = 3 V
Input Currents			
Port 0, P1.2–P1.7, $\overline{EA}$	±10	µA max	V_{IN} = 0 V or V_{DD}
SCLOCK, SDATA/MOSI, MISO, $\overline{SS}$[11]	–10 min, –40 max	µA min/µA max	V_{IN} = 0 V, DV_{DD} = 5 V, Internal Pull-Up
	±10	µA max	V_{IN} = V_{DD}, DV_{DD} = 5 V
RESET	±10	µA max	V_{IN} = 0 V, DV_{DD} = 5 V
	35 min, 105 max	µA min/µA max	V_{IN} = V_{DD}, DV_{DD} = 5 V, Internal Pull-Down
P1.0, P1.1, Ports 2 and 3	±10	µA max	V_{IN} = V_{DD}, DV_{DD} = 5 V
	–180	µA min	V_{IN} = 2 V, DV_{DD} = 5 V
	–660	µA max	
	–20	µA min	V_{IN} = 450 mV, DV_{DD} = 5 V
	–75	µA max	
Input Capacitance	5	pF typ	All Digital Inputs
CRYSTAL OSCILLATOR (XTAL1 AND XTAL2)			
Logic Inputs, XTAL1 Only			
V_{INL}, Input Low Voltage	0.8	V max	DV_{DD} = 5 V
	0.4	V max	DV_{DD} = 3 V
V_{INH}, Input High Voltage	3.5	V min	DV_{DD} = 5 V
	2.5	V min	DV_{DD} = 3 V
XTAL1 Input Capacitance	18	pF typ	
XTAL2 Output Capacitance	18	pF typ	

Parameter	ADuC816BS	Unit	Test Conditions/Comments
POWER REQUIREMENTS (continued)			
Power Supply Currents Normal Mode[16, 17]			
DV_{DD} Current	4	mA max	DV_{DD} = 4.75 V to 5.25 V, Core CLK = 1.57 MHz
	2.1	mA max	DV_{DD} = 2.7 V to 3.6 V, Core CLK = 1.57 MHz
AV_{DD} Current	170	μA max	AV_{DD} = 5.25 V, Core CLK = 1.57 MHz
DV_{DD} Current	15	mA max	DV_{DD} = 4.75 V to 5.25 V, Core CLK = 12.58 MHz
	8	mA max	DV_{DD} = 2.7 V to 3.6 V, Core CLK = 12.58 MHz
AV_{DD} Current	170	μA max	AV_{DD} = 5.25 V, Core CLK = 12.58 MHz
Power Supply Currents Idle Mode[16, 17]			
DV_{DD} Current	1.2	mA max	DV_{DD} = 4.75 V to 5.25 V, Core CLK = 1.57 MHz
	750	μA typ	DV_{DD} = 2.7 V to 3.6 V, Core CLK = 1.57 MHz
AV_{DD} Current	140	μA typ	Measured @ AV_{DD} = 5.25 V, Core CLK = 1.57 MHz
DV_{DD} Current	2	mA typ	DV_{DD} = 4.75 V to 5.25 V, Core CLK = 12.58 MHz
	1	mA typ	DV_{DD} = 2.7 V to 3.6 V, Core CLK = 12.58 MHz
AV_{DD} Current	140	μA typ	Measured at AV_{DD} = 5.25 V, Core CLK = 12.58 MHz
Power Supply Currents Power-Down Mode[16, 17]			Core CLK = 1.57 MHz or 12.58 MHz
DV_{DD} Current	50	μA max	DV_{DD} = 4.75 V to 5.25 V, Osc. On, TIC On
	20	μA max	DV_{DD} = 2.7 V to 3.6 V, Osc. On, TIC On
AV_{DD} Current	1	μA max	Measured at AV_{DD} = 5.25 V, Osc. On or Osc. Off
DV_{DD} Current	20	μA max	DV_{DD} = 4.75 V to 5.25 V, Osc. Off
	5	μA typ	DV_{DD} = 2.7 V to 3.6 V, Osc. Off
Typical Additional Power Supply Currents (AI_{DD} and DI_{DD})			Core CLK = 1.57 MHz, AV_{DD} = DV_{DD} = 5 V
PSM Peripheral	50	μA typ	
Primary ADC	1	mA typ	
Auxiliary ADC	500	μA typ	
DAC	150	μA typ	
Dual Current Sources	400	μA typ	

NOTES

[1]Temperature Range –40°C to +85°C.

[2]These numbers are not production tested but are guaranteed by Design and/or Characterization data on production release.

[3]The primary ADC is factory-calibrated at 25°C with AV_{DD} = DV_{DD} = 5 V yielding this full-scale error. If user power supply or temperature conditions are significantly different from these, an Internal Full-Scale Calibration will restore this error to this level.

[4]Gain Error Drift is a span drift. To calculate Full-Scale Error Drift, add the Offset Error Drift to the Gain Error Drift times the full-scale input.

[5]The auxiliary ADC is factory-calibrated at 25°C with AV_{DD} = DV_{DD} = 5 V yielding this full-scale error of –2.5 LSB. A system zero-scale and full-scale calibration will remove this error altogether.

[6]DAC linearity and AC Specifications are calculated using:
reduced code range of 48 to 4095, 0 to V_{REF}
reduced code range of 48 to 3995, 0 to V_{DD}.

[7]Gain Error is a measure of the span error of the DAC.

[8]In general terms, the bipolar input voltage range to the primary ADC is given by $Range_{ADC} = \pm(V_{REF}\ 2^{RN})/125$, where:
V_{REF} = REFIN(+) to REFIN(–) voltage and V_{REF} = 1.25 V when internal ADC V_{REF} is selected.
RN = decimal equivalent of RN2, RN1, RN0, e.g., V_{REF} = 2.5 V and RN2, RN1, RN0 = 1, 1, 0 the $Range_{ADC} = \pm 1.28$ V.
In unipolar mode the effective range is 0 V to 1.28 V in our example.

[9]1.25 V is used as the reference voltage to the ADC when internal V_{REF} is selected via XREF0 and XREF1 bits in ADC0CON and ADC1CON respectively.

[10]In bipolar mode, the Auxiliary ADC can only be driven to a minimum of A_{GND} – 30 mV as indicated by the Auxiliary ADC absolute AIN voltage limits. The bipolar range is still $-V_{REF}$ to $+V_{REF}$; however, the negative voltage is limited to –30 mV.

[11]Pins configured in I²C-compatible mode or SPI mode, pins configured as digital inputs during this test.

[12]Pins configured in I²C-compatible mode only.

[13]Flash/EE Memory Reliability Characteristics apply to both the Flash/EE program memory and Flash/EE data memory.

[14]Endurance is qualified to 100 Kcycles as per JEDEC Std. 22 method A117 and measured at –40°C, +25°C and +85°C, typical endurance at 25°C is 700 Kcycles.

[15]Retention lifetime equivalent at junction temperature (T_J) = 55°C as per JEDEC Std. 22, Method A117. Retention lifetime based on an activation energy of 0.6eV will derate with junction temperature as shown in Figure 27 in the Flash/EE Memory description section of this data sheet.

[16]Power Supply current consumption is measured in Normal, Idle, and Power-Down Modes under the following conditions:
Normal Mode: Reset = 0.4 V, Digital I/O pins = open circuit, Core Clk changed via CD bits in PLLCON, Core Executing internal software loop.
Idle Mode: Reset = 0.4 V, Digital I/O pins = open circuit, Core Clk changed via CD bits in PLLCON, PCON.0 = 1, Core Execution suspended in idle mode.
Power-Down Mode: Reset = 0.4 V, All P0 pins and P1.2–P1.7 pins = 0.4 V, All other digital I/O pins are open circuit, Core Clk changed via CD bits in PLLCON, PCON.1 = 1, Core Execution suspended in power-down mode, OSC turned ON or OFF via OSC_PD bit (PLLCON.7) in PLLCON SFR.

[17]DV_{DD} power supply current will typically increase by 3 mA (3 V operation) and 10 mA (5 V operation) during a Flash/EE memory program or erase cycle.

Specifications subject to change without notice

Parameter		Min	Max	Unit	Figure
I^2C-COMPATIBLE INTERFACE TIMING					
t_L	SCLOCK Low Pulsewidth	4.7		μs	7
t_H	SCLOCK High Pulsewidth	4.0		μs	7
t_{SHD}	Start Condition Hold Time	0.6		μs	7
t_{DSU}	Data Setup Time	100		μs	7
t_{DHD}	Data Hold Time		0.9	μs	7
t_{RSU}	Setup Time for Repeated Start	0.6		μs	7
t_{PSU}	Stop Condition Setup Time	0.6		μs	7
t_{BUF}	Bus Free Time between a STOP Condition and a START Condition	1.3		μs	7
t_R	Rise Time of Both SCLOCK and SDATA		300	ns	7
t_F	Fall Time of Both SCLOCK and SDATA		300	ns	7
t_{SUP}*	Pulsewidth of Spike Suppressed		50	ns	7

*Input filtering on both the SCLOCK and SDATA inputs suppresses noise spikes less than 50 ns.

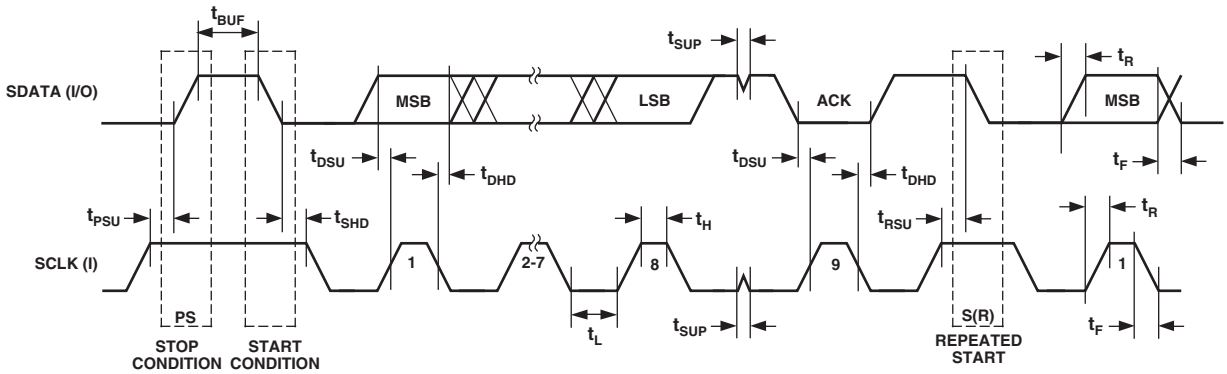


Figure 7. I^2C-Compatible Interface Timing

Parameter		Min	Typ	Max	Unit	Figure
SPI SLAVE MODE TIMING (CPHA = 1)						
t_{SS}	$\overline{SS}$ to SCLOCK Edge	0			ns	10
t_{SL}	SCLOCK Low Pulsewidth		330		ns	10
t_{SH}	SCLOCK High Pulsewidth		330		ns	10
t_{DAV}	Data Output Valid after SCLOCK Edge			50	ns	10
t_{DSU}	Data Input Setup Time before SCLOCK Edge	100			ns	10
t_{DHD}	Data Input Hold Time after SCLOCK Edge	100			ns	10
t_{DF}	Data Output Fall Time		10	25	ns	10
t_{DR}	Data Output Rise Time		10	25	ns	10
t_{SR}	SCLOCK Rise Time		10	25	ns	10
t_{SF}	SCLOCK Fall Time		10	25	ns	10
t_{SFS}	$\overline{SS}$ High after SCLOCK Edge	0			ns	10

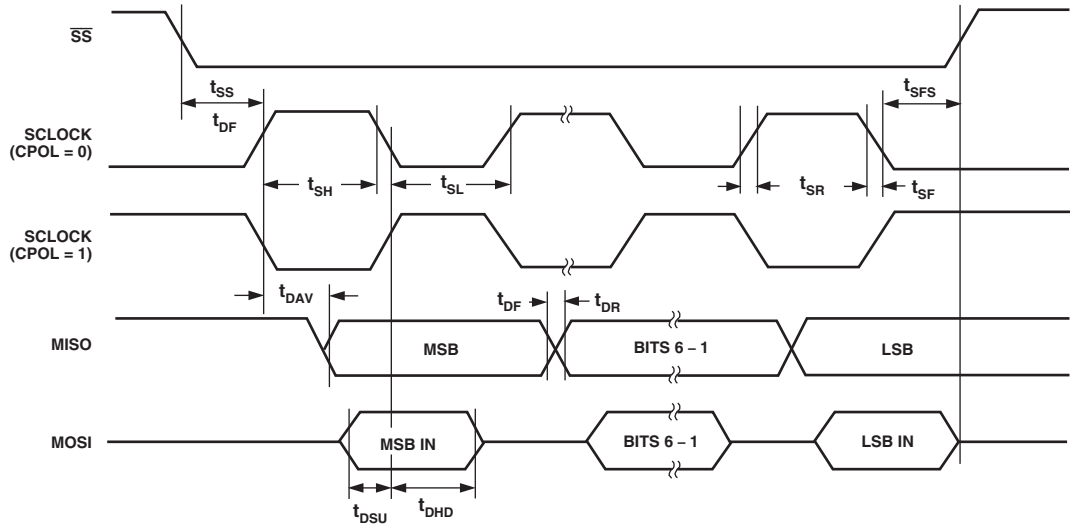


Figure 10. SPI Slave Mode Timing (CPHA = 1)

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

Parameter	Ratings
AV_{DD} to AGND	−0.3 V to +7 V
AV_{DD} to DGND	−0.3 V to +7 V
DV_{DD} to AGND	−0.3 V to +7 V
DV_{DD} to DGND	−0.3 V to +7 V
AGND to DGND[1]	−0.3 V to +0.3 V
AV_{DD} to DV_{DD}	−2 V to +5 V
Analog Input Voltage to AGND[2]	−0.3 V to AV_{DD} +0.3 V
Reference Input Voltage to AGND	−0.3 V to AV_{DD} +0.3 V
AIN/REFIN Current (Indefinite)	30 mA
Digital Input Voltage to DGND	−0.3 V to DV_{DD} +0.3 V
Digital Output Voltage to DGND	−0.3 V to DV_{DD} +0.3 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance (MQFP)	90°C/W
θ_{JA} Thermal Impedance (LFCSP Base Floating)	52°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

[1] AGND and DGND are shorted internally on the ADuC816.
[2] Applies to P1.2 to P1.7 pins operating in analog or digital input modes.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

SPECIAL FUNCTION REGISTERS

All registers except the program counter and the four general-purpose register banks, reside in the SFR area. The SFR registers include control, configuration, and data registers that provide an interface between the CPU and all on-chip peripherals.

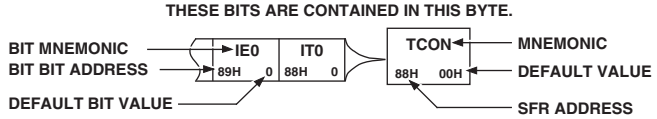
Figure 17 shows a full SFR memory map and SFR contents on RESET; NOT USED indicates unoccupied SFR locations. Unoccupied locations in the SFR address space are not implemented; i.e., no register exists at this location. If an unoccupied location is read, an unspecified value is returned. SFR locations reserved for future use are shaded (RESERVED) and should not be accessed by user software.

ISPI FFH 0	WCOL FEH 0	SPE FDH 0	SPIM FCH 0	CPOL FBH 0	CPHA FAH 1	SPR1 F9H 0	SPR0 F8H 0	BITS
F7H 0	F6H 0	F5H 0	F4H 0	F3H 0	F2H 0	F1H 0	F0H 0	BITS
MDO EFH 0	MDE EEH 0	MCO EDH 0	MDI ECH 0	I2CM EBH 0	I2CRS EAH 0	I2CTX E9H 0	I2CI E8H 0	BITS
E7H 0	E6H 0	E5H 0	E4H 0	E3H 0	E2H 0	E1H 0	E0H 0	BITS
RDY0 DFH 0	RDY1 DEH 0	CAL DDH 0	NOXREF DCH 0	ERR0 DBH 0	ERR1 DAH 0	D9H 0	D8H 0	BITS
CY D7H 0	AC D6H 0	F0 D5H 0	RSI D4H 0	RS0 D3H 0	OV D2H 0	FI D1H 0	P D0H 0	BITS
TF2 CFH 0	EXF2 CEH 0	RCLK CDH 0	TCLK CCH 0	EXEN2 CBH 0	TR2 CAH 0	CNT2 C9H 0	CAP2 C8H 0	BITS
PRE3 C7H 0	PRE2 C6H 0	PRE1 C5H 0	PRE0 C4H 1	WDIR C3H 0	WDS C2H 0	WDE C1H 0	WDWR C0H 0	BITS
BFH 0	PADC BEH 0	PT2 BDH 0	PS BCH 0	PT1 BBH 0	PX1 BAH	PT0 B9H 0	PX0 B8H 0	BITS
$\overline{RD}$ B7H 1	$\overline{WR}$ B6H 1	T1 B5H 1	T0 B4H 1	$\overline{INT1}$ B3H 1	$\overline{INT0}$ B2H 1	TXD B1H 1	RXD B0H 1	BITS
EA AFH 0	EADC AEH 0	ET2 ADH 0	ES ACH 0	ET1 ABH 0	EX1 AAH 0	ET0 A9H 0	EX0 A8H 0	BITS
A7H 1	A6H 1	A5H 1	A4H 1	A3H 1	A2H 1	A1H 1	A0H 1	BITS
SM0 9FH 0	SM1 9EH 0	SM2 9DH 0	REN 9CH 0	TB8 9BH 0	RB8 9AH 0	T1 99H 0	R1 98H 0	BITS
97H 1	96H 1	95H 1	94H 1	93H 1	92H 1	T2EX 91H 1	T2 90H 1	BITS
TF1 8FH 0	TR1 8EH 0	TF0 8DH 0	TR0 8CH 0	IE1 8BH 0	IT1 8AH 0	IE0 89H 0	IT0 88H 0	BITS
87H 1	86H 1	85H 1	84H 1	83H 1	82H 1	81H 1	80H 1	BITS

SPICON F8H 04H	RESERVED	RESERVED	DACL FBH 00H	DACH FCH 00H	DACCON FDH 00H	RESERVED	RESERVED
B F0H 00H	RESERVED	RESERVED	NOT USED	RESERVED	RESERVED	RESERVED	SPIDAT F7H 00H
I2CCON E8H 00H	RESERVED	GN0M* EAH 55H	GN0H* EBH 53H	GN1L* ECH 9AH	GN1H* EDH 59H	RESERVED	RESERVED
ACC E0H 00H	RESERVED	OF0M* E2H 00H	OF0H* E3H 80H	OF1L* E4H 00H	OF1H* E5H 80H	RESERVED	RESERVED
ADCSTAT D8H 00H	RESERVED	ADC0M DAH 00H	ADC0H DBH 00H	ADC1L DCH 00H	ADC1H DDH 00H	RESERVED	PSMCON DFH DEH
PSW D0H 00H	ADCMODE D1H 00H	ADC0CON D2H 07H	ADC1CON D3H 00H	SF D4H 45H	ICON D5H 00H	RESERVED	PLLCON D7H 03H
T2CON C8H 00H	RESERVED	RCAP2L CAH 00H	RCAP2H CBH 00H	TL2 CCH 00H	TH2 CDH 00H	RESERVED	RESERVED
WDCON C0H 10H	RESERVED	CHIPID C2H 16H	RESERVED	RESERVED	RESERVED	EADRL C6H 00H	RESERVED
IP B8H 00H	ECON B9H 00H	RESERVED	RESERVED	EDATA1 BCH 00H	EDATA2 BDH 00H	EDATA3 BEH 00H	EDATA4 BFH 00H
P3 B0H FFH	NOT USED	NOT USED	NOT USED	NOT USED	RESERVED	RESERVED	NOT USED
IE A8H 00H	IEIP2 A9H A0H	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
P2 A0H FFH	TIMECON A1H 00H	HTHSEC A2H 00H	SEC A3H 00H	MIN A4H 00H	HOUR A5H 00H	INTVAL A6H 00H	NOT USED
SCON 98H 00H	SBUF 99H 00H	I2CDAT 9AH 00H	I2CDAT 9BH 00H	NOT USED	NOT USED	NOT USED	NOT USED
P1 90H FFH	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED
TCON 88H 00H	TMOD 89H 00H	TL0 8AH 00H	TL1 8BH 00H	TH0 8CH 00H	TH1 8DH 00H	RESERVED	RESERVED
P0 80H FFH	SP 81H 07H	DPL 82H 00H	DPH 83H 00H	DPP 84H 00H	RESERVED	RESERVED	PCON 87H 00H

*CALIBRATION COEFFICIENTS ARE PRECONFIGURED AT POWER-UP TO FACTORY-CALIBRATED VALUES.

SFR MAP KEY:



SFR NOTE:
SFRs WHOSE ADDRESSES END IN 0H OR 8H ARE BIT-ADDRESSABLE.

Figure 17. Special Function Register Locations and Reset Values

ICON (Current Sources Control Register)
Used to control and configure the various excitation and burnout current source options available on-chip.

SFR Address D5H
Power-On Default Value 00H
Bit Addressable No

---	BO	ADC1IC	ADC0IC	I2PIN	I1PIN	I2EN	I1EN

Table VIII. ICON SFR Bit Designations

Bit	Name	Description
7	---	Reserved for Future Use.
6	BO	Burnout Current Enable Bit. *Set* by user to enable both transducer burnout current sources in the primary ADC signal paths. *Cleared* by user to disable both transducer burnout current sources.
5	ADC1IC	Auxiliary ADC Current Correction Bit. *Set* by user to allow scaling of the Auxiliary ADC by an internal current source calibration word.
4	ADC0IC	Primary ADC Current Correction Bit. *Set* by user to allow scaling of the Primary ADC by an internal current source calibration word.
3	I2PIN*	Current Source-2 Pin Select Bit. *Set* by user to enable current source-2 (200 μA) to external Pin 3 (P1.2/DAC/IEXC1). *Cleared* by user to enable current source-2 (200 μA) to external Pin 4 (P1.3/AIN5/IEXC2).
2	I1PIN*	Current Source-1 Pin Select Bit. *Set* by user to enable current source-1 (200 μA) to external Pin 4 (P1.3/AIN5/IEXC2). *Cleared* by user to enable current source-1 (200 μA) to external Pin 3 (P1.2/DAC/IEXC1).
1	I2EN	Current Source-2 Enable Bit. *Set* by user to turn on excitation current source-2 (200 μA). *Cleared* by user to turn off excitation current source-2 (200 μA).
0	I1EN	Current Source-1 Enable Bit. *Set* by user to turn on excitation current source-1 (200 μA). *Cleared* by user to turn off excitation current source-1 (200 μA).

*Both current sources can be enabled to the same external pin, yielding a 400 μA current source.

ADC0H/ADC0M (Primary ADC Conversion Result Registers)
These two 8-bit registers hold the 16-bit conversion result from the Primary ADC.

SFR Address	ADC0H	High Data Byte	DBH
	ADC0M	Middle Data Byte	DAH
Power-On Default Value	00H	Both Registers	
Bit Addressable	No	Both Registers	

ADC1H/ADC1L (Auxiliary ADC Conversion Result Registers)
These two 8-bit registers hold the 16-bit conversion result from the Auxiliary ADC.

SFR Address	ADC1H	High Data Byte	DDH
	ADC1L	Low Data Byte	DCH
Power-On Default Value	00H	Both Registers	
Bit Addressable	No	Both Registers	

PRIMARY AND AUXILIARY ADC CIRCUIT DESCRIPTION

OVERVIEW

The ADuC816 incorporates two independent sigma-delta ADCs (Primary and Auxiliary) with on-chip digital filtering intended for the measurement of wide dynamic range, low frequency signals such as those in weigh-scale, strain-gauge, pressure transducer or temperature measurement applications.

Primary ADC

This ADC is intended to convert the primary sensor input. The input is buffered and can be programmed for one of 8 input ranges from ±20 mV to ±2.56 V being driven from one of three differential input channel options AIN1/2, AIN3/4, or AIN3/2. The input channel is internally buffered allowing the part to handle significant source impedances on the analog input, allowing R/C filtering (for noise rejection or RFI reduction) to be placed on the analog inputs if required. On-chip burnout currents can also be turned on. These currents can be used to check that a transducer on the selected channel is still operational before attempting to take measurements.

The ADC employs a sigma-delta conversion technique to realize up to 16 bits of no missing codes performance. The sigma-delta modulator converts the sampled input signal into a digital pulse train whose duty cycle contains the digital information. A Sinc3 programmable low-pass filter is then employed to decimate the modulator output data stream to give a valid data conversion result at programmable output rates from 5.35 Hz (186.77 ms) to 105.03 Hz (9.52 ms). A Chopping scheme is also employed to minimize ADC offset errors. A block diagram of the Primary ADC is shown in Figure 18.

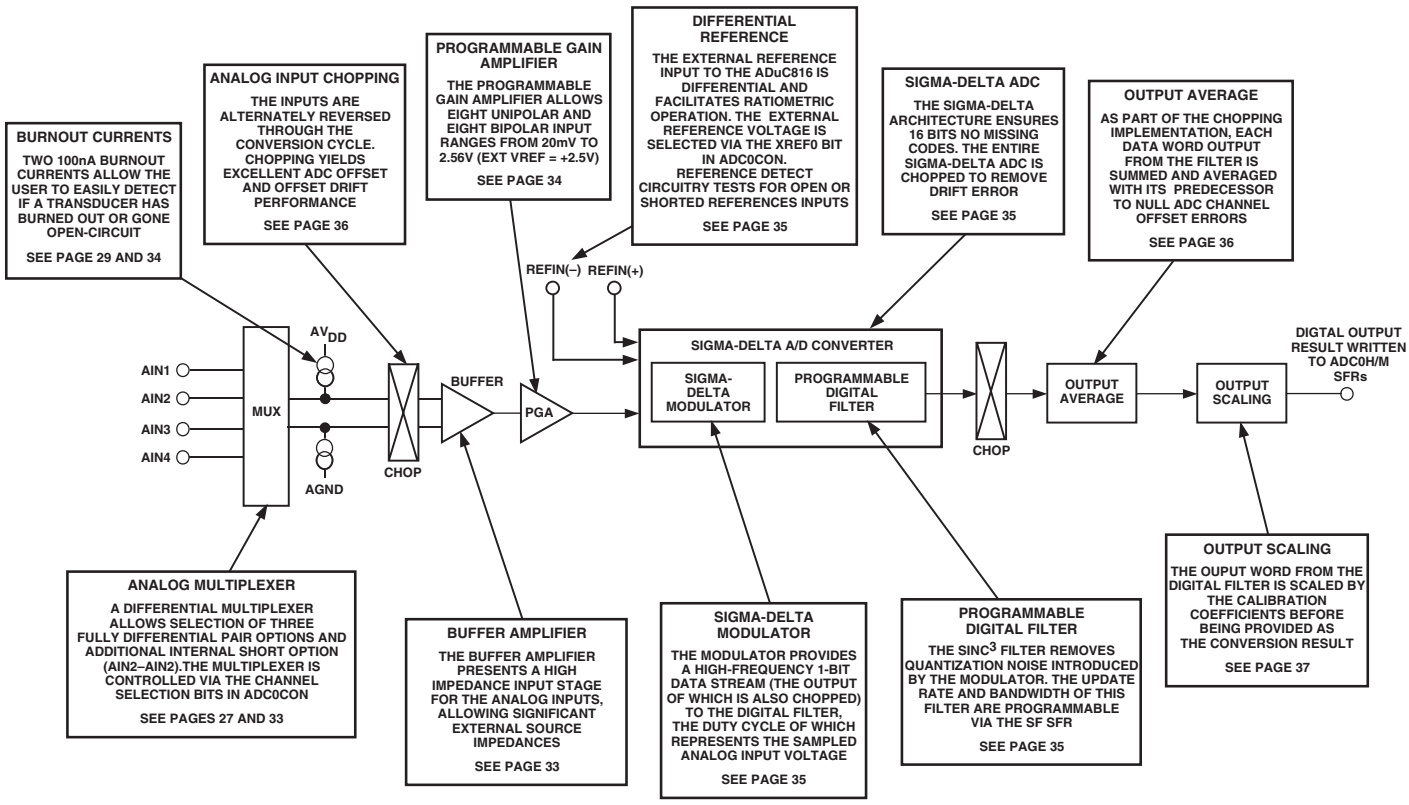


Figure 18. Primary ADC Block Diagram

mended. Deriving the reference input voltage across an external resistor, as shown in Figure 52, will mean that the reference input sees a significant external source impedance. External decoupling on the REFIN(+) and REFIN(–) pins would not be recommended in this type of circuit configuration.

Reference Detect

The ADuC816 includes on-chip circuitry to detect if the part has a valid reference for conversions or calibrations. If the voltage between the external REFIN(+) and REFIN(–) pins goes below 0.3 V or either the REFIN(+) or REFIN(–) inputs is open circuit, the ADuC816 detects that it no longer has a valid reference. In this case, the NOXREF bit of the ADCSTAT SFR is set to a 1. If the ADuC816 is performing normal conversions and the NOXREF bit becomes active, the conversion results revert to all 1s. Therefore, it is not necessary to continuously monitor the status of the NOXREF bit when performing conversions. It is only necessary to verify its status if the conversion result read from the ADC Data Register is all 1s.

If the ADuC816 is performing either an offset or gain calibration and the NOXREF bit becomes active, the updating of the respective calibration registers is inhibited to avoid loading incorrect coefficients to these registers, and the appropriate ERR0 or ERR1 bits in the ADCSTAT SFR are set. If the user is concerned about verifying that a valid reference is in place every time a calibration is performed, the status of the ERR0 or ERR1 bit should be checked at the end of the calibration cycle.

Sigma-Delta Modulator

A sigma-delta ADC generally consists of two main blocks, an analog modulator and a digital filter. In the case of the ADuC816 ADCs, the analog modulators consist of a difference amplifier, an integrator block, a comparator, and a feedback DAC as illustrated in Figure 20.

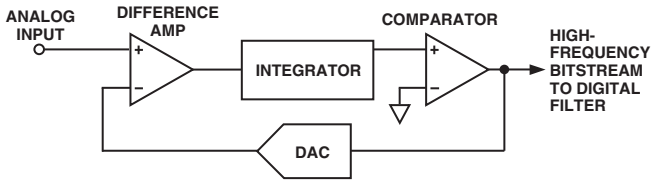


Figure 20. Sigma-Delta Modulator Simplified Block Diagram

In operation, the analog signal sample is fed to the difference amplifier along with the output of the feedback DAC. The difference between these two signals is integrated and fed to the comparator. The output of the comparator provides the input to the feedback DAC so the system functions as a negative feedback loop that tries to minimize the difference signal. The digital data that represents the analog input voltage is contained in the duty cycle of the pulse train appearing at the output of the comparator. This duty cycle data can be recovered as a data word using a subsequent digital filter stage. The sampling frequency of the modulator loop is many times higher than the bandwidth of the input signal. The integrator in the modulator shapes the quantization noise (which results from the analog-to-digital conversion) so that the noise is pushed toward one-half of the modulator frequency.

Digital Filter

The output of the sigma-delta modulator feeds directly into the digital filter. The digital filter then band-limits the response to a frequency significantly lower than one-half of the modulator frequency. In this manner, the 1-bit output of the comparator is translated into a band-limited, low noise output from the ADuC816 ADCs.

The ADuC816 filter is a low-pass, $Sinc^3$ or $(sinx/x)^3$ filter whose primary function is to remove the quantization noise introduced at the modulator. The cutoff frequency and decimated output data rate of the filter are programmable via the SF (Sinc Filter) SFR as described in Table VII.

Figure 21 shows the frequency response of the ADC channel at the default SF word of 69 dec or 45 hex, yielding an overall output update rate of just under 20 Hz.

It should be noted that this frequency response allows frequency components higher than the ADC Nyquist frequency to pass through the ADC, in some cases without significant attenuation. These components may, therefore, be aliased and appear in-band after the sampling process.

It should also be noted that rejection of mains-related frequency components, i.e., 50 Hz and 60 Hz, is seen to be at level of >65 dB at 50 Hz and >100 dB at 60 Hz. This confirms the data sheet specifications for 50 Hz/60 Hz Normal Mode Rejection (NMR) at a 20 Hz update rate.

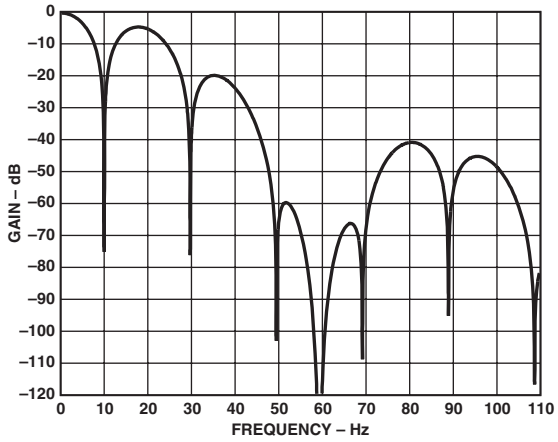


Figure 21. Filter Response, SF = 69 dec

The response of the filter, however, will change with SF word as can be seen in Figure 22, which shows >90 dB NMR at 50 Hz and >70 dB NMR at 60 Hz when SF = 255 dec.

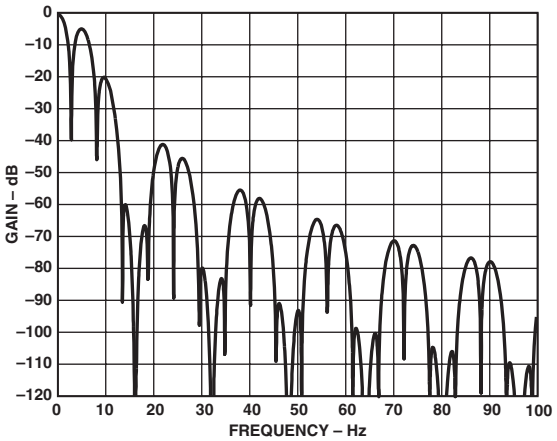


Figure 22. Filter Response, SF = 255 dec

Figures 23 and 24 show the NMR for 50 Hz and 60 Hz across the full range of SF word, i.e., SF = 13 dec to SF = 255 dec.

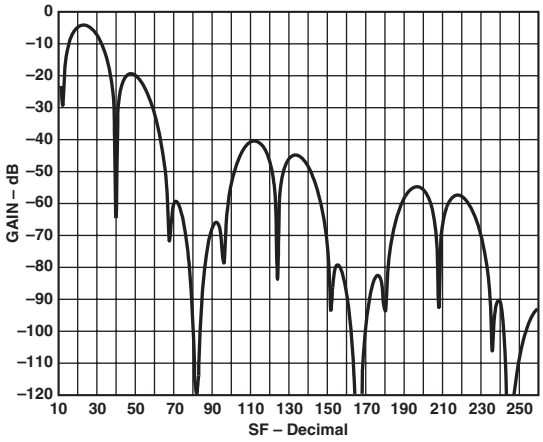


Figure 23. 50 Hz Normal Mode Rejection vs. SF

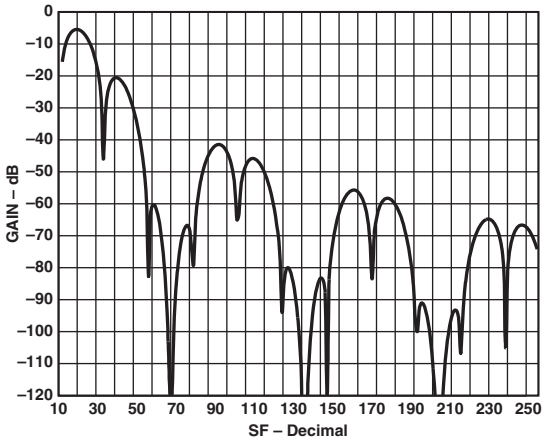


Figure 24. 60 Hz Normal Mode Rejection vs. SF

ADC Chopping

Both ADCs on the ADuC816 implement a chopping scheme whereby the ADC repeatability reverses its inputs. The decimated digital output words from the $Sinc^3$ filters therefore have a positive offset and negative offset term included.

As a result, a final summing stage is included in each ADC so that each output word from the filter is summed and averaged with the previous filter output to produce a new valid output result to be written to the ADC data SFRs. In this way, while the ADC throughput or update rate is as discussed earlier and illustrated in Table VII, the full settling time through the ADC (or the time to a first conversion result), will actually be given by $2 \times t_{ADC}$.

The chopping scheme incorporated in the ADuC816 ADC results in excellent dc offset and offset drift specifications and is extremely beneficial in applications where drift, noise rejection, and optimum EMI rejection are important factors.

Calibration

The ADuC816 provides four calibration modes that can be programmed via the mode bits in the ADCMODE SFR detailed in Table IV. In fact, every ADuC816 has already been factory calibrated. The resultant Offset and Gain calibration coefficients for both the primary and auxiliary ADCs are stored on-chip in manufacturing-specific Flash/EE memory locations. At power-on, these factory calibration coefficients are automatically downloaded to the calibration registers in the ADuC816 SFR space. Each ADC (primary and auxiliary) has dedicated calibration SFRs, these have been described earlier as part of the general ADC SFR description. However, the factory calibration values in the ADC calibration SFRs will be overwritten if any one of the four calibration options are initiated and that ADC is enabled via the ADC enable bits in ADCMODE.

Even though an internal offset calibration mode is described below, it should be recognized that both ADCs are chopped. This chopping scheme inherently minimizes offset and means that an internal offset calibration should never be required. Also, because factory 5 V/25°C gain calibration coefficients are automatically present at power-on, an internal full-scale calibration will only be required if the part is being operated at 3 V or at temperatures significantly different from 25°C.

The ADuC816 offers "internal" or "system" calibration facilities. For full calibration to occur on the selected ADC, the calibration logic must record the modulator output for two different input conditions. These are "zero-scale" and "full-scale" points. These points are derived by performing a conversion on the different input voltages provided to the input of the modulator during calibration. The result of the "zero-scale" calibration conversion is stored in the Offset Calibration Registers for the appropriate ADC. The result of the "full-scale" calibration conversion is stored in the Gain Calibration Registers for the appropriate ADC. With these readings, the calibration logic can calculate the offset and the gain slope for the input-to-output transfer function of the converter.

During an "internal" zero-scale or full-scale calibration, the respective "zero" input and "full-scale" input are automatically connected to the ADC input pins internally to the device. A "system" calibration, however, expects the system zero-scale and system full-scale voltages to be applied to the external ADC pins before the calibration mode is initiated. In this way external ADC errors are taken into account and minimized as a result of system calibration. It should also be noted that to optimize calibration accuracy, all ADuC816 ADC calibrations are carried out automatically at the slowest update rate.

Internally in the ADuC816, the coefficients are normalized before being used to scale the words coming out of the digital filter. The offset calibration coefficient is subtracted from the result prior to the multiplication by the gain coefficient. All ADuC816 ADC specifications will only apply after a zero-scale and full-scale calibration at the operating point (supply voltage/temperature) of interest.

From an operational point of view, a calibration should be treated like another ADC conversion. A zero-scale calibration (if required) should always be carried out before a full-scale calibration. System software should monitor the relevant ADC RDY0/1 bit in the ADCSTAT SFR to determine end of calibration via a polling sequence or interrupt driven routine.

Serial Safe Mode

This mode disables serial download capability on the device. If Serial Safe mode is activated and an attempt is made to reset the part into serial download mode, i.e., RESET asserted and deasserted with $\overline{\text{PSEN}}$ low, the part will interpret the serial download reset as a normal reset only. It will, therefore, not enter serial download mode but only execute a normal reset sequence. Serial Safe mode can only be disabled by initiating a code-erase command in parallel programming mode.

Using the Flash/EE Data Memory

The user Flash/EE data memory array consists of 640 bytes that are configured into 160 (00H to 9FH) 4-byte pages as shown in Figure 29.

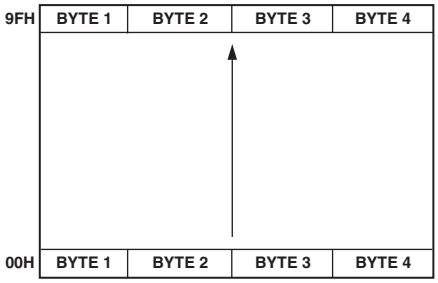


Figure 29. Flash/EE Data Memory Configuration

As with other ADuC816 user-peripheral circuits, the interface to this memory space is via a group of registers mapped in the SFR space. A group of four data registers (EDATA1–4) are used to hold 4-byte page data just accessed. EADRL is used to hold the 8-bit address of the page to be accessed. Finally, ECON is an 8-bit control register that may be written with one of five Flash/EE memory access commands to trigger various read, write, erase, and verify functions. These registers can be summarized as follows:

ECON: SFR Address: B9H
Function: Controls access to 640 Bytes Flash/EE Data Space.
Default: 00H

EADRL: SFR Address: C6H
Function: Holds the Flash/EE Data Page Address. (640 Bytes => 160 Page Addresses.)
Default: 00H

EDATA 1–4:
SFR Address: BCH to BFH respectively
Function: Holds Flash/EE Data memory page write or page read data bytes.
Default : EDATA1–2 –> 00H
EDATA3–4 –> 00H

A block diagram of the SFR interface to the Flash/EE Data Memory array is shown in Figure 30.

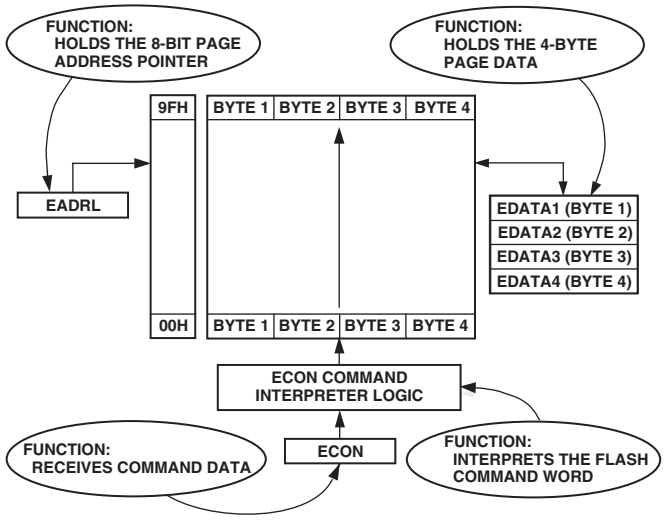


Figure 30. Flash/EE Data Memory Control and Configuration

ECON—Flash/EE Memory Control SFR

This SFR acts as a command interpreter and may be written with one of five command modes to enable various read, program and erase cycles as detailed in Table XIII:

Table XIII. ECON–Flash/EE Memory Control Register Command Modes

Command Byte	Command Mode
01H	READ COMMAND. Results in four bytes being read into EDATA1–4 from memory page address contained in EADRL.
02H	PROGRAM COMMAND. Results in four bytes (EDATA1–4) being written to memory page address in EADRL. This write command assumes the designated "write" page has been pre-erased.
03H	RESERVED FOR INTERNAL USE. 03H should not be written to the ECON SFR.
04H	VERIFY COMMAND. Allows the user to verify if data in EDATA1–4 is contained in page address designated by EADRL. A subsequent read of the ECON SFR will result in a "zero" being read if the verification is valid, a nonzero value will be read to indicate an invalid verification.
05H	ERASE COMMAND. Results in an erase of the 4-byte page designated in EADRL.
06H	ERASE-ALL COMMAND. Results in erase of the full Flash/EE Data memory 160-page (640 bytes) array.
07H to FFH	RESERVED COMMANDS. Commands reserved for future use.

USER INTERFACE TO OTHER ON-CHIP ADuC816 PERIPHERALS

The following section gives a brief overview of the various peripherals also available on-chip. A summary of the SFRs used to control and configure these peripherals is also given.

DAC

The ADuC816 incorporates a 12-bit, voltage output DAC on-chip. It has a rail-to-rail voltage output buffer capable of driving 10 kΩ/100 pF. It has two selectable ranges, 0 V to V_{REF} (the internal bandgap 2.5 V reference) and 0 V to AV_{DD}. It can operate in 12-bit or 8-bit mode. The DAC has a control register, DACCON, and two data registers, DACH/L. The DAC output can be programmed to appear at Pin 3 or Pin 12. It should be noted that in 12-bit mode, the DAC voltage output will be updated as soon as the DACL data SFR has been written; therefore, the DAC data registers should be updated as DACH first followed by DACL.

DACCON	**DAC Control Register**
SFR Address	FDH
Power-On Default Value	00H
Bit Addressable	No

---	---	---	**DACPIN**	**DAC8**	**DACRN**	**$\overline{\text{DACCLR}}$**	**DACEN**

Table XIV. DACCON SFR Bit Designations

Bit	Name	Description
7	---	Reserved for Future Use.
6	---	Reserved for Future Use.
5	---	Reserved for Future Use.
4	DACPIN	DAC Output Pin Select. *Set* by the user to direct the DAC output to Pin 12 (P1.7/AIN4/DAC). *Cleared* by user to direct the DAC output to Pin 3 (P1.2/DAC/IEXC1).
3	DAC8	DAC 8-bit Mode Bit. *Set* by user to enable 8-bit DAC operation. In this mode the 8-bits in DACL SFR are routed to the 8 MSBs of the DAC and the 4 LSBs of the DAC are set to zero. *Cleared* by user to operate the DAC in its normal 12-bit mode of operation.
2	DACRN	DAC Output Range Bit. *Set* by user to configure DAC range of 0 – AV_{DD}. *Cleared* by user to configure DAC range of 0 – 2.5 V.
1	$\overline{\text{DACCLR}}$	DAC Clear Bit. *Set* to "1" by user to enable normal DAC operation. *Cleared* to "0" by user to reset DAC data registers DACl/H to zero.
0	DACEN	DAC Enable Bit. *Set* to "1" by user to enable normal DAC operation. *Cleared* to "0" by user to power-down the DAC.

DACH/L	**DAC Data Registers**	
Function	DAC Data Registers, written by user to update the DAC output.	
SFR Address	DACL (DAC Data Low Byte)	–>FBH
	DACH (DAC Data High Byte)	–>FCH
Power-On Default Value	00H	–>Both Registers
Bit Addressable	No	–>Both Registers

The 12-bit DAC data should be written into DACH/L right-justified such that DACL contains the lower eight bits, and the lower nibble of DACH contains the upper four bits.

TIMECON **TIC CONTROL REGISTER**
SFR Address A1H
Power-On Default Value 00H
Bit Addressable No

---	---	ITS1	ITS0	STI	TII	TIEN	TCEN

Table XVI. TIMECON SFR Bit Designations

Bit	Name	Description
7	---	Reserved for Future Use.
6	---	Reserved for Future Use. For future product code compatibility this bit should be written as a '1.'
5	ITS1	Interval Timebase Selection Bits.
4	ITS0	Written by user to determine the interval counter update rate. ITS1 ITS0 Interval Timebase 0 0 1/128 Second 0 1 Seconds 1 0 Minutes 1 1 Hours
3	STI	Single Time Interval Bit. *Set* by user to generate a single interval timeout. If set, a timeout will clear the TIEN bit. *Cleared* by user to allow the interval counter to be automatically reloaded and start counting again at each interval timeout.
2	TII	TIC Interrupt Bit. *Set* when the 8-bit Interval Counter matches the value in the INTVAL SFR. *Cleared* by user software.
1	TIEN	Time Interval Enable Bit. *Set* by user to enable the 8-bit time interval counter. *Cleared* by user to disable and clear the contents of the interval counter.
0	TCEN	Time Clock Enable Bit. *Set* by user to enable the time clock to the time interval counters. *Cleared* by user to disable the clock to the time interval counters and clear the time interval SFRs. The time registers (HTHSEC, SEC, MIN and HOUR) can be written while TCEN is low.

Power Supply Monitor

As its name suggests, the Power Supply Monitor, once enabled, monitors both supplies (AVDD or DVDD) on the ADuC816. It will indicate when any of the supply pins drop below one of four user-selectable voltage trip points from 2.63 V to 4.63 V. For correct operation of the Power Supply Monitor function, AV_{DD} must be equal to or greater than 2.7 V. Monitor function is controlled via the PSMCON SFR. If enabled via the IEIP2 SFR, the monitor will interrupt the core using the PSMI bit in the PSMCON SFR. This bit will not be cleared until the failing power supply has returned above the trip point for at least 250 ms. This monitor function allows the user to save working registers to avoid possible data loss due to the low supply condition, and also ensures that normal code execution will not resume until a safe supply level has been well established. The supply monitor is also protected against spurious glitches triggering the interrupt circuit.

PSMCON **Power Supply Monitor Control Register**

SFR Address DFH
Power-On Default Value DEH
Bit Addressable No

CMPD	CMPA	PSMI	TPD1	TPD0	TPA1	TPA0	PSMEN

Table XVIII. PSMCON SFR Bit Designations

Bit	Name	Description
7	CMPD	DVDD Comparator Bit. This is a read-only bit and directly reflects the state of the DVDD comparator. Read "1" indicates the DVDD supply is above its selected trip point. Read "0" indicates the DVDD supply is below its selected trip point.
6	CMPA	AVDD Comparator Bit. This is a read-only bit and directly reflects the state of the AVDD comparator. Read "1" indicates the AVDD supply is above its selected trip point. Read "0" indicates the AVDD supply is below its selected trip point.
5	PSMI	Power Supply Monitor Interrupt Bit. This bit will be set high by the MicroConverter if either CMPA or CMPD are low, indicating low analog or digital supply. The PSMI bit can be used to interrupt the processor. Once CMPD and/or CMPA return (and remain) high, a 250 ms counter is started. When this counter times out, the PSMI interrupt is cleared. PSMI can also be written by the user. However, if either comparator output is low, it is not possible for the user to clear PSMI.
4	TPD1	DVDD Trip Point Selection Bits.
3	TPD0	These bits select the DVDD trip-point voltage as follows: TPD1 TPD0 Selected DVDD Trip Point (V) 0 0 4.63 0 1 3.08 1 0 2.93 1 1 2.63
2	TPA1	AVDD Trip Point Selection Bits.
1	TPA0	These bits select the AVDD trip-point voltage as follows: TPA1 TPA0 Selected AVDD Trip Point (V) 0 0 4.63 0 1 3.08 1 0 2.93 1 1 2.63
0	PSMEN	Power Supply Monitor Enable Bit. *Set* to "1" by the user to enable the Power Supply Monitor Circuit. *Cleared* to "0" by the user to disable the Power Supply Monitor Circuit.

SERIAL PERIPHERAL INTERFACE

The ADuC816 integrates a complete hardware Serial Peripheral Interface (SPI) interface on-chip. SPI is an industry standard synchronous serial interface that allows eight bits of data to be synchronously transmitted and received simultaneously, i.e., full duplex. It should be noted that the SPI physical interface is shared with the I^2C interface and therefore the user can only enable one or the other interface at any given time (see SPE in SPICON below). The system can be configured for Master or Slave operation and typically consists of four pins, namely:

MISO (Master In, Slave Out Data I/O Pin), Pin 14

The MISO (master in slave out) pin is configured as an input line in master mode and an output line in slave mode. The MISO line on the master (data in) should be connected to the MISO line in the slave device (data out). The data is transferred as byte wide (8-bit) serial data, MSB first.

MOSI (Master Out, Slave In Pin), Pin 27

The MOSI (master out slave in) pin is configured as an output line in master mode and an input line in slave mode. The MOSI line on the master (data out) should be connected to the MOSI line in the slave device (data in). The data is transferred as byte wide (8-bit) serial data, MSB first.

SCLOCK (Serial Clock I/O Pin), Pin 26

The master clock (SCLOCK) is used to synchronize the data being transmitted and received through the MOSI and MISO data lines. A single data bit is transmitted and received in each SCLOCK period. Therefore, a byte is transmitted/received after eight SCLOCK periods. The SCLOCK pin is configured as an output in master mode and as an input in slave mode. In master mode the bit-rate, polarity and phase of the clock are controlled by the CPOL, CPHA, SPR0 and SPR1 bits in the SPICON SFR (see Table XIX below). In slave mode the SPICON register will have to be configured with the phase and polarity (CPHA and CPOL) of the expected input clock. In both master and slave mode the data is transmitted on one edge of the SCLOCK signal and sampled on the other. It is important therefore that the CPHA and CPOL are configured the same for the master and slave devices.

$\overline{SS}$ (Slave Select Input Pin), Pin 13

The Slave Select ($\overline{SS}$) input pin is only used when the ADuC816 is configured in slave mode to enable the SPI peripheral. This line is active low. Data is only received or transmitted in slave mode when the $\overline{SS}$ pin is low, allowing the ADuC816 to be used in single master, multislave SPI configurations. If CPHA = 1 then the $\overline{SS}$ input may be permanently pulled low. With CPHA = 0 then the $\overline{SS}$ input must be driven low before the first bit in a byte wide transmission or reception and return high again after the last bit in that byte wide transmission or reception. In SPI Slave Mode, the logic level on the external $\overline{SS}$ pin (Pin 13), can be read via the SPR0 bit in the SPICON SFR.

The following SFR registers are used to control the SPI interface.

SPICON:	**SPI Control Register**
SFR Address	F8H
Power-On Default Value	04H
Bit Addressable	Yes

ISPI	WCOL	SPE	SPIM	CPOL	CPHA	SPR1	SPR0

Table XIX. SPICON SFR Bit Designations

Bit	Name	Description
7	ISPI	SPI Interrupt Bit. *Set* by MicroConverter at the end of each SPI transfer. *Cleared* directly by user code or indirectly by reading the SPIDAT SFR
6	WCOL	Write Collision Error Bit. *Set* by MicroConverter if SPIDAT is written to while an SPI transfer is in progress. *Cleared* by user code.
5	SPE	SPI Interface Enable Bit. *Set* by user to enable the SPI interface. *Cleared* by user to enable the I^2C interface.
4	SPIM	SPI Master/Slave Mode Select Bit. *Set* by user to enable Master Mode operation (SCLOCK is an output). *Cleared* by user to enable Slave Mode operation (SCLOCK is an input).
3	CPOL	Clock Polarity Select Bit. *Set* by user if SCLOCK idles high. *Cleared* by user if SCLOCK idles low.
2	CPHA	Clock Phase Select Bit. *Set* by user if leading SCLOCK edge is to transmit data. *Cleared* by user if trailing SCLOCK edge is to transmit data.

Table XIX. SPICON SFR Bit Designations (*continued*)

Bit	Name	Description
1 0	SPR1 SPR0	SPI Bit-Rate Select Bits. These bits select the SCLOCK rate (bit-rate) in Master Mode as follows: SPR1 SPR0 Selected Bit Rate 0 0 $f_{CORE}/2$ 0 1 $f_{CORE}/4$ 1 0 $f_{CORE}/8$ 1 1 $f_{CORE}/16$ In SPI Slave Mode, i.e., SPIM = 0, the logic level on the external $\overline{SS}$ pin (Pin 13), can be read via the SPR0 bit.

NOTE
The CPOL and CPHA bits should both contain the same values for master and slave devices.

SPIDAT **SPI Data Register**

Function: The SPIDAT SFR is written by the user to transmit data over the SPI interface or read by user code to read data just received by the SPI interface.

SFR Address: F7H

Power-On Default Value: 00H

Bit Addressable: No

Using the SPI Interface

Depending on the configuration of the bits in the SPICON SFR shown in Table XIX, the ADuC816 SPI interface will transmit or receive data in a number of possible modes. Figure 32 shows all possible ADuC816 SPI configurations and the timing relationships and synchronization between the signals involved. Also shown in this figure is the SPI interrupt bit (ISPI) and how it is triggered at the end of each byte-wide communication.

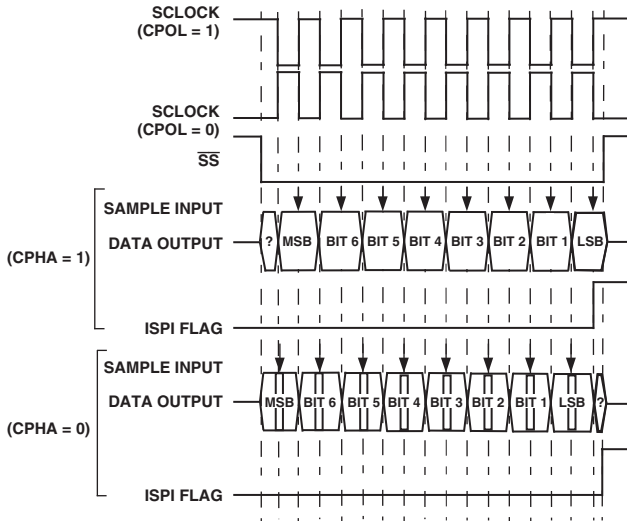


Figure 32. SPI Timing, All Modes

SPI Interface—Master Mode

In master mode, the SCLOCK pin is always an output and generates a burst of eight clocks whenever user code writes to the SPIDAT register. The SCLOCK bit rate is determined by SPR0 and SPR1 in SPICON. It should also be noted that the $\overline{SS}$ pin is not used in master mode. If the ADuC816 needs to assert the $\overline{SS}$ pin on an external slave device, a Port digital output pin should be used.

In master mode a byte transmission or reception is initiated by a write to SPIDAT. Eight clock periods are generated via the SCLOCK pin and the SPIDAT byte being transmitted via MOSI. With each SCLOCK period a data bit is also sampled via MISO. After eight clocks, the transmitted byte will have been completely transmitted and the input byte will be waiting in the input shift register. The ISPI flag will be set automatically and an interrupt will occur if enabled. The value in the shift register will be latched into SPIDAT.

SPI Interface—Slave Mode

In slave mode the SCLOCK is an input. The $\overline{SS}$ pin must also be driven low externally during the byte communication.

Transmission is also initiated by a write to SPIDAT. In slave mode, a data bit is transmitted via MISO and a data bit is received via MOSI through each input SCLOCK period. After eight clocks, the transmitted byte will have been completely transmitted and the input byte will be waiting in the input shift register. The ISPI flag will be set automatically and an interrupt will occur if enabled. The value in the shift register will be latched into SPIDAT only when the transmission/reception of a byte has been completed. The end of transmission occurs after the eighth clock has been received, if CPHA = 1 or when $\overline{SS}$ returns high if CPHA = 0.

T2CON **Timer/Counter 2 Control Register**
SFR Address C8H
Power-On Default Value 00H
Bit Addressable Yes

TF2	EXF2	RCLK	TCLK	EXEN2	TR2	CNT2	CAP2

Table XXV. T2CON SFR Bit Designations

Bit	Name	Description
7	TF2	Timer 2 Overflow Flag. *Set* by hardware on a timer 2 overflow. TF2 will not be set when either RCLK or TCLK = 1. *Cleared* by user software.
6	EXF2	Timer 2 External Flag. *Set* by hardware when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. *Cleared* by user user software.
5	RCLK	Receive Clock Enable Bit. *Set* by user to enable the serial port to use timer 2 overflow pulses for its receive clock in serial port Modes 1 and 3. *Cleared* by user to enable timer 1 overflow to be used for the receive clock.
4	TCLK	Transmit Clock Enable Bit. *Set* by user to enable the serial port to use timer 2 overflow pulses for its transmit clock in serial port Modes 1 and 3. *Cleared* by user to enable timer 1 overflow to be used for the transmit clock.
3	EXEN2	Timer 2 External Enable Flag. *Set* by user to enable a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. *Cleared* by user for Timer 2 to ignore events at T2EX.
2	TR2	Timer 2 Start/Stop Control Bit. *Set* by user to start timer 2. *Cleared* by user to stop timer 2.
1	CNT2	Timer 2 Timer or Counter Function Select Bit. *Set* by user to select counter function (input from external T2 pin). *Cleared* by user to select timer function (input from on-chip core clock).
0	CAP2	Timer 2 Capture/Reload Select Bit. *Set* by user to enable captures on negative transitions at T2EX if EXEN2 = 1. *Cleared* by user to enable auto-reloads with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to autoreload on Timer 2 overflow.

Timer/Counter 2 Data Registers
Timer/Counter 2 also has two pairs of 8-bit data registers associated with it. These are used as both timer data registers and timer capture/reload registers.

TH2 and TL2
Timer 2, data high byte and low byte.
SFR Address = CDhex, CChex respectively.

RCAP2H and RCAP2L
Timer 2, Capture/Reload byte and low byte.
SFR Address = CBhex, CAhex respectively.

Mode 0: 8-Bit Shift Register Mode
Mode 0 is selected by clearing both the SM0 and SM1 bits in the SFR SCON. Serial data enters and exits through RXD. TXD outputs the shift clock. Eight data bits are transmitted or received. Transmission is initiated by any instruction that writes to SBUF. The data is shifted out of the RXD line. The eight bits are transmitted with the least-significant bit (LSB) first, as shown in Figure 39.

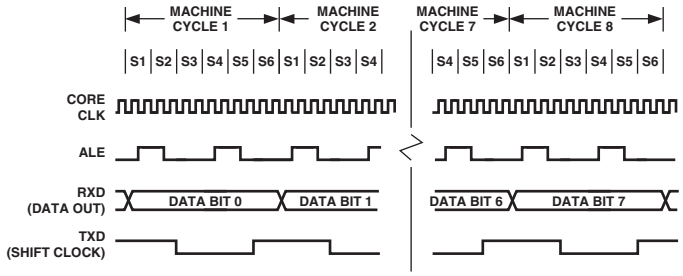


Figure 39. UART Serial Port Transmission, Mode 0

Reception is initiated when the receive enable bit (REN) is 1 and the receive interrupt bit (RI) is 0. When RI is cleared the data is clocked into the RXD line and the clock pulses are output from the TXD line.

Mode 1: 8-Bit UART, Variable Baud Rate
Mode 1 is selected by clearing SM0 and setting SM1. Each data byte (LSB first) is preceded by a start bit(0) and followed by a stop bit(1). Therefore 10 bits are transmitted on TXD or received on RXD. The baud rate is set by the Timer 1 or Timer 2 overflow rate, or a combination of the two (one for transmission and the other for reception).

Transmission is initiated by writing to SBUF. The "write to SBUF" signal also loads a 1 (stop bit) into the ninth bit position of the transmit shift register. The data is output bit by bit until the stop bit appears on TXD and the transmit interrupt flag (TI) is automatically set as shown in Figure 40.

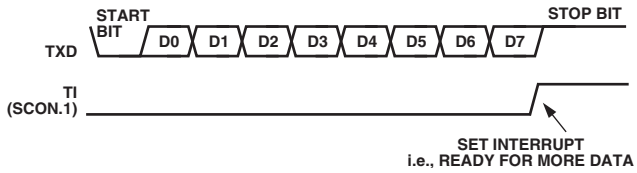


Figure 40. UART Serial Port Transmission, Mode 0

Reception is initiated when a 1-to-0 transition is detected on RXD. Assuming a valid start bit was detected, character reception continues. The start bit is skipped and the eight data bits are clocked into the serial port shift register. When all eight bits have been clocked in, the following events occur:

The eight bits in the receive shift register are latched into SBUF

The ninth bit (Stop bit) is clocked into RB8 in SCON

The Receiver interrupt flag (RI) is set

if, and only if, the following conditions are met at the time the final shift pulse is generated:

RI = 0, and

Either SM2 = 0, or SM2 = 1 and the received stop bit = 1.

If either of these conditions is not met, the received frame is irretrievably lost, and RI is not set.

Mode 2: 9-Bit UART with Fixed Baud Rate
Mode 2 is selected by setting SM0 and clearing SM1. In this mode the UART operates in 9-bit mode with a fixed baud rate. The baud rate is fixed at Core_Clk/64 by default, although by setting the SMOD bit in PCON, the frequency can be doubled to Core_Clk/32. Eleven bits are transmitted or received, a start bit(0), eight data bits, a programmable ninth bit and a stop bit(1). The ninth bit is most often used as a parity bit, although it can be used for anything, including a ninth data bit if required.

To transmit, the eight data bits must be written into SBUF. The ninth bit must be written to TB8 in SCON. When transmission is initiated the eight data bits (from SBUF) are loaded onto the transmit shift register (LSB first). The contents of TB8 are loaded into the ninth bit position of the transmit shift register. The transmission will start at the next valid baud rate clock. The TI flag is set as soon as the stop bit appears on TXD.

Reception for Mode 2 is similar to that of Mode 1. The eight data bytes are input at RXD (LSB first) and loaded onto the receive shift register. When all eight bits have been clocked in, the following events occur:

The eight bits in the receive shift register are latched into SBUF

The ninth data bit is latched into RB8 in SCON

The Receiver interrupt flag (RI) is set

if, and only if, the following conditions are met at the time the final shift pulse is generated:

RI = 0, and

Either SM2 = 0, or SM2 = 1 and the received stop bit = 1.

If either of these conditions is not met, the received frame is irretrievably lost, and RI is not set.

Mode 3: 9-Bit UART with Variable Baud Rate
Mode 3 is selected by setting both SM0 and SM1. In this mode the 8051 UART serial port operates in 9-bit mode with a variable baud rate determined by either Timer 1 or Timer 2. The operation of the 9-bit UART is the same as for Mode 2 but the baud rate can be varied as for Mode 1.

In all four modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

UART Serial Port Baud Rate Generation
Mode 0 Baud Rate Generation
The baud rate in Mode 0 is fixed:

Mode 0 Baud Rate = (Core Clock Frequency[1]/12)

NOTE
[1]In these descriptions Core Clock Frequency refers to the core clock frequency selected via the CD0–2 bits in the PLLCON SFR.

Mode 2 Baud Rate Generation
The baud rate in Mode 2 depends on the value of the SMOD bit in the PCON SFR. If SMOD = 0, the baud rate is 1/64 of the core clock. If SMOD = 1, the baud rate is 1/32 of the core clock:

Mode 2 Baud Rate = $(2^{SMOD}/64) \times$ (Core Clock Frequency)

Modes 1 and 3 Baud Rate Generation
The baud rates in Modes 1 and 3 are determined by the overflow rate in Timer 1 or Timer 2, or both (one for transmit and the other for receive).

IEIP2: **Secondary Interrupt Enable and Priority Register**
SFR Address A9H
Power-On Default Value A0H
Bit Addressable No

---	PTI	PPSM	PSI	---	ETI	EPSM	ESI

Table XXXII. IEIP2 SFR Bit Designations

Bit	Name	Description
7	---	Reserved for Future Use.
6	PTI	Written by User to Select TIC Interrupt Priority ("1" = High; "0" = Low).
5	PPSM	Written by User to Select Power Supply Monitor Interrupt Priority ("1" = High; "0" = Low).
4	PSI	Written by User to Select SPI/I^{2}C Serial Port Interrupt Priority ("1" = High; "0" = Low).
3	---	Reserved, This Bit Must Be "0."
2	ETI	Written by User to Enable "1" or Disable "0" TIC Interrupt.
1	EPSM	Written by User to Enable "1" or Disable "0" Power Supply Monitor Interrupt.
0	ESI	Written by User to Enable "1" or Disable "0" SPI/I^{2}C Serial Port Interrupt.

Interrupt Priority
The Interrupt Enable registers are written by the user to enable individual interrupt sources, while the Interrupt Priority registers allow the user to select one of two priority levels for each interrupt. An interrupt of a high priority may interrupt the service routine of a low priority interrupt, and if two interrupts of different priority occur at the same time, the higher level interrupt will be serviced first. An interrupt cannot be interrupted by another interrupt of the same priority level. If two interrupts of the same priority level occur simultaneously, a polling sequence is observed as shown in Table XXXIII.

Table XXXIII. Priority within an Interrupt Level

Source	Priority	Description
PSMI	1 (Highest)	Power Supply Monitor Interrupt
WDS	2	Watchdog Interrupt
IE0	3	External Interrupt 0
RDY0/RDY1	4	ADC Interrupt
TF0	5	Timer/Counter 0 Interrupt
IE1	6	External Interrupt 1
TF1	7	Timer/Counter 1 Interrupt
I2CI + ISPI	8	I^{2}C/SPI Interrupt
RI + TI	9	Serial Interrupt
TF2 + EXF2	10	Timer/Counter 2 Interrupt
TII	11 (Lowest)	Time Interval Counter Interrupt

Interrupt Vectors
When an interrupt occurs the program counter is pushed onto the stack and the corresponding interrupt vector address is loaded into the program counter. The interrupt vector addresses are shown in Table XXXIV.

Table XXXIV. Interrupt Vector Addresses

Source	Vector Address
IE0	0003 Hex
TF0	000B Hex
IE1	0013 Hex
TF1	001B Hex
RI + TI	0023 Hex
TF2 + EXF2	002B Hex
RDY0/RDY1 (ADC)	0033 Hex
II^{2}C + ISPI	003B Hex
PSMI	0043 Hex
TII	0053 Hex
WDS (WDIR = 1)*	005B Hex

*The watchdog can be configured to generate an interrupt instead of a reset when it times out. This is used for logging errors or to examine the internal status of the microcontroller core to understand, from a software debug point of view, why a watchdog timeout occurred. The watchdog interrupt is slightly different from the normal interrupts in that its priority level is always set to 1 and it is not possible to disable the interrupt via the global disable bit (EA) in the IE SFR. This is done to ensure that the interrupt will always be responded to if a watchdog timeout occurs. The watchdog will only produce an interrupt if the watchdog timeout is greater than zero.

It should also be noted that variations in the excitation current do not affect the measurement system, as the input voltage from the RTD and reference voltage across R1 vary ratiometrically with the excitation current. Resistor R1 must, however, have a low temperature coefficient to avoid errors in the reference voltage over temperature.

QUICKSTART DEVELOPMENT SYSTEM

The QuickStart Development System is a full featured, low cost development tool suite supporting the ADuC816. The system consists of the following PC-based (Windows-compatible) hardware and software development tools.

Hardware:	ADuC816 Evaluation Board, Plug-In Power Supply and Serial Port Cable
Code Development:	8051 Assembler C Compiler (2 Kcode Limited)
Code Functionality:	ADSIM, Windows MicroConverter Code Simulator
In-Circuit Code Download:	Serial Downloader
In-Circuit Debugger:	Serial Port Debugger
Misc. Other:	CD-ROM Documentation and Two Additional Prototype Devices

Figures 53 shows the typical components of a QuickStart Development System while Figure 54 shows a typical debug session. A brief description of some of the software tools' components in the QuickStart Development System is given below.

Figure 53. Components of the QuickStart Development System

Download—In-Circuit Serial Downloader

The Serial Downloader is a software program that allows the user to serially download an assembled program (Intel Hex format file) to the on-chip program FLASH memory via the serial COM1 port on a standard PC. An Application Note (uC004) detailing this serial download protocol is available from www.analog.com/microconverter.

DeBug—In-Circuit Debugger

The Debugger is a Windows application that allows the user to debug code execution on silicon using the MicroConverter UART serial port. The debugger provides access to all on-chip peripherals during a typical debug session as well as single-step and break-point code execution control.

ADSIM—Windows Simulator

The Simulator is a Windows application that fully simulates all the MicroConverter functionality including ADC and DAC peripherals. The simulator provides an easy-to-use, intuitive, interface to the MicroConverter functionality and integrates many standard debug features; including multiple breakpoints, single stepping; and code execution trace capability. This tool can be used both as a tutorial guide to the part as well as an efficient way to prove code functionality before moving to a hardware platform.

The QuickStart development tool-suite software is freely available at the Analog Devices MicroConverter Website www.analog.com/microconverter.

Figure 54. Typical Debug Session