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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	CANbus, SCI
Peripherals	POR, PWM, WDT
Number of I/O	53
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BFQFP
Supplier Device Package	100-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd64f7047fw40v

Instruction Code Format:

Item	Format	Explanation
Instruction	Described in mnemonic. `OP.Sz SRC,DEST`	OP: Operation code Sz: Size SRC: Source DEST: Destination Rm: Source register Rn: Destination register imm: Immediate data disp: Displacement*2
Instruction code	Described in MSB ↔ LSB order	mmmm: Source register nnnn: Destination register 0000: R0 0001: R1 . . . 1111: R15 iiii: Immediate data dddd: Displacement
Outline of the Operation	→, ←	Direction of transfer
	(xx)	Memory operand
	M/Q/T	Flag bits in the SR
	&	Logical AND of each bit
	|	Logical OR of each bit
	^	Exclusive OR of each bit
	~	Logical NOT of each bit
	<<n	n-bit left shift
	>>n	n-bit right shift
Execution states	—	Value when no wait states are inserted*1
T bit	—	Value of T bit after instruction is executed. An em-dash (—) in the column means no change.

Notes: 1. Instruction execution states: The execution states shown in the table are minimums. The actual number of states may be increased when (1) contention occurs between instruction fetches and data access, or (2) when the destination register of the load instruction (memory → register) equals to the register used by the next instruction.

2. Depending on the operand size, displacement is scaled by ×1, ×2, or ×4. For details, refer the *SH-1/SH-2/SH-DSP Programming Manual*.

6.3.4 Interrupt Priority Registers A, D to I, K (IPRA, IPRD to IPRI, IPRK)

Interrupt priority registers are nine 16-bit readable/writable registers that set priority levels from 0 to 15 for interrupts except NMI. For the correspondence between interrupt request sources and IPR, refer to table 6.2 Interrupt Request Sources, Vector Address, and Interrupt Priority Level. Each of the corresponding interrupt priority ranks are established by setting a value from H'0 to H'F in each of the four-bit groups 15 to 12, 11 to 8, 7 to 4 and 3 to 0. Reserved bits that are not assigned should be set H'0 (B'0000.)

Bit	Bit Name	Initial Value	R/W	Description
15	IPR15	0	R/W	These bits set priority levels for the corresponding interrupt source. 0000: Priority level 0 (lowest) 0001: Priority level 1 0010: Priority level 2 0011: Priority level 3 0100: Priority level 4 0101: Priority level 5 0110: Priority level 6 0111: Priority level 7 1000: Priority level 8 1001: Priority level 9 1010: Priority level 10 1011: Priority level 11 1100: Priority level 12 1101: Priority level 13 1110: Priority level 14 1111: Priority level 15 (highest)
14	IPR14	0	R/W	
13	IPR13	0	R/W	
12	IPR12	0	R/W	
11	IPR11	0	R/W	These bits set priority levels for the corresponding interrupt source. 0000: Priority level 0 (lowest) 0001: Priority level 1 0010: Priority level 2 0011: Priority level 3 0100: Priority level 4 0101: Priority level 5 0110: Priority level 6 0111: Priority level 7 1000: Priority level 8 1001: Priority level 9 1010: Priority level 10 1011: Priority level 11 1100: Priority level 12 1101: Priority level 13 1110: Priority level 14 1111: Priority level 15 (highest)
10	IPR10	0	R/W	
9	IPR9	0	R/W	
8	IPR8	0	R/W	

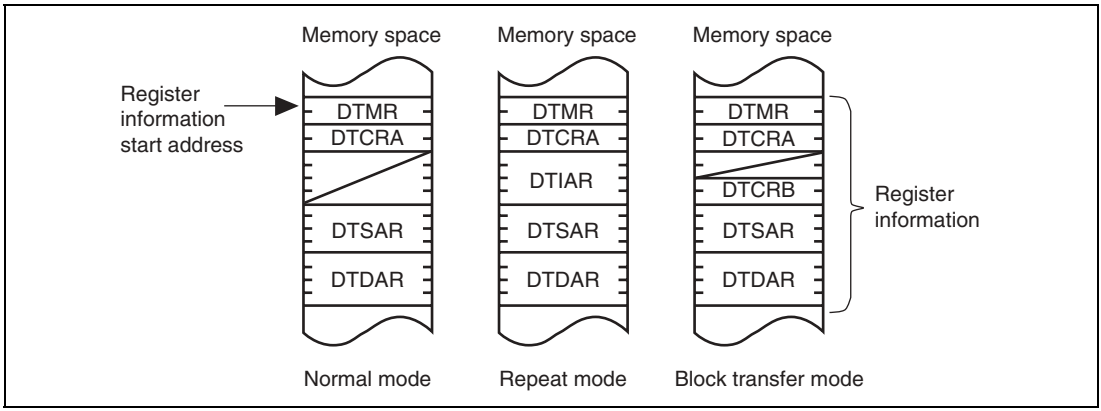


Figure 8.3 DTC Register Information Allocation in Memory Space

Figure 8.4 shows the correspondence between DTC vector addresses and register information allocation. For each DTC activating source there are 2 bytes in the DTC vector table, which contain the register information start address.

Table 8.1 shows the correspondence between activating sources and vector addresses. When activating with software, the vector address is calculated as H'0400 + DTVEC[7:0].

Through DTC activation, a register information start address is read from the vector table, then register information placed in memory space is read from that register information start address. Always designate register information start addresses in multiples of four.

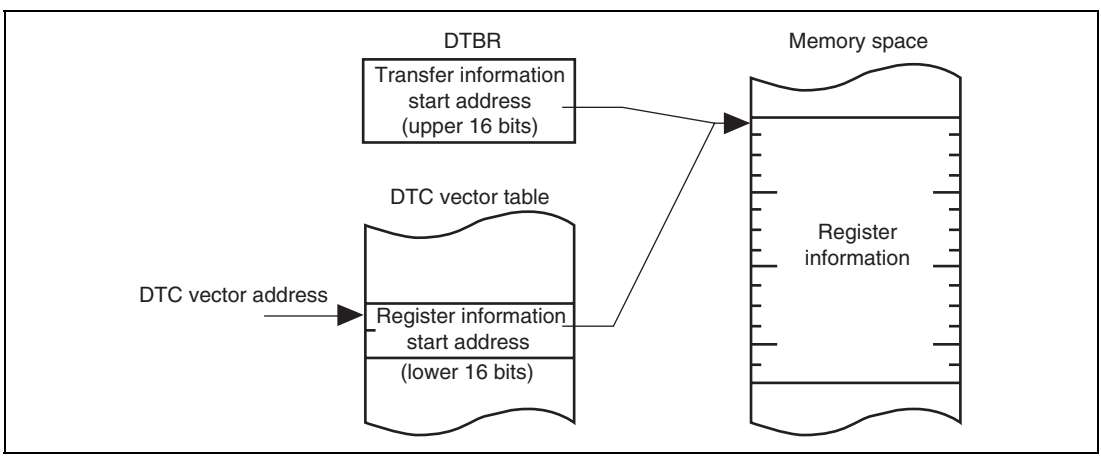


Figure 8.4 Correspondence between DTC Vector Address and Transfer Information

10.2 Input/Output Pins

Table 10.2 MTU Pins

Channel	Symbol	I/O	Function
Common	TCLKA	Input	External clock A input pin (Channel 1 phase counting mode A phase input)
	TCLKB	Input	External clock B input pin (Channel 1 phase counting mode B phase input)
	TCLKC	Input	External clock C input pin (Channel 2 phase counting mode A phase input)
	TCLKD	Input	External clock D input pin (Channel 2 phase counting mode B phase input)
0	TIOC0A	I/O	TGRA_0 input capture input/output compare output/PWM output pin
	TIOC0B	I/O	TGRB_0 input capture input/output compare output/PWM output pin
	TIOC0C	I/O	TGRC_0 input capture input/output compare output/PWM output pin
	TIOC0D	I/O	TGRD_0 input capture input/output compare output/PWM output pin
1	TIOC1A	I/O	TGRA_1 input capture input/output compare output/PWM output pin
	TIOC1B	I/O	TGRB_1 input capture input/output compare output/PWM output pin
2	TIOC2A	I/O	TGRA_2 input capture input/output compare output/PWM output pin
	TIOC2B	I/O	TGRB_2 input capture input/output compare output/PWM output pin
3	TIOC3A	I/O	TGRA_3 input capture input/output compare output/PWM output pin
	TIOC3B	I/O	TGRB_3 input capture input/output compare output/PWM output pin
	TIOC3C	I/O	TGRC_3 input capture input/output compare output/PWM output pin
	TIOC3D	I/O	TGRD_3 input capture input/output compare output/PWM output pin
4	TIOC4A	I/O	TGRA_4 input capture input/output compare output/PWM output pin
	TIOC4B	I/O	TGRB_4 input capture input/output compare output/PWM output pin
	TIOC4C	I/O	TGRC_4 input capture input/output compare output/PWM output pin
	TIOC4D	I/O	TGRD_4 input capture input/output compare output/PWM output pin

Operation when Error Occurs during Normal Mode Operation, and Operation is Restarted in Phase Counting Mode: Figure 10.88 shows an explanatory diagram of the case where an error occurs in normal mode and operation is restarted in phase counting mode after re-setting.

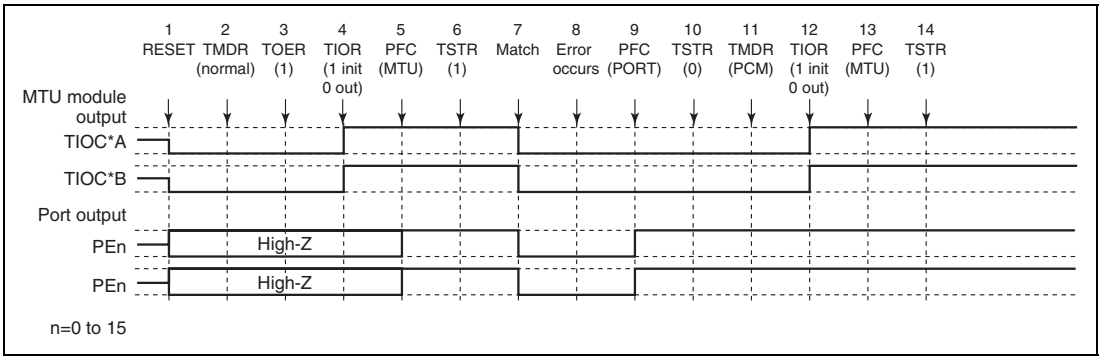


Figure 10.88 Error Occurrence in Normal Mode, Recovery in Phase Counting Mode

1 to 10 are the same as in Figure 10.85.

11. Set phase counting mode.
12. Initialize the pins with TIOR.
13. Set MTU output with the PFC.
14. Operation is restarted by TSTR.

Note: Phase counting mode can only be set for channels 1 and 2, and therefore TOER setting is not necessary.

Section 15 Controller Area Network 2 (HCAN2)

The Controller Area Network 2 (HCAN2) is a module for controlling a controller area network (CAN) for realtime communication in vehicular and industrial equipment systems, etc. For details on CAN specification, refer to Bosch CAN Specification Version 2.0 1991, Robert Bosch GmbH.

The block diagram of the HCAN2 is shown in figure 15.1.

15.1 Features

- CAN version: Bosch 2.0B active compatible (conform to ISO-11898 specification)
  Communication systems: NRZ (Non-Return to Zero) system (with bit-stuffing function)
  Broadcast communication system
  Transmission path: Bidirectional 2-wire serial communication
  Communication speed: Max. 1 Mbps
  Data length: 0 to 8 bytes
- Number of channels: 1 channel
- Data buffers: 32 buffers (two receive-only buffer and 30 buffers settable for transmission/reception)
- Data transmission: Can select from two methods
  Mailbox (buffer) number order (high-to-low)
  Message priority (identifier) reverse-order (high-to-low)
- Data reception: Two methods
  Message identifier match (transmit/receive-setting buffers)
  Reception with message identifier masked (receive-only)
- Interrupt sources: 14 (allocate to four independent interrupt vectors)
  Error interrupt
  Reset processing interrupt
  Message reception interrupt
  Message transmission interrupt
- HCAN2 operating modes
  Hardware reset
  Software reset
  Normal status (error-active, error-passive)
  Bus off status
  HCAN2 configuration mode
  HCAN2 sleep mode
  HCAN2 halt mode

- Other feature

  The DTC can be activated by message receive mailbox (HCAN2 mailbox 0 only)
- Module standby mode can be set
- Read section 15.8, Usage Notes.

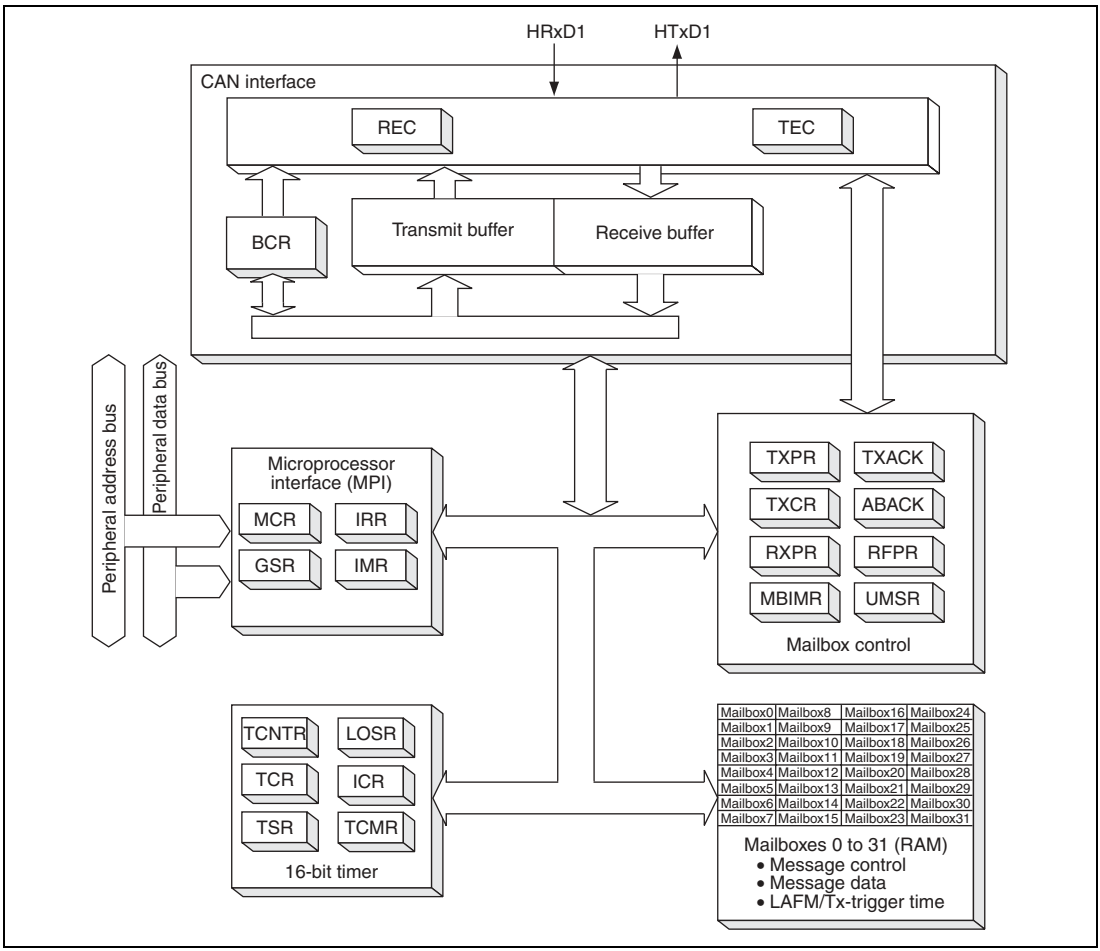


Figure 15.1 HCAN2 Block Diagram

Microprocessor Interface (MPI): The MPI allows communication between the CPU and HCAN2's registers/mailboxes to control the timer unit and memory interface. It also contains the wakeup control logic that detects the CAN bus activities and notifies to the MPI and other parts of the HCAN2 so that the HCAN2 can automatically exit HCAN2 sleep mode.

Mailbox (MB): The mailbox is essentially arrayed on the RAM as message buffers. There are 32 mailboxes, and each mailbox has the following information.

- CAN message control

Bit	Bit Name	Initial Value	R/W	Description
4	GSR4	0	R	Halt/Sleep Status Bit Indicates whether the HCAN2 interface is in halt mode or sleep mode. 0: Not in halt or sleep mode 1: In halt (MCR1 = 1) or sleep (MCR5 = 1) mode [Setting condition] • MCR1 or MCR5 is set, and CAN bus is suspended or in the idle state.
3	GSR3	1	R	Reset Status Bit Indicates whether the HCAN2 module is in the normal operating state or the reset state. [Setting condition] • When entering configuration mode after the HCAN2 internal reset has finished [Clearing condition] • When entering normal operation mode after the MCR0 bit in MCR is cleared to 0 (Note that there is a delay between clearing of the MCR0 bit and the GSR3 bit.)
2	GSR2	1	R	Message Transmission Status Flag Flag that indicates whether the module is currently in the message transmission period. [Setting condition] • No message transmission requests [Clearing condition] • Transmission is in progress
1	GSR1	0	R	Transmit/Receive Warning Flag [Clearing conditions] • When TEC < 96 and REC < 96 • When TEC ≥ 256 [Setting condition] • When 256 > TEC ≥ 96 or 256 >REC ≥ 96

15.3.10 Transmit Acknowledge Registers (TXACK1, TXACK0)

TXACK1 and TXACK0 are 16-bit registers containing status flags that indicate normal transmission of mailbox transmit messages.

- TXACK1

Bit	Bit Name	Initial Value	R/W	Description
15	TXACK31	0	R/W	Status flags that indicate error-free transmission of the transmit message in the corresponding mailboxes from 16 to 31. When the message in mailbox n (n = 16 to 31) has been transmitted error-free, TXACKn is set to 1. [Setting condition] • Completion of message transmission for corresponding mailbox [Clearing condition] • Writing 1 Notes: 1. Writing operation by the CPU is valid only for clearing condition (writing 1) of set status. 2. Restrictions apply to the use of the mailbox 31 for transmission. Carefully read section 15.8, Usage Notes.
14	TXACK30	0	R/W	
13	TXACK29	0	R/W	
12	TXACK28	0	R/W	
11	TXACK27	0	R/W	
10	TXACK26	0	R/W	
9	TXACK25	0	R/W	
8	TXACK24	0	R/W	
7	TXACK23	0	R/W	
6	TXACK22	0	R/W	
5	TXACK21	0	R/W	
4	TXACK20	0	R/W	
3	TXACK19	0	R/W	
2	TXACK18	0	R/W	
1	TXACK17	0	R/W	
0	TXACK16	0	R/W	

the mailbox empty interrupt bit (IMR8) in the interrupt mask register (IMR) are both simultaneously set to enable interrupts, interrupts may be sent to the CPU.

However, a transmit wait message cannot be canceled at the following times:

- During internal arbitration or CAN bus arbitration
- During data frame or remote frame transmission

Figure 15.9 shows a flowchart for transmit message cancellation.

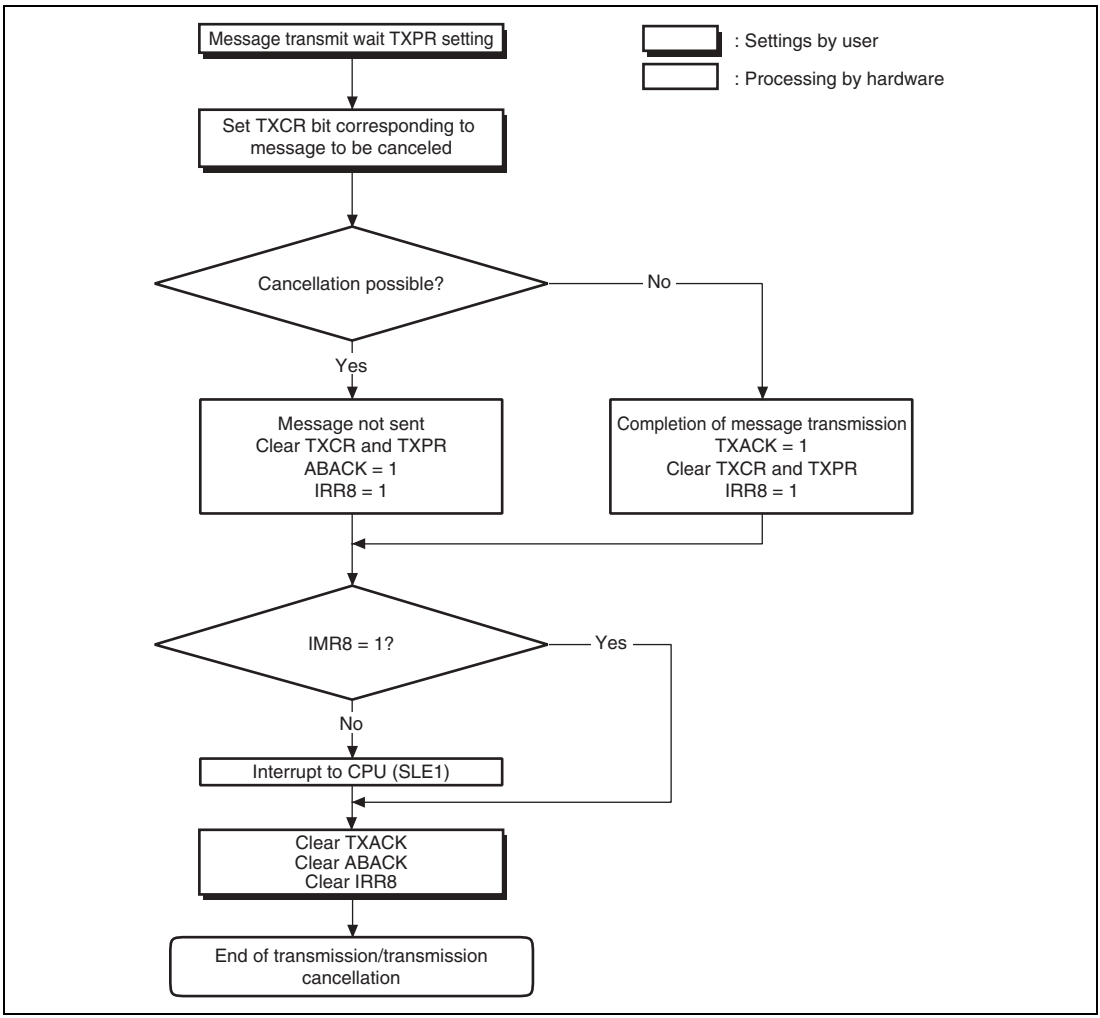


Figure 15.9 Transmit Message Cancellation Flowchart

- Remote frame reception

  Two kinds of messages—data frames and remote frames—can be stored in mailboxes. A remote frame differs from a data frame in that the value of the remote transmission request bit (RTR) in the message control and the data field are 0 bytes long. The data length to be returned in a data frame must be stored in the data length code (DLC) in the control field.

  When a remote frame (RTR = recessive) is received, the corresponding bit is set in the remote request wait register (RFPR). If the corresponding bit (MBIMR0 to MBIMR31) in the mailbox interrupt mask register (MBIMR) and the remote frame request interrupt mask (IRR2) in the interrupt mask register (IMR) are set to the interrupt enable value at this time, an interrupt request (RM1) can be sent to the CPU.

Unread Message Overwrite: If the receive message identifier matches the mailbox identifier, the receive message is stored in the mailbox regardless of whether the mailbox contains an unread message or not. If a message overwrite occurs, the corresponding bit (UMSR0 to UMSR31) is set in the unread message register (UMSR). In overwriting an unread message, when a new message is received before the corresponding bit in the receive complete register (RXPR) has been cleared, the unread message register (UMSR) is set. If the unread interrupt flag (IRR9) in the interrupt mask register (IMR) is set to the interrupt enable value at this time, an interrupt can be sent to the CPU. Figure 15.11 shows a flowchart for unread message overwriting.

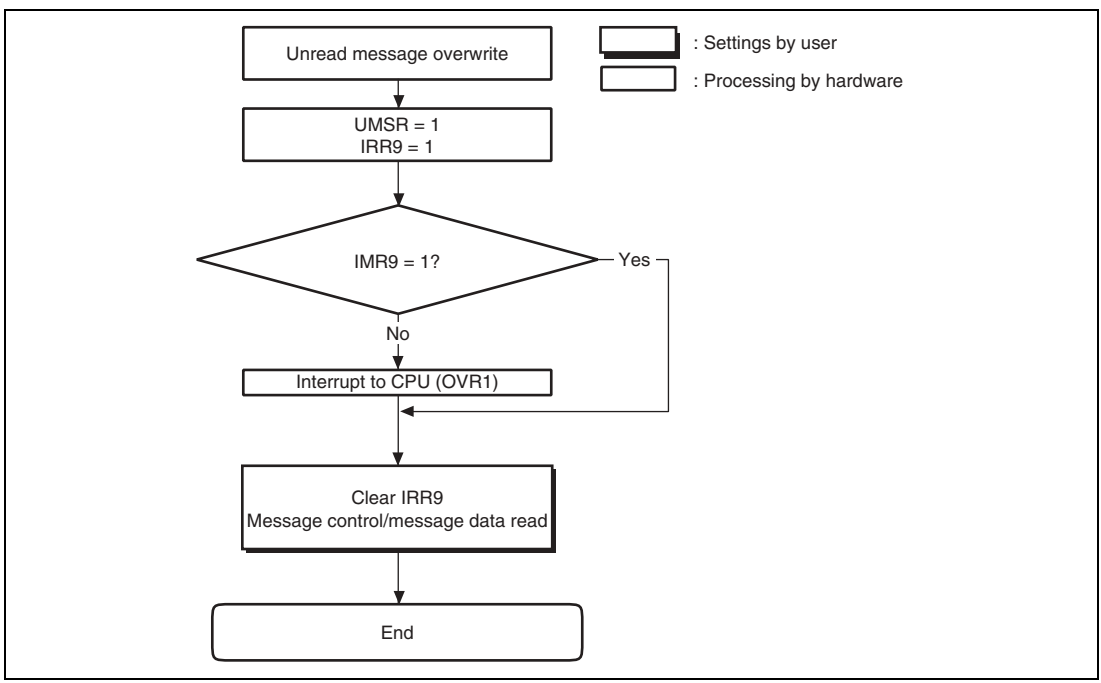


Figure 15.11 Unread Message Overwrite Flowchart

16.6.2 Interrupt Signal Timing

Timing of TGF Flag Setting by Compare Match: Figure 16.12 shows the timing of setting of the TGF flag in the timer status register (TSR) on a compare match between TCNT and TPDR, and the timing of the TGI interrupt request signal. The timing is the same for a compare match between TCNT and 2Td.

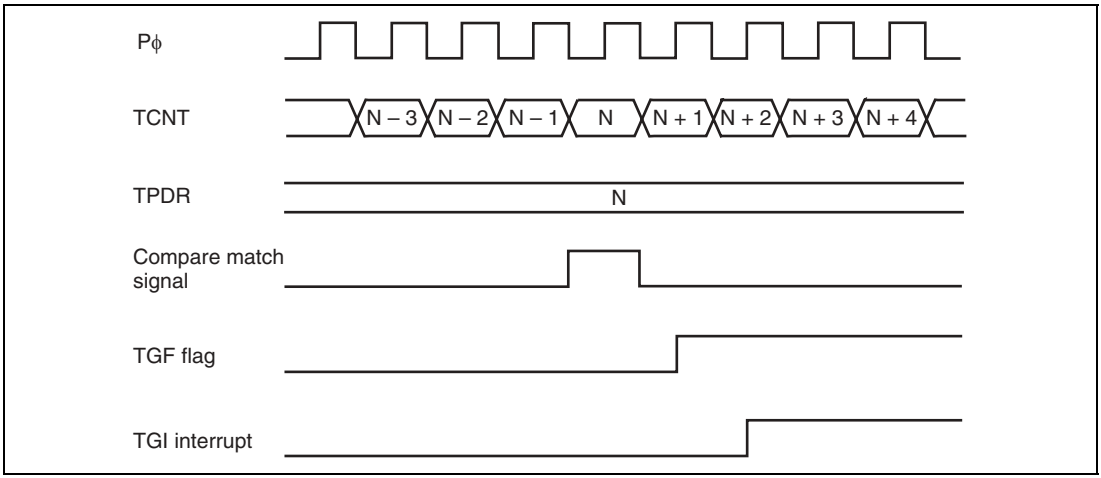


Figure 16.12 TGI Interrupt Timing

Status Flag Clearing Timing: A status flag is cleared when the CPU reads 1 from the flag, then 0 is written to it. When the DTC controller is activated, the flag is cleared automatically. Figure 16.13 shows the timing of status flag clearing by the CPU, and figure 16.14 shows the timing of status flag clearing by the DTC.

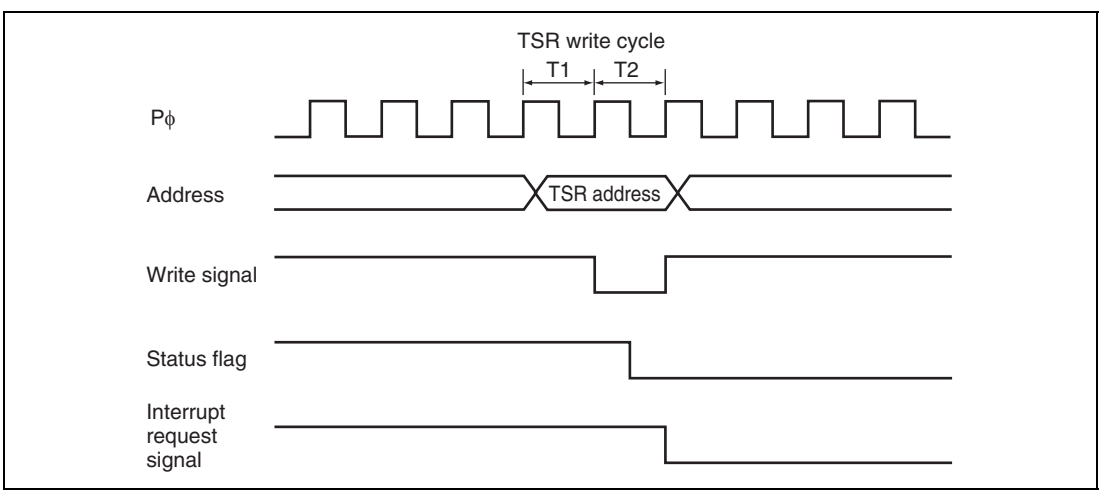


Figure 16.13 Timing of Status Flag Clearing by CPU

Table 19.4 Boot Mode Operation

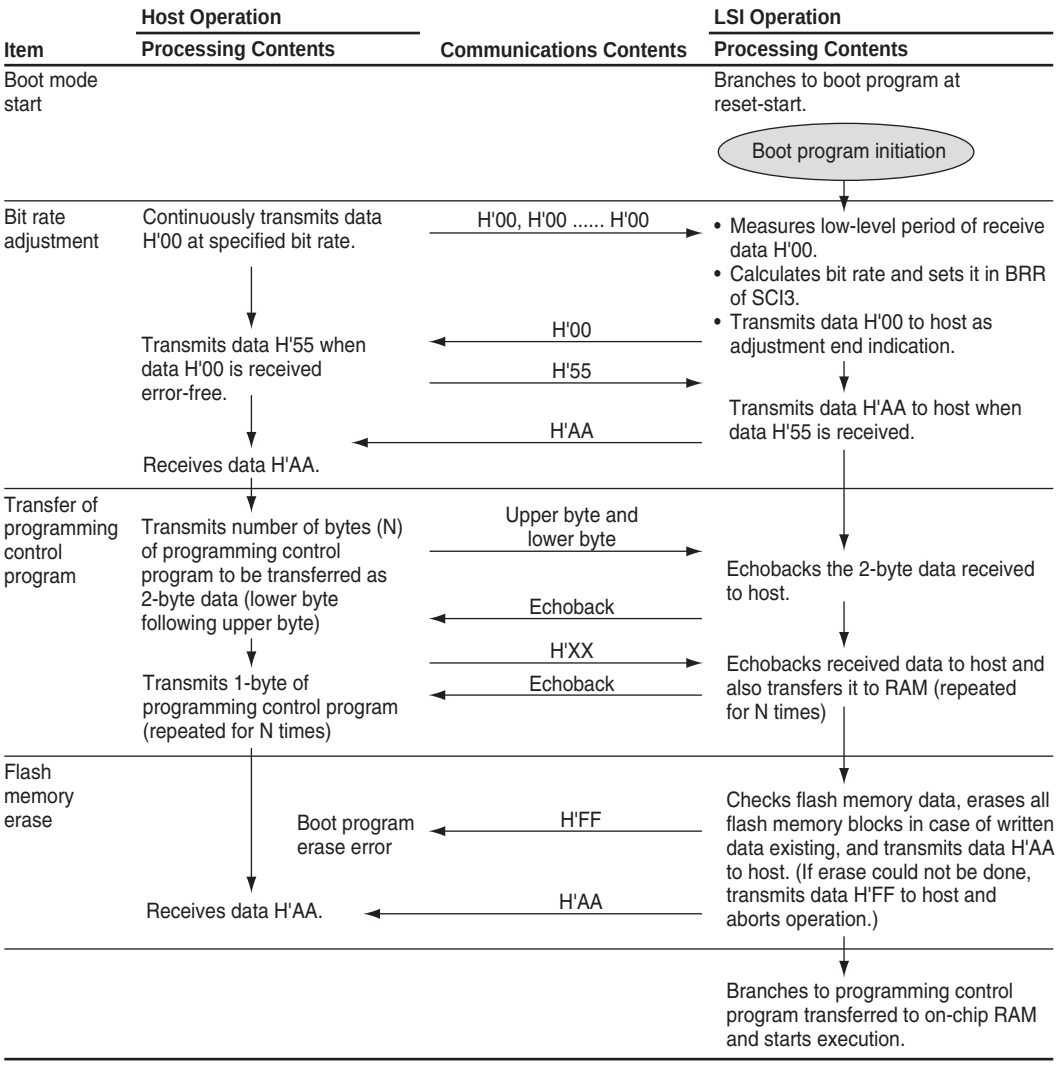
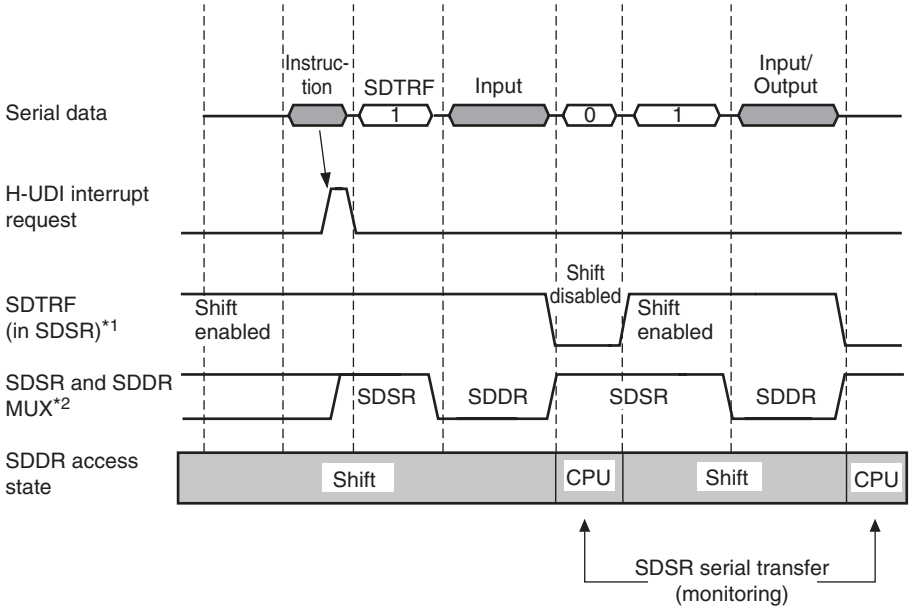


Table 19.5 Peripheral Clock (Pϕ) Frequencies for which Automatic Adjustment of LSI Bit Rate is Possible

Host Bit Rate	Peripheral Clock Frequency Range of LSI
9,600 bps	4 to 40 MHz
19,200 bps	8 to 40 MHz



Notes: *1 SDTRF flag (in SDSR): Indicates whether SDDR access by the CPU or serial transfer data input/output to SDDR is possible.

1	SDDR is shift-enabled. Do not access SDDR until SDTRF = 0.
0	SDDR is shift-disabled. SDDR access by the CPU is enabled.

Conditions:
- SDTRF = 1
  - — When $\overline{\text{TRST}}$ = 0
  - — When the CPU writes 1
  - — In bypass mode
- SDTRF = 0
  - — End of SDDR shift access in serial transfer

*2 SDSR/SDDR (Update-DR state) internal MUX switchover timing
- Switchover from SDSR to SDDR: On completion of serial transfer in which SDTRF = 1 is output from TDO
- Switchover from SDDR to SDSR: On completion of serial transfer to SDDR

Figure 22.2 Data Input/Output Timing Chart (1)

23.5 Usage Notes

23.5.1 Initialization

The debugger's internal buffers and processing states are initialized in the following cases:

1. In a power-on reset
2. In hardware standby mode
3. When $\overline{\text{AUDRST}}$ is driven low
4. When the AUDSRST bit in the SYSCR register is cleared to 0 (see section 24.2.2)
5. When the MSTP3 bit in the MSTCR2 register is set to 1 (see section 24.2.3)

23.5.2 Operation in Software Standby Mode

The debugger is not initialized in software standby mode. However, since this LSI's internal operation halts in software standby mode:

1. When AUDMD is high (RAM monitor mode), Ready is not returned (Not Ready continues to be returned).

   However, when operating on an external input clock, the protocol continues.
2. When AUDMD is low (branch trace mode), operation stops. However, operation continues when software standby is released.

23.5.3 Setting the PA15/CK/$\overline{\text{POE6}}$/$\overline{\text{TRST}}$/$\overline{\text{BACK}}$ pin

There is a debugging tool for generating the AUDCK signal from the CK signal. See the manual of the debugging tool to set the pin function controller (PFC).

23.5.4 Pin States

1. HSTBY/module standby

AUDMD	Z
AUDCK	Z
$\overline{\text{AUDSYNC}}$	Z
AUDATA	Z

2. $\overline{\text{AUDRST}}$ = low-level input

AUDMD	Input	
AUDCK	(1) AUDMD = high: Input	(2) AUDMD = low: High-level Output
$\overline{\text{AUDSYNC}}$	(1) AUDMD = high: Input	(2) AUDMD = low: High-level Output
$\overline{\text{AUDRST}}$	Low-level input	

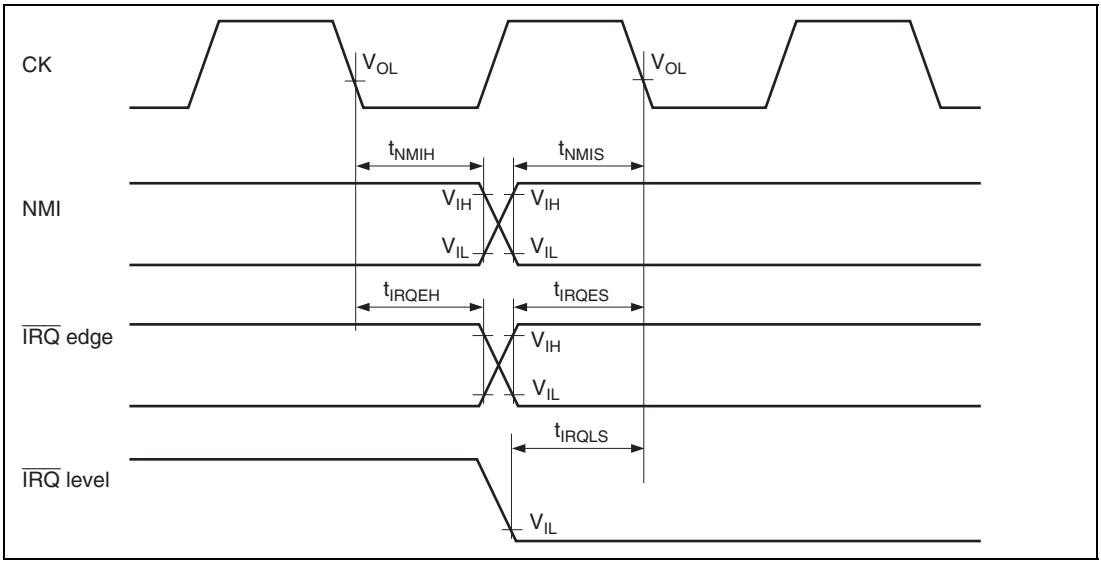


Figure 25.7 Interrupt Signal Input Timing

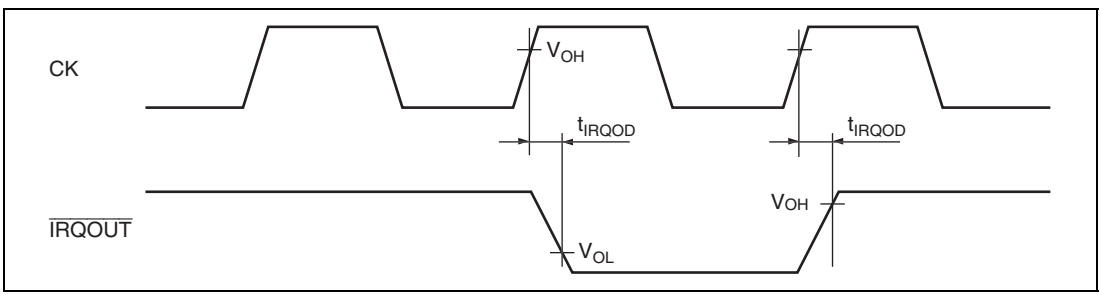


Figure 25.8 Interrupt Signal Output Timing

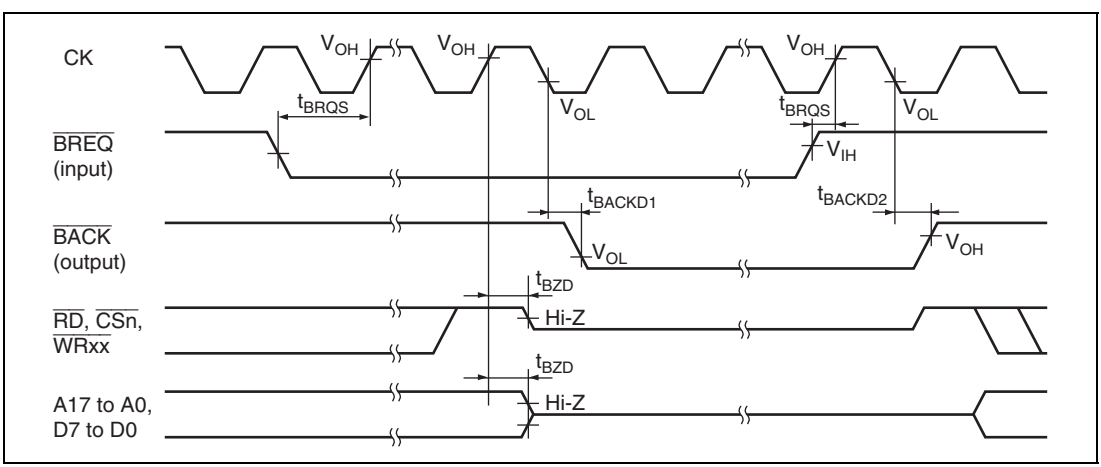


Figure 25.9 Bus Release Timing

25.3.6 I/O Port Timing

Table 25.8 shows I/O port timing.

Table 25.8 I/O Port Timing

Conditions: V_{CC} = 5.0 V ±0.5 V, AV_{CC} = 5.0 V ±0.5 V, V_{SS} = $PLLV_{SS}$ = AV_{SS} = 0 V, T_a = –20°C to +75°C (Standard product)*, T_a = –40°C to +85°C (Wide temperature-range product)*.

Item	Symbol	Min	Max	Unit	Figures
Port output data delay time	t_{PWD}	—	100	ns	Figure 25.15
Port input hold time	t_{PRH}	19	—	ns	
Port input setup time	t_{PRS}	19	—	ns	

[Operating precautions]

The port input signals are asynchronous. They are, however, considered to have been changed at CK clock falling edge with two-state intervals shown in figure 25.15. If the setup times shown here are not observed, recognition may be delayed until the clock falling two states after that timing.

Note: * See page 2 for correspondence of the standard product, wide temperature-range product, and product model name.

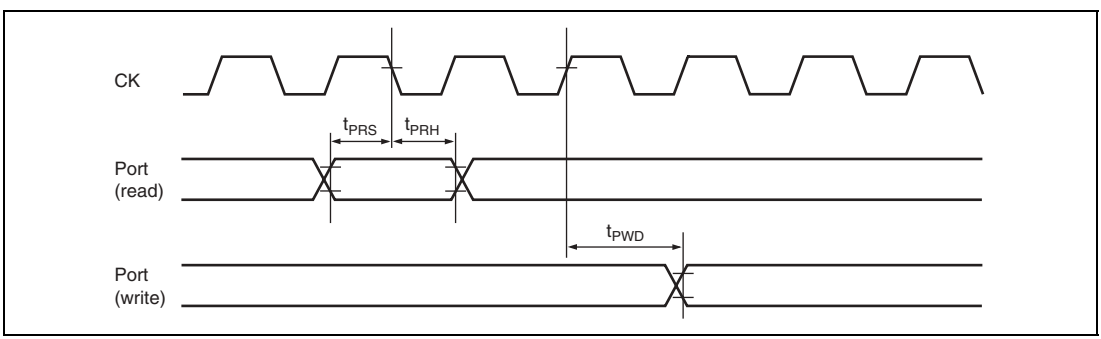
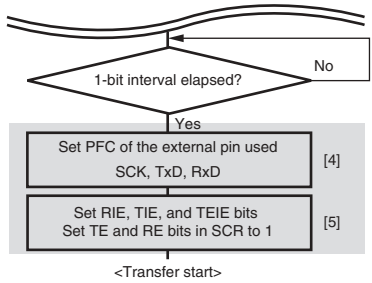


Figure 25.15 I/O Port Input/Output timing

Item	Page	Revisions (See Manual for Details)
Figure 12.15 Sample SCI Initialization Flowchart	369	 Description [4] deleted.
13.3.2 A/D Control/Status Registers 0, 1 (ADCSR_0, ADCSR_1)	383	**Bit** / **Bit Name** / **Initial Value** / **R/W** / **Description** 7 / ADF / 0 / R/(W)* / A/D End Flag A status flag that indicates the end of A/D conversion. [Setting conditions] • When A/D conversion ends in single mode • When A/D conversion ends on all specified channels in scan mode [Clearing conditions] • When 0 is written after reading ADF = 1 • When the DTC is activated by an ADI interrupt and ADDR is read with the DISEL bit in DTMR of DTC = 0
14.2.2 Compare Match Timer Control/Status Register_0 and 1 (CMCSR_0, CMCSR_1)	399	**Bit** / **Bit Name** / **Initial Value** / **R/W** / **Description** 7 / CMF / 0 / R/(W)* / Compare Match Flag This flag indicates whether or not the CMCNT and CMCOR values have matched. 0: CMCNT and CMCOR values have not matched 1: CMCNT and CMCOR values have matched [Clearing conditions] • Write 0 to CMF after reading 1 from it • When the DTC is activated by an CMI interrupt and data is transferred with the DISEL bit in DTMR of DTC = 0