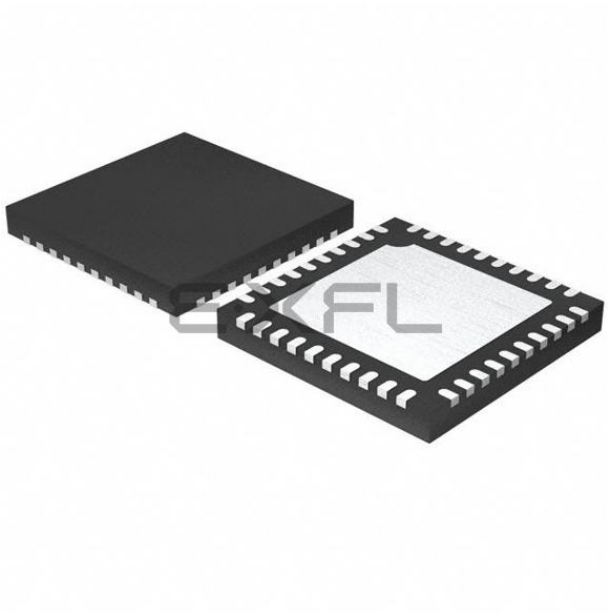


Welcome to E-XFL.COM

Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

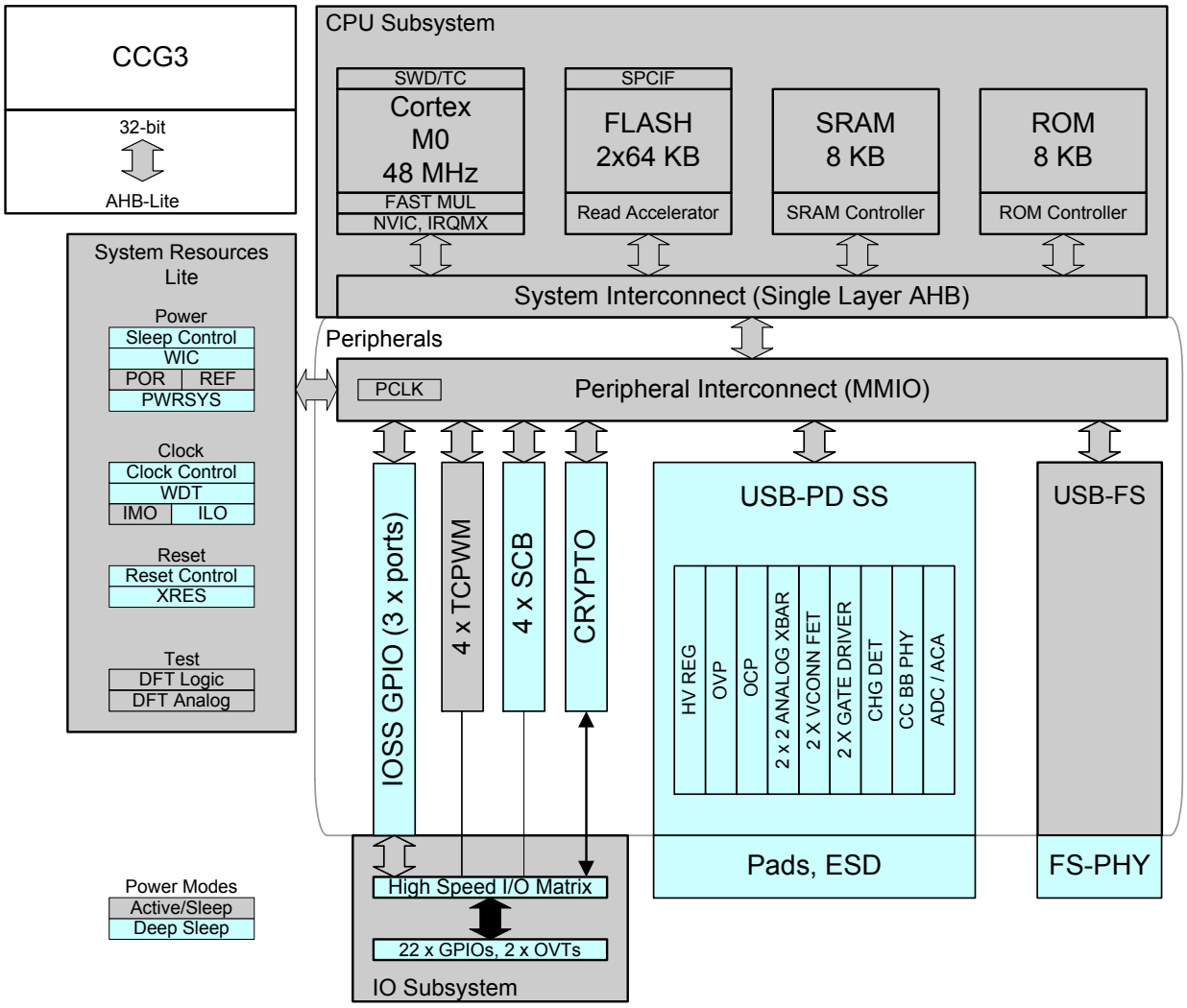
Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	USB Type C
Core Processor	ARM® Cortex®-M0
Program Memory Type	FLASH (128kB)
Controller Series	-
RAM Size	8K x 8
Interface	I²C, SPI, UART/USART, USB
Number of I/O	16
Voltage - Supply	2.7V ~ 21.5V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cypd3120-40lqxi

Contents

EZ-PD CCG3 Block Diagram

Figure 1. EZ-PD CCG3 Block Diagram[1]



Note
1. See Acronyms section for more details.

The I^2C port on SCB 1-3 blocks of EZ-PD CCG3 are not completely compliant with the I^2C specification in the following aspects:

- The GPIO cells for SCB 1's I^2C port are not overvoltage-tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I^2C system.
- Fast-mode Plus has an I_{OL} specification of 20 mA at a V_{OL} of 0.4V. The GPIO cells can sink a maximum of 8-mA I_{OL} with a V_{OL} maximum of 0.6V.
- Fast-mode and Fast-mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the bus load.

Timer/Counter/PWM Block (TCPWM)

EZ-PD CCG3 has four TCPWM blocks. Each implements a 16-bit timer, counter, pulse-width modulator (PWM), and quadrature decoder functionality.

GPIO

EZ-PD CCG3 has up to 20 GPIOs (these GPIOs can be configured for GPIOs, SCB, SBU, and Aux signals) and SWD pins, which can also be used as GPIOs. The I^2C pins from SCB 0 are overvoltage-tolerant.

The GPIO block implements the following:

- Seven drive strength modes:
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode)
- Selectable slew rates for dV/dt related noise control to improve EMI

During power-on and reset, the I/O pins are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Pinouts

Table 2. CCG3 Pin Description for 42-CSP, 32-QFN and 40-QFN Devices

Pin Map 42-CSP	Pin Map 32-QFN	Pin Map 40-QFN	Name	Description
A5	N/A	1	VBUS_P_CTRL1	VBUS Gate Driver Control 1 for Producer Switch
A6	1	2	VBUS_P_CTRL0	VBUS Gate Driver Control 0 for Producer Switch
B6	2	3	CC2	USB PD connector detect/Configuration Channel 2
C5	N/A	N/A	CC2	USB PD connector detect/Configuration Channel 2
D4	3	4	V5V	5.0V – 5.5V supply for VCONN FETs
C6	4	5	CC1	USB PD connector detect/Configuration Channel 1
D6	N/A	N/A	CC1	USB PD connector detect/Configuration Channel 1
E6	N/A	6	VCONN	VCONN Input - provides Ra termination for cable applications
F6	5	7	P1.0	GPIO/UART_2_TX / SPI_2_MISO
D5	N/A	8	P1.1	GPIO/UART_2_RX / SPI_2_SEL
E5	6	9	P1.2	GPIO/UART_0_RX/ UART_3_CTS/ SPI_3_MOSI/ I2C_3_SCL / HPD
G6	7	10	P1.3	GPIO/UART_0_TX/ UART_3_RTS/ SPI_3_CLK/ I2C_3_SDA
E4	N/A	11	AUX_P / P1.6	DisplayPort AUX_P signal / GPIO / UART_1_TX / SPI_1_MISO
F5	8	12	SBU1 / P1.4	USB Type-C SBU1 signal / GPIO / UART_3_TX/ SPI_3_MISO/ SWD_1_CLK
G5	9	13	SBU2 / P1.5	USB Type-C SBU2 signal / GPIO / UART_3_RX/ SPI_3_SEL/ SWD_1_DAT
G4	N/A	14	AUX_N / P1.7	DisplayPort AUX_N signal / GPIO / UART_1_RX / SPI_1_SEL
F4	10	15	P2.0	GPIO / UART_1_CTS / SPI_1_CLK/ I2C_1_SCL / SWD_0_DAT
G3	11	16	P2.1	GPIO / UART_1_RTS / SPI_1_MOSI/ I2C_1_SDA / SWD_0_CLK
G2	13	17	VDDD	VDDD Supply Input / Output (2.7 V–5.5 V)
F3	14	18	VDDIO	1.71 V–5.5 V supply for I/Os. This supply also powers the global analog multiplex buses.
F2	15	19	VCCD	1.8V regulator output for filter capacitor
G1	16	20	VSYS	System Power Supply (2.7 V–5.5 V)
F1	17	21	DPLUS	USB 2.0 DP
E1	18	22	DMINUS	USB 2.0 DM
E2	19	23	P2.4	GPIO
D3	20	24	P2.5	GPIO / UART_0_TX/ SPI_0_MOSI
D2	N/A	25	P2.6	GPIO / UART_0_RX/ SPI_0_CLK
D1	21	26	XRES	External Reset Input. Internally pulled-up to VDDIO.
C3	22	27	P0.0	I2C_0_SDA / GPIO_OVT / UART_0_CTS / SPI_0_SEL/ TCPWM0
C2	23	28	P0.1	I2C_0_SCL / GPIO_OVT / UART_0_RTS / SPI_0_MISO/ TCPWM1

Table 2. CCG3 Pin Description for 42-CSP, 32-QFN and 40-QFN Devices *(continued)*

Pin Map 42-CSP	Pin Map 32-QFN	Pin Map 40-QFN	Name	Description
C1	N/A	29	VBUS_C_CTRL1	VBUS Gate Driver Control 1 for Consumer Switch
C4	24	30	VBUS_C_CTRL0	VBUS Gate Driver Control 0 for Consumer Switch
B1	25	31	VBUS	VBUS Input
A1	26	32	VBUS_DISCHARGE	VBUS Discharge Control output
E3	12, 27	33	VSS	Ground Supply (GND)
	EPAD	EPAD	VSS	
A2	28	34	P3.2	GPIO / TCPWM0
B2	N/A	35	P3.3	GPIO / TCPWM1
B3	29	36	P3.4	GPIO / UART_2_CTS / SPI_2_MOSI/ I2C_2_SDA / TCPWM2
A3	30	37	P3.5	GPIO / UART_2_RTS / SPI_2_CLK/ I2C_2_SCL / TCPWM3
B4	N/A	38	P3.6	GPIO
A4	31	39	OC	Over-current Sensor Input
B5	32	40	VBUS_P	VBUS Producer Input

Figure 6. Pinout of 42-WLCSP Bottom (Balls Up) View

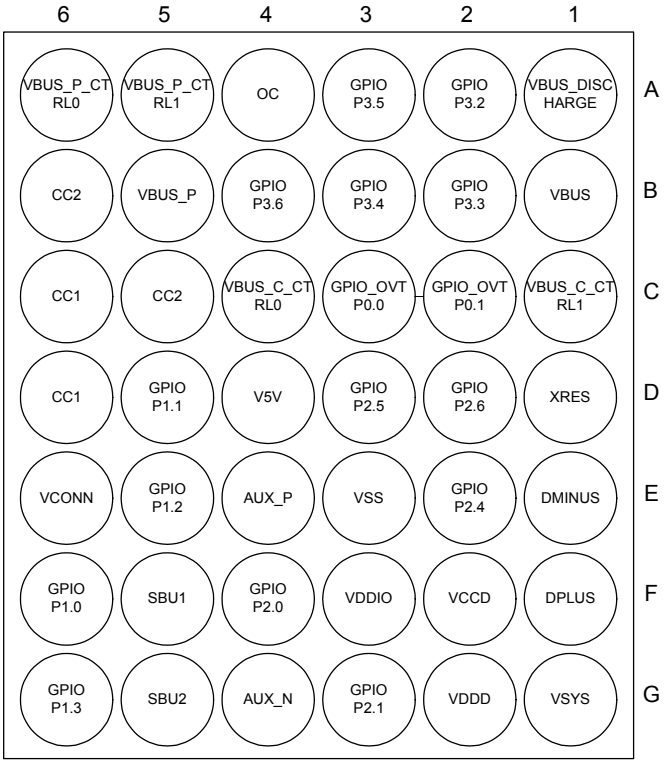
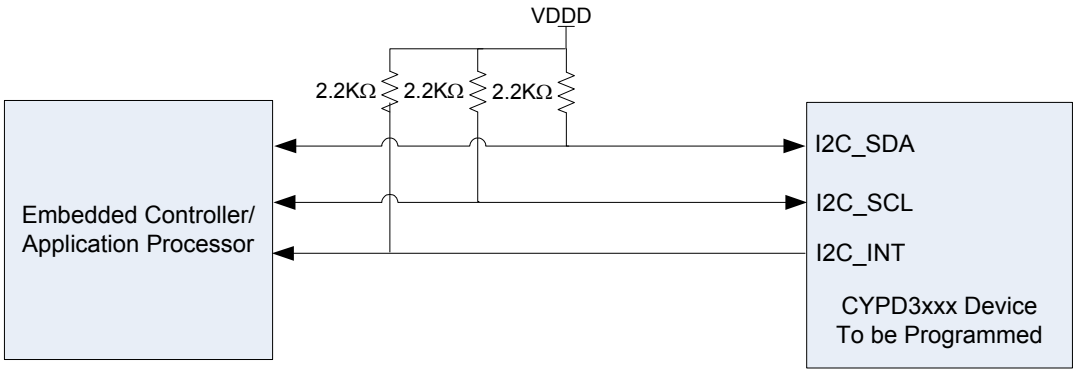


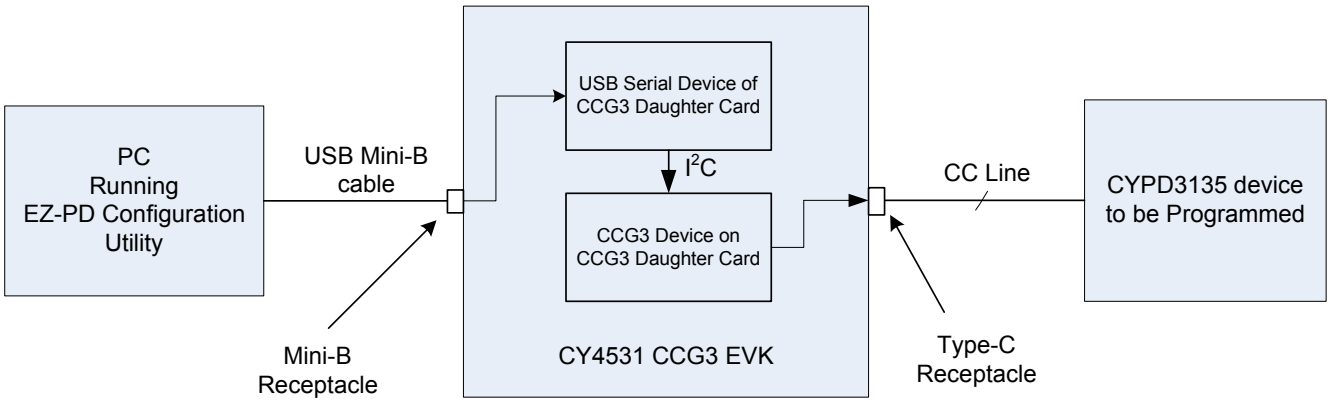
Figure 8. Application Firmware Update over I²C Interface



Application Firmware Update over CC Line

This method primarily applies to CYPD3135 device of the CCG3 family. In these applications, the CY4531 CCG3 EVK can be used to send programming and configuration data as Cypress specific Vendor Defined Messages (VDMs) over the CC line. The CY4531 CCG3 EVK is connected to the system containing CCG3 device on one end and a Windows PC running the EZ-PDTM Configuration Utility as shown in Figure 9 on the other end to program the CCG3 device.

Figure 9. Application Firmware Update over CC Line



Application Firmware Update over USB

This method primarily applies to the CYPD3120 and CYPD3121 devices of the CCG3 family. In these applications, the firmware update can be performed over the D+/D- lines (USB2.0) using various possible options as shown in Figure 10. Option 1 is to have a Windows PC running EZ-PD™ Configuration Utility connected to the device to be programmed via the CY4531 CCG3 EVK. This setup can be avoided using option 2, where the user has a Type-A to Type-C cable. This option requires that the system contain the CCG3 device to be programmed to have a Type-C receptacle. The other option (Option 3) is to have a Windows PC with a native Type-C connector as shown in Figure 10.

Figure 10. Application Firmware Update over USB

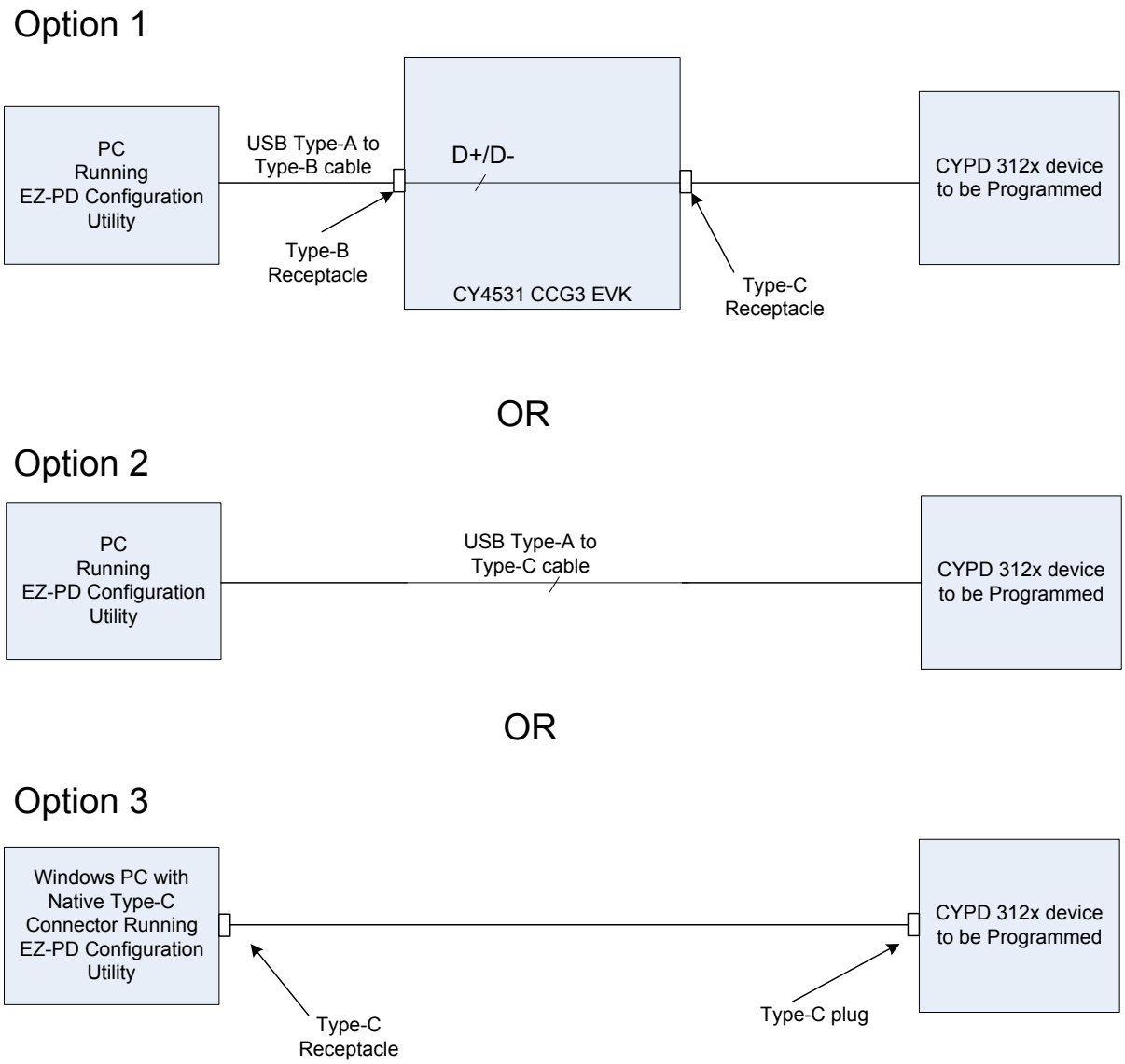
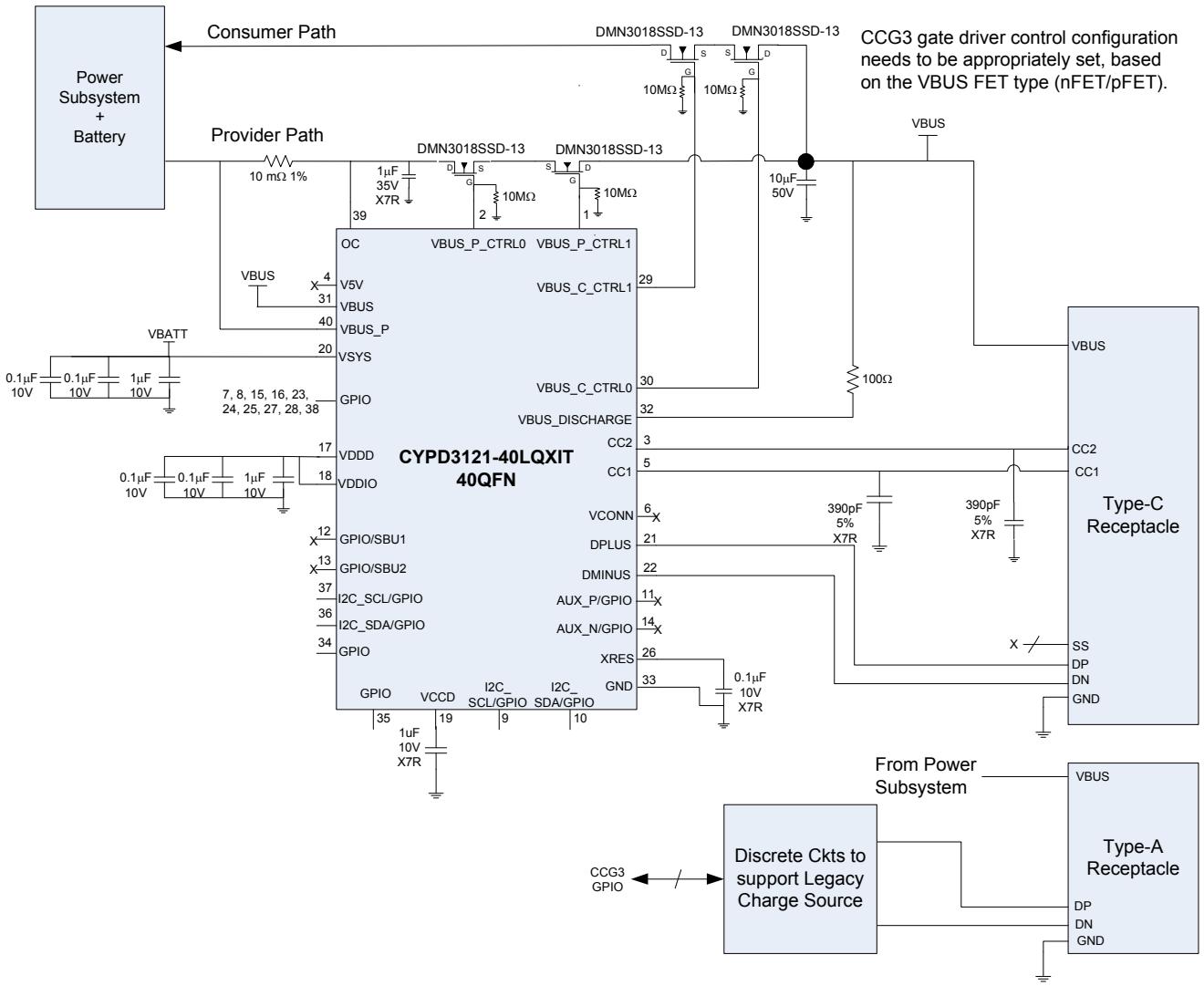


Figure 12 illustrates a power bank application diagram using a CCG3 device. In this application, the Type-C receptacle is used for providing as well as consuming power. The consumer path will be active when the battery is charged using a Type-C power source that is connected to the Type-C receptacle in Figure 12. The provider path will be active when the power bank is used for providing power to a sink device connected to the Type-C receptacle. Additionally, a Type-A receptacle can also be provided for providing power to the sinks that have a legacy USB interface.

The CCG3 device negotiates power contracts between the power bank and the sink/source device connected to the Type-C receptacle. The CCG3 device also controls and drives the provider and consumer path FETs and can monitor overcurrent and overvoltage conditions on the Type-C VBUS line.

Figure 12. Power Bank Application Diagram (40-QFN Device)



Electrical Specifications

Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{SYS_MAX}	Digital supply relative to V_{SS}	–0.5	–	6	V	Absolute max
V_{5V}	Max supply voltage relative to V_{SS}	–	–	6	V	
$V_{BUS\_MAX\_ON}$	Max supply voltage relative to V_{SS}, V_{BUS} regulator enabled	–	–	26	V	
$V_{BUS\_MAX\_OFF}$	Max supply voltage relative to V_{SS}, V_{BUS} regulator enabled 100% of the time	–	–	24.5	V	
	Max supply voltage relative to V_{SS}, V_{BUS} regulator enabled 25% of the time	–	–	26	V	
V_{DDIO_MAX}	Max supply voltage relative to V_{SS}	–	–	6	V	
V_{GPIO_ABS}	GPIO voltage	–0.5	–	VDDIO + 0.5	V	
$V_{GPIO\_OVT\_ABS}$	OVT GPIO voltage	–0.5	–	6	V	
I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	
V_{CONN_MAX}	Max voltage relative to V_{SS}	–	–	6	V	
V_{CC_ABS}	Max voltage on CC1 and CC2 pins	–	–	6	V	
$I_{GPIO\_INJECTION}$	GPIO injection current, Max for V_{IH} > VDDD, and Min for V_{IL} < V_{SS}	–0.5	–	0.5	mA	Absolute max, current injected per pin
ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	–
ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	–
LU	Pin current for latch-up	–100	–	100	mA	Tested at 125 °C
ESD_IEC_CON	Electrostatic discharge IEC61000-4-2	8000	–	–	V	Contact discharge on CC1, CC2, VBUS, DPLUS, DMINUS, SBU1 and SBU2 pins
ESD_IEC_AIR	Electrostatic discharge IEC61000-4-2	15000	–	–	V	Air discharge for CC1, CC2, VBUS, DPLUS, DMINUS, SBU1 and SBU2 pins

Table 5. AC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#4	F_{CPU}	CPU input frequency	DC	–	48	MHz	All VDDD
SID.PWR#20	T_{SLEEP}	Wakeup from sleep mode	–	0	–	µs	–
SID.PWR#21	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	–	35	µs	–
SID.XRES#5	T_{XRES}	External reset pulse width	5	–	–	µs	All VDDIO
SYS.FES#1	$T_{\_PWR\_RDY}$	Power-up to “Ready to accept I^2C/CC command”	–	5	25	ms	–

I/O

Table 6. I/O DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.GIO#37	V_{IH_CMOS}	Input voltage HIGH threshold	0.7 × VDDIO	–	–	V	CMOS input
SID.GIO#38	V_{IL_CMOS}	Input voltage LOW threshold	–	–	0.3 × VDDIO	V	CMOS input
SID.GIO#39	$V_{IH\_VDDIO2.7-}$	LVTTL input, VDDIO < 2.7 V	0.7× VDDIO	–	–	V	–
SID.GIO#40	$V_{IL\_VDDIO2.7-}$	LVTTL input, VDDIO < 2.7 V	–	–	0.3 × VDDIO	V	–
SID.GIO#41	$V_{IH\_VDDIO2.7+}$	LVTTL input, VDDIO ≥ 2.7 V	2.0	–	–	V	–
SID.GIO#42	$V_{IL\_VDDIO2.7+}$	LVTTL input, VDDIO ≥ 2.7 V	–	–	0.8	V	–
SID.GIO#33	V_{OH_3V}	Output voltage HIGH level	VDDIO –0.6	–	–	V	I_{OH} = 4 mA at 3V VDDIO
SID.GIO#34	$V_{OH\_1.8V}$	Output voltage HIGH level	VDDIO –0.5	–	–	V	I_{OH} = 1 mA at 1.8V VDDIO
SID.GIO#35	$V_{OL\_1.8V}$	Output voltage LOW level	–	–	0.6	V	I_{OL} = 4 mA at 1.8V VDDIO
SID.GIO#36	V_{OL_3V}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 4 mA at 3V VDDIO for SBU and AUX pins
SID.GIO#5	R_{PU}	Pull-up resistor value	3.5	5.6	8.5	kΩ	+25 °C T_A, all VDDIO
SID.GIO#6	R_{PD}	Pull-down resistor value	3.5	5.6	8.5	kΩ	+25 °C T_A, all VDDIO
SID.GIO#16	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	+25 °C T_A, all VDDIO. Guaranteed by characterization.
SID.GIO#17	C_{PIN}	Max pin capacitance	–	3.0	7	pF	All VDDIO, all packages, all I/Os except SBU and AUX. Guaranteed by characterization.
SID.GIO#17A	C_{PIN_SBU}	Max pin capacitance	–	16	18	pF	All VDDIO, all packages, SBU pins only. Guaranteed by characterization.
SID.GIO#17B	C_{PIN_AUX}	Max pin capacitance	–	12	14	pF	All VDDIO, all packages, AUX pins only. Guaranteed by characterization.
SID.GIO#43	V_{HYSTTL}	Input hysteresis, LVTTL VDDIO > 2.7 V	15	40	–	mV	Guaranteed by characterization
SID.GIO#44	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × VDDIO	–	–	mV	VDDIO < 4.5 V. Guaranteed by characterization.
SID69	I_{DIODE}	Current through protection diode to VDDIO/Vss	–	–	100	µA	Guaranteed by characterization
SID.GIO#45	I_{TOT_GPIO}	Maximum total sink chip current	–	–	85	mA	Guaranteed by characterization

I²C

Table 10. Fixed I²C DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	–	60	µA	–
SID150	I_{I2C2}	Block current consumption at 400 kHz	–	–	185	µA	–
SID151	I_{I2C3}	Block current consumption at 1 Mbps	–	–	390	µA	–
SID152	I_{I2C4}	I²C enabled in Deep Sleep mode	–	–	1.4	µA	–

Table 11. Fixed I²C AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID153	F_{I2C1}	Bit rate	–	–	1	Mbps	–

Table 12. Fixed UART DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID160	I_{UART1}	Block current consumption at 100 Kb/s	–	–	125	µA	–
SID161	I_{UART2}	Block current consumption at 1000 Kb/s	–	–	312	µA	–

Table 13. Fixed UART AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID162	F_{UART}	Bit rate	–	–	1	Mbps	–

Table 14. Fixed SPI DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID163	I_{SPI1}	Block current consumption at 1 Mb/s	–	–	360	µA	–
SID164	I_{SPI2}	Block current consumption at 4 Mb/s	–	–	560	µA	–
SID165	I_{SPI3}	Block current consumption at 8 Mb/s	–	–	600	µA	–

Table 15. Fixed SPI AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID166	F_{SPI}	SPI Operating frequency (Master; 6X oversampling)	–	–	8	MHz	–

Table 16. Fixed SPI Master Mode AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID167	T_{DMO}	MOSI Valid after SClock driving edge	–	–	15	ns	–
SID168	T_{DSI}	MISO Valid before SClock capturing edge	20	–	–	ns	Full clock, late MISO sampling
SID169	T_{HMO}	Previous MOSI data hold time	0	–	–	ns	Referred to slave capturing edge

Table 17. Fixed SPI Slave Mode AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID170	T_{DMI}	MOSI Valid before Sclock capturing edge	40	–	–	ns	–
SID171	T_{DSO}	MISO Valid after Sclock driving edge	–	–	42 + 3 × T_{CPU}	ns	T_{CPU} = 1/F_{CPU}
SID171A	T_{DSO_EXT}	MISO Valid after Sclock driving edge in Ext Clk mode	–	–	48	ns	–
SID172	T_{HSO}	Previous MISO data hold time	0	–	–	ns	–
SID172A	$T_{SSELSCK}$	SSEL Valid to first SCK Valid edge	100	–	–	ns	–

System Resources

Power-on-Reset (POR) with Brown Out SWD Interface

Table 18. Imprecise Power On Reset (PRES) (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID185	$V_{RISEIPOR}$	Power-on Reset (POR) rising trip voltage	0.80	–	1.50	V	–
SID186	$V_{FALLIPOR}$	POR falling trip voltage	0.70	–	1.4	V	–

Table 19. Precise Power On Reset (POR) (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190	$V_{FALLPPOR}$	Brown-out Detect (BOD) trip voltage in active/sleep modes	1.48	–	1.62	V	–
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep mode	1.1	–	1.5	V	–

Table 20. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.SWD#1	F_SWDCLK1	3.3 V ≤ VDDIO ≤ 5.5 V	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#2	F_SWDCLK2	1.8 V ≤ VDDIO ≤ 3.3 V	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#3	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 × T	–	–	ns	Guaranteed by characterization
SID.SWD#4	T_SWDI_HOLD	T = 1/f SWDCLK	0.25 × T	–	–	ns	Guaranteed by characterization
SID.SWD#5	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.50 × T	ns	Guaranteed by characterization
SID.SWD#6	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	Guaranteed by characterization

Packaging

Table 39. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature	Industrial	–40	25	85	°C
		Extended Industrial			105	°C
T_J	Operating junction temperature	Industrial	–40	25	100	°C
		Extended Industrial			125	°C
T_{JA}	Package θ_{JA} (40-pin QFN)	–	–	–	17	°C/W
T_{JC}	Package θ_{JC} (40-pin QFN)	–	–	–	2	°C/W
T_{JA}	Package θ_{JA} (42-ball WLCSP)	–	–	–	34	°C/W
T_{JC}	Package θ_{JC} (42-ball WLCSP)	–	–	–	0.3	°C/W
T_{JA}	Package θ_{JA} (32-pin QFN)	–	–	–	18	°C/W
T_{JC}	Package θ_{JC} (32-pin QFN)	–	–	–	4	°C/W

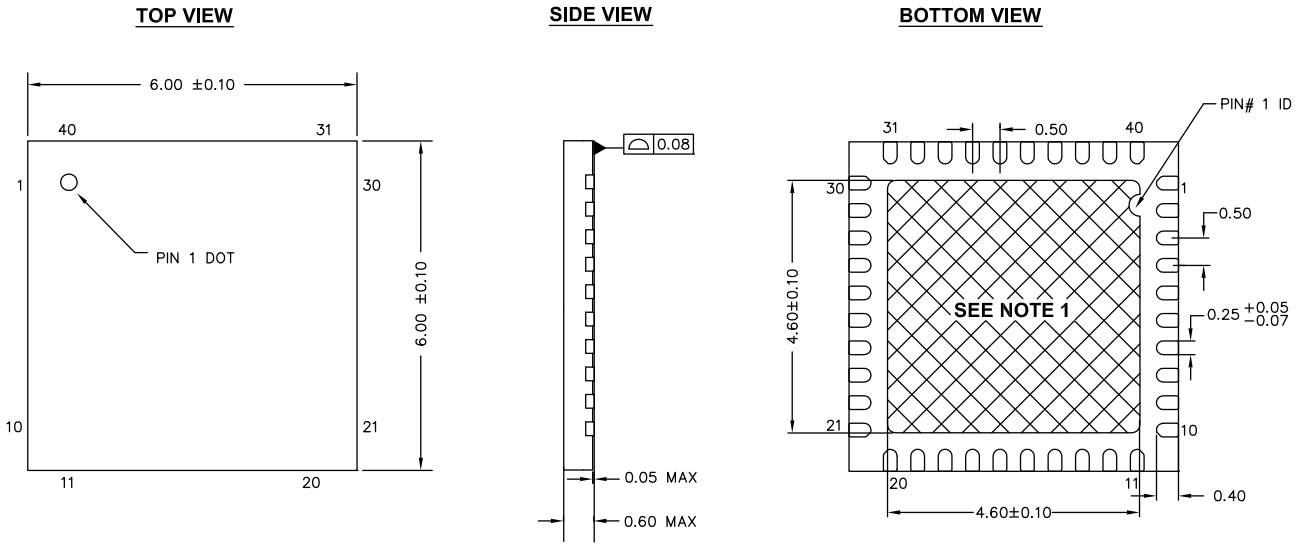
Table 40. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time within 5 °C of Peak Temperature
40-pin QFN	260 °C	30 seconds
42-ball WLCSP	260 °C	30 seconds
32-pin QFN	260 °C	30 seconds

Table 41. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
42-ball WLCSP	MSL 1
40-pin QFN	MSL 3
32-pin QFN	MSL 3

Figure 17. 40-pin QFN Package Outline, 001-80659

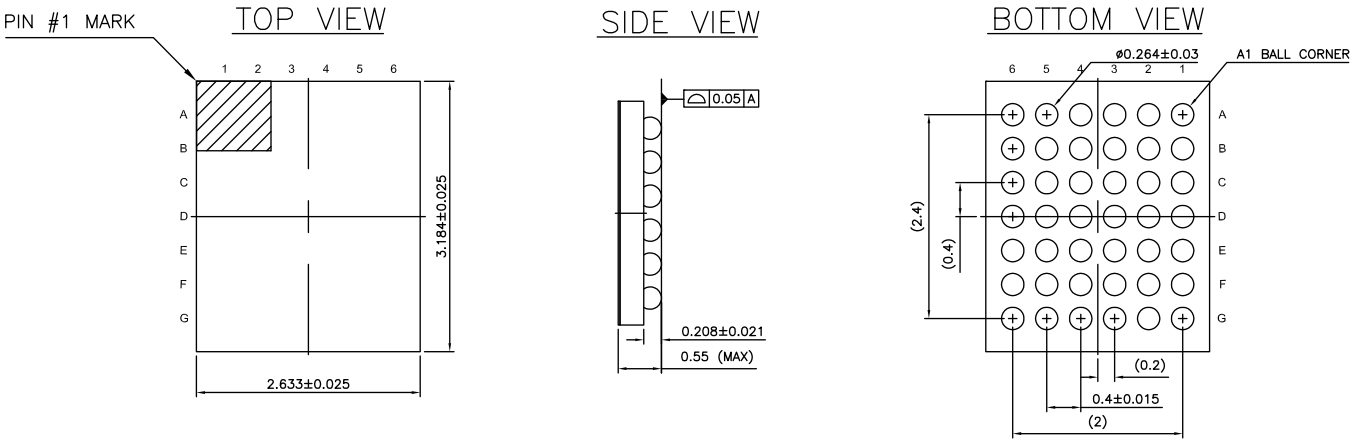


NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT: 68 ±2 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-80659 *A

Figure 18. 42-ball CSP Package Outline, 002-04062



002-04062 *A

ALL DIMENSIONS ARE IN MM
JEDEC Publication 95; Design Guide 4.18

Acronyms

Table 42. Acronyms Used in this Document

Acronym	Description
ADC	analog-to-digital converter
AES	advanced encryption standard
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus
API	application programming interface
ARM®	advanced RISC machine, a CPU architecture
BMC	Biphase Mark Code
CC	configuration channel
CCG3	Cable Controller Generation 3
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
CS	current sense
DFP	downstream facing port
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DRP	dual role port
EEPROM	electrically erasable programmable read-only memory
EMCA	electronically marked cable assembly, a USB cable that includes an IC that reports cable characteristics (e.g., current rating) to the Type-C ports
EMI	electromagnetic interference
ESD	electrostatic discharge
FS	full-speed
GPIO	general-purpose input/output
HPD	hot plug detect
IC	integrated circuit
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
IOSS	input/output subsystem
I/O	input/output, see also GPIO
LDO	low-dropout regulator
LVD	low-voltage detect
LVTTL	low-voltage transistor-transistor logic
MCU	microcontroller unit
MMIO	memory mapped input/output
NC	no connect
NMI	nonmaskable interrupt
NVIC	nested vectored interrupt controller

Table 42. Acronyms Used in this Document *(continued)*

Acronym	Description
opamp	operational amplifier
OCP	overcurrent protection
OVP	overvoltage protection
PCB	printed circuit board
PD	power delivery
PGA	programmable gain amplifier
PHY	physical layer
POR	power-on reset
PRES	precise power-on reset
PSoC®	Programmable System-on-Chip™
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RX	receive
SAR	successive approximation register
SCB	serial communication block
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SHA	secure hash algorithm
SPI	Serial Peripheral Interface, a communications protocol
SRAM	static random access memory
SWD	serial wire debug, a test protocol
TCPWM	timer/counter pulse-width modulator
Thunderbolt™	Trademark of Intel
TX	transmit
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
USB	Universal Serial Bus
USB PD	USB Power Delivery
USB-FS	USB Full-Speed
USBIO	USB input/output, CCG2 pins used to connect to a USB port
USBPD SS	USB PD subsystem
VDM	vendor defined messages
XRES	external reset I/O pin

Document Conventions

Units of Measure

Table 43. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
Hz	hertz
KB	1024 bytes
kHz	kilohertz
kΩ	kilo ohm
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
V	volt

Document History Page

Document Title: EZ-PD™ CCG3 USB Type-C Port Controller Document Number: 002-03288				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	4905678	VGT	09/11/2015	New data sheet.
*A	4953333	VGT	10/08/2015	Updated General Description: Updated the number of GPIOs to 20. Updated Functional Overview: Updated GPIO: Updated the number of GPIOs to 20. Updated Pinouts: Updated Table 2. Updated Figure 4. Added Figure 6.
*B	5007726	VGT	11/25/2015	Changed status from Advance to Preliminary. Updated Features. Added EZ-PD CCG3 Block Diagram. Updated Functional Overview: Updated USB-PD Subsystem (USBPD SS) (Updated description). Added Full-Speed USB Subsystem. Updated Pinouts: Updated Table 2. Updated Figure 4. Updated Figure 6. Added Applications. Updated Electrical Specifications: Updated Absolute Maximum Ratings: Updated Table 3. Updated Device-Level Specifications: Updated Table 4. Updated Table 5. Updated I/O: Updated Table 6. Updated XRES: Updated Table 8. Updated System Resources: Updated Power-on-Reset (POR) with Brown Out SWD Interface: Updated Table 18. Updated Table 19. Updated Table 20. Updated Internal Main Oscillator: Updated Table 22. Updated Internal Low-Speed OscillatorPower Down: Updated Table 23. Updated Table 24. Updated Internal Low-Speed OscillatorPower Down: Updated Table 25.

Document History Page *(continued)*

Document Title: EZ-PD™ CCG3 USB Type-C Port Controller Document Number: 002-03288				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*B (cont.)	5007726	VGT	11/25/2015	Updated Analog to Digital Converter: Updated Table 32. Updated Table 33. Updated Packaging: Added Figure 18 (spec 002-04062 *A).
*C	5080470	VGT	01/11/2016	Updated General Description. Updated Features. Updated Logic Block Diagram. Updated Power Systems Overview. Updated Pinouts: Updated Table 2. Added table “CCG3 Pin Description for 16-SOIC Device”. Added figure “Pinout of 16-SOIC Package (Top View)”. Updated Applications: Updated Figure . Updated Figure 11. Updated figure “Power Adapter Application Diagram (16-SOIC Device)”. Updated Figure 15. Updated Ordering Information. Updated Packaging: Added spec 51-85022 *E. Added Errata.
*D	5137796	VGT	03/09/2016	Updated Pinouts: Updated table “CCG3 Pin Description for 16-SOIC Device”. Updated figure “Pinout of 16-SOIC Package (Top View)”. Updated Applications: Updated Figure 11. Updated Figure 12. Updated Ordering Information Updated Errata. Updated to new template.
*E	5240836	VGT	04/28/2016	Updated General Description: Updated description. Updated Features: Updated Type-C and USB-PD Support: Updated description. Updated Packages: Updated description. Updated Logic Block Diagram. Updated Functional Overview: Updated Integrated Billboard Device: Updated description. Updated USB-PD Subsystem (USBPD SS): Updated description. Added Figure 2 and Figure 5.

Document History Page *(continued)*

Document Title: EZ-PD™ CCG3 USB Type-C Port Controller Document Number: 002-03288				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*E (cont.)	5240836	VGT	04/28/2016	Updated Power Systems Overview: Updated description. Updated Figure 3. Updated Pinouts: Updated Table 2: Updated details in “Description” column corresponding to VDDIO pin. Removed table “CCG3 Pin Description for 16-SOIC Device”. Removed figure “Pinout of 16-SOIC Package (Top View)”. Updated Applications: Removed figure “Power Adapter Application Diagram (16-SOIC Device)”. Added Figure 12. Updated Electrical Specifications: Updated Device-Level Specifications: Updated Table 4. Updated details in “Details/Conditions” column corresponding to “SID.PWR#1_A” Spec ID and “V_{SYS}” parameter. Replaced “V_{DDD}” with “5.5” in “Max” column corresponding to “SID.PWR#13” Spec ID and “V_{DDIO}” parameter. Added “SID.PWR#13_A” Spec ID corresponding to “V_{DDIO}” parameter and its details. Added “SID.PWR#1_C” and “SID.PWR#1_D” Spec IDs corresponding to “V_{SYS}” parameter and its details. Replaced “enabled” with “disabled” in “Details/Conditions” column corresponding to “SID.PwR#28” Spec ID and “V_{BUS}” parameter. Updated details in “Description” and “Details/Conditions” columns corresponding to “SID307” Spec ID and “I_{DD_XR}” parameter. Updated System Resources: Added Gate Driver Specifications, Charger Detect. Updated Ordering Information: Updated part numbers. Updated details in “Application” column corresponding to part number “CYPD3121-40LQXIT”. Updated Ordering Code Definitions Updated Packaging: Removed spec 51-85022 *E. Removed Errata.
*F	5342389	VGT	07/28/2016	Added Available Firmware and Software Tools, CCG3 Programming and Bootloading, and References and Links to Applications Collaterals. Added descriptive notes for the application diagrams. Updated Features, Applications and Timer/Counter/PWM Block (TCPWM). Updated Table 2 through Table 6, Table 18, Table 19, Table 22, Table 23, Table 25, and Table 31 through Table 38. Updated Figure 7, Figure 8, Figure , Figure 11, and Figure 19 (package diagram spec 001-42168 *E). Added Figure 5, Figure 13, and Figure 14. Added Table 26, Table 27, Table 37, and Table 39 through Table 41. Added VDM in Acronyms. Updated Cypress logo and copyright information.
*G	5449433	VGT	09/26/2016	Added Table 34 through Table 36. Updated Table 3, Table 4, Table 6, and Table 37. Updated Copyright and Disclaimer. Added Compliance information in Sales, Solutions, and Legal Information.