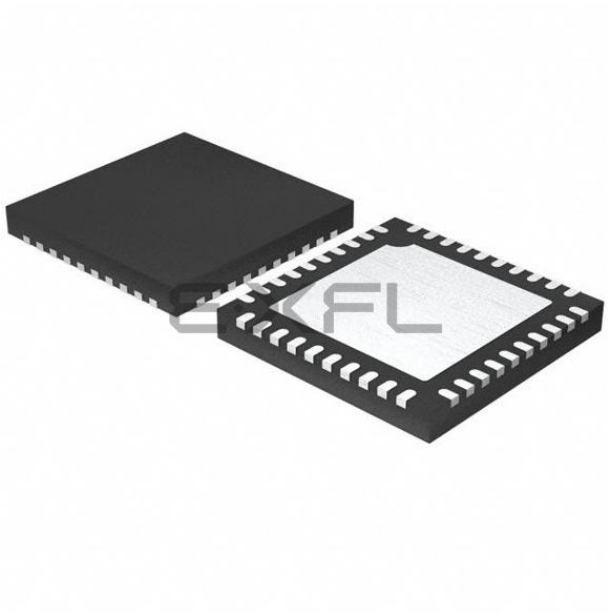

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Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	USB Type C
Core Processor	ARM® Cortex®-M0
Program Memory Type	FLASH (128kB)
Controller Series	-
RAM Size	8K x 8
Interface	I²C, SPI, UART/USART, USB
Number of I/O	16
Voltage - Supply	2.7V ~ 21.5V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cypd3120-40lqxit

Functional Overview

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in EZ-PD CCG3 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex-M3 and M4, thus enabling upward compatibility. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor up from the Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a serial wire debug (SWD) interface, which is a two-wire form of JTAG. The debug configuration used for EZ-PD CCG3 has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The EZ-PD CCG3 device has a flash module with two banks of 64 KB flash, a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 1 wait-state (WS) access time at 48 MHz and with 0-WS access time at 24 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

Crypto Block

CCG3 integrates a crypto block for hardware assisted authentication of firmware images. It also supports field upgradeability of firmware in a trusted ecosystem. The CCG3 Crypto block provides cryptography functionality. It includes hardware acceleration blocks for AES (Advanced Encryption Standard) block cipher, SHA-1 (Secure Hash Algorithm) and SHA-2 hash, Cyclic Redundancy Check (CRC) and pseudo random number generation.

Integrated Billboard Device

CCG3 integrates a complete full speed USB 2.0 device controller capable of functioning as a Billboard class device. The USB 2.0 device controller can also support other device classes.

USB-PD Subsystem (USBPD SS)

The USB-PD sub-system contains all of the blocks related to USB Type-C and Power Delivery. The sub-system is comprised of the following:

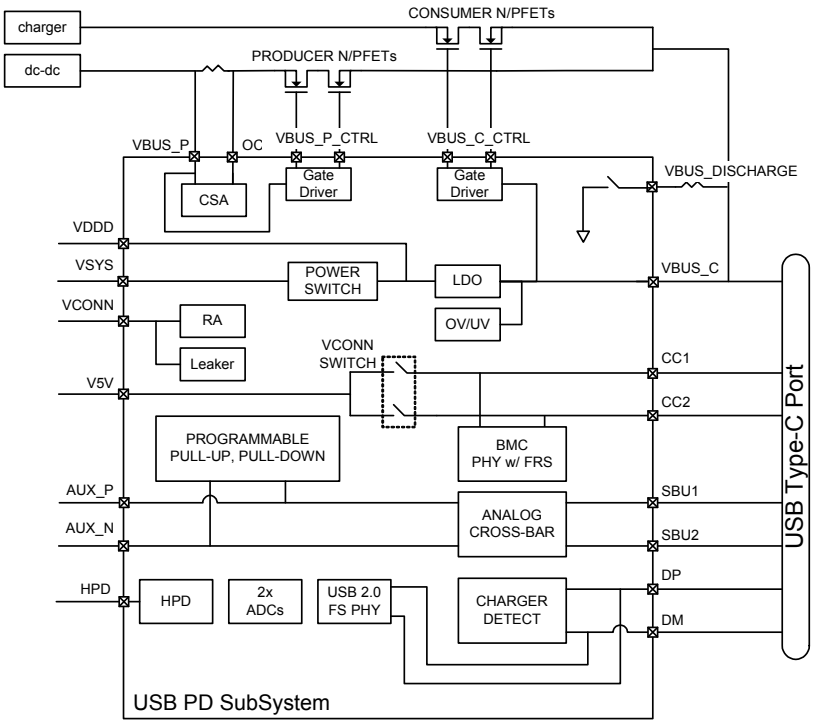
- BMC PHY: USB-PD Transceiver with Fast Role Swap (FRS) transmit and detect
- VCONN power FETs for the CC lines
- VCONN Ra Termination and Leakers
- Analog Cross-Bar to switch between the SBU1/SBU2 and AUX_P/AUX_N pins
- Programmable Pull-up and Pull-down termination on the AUX_P/AUX_N pins
- HPD Processor
- VBUS_C Regulator (20V LDO)
- Power Switch between VSYS supply and VBUS_C Regulator output
- VBUS_C Over-Voltage (OV) and Under-Voltage (UV) Detectors
- Current Sense Amplifier (CSA) for over current detection
- Gate Drivers for VBUS_P and VBUS_C external Power FETs
- VBUS_C discharge switch
- USB2.0 Full-Speed (FS) PHY with integrated 5.0V to 3.3V regulator
- Charger Detection / Emulation for USB BC1.2 and other proprietary protocols
- 2 instances of 8-bit SAR ADCs
- 8kV IEC ESD Protection on the following pins: VBUS_C, CC1, CC2, SBU1, SBU2, DP, DM

The EZ-PD™ CCG3 USB-PD subsystem interfaces to the pins of a USB Type-C connector. It includes a USB Type-C baseband transceiver and physical-layer logic. This transceiver performs the BMC and the 4b/5b encoding and decoding functions as well as integrating the 1.2V analog front end. This subsystem integrates the required terminations to identify the role of the CCG3 device, including Rp and Rd for UFP/DFP roles and Ra for EMCA/VCONN powered accessories. The programmable VCONN leakers are included in order to discharge VCONN capacitance during a disconnect event. It also integrates power FETs for supplying VCONN power to the CC1/CC2 pins from the V5V pin. The Analog Cross-Bar allows for connecting either of the SBU1/SBU2 pins to either of the AUX_P/AUX_N pins to support DisplayPort sideband signaling. The integrated HPD processor can be used to control or monitor the HPD signal of a DisplayPort source or sink.

The OV/UV (Over-Voltage/Under-Voltage) block monitors the VBUS_C supply for programmable over-voltage and under-voltage conditions. The CSA amplifies the voltage across an external sense resistor, which is proportional to the current being drawn from the external DC-DC VBUS supply converter. The CSA output can either be measured with an ADC or configured to detect an over-current condition. The VBUS_P and VBUS_C gate drivers control the gates of external power FETs for the VBUS_C and VBUS_P supplies. The gate drivers can be configured to support both P and N type external power FETs. The gate drivers are configured by default for nFET devices. In applications using pFETs, the gate drivers must be appropriately configured. The OV/UV and CSA blocks can generate interrupts to automatically turn off the power FETs for the programmed over-voltage and over-current conditions. The VBUS_C discharge switch allows for discharging the VBUS_C line through an external resistor.

The USB-PD sub-system also contains two 8-bit Successive Approximation Register (SAR) ADCs for analog to digital conversions. Each ADC includes an 8-bit DAC and a comparator. The DAC output forms the positive input of the comparator. The negative input of the comparator is from a 4-input multiplexer. The four inputs of the multiplexer are a pair of global analog multiplex busses, an internal bandgap voltage and an internal voltage proportional to the absolute temperature. Each GPIO pin can be connected to the global Analog Multiplex Busses through a switch, which allows either ADC to sample the pin voltage. When sensing the GPIO pin voltage with an ADC, the pin voltage cannot exceed the VDDD or VDDIO supply values.

Figure 2. USB-PD Subsystem



Full-Speed USB Subsystem

The FSUSB subsystem contains a full speed USB device controller as described in the Integrated Billboard Device section.

Peripherals

Serial Communication Blocks (SCB)

EZ-PD CCG3 has four SCBs, which can be configured to implement an I²C, SPI, or UART interface. The hardware I²C blocks implement full multi-master and slave interfaces capable of multimaster arbitration. In the SPI mode, the SCB blocks can be configured to act as master or slave.

In the I²C mode, the SCB blocks are capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and have flexible buffering options to reduce interrupt overhead and latency for the CPU. These blocks also support I²C that creates a mailbox address range in the memory of EZ-PD CCG3 and effectively reduce I²C communication to reading from and writing to an array in memory. In addition, the blocks support 8-deep FIFOs for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduce the need for clock stretching caused by the CPU not having read data on time.

The I²C peripherals are compatible with the I²C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I²C-bus specification and user manual (UM10204).

The I²C bus I/Os are implemented with GPIO in open-drain modes.

The I^2C port on SCB 1-3 blocks of EZ-PD CCG3 are not completely compliant with the I^2C specification in the following aspects:

- The GPIO cells for SCB 1's I^2C port are not overvoltage-tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I^2C system.
- Fast-mode Plus has an I_{OL} specification of 20 mA at a V_{OL} of 0.4V. The GPIO cells can sink a maximum of 8-mA I_{OL} with a V_{OL} maximum of 0.6V.
- Fast-mode and Fast-mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the bus load.

Timer/Counter/PWM Block (TCPWM)

EZ-PD CCG3 has four TCPWM blocks. Each implements a 16-bit timer, counter, pulse-width modulator (PWM), and quadrature decoder functionality.

GPIO

EZ-PD CCG3 has up to 20 GPIOs (these GPIOs can be configured for GPIOs, SCB, SBU, and Aux signals) and SWD pins, which can also be used as GPIOs. The I^2C pins from SCB 0 are overvoltage-tolerant.

The GPIO block implements the following:

- Seven drive strength modes:
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode)
- Selectable slew rates for dV/dt related noise control to improve EMI

During power-on and reset, the I/O pins are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Table 2. CCG3 Pin Description for 42-CSP, 32-QFN and 40-QFN Devices *(continued)*

Pin Map 42-CSP	Pin Map 32-QFN	Pin Map 40-QFN	Name	Description
C1	N/A	29	VBUS_C_CTRL1	VBUS Gate Driver Control 1 for Consumer Switch
C4	24	30	VBUS_C_CTRL0	VBUS Gate Driver Control 0 for Consumer Switch
B1	25	31	VBUS	VBUS Input
A1	26	32	VBUS_DISCHARGE	VBUS Discharge Control output
E3	12, 27	33	VSS	Ground Supply (GND)
	EPAD	EPAD	VSS	
A2	28	34	P3.2	GPIO / TCPWM0
B2	N/A	35	P3.3	GPIO / TCPWM1
B3	29	36	P3.4	GPIO / UART_2_CTS / SPI_2_MOSI/ I2C_2_SDA / TCPWM2
A3	30	37	P3.5	GPIO / UART_2_RTS / SPI_2_CLK/ I2C_2_SCL / TCPWM3
B4	N/A	38	P3.6	GPIO
A4	31	39	OC	Over-current Sensor Input
B5	32	40	VBUS_P	VBUS Producer Input

Figure 4. Pinout of 40-QFN Package (Top View)

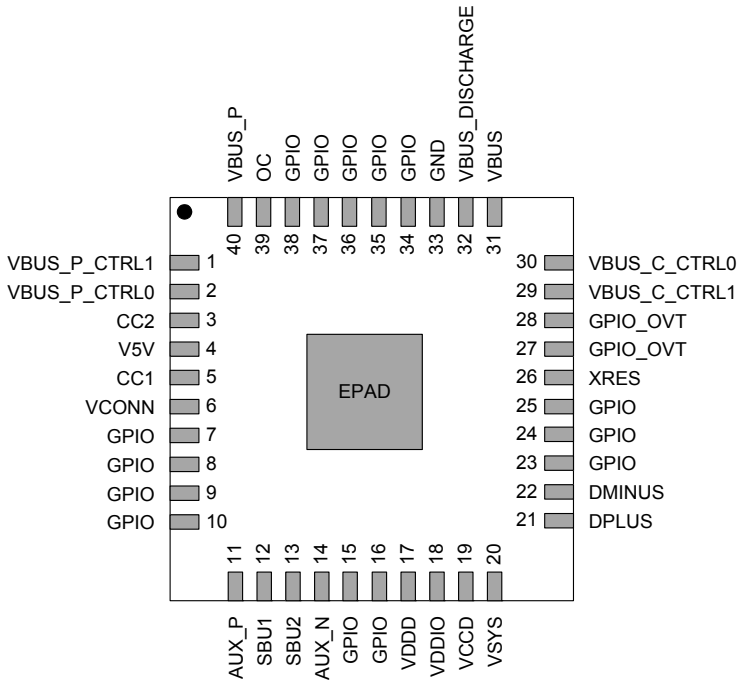


Figure 5. Pinout of 32-QFN Package (Top View)

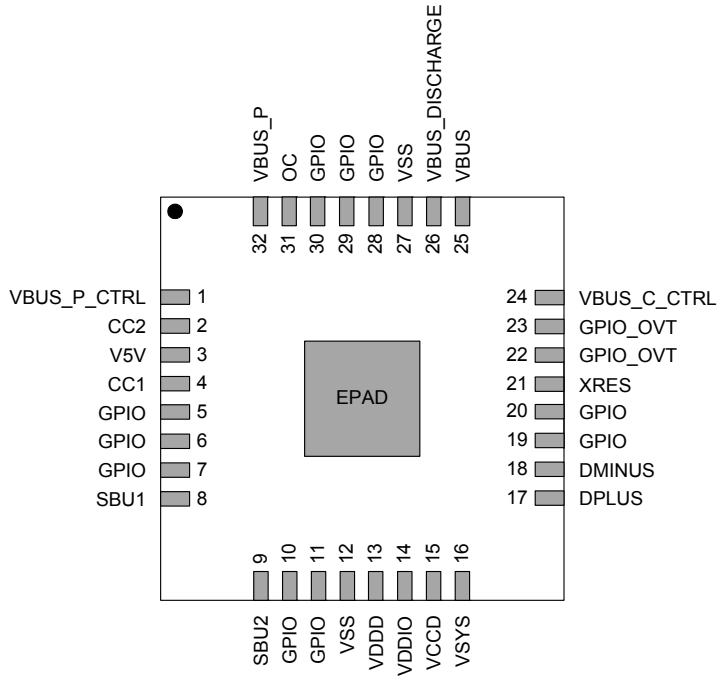
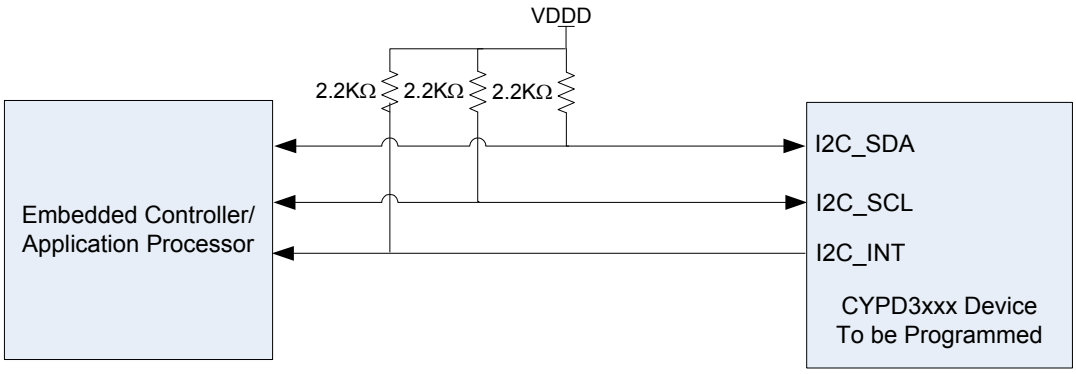


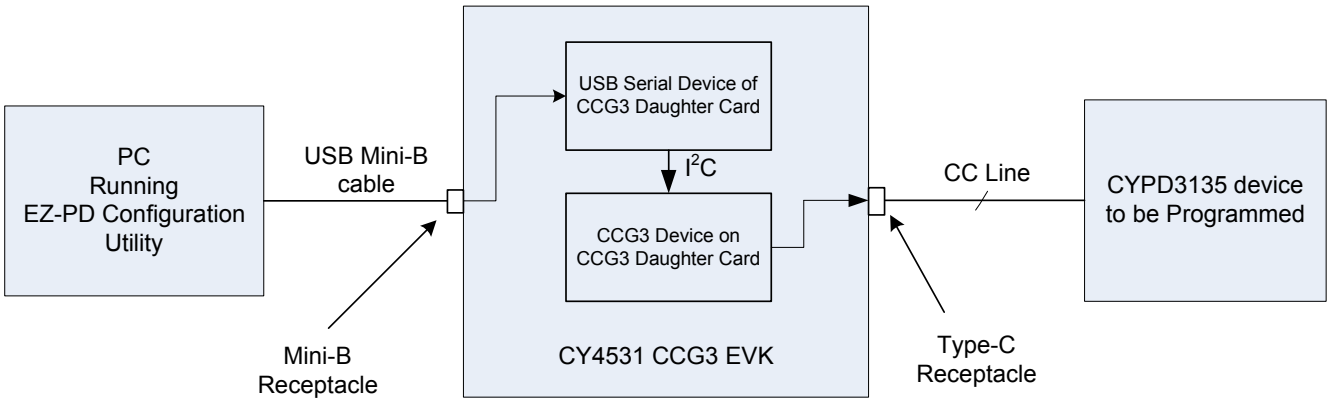
Figure 8. Application Firmware Update over I²C Interface



Application Firmware Update over CC Line

This method primarily applies to CYPD3135 device of the CCG3 family. In these applications, the CY4531 CCG3 EVK can be used to send programming and configuration data as Cypress specific Vendor Defined Messages (VDMs) over the CC line. The CY4531 CCG3 EVK is connected to the system containing CCG3 device on one end and a Windows PC running the EZ-PDTM Configuration Utility as shown in Figure 9 on the other end to program the CCG3 device.

Figure 9. Application Firmware Update over CC Line



Application Firmware Update over USB

This method primarily applies to the CYPD3120 and CYPD3121 devices of the CCG3 family. In these applications, the firmware update can be performed over the D+/D- lines (USB2.0) using various possible options as shown in Figure 10. Option 1 is to have a Windows PC running EZ-PD™ Configuration Utility connected to the device to be programmed via the CY4531 CCG3 EVK. This setup can be avoided using option 2, where the user has a Type-A to Type-C cable. This option requires that the system contain the CCG3 device to be programmed to have a Type-C receptacle. The other option (Option 3) is to have a Windows PC with a native Type-C connector as shown in Figure 10.

Applications

Figure 11 illustrates the application diagram of a power adapter using a CCG3 device. In this application, CCG3 is used as DFP (power provider) only. The maximum power profile that can be supported by power adapters is up to 20 V, 100 W using 40-pin QFN CCG3 devices. CCG3 has the ability to drive both types of FETs and the state of GPIO P1.0 (floating or grounded) indicates the type of FET (N-MOS or P-MOS FET) being used in the power provider path.

CCG3 integrates all termination resistors and uses GPIOs (VSEL0 and VSEL1) to indicate the negotiated power profile. If required, the power profile can also be selected using CCG3 serial interfaces (I^2C, SPI) or PWM. The VBUS voltage on the Type-C port is monitored using internal circuits to detect under-voltage and overvoltage conditions. To ensure quick discharge of VBUS when the power adapter cable is detached, a discharge path is provided with a resistor connected to the VBUS_DISCHARGE pin of the CCG3 device.

Overcurrent protection is enabled by sensing the current through the 10-mΩ sense resistor using the “OC” and “VBUS_P” pins of the CCG3 device. The VBUS provider through the Type-C connector can be turned on or off using the provider path FETs. The power provider FETs are controlled by high-voltage gate driver outputs (VBUS_P_CTRL0 and VBUS_P_CTRL1 pins of CCG3 device). The CCG3 device is also capable of supporting proprietary charging protocols over the DP and DM lines of the Type-C receptacle. By providing a 5-V source at the V5V pin of the CCG3 device, the device becomes capable of delivering the VCONN supply over either the CC1 or CC2 pins of the Type-C connector.

Figure 11. Power Adapter Application Diagram (40-QFN Device)

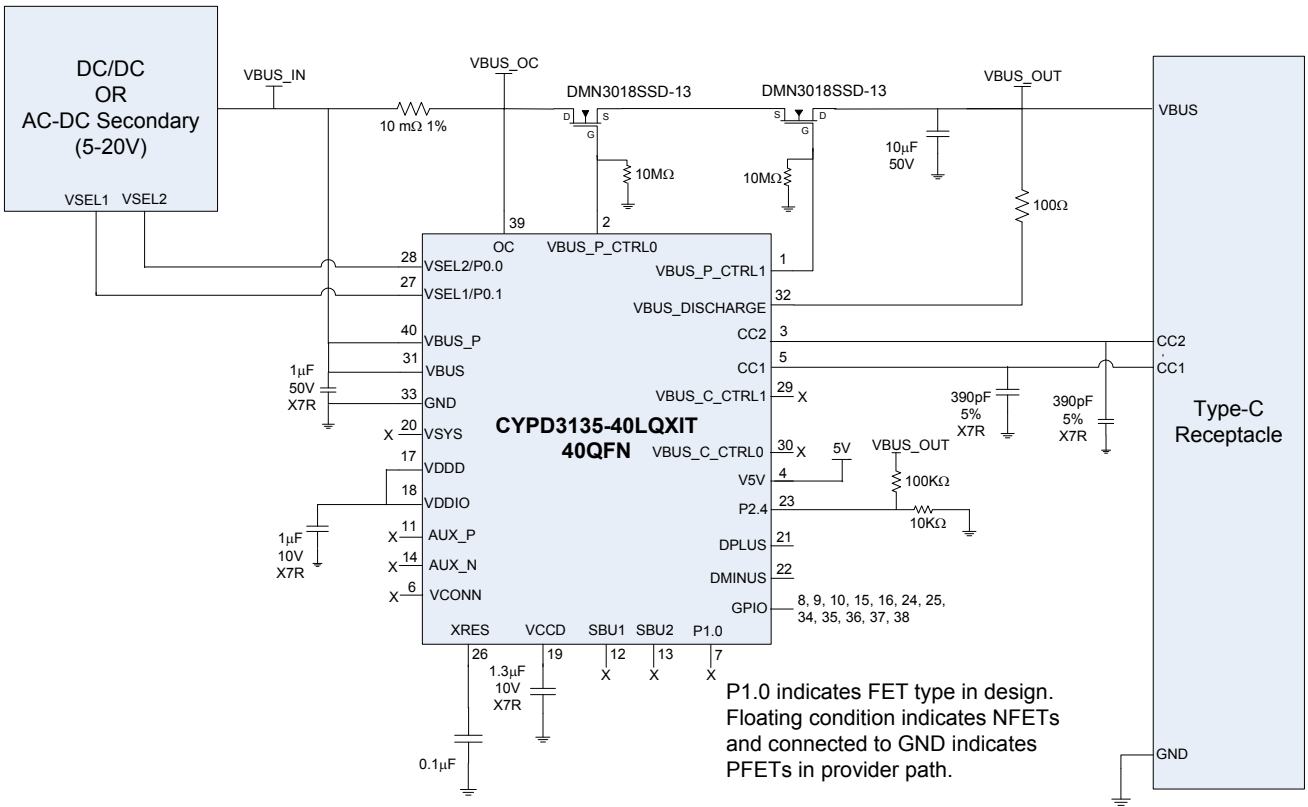


Figure 12 illustrates a power bank application diagram using a CCG3 device. In this application, the Type-C receptacle is used for providing as well as consuming power. The consumer path will be active when the battery is charged using a Type-C power source that is connected to the Type-C receptacle in Figure 12. The provider path will be active when the power bank is used for providing power to a sink device connected to the Type-C receptacle. Additionally, a Type-A receptacle can also be provided for providing power to the sinks that have a legacy USB interface.

The CCG3 device negotiates power contracts between the power bank and the sink/source device connected to the Type-C receptacle. The CCG3 device also controls and drives the provider and consumer path FETs and can monitor overcurrent and overvoltage conditions on the Type-C VBUS line.

Figure 12. Power Bank Application Diagram (40-QFN Device)

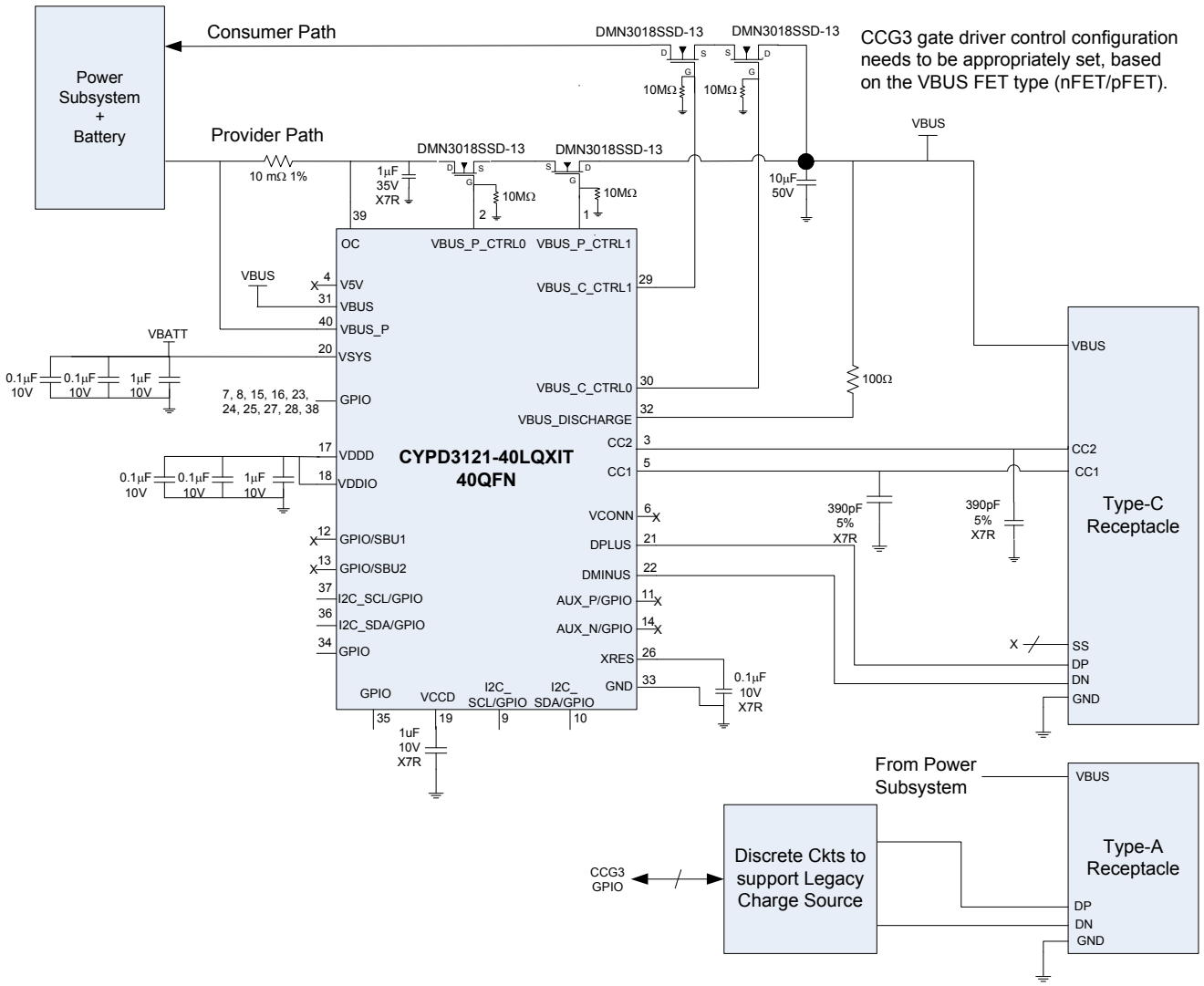


Figure 14 illustrates a USB Type-C to HDMI adapter application, which enables connectivity between a PC that supports a Type-C port with DisplayPort Alternate Mode support and a legacy monitor that has HDMI interface. It enables users of any Notebook that implements USB-Type C to connect to other display types.

This application meets the requirements described in Section 4.3 of the VESA DisplayPort Alt Mode on USB Type-C Standard Version 1.0. This application supports display output at a resolution of up to 4K Ultra HD (3840x2160) at 60 Hz.

Figure 14. USB Type-C to HDMI Adapter Application

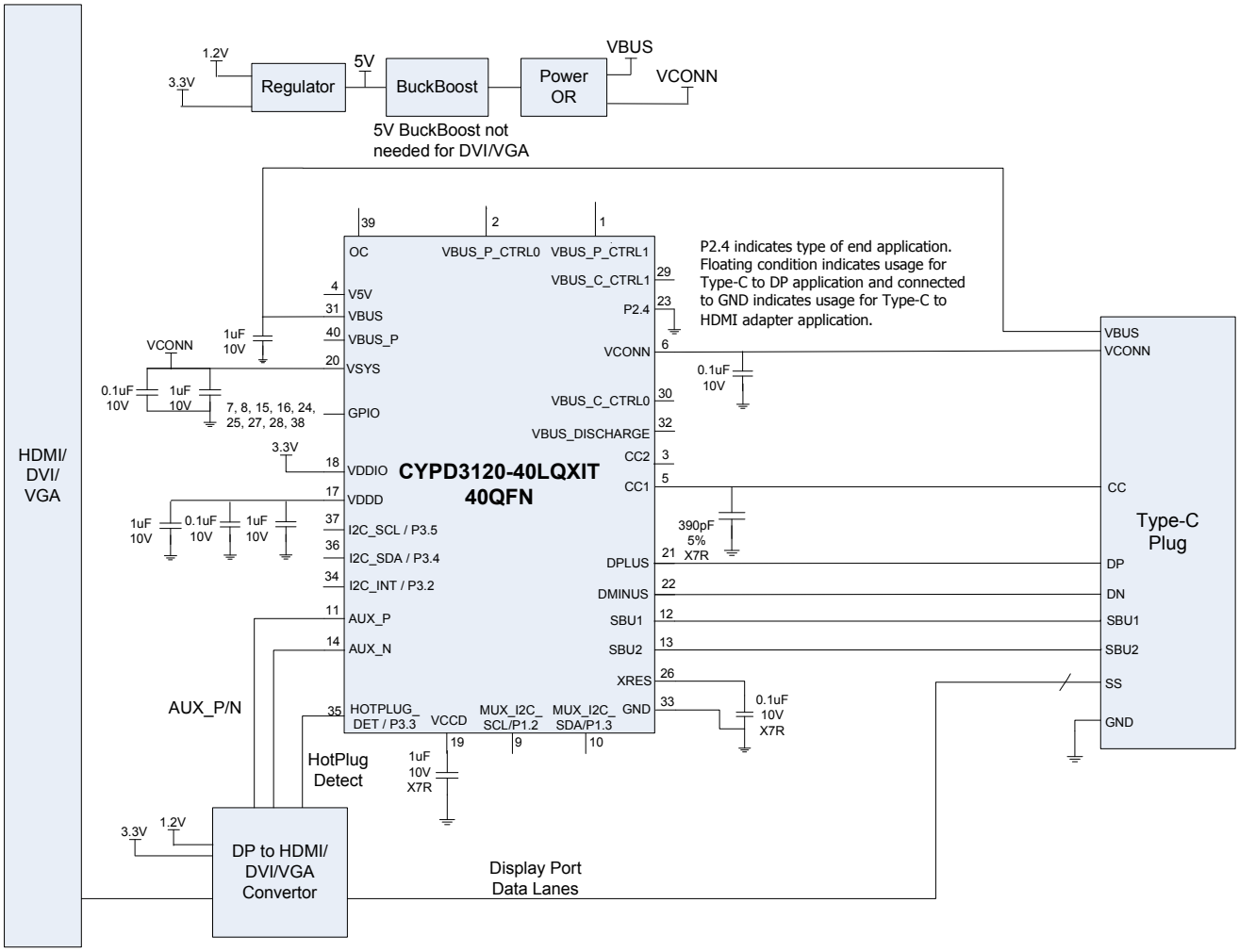
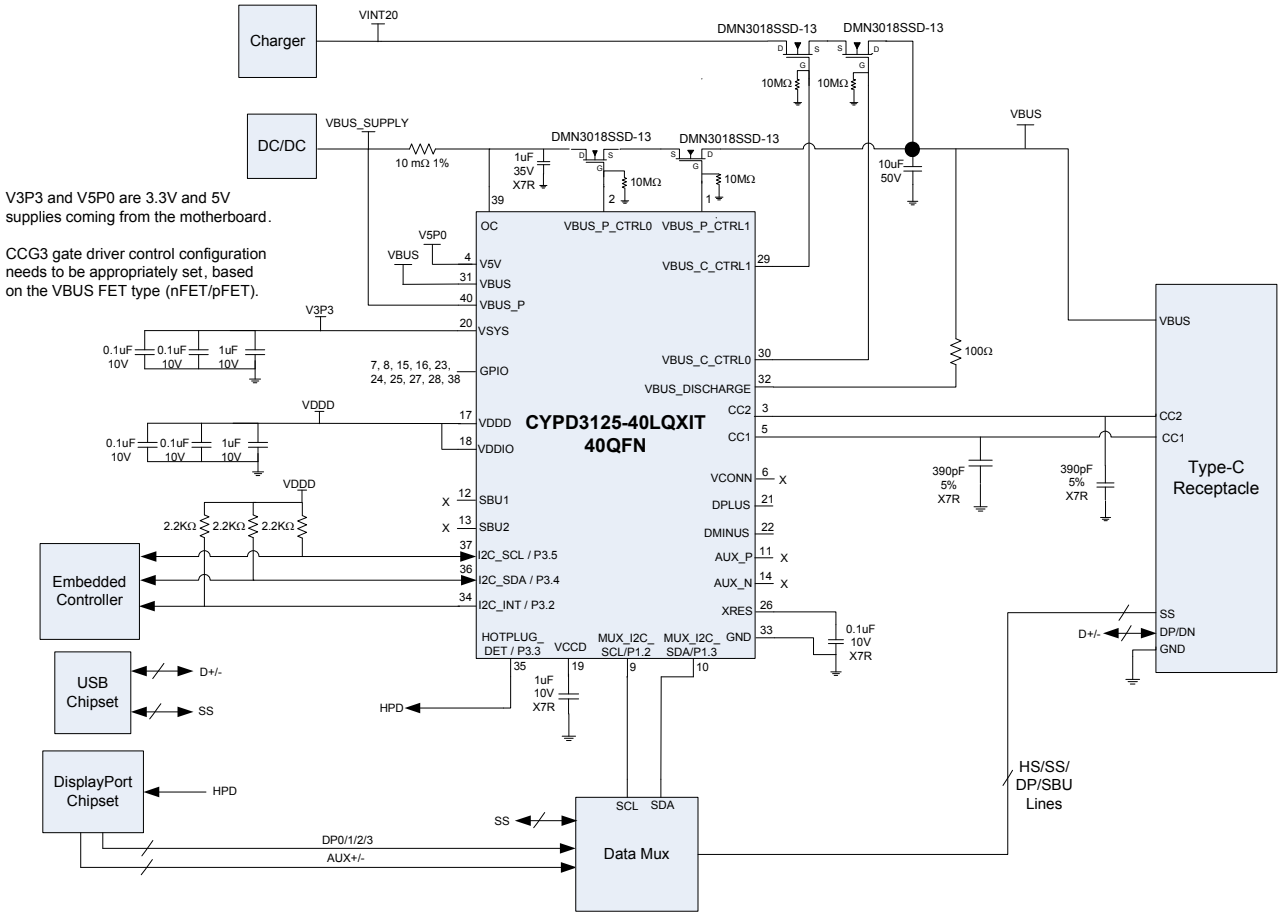


Figure 15 illustrates a Notebook DRP application diagram using a CCG3 device. The Type-C port can be used as a power provider or a power consumer. The CCG3 device communicates with the embedded controller (EC) over I^2C. It also controls the Data Mux to route the HighSpeed signals either to the USB chipset (during normal mode) or the DisplayPort Chipset (during Alternate Mode). The SBU, SuperSpeed, and HighSpeed lines are routed directly from the Display Mux of the notebook to the Type-C receptacle.

Figure 15. DRP Application Diagram



Electrical Specifications

Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{SYS_MAX}	Digital supply relative to V_{SS}	–0.5	–	6	V	Absolute max
V_{5V}	Max supply voltage relative to V_{SS}	–	–	6	V	
$V_{BUS\_MAX\_ON}$	Max supply voltage relative to V_{SS}, V_{BUS} regulator enabled	–	–	26	V	
$V_{BUS\_MAX\_OFF}$	Max supply voltage relative to V_{SS}, V_{BUS} regulator enabled 100% of the time	–	–	24.5	V	
	Max supply voltage relative to V_{SS}, V_{BUS} regulator enabled 25% of the time	–	–	26	V	
V_{DDIO_MAX}	Max supply voltage relative to V_{SS}	–	–	6	V	
V_{GPIO_ABS}	GPIO voltage	–0.5	–	VDDIO + 0.5	V	
$V_{GPIO\_OVT\_ABS}$	OVT GPIO voltage	–0.5	–	6	V	
I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	
V_{CONN_MAX}	Max voltage relative to V_{SS}	–	–	6	V	
V_{CC_ABS}	Max voltage on CC1 and CC2 pins	–	–	6	V	
$I_{GPIO\_INJECTION}$	GPIO injection current, Max for V_{IH} > VDDD, and Min for V_{IL} < V_{SS}	–0.5	–	0.5	mA	Absolute max, current injected per pin
ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	–
ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	–
LU	Pin current for latch-up	–100	–	100	mA	Tested at 125 °C
ESD_IEC_CON	Electrostatic discharge IEC61000-4-2	8000	–	–	V	Contact discharge on CC1, CC2, VBUS, DPLUS, DMINUS, SBU1 and SBU2 pins
ESD_IEC_AIR	Electrostatic discharge IEC61000-4-2	15000	–	–	V	Air discharge for CC1, CC2, VBUS, DPLUS, DMINUS, SBU1 and SBU2 pins

Device-Level Specifications

All specifications are valid for –40 °C ≤ TA ≤ 105 °C and TJ ≤ 120 °C, except where noted.

Table 4. DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.PWR#1	VSYS	–	2.7	–	5.5	V	UFP Mode.
SID.PWR#1_A	VSYS	–	3	–	5.5	V	DFP/DRP or Gate Driver Modes
SID.PWR#23	VCONN	Power Supply Input Voltage	2.7	–	5.5	V	–
SID.PWR#13	VDDIO	IO Supply Voltage	1.71	–	5.5[2]	V	2.7V < VDDD < 5.5 V
SID.PWR#13_A	VDDIO	IO Supply Voltage for ADC operation	2.7	–	5.5	V	2.7V < VDDD < 5.5 V
SID.PWR24	VCCD	Output Voltage for core Logic	–	1.8	–	V	–
SID.PWR#4	IDD	Supply current	–	25	–	mA	From VSYS or VBUS VBUS = 5V, T_A = 25 °C / VSYS = 5 V, TA = 25 °C FS USB, CC IO in Tx or Rx, no I/O sourcing current, 2 SCBs at 1 Mbps, CPU at 24 MHz.
SID.PWR#1_B	VSYS	Power supply for USB operation	4.5	–	5.5	V	USB configured, USB Regulator enabled
SID.PWR#1_C	VSYS	Power supply for USB operation	3.15	–	3.45	V	USB configured, USB Regulator disabled
SID.PWR#1_D	VSYS	Power supply for charger detect/emulation operation	3.15	–	5.5	V	–40 °C to +85 °C T_A
SID.PWR#27	VBUS	Power supply input voltage	3.5	–	21.5	V	FS USB disabled. Total current consumption from VBUS <15 mA.
SID.PwR#28	VBUS	Power supply input voltage for USB operation	4.5	–	21.5	V	FS USB configured, USB Regulator disabled
SID.PWR#30	VBUS_P	Power supply input voltage	4.00	–	21.5	V	
SID.PWR#15	C_{efc}	External regulator voltage bypass for VCCD	1	1.3	1.6	µF	X5R ceramic or better
SID.PWR#16	C_{exc}	Power supply decoupling capacitor for VSYS	0.8	1	–	µF	X5R ceramic or better
Sleep Mode. VSYS = 2.7 V to 5.5 V. Typical values measured at V_{DD} = 3.3 V and TA = 25 °C.							
SID25A	I_{DD20A}	CC, I^2C, WDT wakeup on. IMO at 48 MHz.	–	3.5	–	mA	VSYS = 3.3 V, T_A = 25 °C, All blocks except CPU are on, CC IO on, USB in Suspend Mode, no I/O sourcing current
Deep Sleep Mode							
SID_DS	I_{DD_DS}	VSYS = 3.0 to 3.6 V. CC Attach, I^2C, WDT Wakeup on.	–	30	–	µA	Power Source = VSYS, DFP Mode, Type-C Not Attached. CC Attach, I^2C and WDT enabled for Wakeup.
XRES Current							
SID307	I_{DD_XR}	Supply current while XRES asserted. This does not include current drawn due to the XRES internal pull-up resistor.	–	30	–	µA	Power Source = VSYS = 3.3 V, Type-C device not attached, T_A = 25 °C

Note

2. If VDDIO > VDDD, GPIO P2.4 cannot be used. It must be left unconnected. See Table 2 for pin numbers.

Table 6. I/O DC Specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
OVT							
SID.GIO#46	I_{IHS}	Input current when Pad > VDDIO for OVT inputs	–	–	10.00	µA	Per I^2C specification

Table 7. I/O AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID70	T_{RISEF}	Rise time in Fast Strong mode	2	–	12	ns	3.3 V VDDIO, C_{load} = 25 pF
SID71	T_{FALLF}	Fall time in Fast Strong mode	2	–	12	ns	3.3 V VDDIO, C_{load} = 25 pF

XRES

Table 8. XRES DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.XRES#1	V_{IH_XRES}	Input voltage HIGH threshold on XRES pin	0.7 × VDDIO	–	–	V	CMOS input
SID.XRES#2	V_{IL_XRES}	Input voltage LOW threshold on XRES pin	–	–	0.3 × VDDIO	V	CMOS input
SID.XRES#3	C_{IN_XRES}	Input capacitance on XRES pin	–	–	7	pF	Guaranteed by characterization
SID.XRES#4	$V_{HYSXRES}$	Input voltage hysteresis on XRES pin	–	0.05 × VDDIO	–	mV	Guaranteed by characterization

Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

Pulse Width Modulation (PWM) for GPIO Pins

Table 9. PWM AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.3	$T_{CPWMFREQ}$	Operating frequency	–	–	Fc	MHz	Fc max = CLK_SYS. Maximum = 48 MHz.
SID.TCPWM.4	$T_{PWMENEXT}$	Input trigger pulse width	2/Fc	–	–	ns	For all trigger events
SID.TCPWM.5	T_{PWMEXT}	Output trigger pulse width	2/Fc	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	T_{CRES}	Resolution of counter	1/Fc	–	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWM_{RES}	PWM resolution	1/Fc	–	–	ns	Minimum pulse width of PWM output
SID.TCPWM.5C	Q_{RES}	Quadrature inputs resolution	1/Fc	–	–	ns	Minimum pulse width between quadrature-phase inputs

Table 29. Gate Driver AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
AC.NGDO.1	T_{ON}	Gate turn-on time to gate_driver_supply_voltage + 5V for supply voltage ≥ 5V and VBUS * 2 for supply voltage < 5V	–	–	1	ms	1. Gate driver configuration = NFET 2. Load = The gate of a SI9936 MOSFET

SBU

Table 30. Analog Crossbar Switch Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.SBU.1	Ron_sw	Switch ON Resistance	–	–	10	Ω	Voltage input from 0 V to 3.6 V
SID.SBU.2	Rpu_aux_1	AUX_P/N Pull-up Resistance – 100k	80	–	120	kΩ	–
SID.SBU.3	Rpu_aux_2	AUX_P/N Pull-up Resistance – 1M	0.8	–	1.2	MΩ	–
SID.SBU.4	Rpd_aux_1	AUX_P/N Pull-down Resistance – 100k	80	–	120	kΩ	–
SID.SBU.5	Rpd_aux_2	AUX_P/N Pull-down Resistance – 1M	0.8	–	1.2	MΩ	–
SID.SBU.6	Rpd_aux_3	AUX_P/N Pull-down Resistance – 470k	329	–	611	kΩ	–
SID.SBU.7	Rpd_aux_4	AUX_P/N Pull-down Resistance – 4.7M	3.29	–	6.11	MΩ	–

Charger Detect

Table 31. Charger Detect Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CD.1	VDAT_REF	BC1.2 Data Detect Voltage Threshold	250	–	400	mV	–
SID.CD.2	VDM_SRC	BC1.2 DM Voltage Source	500	–	700	mV	With current sink of 25 µA–175 µA
SID.CD.3	VDP_SRC	BC1.2 DP Voltage Source	500	–	700	mV	With current sink of 25 µA–175 µA
SID.CD.4	IDM_SINK	BC1.2 DM Current Sink	25	–	175	µA	–
SID.CD.5	IDP_SINK	BC1.2 DP Current Sink	25	–	175	µA	–
SID.CD.6	IDP_SRC	BC1.2 DP DCD Current Source	7	–	13	µA	–
SID.CD.7	RDP_UP	USB FS DP Pull-up Termination	0.9	–	1.575	kΩ	–
SID.CD.8	RDM_UP	USB FS DM Pull-up Termination	0.9	–	1.575	kΩ	–
SID.CD.9	RDP_DWN	USB FS DP Pull-down Termination	14.25	–	24.8	kΩ	–
SID.CD.10	RDM_DWN	USB FS DM Pull-down Termination	14.25	–	24.8	kΩ	–
SID.CD.11	RDAT_LKG	DP/DM Data Line Leakage Termination	300	–	500	kΩ	The charger detect function and data line leakage is enabled.
SID.CD.12	RDCP_DAT	BC1.2 DCP Port Resistance between DP and DM	–	–	40	Ω	–
SID.CD.13	VSETH	USB FS Logic Threshold	1.26	–	1.54	V	–

Analog to Digital Converter

Table 32. ADC DC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.ADC.1	Resolution	ADC resolution	–	8	–	Bits	–
SID.ADC.2	INL	Integral non-linearity	–1.5	–	1.5	LSB	–
SID.ADC.3	DNL	Differential non-linearity	–2.5	–	2.5	LSB	–
SID.ADC.4	Gain Error	Gain error	–1	–	1	LSB	–

Table 33. ADC AC Specifications (Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.ADC.5	SLEW_Max	Rate of change of sampled voltage signal	–	–	3	V/ms	–

Table 34. VBUS_C Regulator DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.20vreg.1	VBUSREG	VBUS regulator output voltage measured at VDDD for VBUS = 4.5 V to 21.5 V	3	–	3.6	V	VBUS = 4.5 V - 21.5 V range. VDDD voltage measured with no load and a load of 30 mA.
SID.20vreg.2	VBUSREG2	VBUS regulator output voltage measured at VDDD for VBUS = 3.5 V to 21.5 V	3	–	3.6	V	VBUS = 4.5 V - 21.5 V range. VDDD voltage measured with no load and a load of 15 mA.
SID.20vreg.6	VBUSLINREG	VBUS regulator line regulation for VBUS from 4.5 V to 21.5 V	–	–	0.5	%/V	VBUS supply varied from 4.5 V to 21.5 V and the change in the VDDD measured. Guaranteed by Characterization.
SID.20vreg.8	VBUSLOADREG	VBUS regulator load regulation for VBUS from 4.5 V to 21.5 V	–	–	0.2	%/mA	Supply of 4.5 V - 21.5 V applied on VBUS and the load current swept from 0 to 30 mA. The change in VDDD is measured. Guaranteed by Characterization.

Table 35. VBUS_C Regulator AC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
AC.20vreg.1	T_{START}	Regulator Start-up time	–	–	120	µs	Apply VBUS and measure start time on VDDD pin.
AC.20vreg.2	T_{STOP}	Regulator power down time	–	–	1	µs	Time from assertion of an internal disable signal to for load current on VDDD to decrease from 30 mA to 10 µA.

Table 36. VSYS Switch Specification

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.vddsw.1	Res_sw	Resistance from VSYS supply input to the output supply VDDD	–	–	1.5	Ω	Measured with a load current of 5 mA - 10 mA on VDDD.

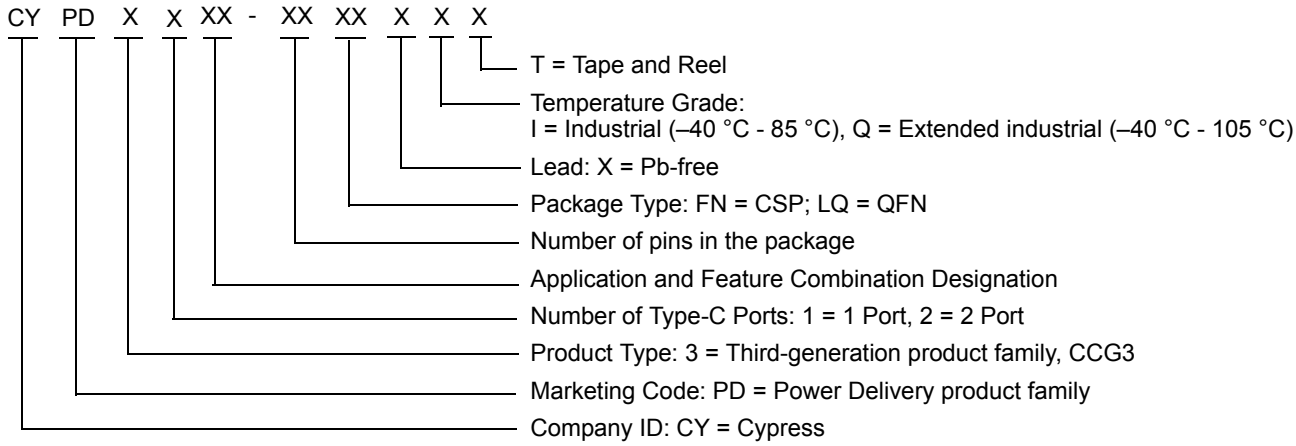
Ordering Information

Table 38 lists the EZ-PD CCG3 part numbers and features.

Table 38. EZ-PD CCG3 Ordering Information

Part Number	Application	Termination Resistor	Role	Default FW	Package	Si ID
CYPD3120-40LQXIT	Dongle	R_P, R_D[4], R_{D_DB}	UFP	USB Bootloader and Application FW	40-QFN	1D00
CYPD3121-40LQXIT	Power Banks	R_P[5], R_D, R_{D_DB}[6]	DRP	USB Bootloader	40-QFN	1D02
CYPD3122-40LQXIT	Monitor (DFP)	R_P, R_D, R_{D_DB}	DFP	I^2C Bootloader	40-QFN	1D03
CYPD3123-40LQXIT	Charge-through Dongle	R_P, R_D, R_{D_DB}	DRP	USB Bootloader and Application FW	40-QFN	1D09
CYPD3125-40LQXIT	Notebooks, Smartphones	R_P, R_D, R_{D_DB}	DRP	I^2C Bootloader	40-QFN	1D04
CYPD3126-42FNXIT	DRP	R_P, R_D[4], R_{D_DB}	DRP	I^2C Bootloader	42-CSP	1D07
CYPD3135-32LQXQT	Power Adapter	R_P	DFP	CC Bootloader and Application FW	32-QFN	1D08
CYPD3135-40LQXIT	Power Adapter	R_P	DFP	CC Bootloader and Application FW	40-QFN	1D05
CYPD3135-40LQXQT	Power Adapter	R_P	DFP	CC Bootloader and Application FW	40-QFN	1D05

Ordering Code Definitions



Notes
3. Termination resistor denoting an EMCA.
4. Termination resistor denoting an upstream facing port.
5. Termination resistor denoting a downstream facing port.
6. Termination resistor denoting dead battery termination.

Packaging

Table 39. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature	Industrial	–40	25	85	°C
		Extended Industrial			105	°C
T_J	Operating junction temperature	Industrial	–40	25	100	°C
		Extended Industrial			125	°C
T_{JA}	Package θ_{JA} (40-pin QFN)	–	–	–	17	°C/W
T_{JC}	Package θ_{JC} (40-pin QFN)	–	–	–	2	°C/W
T_{JA}	Package θ_{JA} (42-ball WLCSP)	–	–	–	34	°C/W
T_{JC}	Package θ_{JC} (42-ball WLCSP)	–	–	–	0.3	°C/W
T_{JA}	Package θ_{JA} (32-pin QFN)	–	–	–	18	°C/W
T_{JC}	Package θ_{JC} (32-pin QFN)	–	–	–	4	°C/W

Table 40. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time within 5 °C of Peak Temperature
40-pin QFN	260 °C	30 seconds
42-ball WLCSP	260 °C	30 seconds
32-pin QFN	260 °C	30 seconds

Table 41. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
42-ball WLCSP	MSL 1
40-pin QFN	MSL 3
32-pin QFN	MSL 3

Document Conventions

Units of Measure

Table 43. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
Hz	hertz
KB	1024 bytes
kHz	kilohertz
kΩ	kilo ohm
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
V	volt

References and Links to Applications Collaterals

Knowledge Base Articles

- Key Differences Among EZ-PD™ CCG1, CCG2, CCG3 and CCG4 - KBA210740
- Programming EZ-PD™ CCG2, EZ-PD™ CCG3 and EZ-PD™ CCG4 Using PSoC® Programmer and MiniProg3 - KBA96477
- CCGX Frequently Asked Questions (FAQs) - KBA97244
- Handling Precautions for CY4501 CCG1 DVK - KBA210560
- Cypress EZ-PD™ CCGx Hardware - KBA204102
- Difference between USB Type-C and USB-PD - KBA204033
- CCGx Programming Methods - KBA97271
- Getting started with Cypress USB Type-C Products - KBA04071
- Type-C to DisplayPort Cable Electrical Requirements
- Dead Battery Charging Implementation in USB Type-C Solutions - KBA97273
- Termination Resistors Required for the USB Type-C Connector – KBA97180
- VBUS Bypass Capacitor Recommendation for Type-C Cable and Type-C to Legacy Cable/Adapter Assemblies – KBA97270
- Need for Regulator and Auxiliary Switch in Type-C to DisplayPort (DP) Cable Solution - KBA97274
- Need for a USB Billboard Device in Type-C Solutions – KBA97146
- CCG1 Devices in Type-C to Legacy Cable/Adapter Assemblies – KBA97145
- Cypress USB Type-C Controller Supported Solutions – KBA97179
- Termination Resistors for Type-C to Legacy Ports – KBA97272
- Handling Instructions for CY4502 CCG2 Development Kit – KBA97916
- Thunderbolt™ Cable Application Using CCG3 Devices - KBA210976
- Power Adapter Application Using CCG3 Devices - KBA210975
- Methods to Upgrade Firmware on CCG3 Devices - KBA210974
- Device Flash Memory Size and Advantages - KBA210973
- Applications of EZ-PD™ CCG4 - KBA210739

Application Notes

- AN96527 - Designing USB Type-C Products Using Cypress's CCG1 Controllers
- AN95615 - Designing USB 3.1 Type-C Cables Using EZ-PD™ CCG2
- AN95599 - Hardware Design Guidelines for EZ-PD™ CCG2
- AN210403 - Hardware Design Guidelines for Dual Role Port Applications Using EZ-PD™ USB Type-C Controllers
- AN210771 - Getting Started with EZ-PD™ CCG4

Reference Designs

- EZ-PD™ CCG2 Electronically Marked Cable Assembly (EMCA) Paddle Card Reference Design
- EZ-PD™ CCG2 USB Type-C to DisplayPort Cable Solution
- CCG1 USB Type-C to DisplayPort Cable Solution
- CCG1 USB Type-C to HDMI/DVI/VGA Adapter Solution
- EZ-PD™ CCG2 USB Type-C to HDMI Adapter Solution
- CCG1 Electronically Marked Cable Assembly (EMCA) Paddle Card Reference Design
- CCG1 USB Type-C to Legacy USB Device Cable Paddle Card Reference Schematics
- EZ-USB GX3 USB Type-C to Gigabit Ethernet Dongle
- EZ-PD™ CCG2 USB Type-C Monitor/Dock Solution
- CCG2 20W Power Adapter Reference Design
- CCG2 18W Power Adapter Reference Design
- EZ-USB GX3 USB Type-A to Gigabit Ethernet Reference Design Kit

Kits

- CY4501 CCG1 Development Kit
- CY4502 EZ-PD™ CCG2 Development Kit
- CY4531 EZ-PD CCG3 Evaluation Kit
- CY4541 EZ-PD™ CCG4 Evaluation Kit

Datasheets

- CCG1 Datasheet: USB Type-C Port Controller with Power Delivery
- CYPD1120 Datasheet: USB Power Delivery Alternate Mode Controller on Type-C
- CCG2: USB Type-C Port Controller Datasheet
- CCG4: Two-Port USB Type-C Controller Datasheet

Document History Page

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Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	4905678	VGT	09/11/2015	New data sheet.
*A	4953333	VGT	10/08/2015	Updated General Description: Updated the number of GPIOs to 20. Updated Functional Overview: Updated GPIO: Updated the number of GPIOs to 20. Updated Pinouts: Updated Table 2. Updated Figure 4. Added Figure 6.
*B	5007726	VGT	11/25/2015	Changed status from Advance to Preliminary. Updated Features. Added EZ-PD CCG3 Block Diagram. Updated Functional Overview: Updated USB-PD Subsystem (USBPD SS) (Updated description). Added Full-Speed USB Subsystem. Updated Pinouts: Updated Table 2. Updated Figure 4. Updated Figure 6. Added Applications. Updated Electrical Specifications: Updated Absolute Maximum Ratings: Updated Table 3. Updated Device-Level Specifications: Updated Table 4. Updated Table 5. Updated I/O: Updated Table 6. Updated XRES: Updated Table 8. Updated System Resources: Updated Power-on-Reset (POR) with Brown Out SWD Interface: Updated Table 18. Updated Table 19. Updated Table 20. Updated Internal Main Oscillator: Updated Table 22. Updated Internal Low-Speed OscillatorPower Down: Updated Table 23. Updated Table 24. Updated Internal Low-Speed OscillatorPower Down: Updated Table 25.