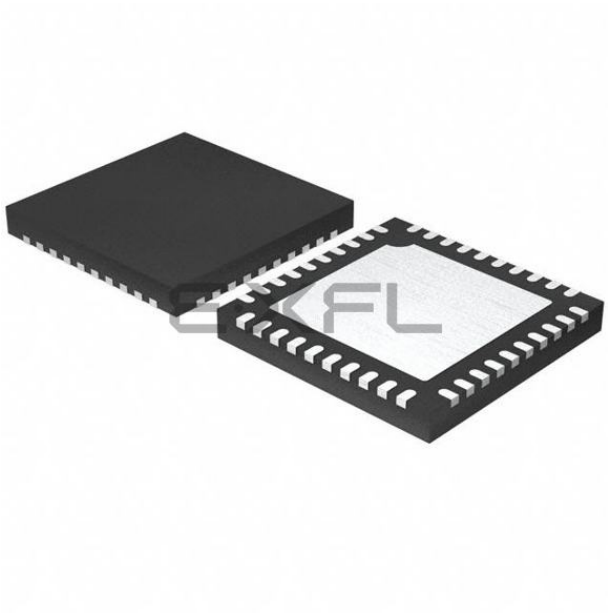

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Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	USB Type C
Core Processor	ARM® Cortex®-M0
Program Memory Type	FLASH (128kB)
Controller Series	-
RAM Size	8K x 8
Interface	I²C, SPI, UART/USART, USB
Number of I/O	16
Voltage - Supply	2.7V ~ 21.5V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cypd3121-40lqxit

Functional Overview

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in EZ-PD CCG3 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex-M3 and M4, thus enabling upward compatibility. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor up from the Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a serial wire debug (SWD) interface, which is a two-wire form of JTAG. The debug configuration used for EZ-PD CCG3 has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The EZ-PD CCG3 device has a flash module with two banks of 64 KB flash, a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 1 wait-state (WS) access time at 48 MHz and with 0-WS access time at 24 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

Crypto Block

CCG3 integrates a crypto block for hardware assisted authentication of firmware images. It also supports field upgradeability of firmware in a trusted ecosystem. The CCG3 Crypto block provides cryptography functionality. It includes hardware acceleration blocks for AES (Advanced Encryption Standard) block cipher, SHA-1 (Secure Hash Algorithm) and SHA-2 hash, Cyclic Redundancy Check (CRC) and pseudo random number generation.

Integrated Billboard Device

CCG3 integrates a complete full speed USB 2.0 device controller capable of functioning as a Billboard class device. The USB 2.0 device controller can also support other device classes.

USB-PD Subsystem (USBPD SS)

The USB-PD sub-system contains all of the blocks related to USB Type-C and Power Delivery. The sub-system is comprised of the following:

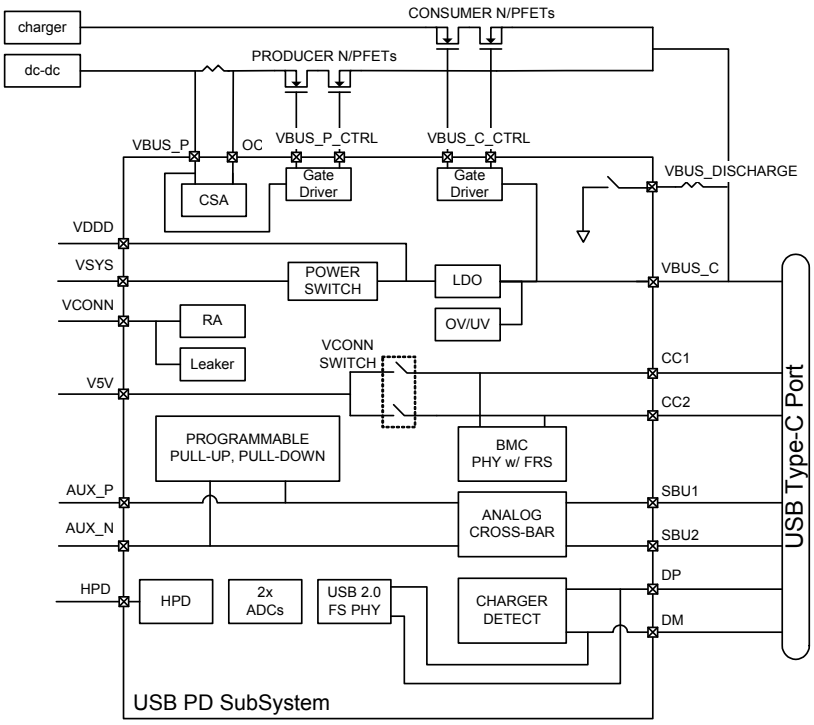
- BMC PHY: USB-PD Transceiver with Fast Role Swap (FRS) transmit and detect
- VCONN power FETs for the CC lines
- VCONN Ra Termination and Leakers
- Analog Cross-Bar to switch between the SBU1/SBU2 and AUX_P/AUX_N pins
- Programmable Pull-up and Pull-down termination on the AUX_P/AUX_N pins
- HPD Processor
- VBUS_C Regulator (20V LDO)
- Power Switch between VSYS supply and VBUS_C Regulator output
- VBUS_C Over-Voltage (OV) and Under-Voltage (UV) Detectors
- Current Sense Amplifier (CSA) for over current detection
- Gate Drivers for VBUS_P and VBUS_C external Power FETs
- VBUS_C discharge switch
- USB2.0 Full-Speed (FS) PHY with integrated 5.0V to 3.3V regulator
- Charger Detection / Emulation for USB BC1.2 and other proprietary protocols
- 2 instances of 8-bit SAR ADCs
- 8kV IEC ESD Protection on the following pins: VBUS_C, CC1, CC2, SBU1, SBU2, DP, DM

The EZ-PD™ CCG3 USB-PD subsystem interfaces to the pins of a USB Type-C connector. It includes a USB Type-C baseband transceiver and physical-layer logic. This transceiver performs the BMC and the 4b/5b encoding and decoding functions as well as integrating the 1.2V analog front end. This subsystem integrates the required terminations to identify the role of the CCG3 device, including Rp and Rd for UFP/DFP roles and Ra for EMCA/VCONN powered accessories. The programmable VCONN leakers are included in order to discharge VCONN capacitance during a disconnect event. It also integrates power FETs for supplying VCONN power to the CC1/CC2 pins from the V5V pin. The Analog Cross-Bar allows for connecting either of the SBU1/SBU2 pins to either of the AUX_P/AUX_N pins to support DisplayPort sideband signaling. The integrated HPD processor can be used to control or monitor the HPD signal of a DisplayPort source or sink.

The OV/UV (Over-Voltage/Under-Voltage) block monitors the VBUS_C supply for programmable over-voltage and under-voltage conditions. The CSA amplifies the voltage across an external sense resistor, which is proportional to the current being drawn from the external DC-DC VBUS supply converter. The CSA output can either be measured with an ADC or configured to detect an over-current condition. The VBUS_P and VBUS_C gate drivers control the gates of external power FETs for the VBUS_C and VBUS_P supplies. The gate drivers can be configured to support both P and N type external power FETs. The gate drivers are configured by default for nFET devices. In applications using pFETs, the gate drivers must be appropriately configured. The OV/UV and CSA blocks can generate interrupts to automatically turn off the power FETs for the programmed over-voltage and over-current conditions. The VBUS_C discharge switch allows for discharging the VBUS_C line through an external resistor.

The USB-PD sub-system also contains two 8-bit Successive Approximation Register (SAR) ADCs for analog to digital conversions. Each ADC includes an 8-bit DAC and a comparator. The DAC output forms the positive input of the comparator. The negative input of the comparator is from a 4-input multiplexer. The four inputs of the multiplexer are a pair of global analog multiplex busses, an internal bandgap voltage and an internal voltage proportional to the absolute temperature. Each GPIO pin can be connected to the global Analog Multiplex Busses through a switch, which allows either ADC to sample the pin voltage. When sensing the GPIO pin voltage with an ADC, the pin voltage cannot exceed the VDDD or VDDIO supply values.

Figure 2. USB-PD Subsystem



Full-Speed USB Subsystem

The FSUSB subsystem contains a full speed USB device controller as described in the Integrated Billboard Device section.

Peripherals

Serial Communication Blocks (SCB)

EZ-PD CCG3 has four SCBs, which can be configured to implement an I²C, SPI, or UART interface. The hardware I²C blocks implement full multi-master and slave interfaces capable of multimaster arbitration. In the SPI mode, the SCB blocks can be configured to act as master or slave.

In the I²C mode, the SCB blocks are capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and have flexible buffering options to reduce interrupt overhead and latency for the CPU. These blocks also support I²C that creates a mailbox address range in the memory of EZ-PD CCG3 and effectively reduce I²C communication to reading from and writing to an array in memory. In addition, the blocks support 8-deep FIFOs for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduce the need for clock stretching caused by the CPU not having read data on time.

The I²C peripherals are compatible with the I²C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I²C-bus specification and user manual (UM10204).

The I²C bus I/Os are implemented with GPIO in open-drain modes.

The I^2C port on SCB 1-3 blocks of EZ-PD CCG3 are not completely compliant with the I^2C specification in the following aspects:

- The GPIO cells for SCB 1's I^2C port are not overvoltage-tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I^2C system.
- Fast-mode Plus has an I_{OL} specification of 20 mA at a V_{OL} of 0.4V. The GPIO cells can sink a maximum of 8-mA I_{OL} with a V_{OL} maximum of 0.6V.
- Fast-mode and Fast-mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the bus load.

Timer/Counter/PWM Block (TCPWM)

EZ-PD CCG3 has four TCPWM blocks. Each implements a 16-bit timer, counter, pulse-width modulator (PWM), and quadrature decoder functionality.

GPIO

EZ-PD CCG3 has up to 20 GPIOs (these GPIOs can be configured for GPIOs, SCB, SBU, and Aux signals) and SWD pins, which can also be used as GPIOs. The I^2C pins from SCB 0 are overvoltage-tolerant.

The GPIO block implements the following:

- Seven drive strength modes:
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode)
- Selectable slew rates for dV/dt related noise control to improve EMI

During power-on and reset, the I/O pins are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Pinouts

Table 2. CCG3 Pin Description for 42-CSP, 32-QFN and 40-QFN Devices

Pin Map 42-CSP	Pin Map 32-QFN	Pin Map 40-QFN	Name	Description
A5	N/A	1	VBUS_P_CTRL1	VBUS Gate Driver Control 1 for Producer Switch
A6	1	2	VBUS_P_CTRL0	VBUS Gate Driver Control 0 for Producer Switch
B6	2	3	CC2	USB PD connector detect/Configuration Channel 2
C5	N/A	N/A	CC2	USB PD connector detect/Configuration Channel 2
D4	3	4	V5V	5.0V – 5.5V supply for VCONN FETs
C6	4	5	CC1	USB PD connector detect/Configuration Channel 1
D6	N/A	N/A	CC1	USB PD connector detect/Configuration Channel 1
E6	N/A	6	VCONN	VCONN Input - provides Ra termination for cable applications
F6	5	7	P1.0	GPIO/UART_2_TX / SPI_2_MISO
D5	N/A	8	P1.1	GPIO/UART_2_RX / SPI_2_SEL
E5	6	9	P1.2	GPIO/UART_0_RX/ UART_3_CTS/ SPI_3_MOSI/ I2C_3_SCL / HPD
G6	7	10	P1.3	GPIO/UART_0_TX/ UART_3_RTS/ SPI_3_CLK/ I2C_3_SDA
E4	N/A	11	AUX_P / P1.6	DisplayPort AUX_P signal / GPIO / UART_1_TX / SPI_1_MISO
F5	8	12	SBU1 / P1.4	USB Type-C SBU1 signal / GPIO / UART_3_TX/ SPI_3_MISO/ SWD_1_CLK
G5	9	13	SBU2 / P1.5	USB Type-C SBU2 signal / GPIO / UART_3_RX/ SPI_3_SEL/ SWD_1_DAT
G4	N/A	14	AUX_N / P1.7	DisplayPort AUX_N signal / GPIO / UART_1_RX / SPI_1_SEL
F4	10	15	P2.0	GPIO / UART_1_CTS / SPI_1_CLK/ I2C_1_SCL / SWD_0_DAT
G3	11	16	P2.1	GPIO / UART_1_RTS / SPI_1_MOSI/ I2C_1_SDA / SWD_0_CLK
G2	13	17	VDDD	VDDD Supply Input / Output (2.7 V–5.5 V)
F3	14	18	VDDIO	1.71 V–5.5 V supply for I/Os. This supply also powers the global analog multiplex buses.
F2	15	19	VCCD	1.8V regulator output for filter capacitor
G1	16	20	VSYS	System Power Supply (2.7 V–5.5 V)
F1	17	21	DPLUS	USB 2.0 DP
E1	18	22	DMINUS	USB 2.0 DM
E2	19	23	P2.4	GPIO
D3	20	24	P2.5	GPIO / UART_0_TX/ SPI_0_MOSI
D2	N/A	25	P2.6	GPIO / UART_0_RX/ SPI_0_CLK
D1	21	26	XRES	External Reset Input. Internally pulled-up to VDDIO.
C3	22	27	P0.0	I2C_0_SDA / GPIO_OVT / UART_0_CTS / SPI_0_SEL/ TCPWM0
C2	23	28	P0.1	I2C_0_SCL / GPIO_OVT / UART_0_RTS / SPI_0_MISO/ TCPWM1

Table 2. CCG3 Pin Description for 42-CSP, 32-QFN and 40-QFN Devices *(continued)*

Pin Map 42-CSP	Pin Map 32-QFN	Pin Map 40-QFN	Name	Description
C1	N/A	29	VBUS_C_CTRL1	VBUS Gate Driver Control 1 for Consumer Switch
C4	24	30	VBUS_C_CTRL0	VBUS Gate Driver Control 0 for Consumer Switch
B1	25	31	VBUS	VBUS Input
A1	26	32	VBUS_DISCHARGE	VBUS Discharge Control output
E3	12, 27	33	VSS	Ground Supply (GND)
	EPAD	EPAD	VSS	
A2	28	34	P3.2	GPIO / TCPWM0
B2	N/A	35	P3.3	GPIO / TCPWM1
B3	29	36	P3.4	GPIO / UART_2_CTS / SPI_2_MOSI/ I2C_2_SDA / TCPWM2
A3	30	37	P3.5	GPIO / UART_2_RTS / SPI_2_CLK/ I2C_2_SCL / TCPWM3
B4	N/A	38	P3.6	GPIO
A4	31	39	OC	Over-current Sensor Input
B5	32	40	VBUS_P	VBUS Producer Input

Figure 4. Pinout of 40-QFN Package (Top View)

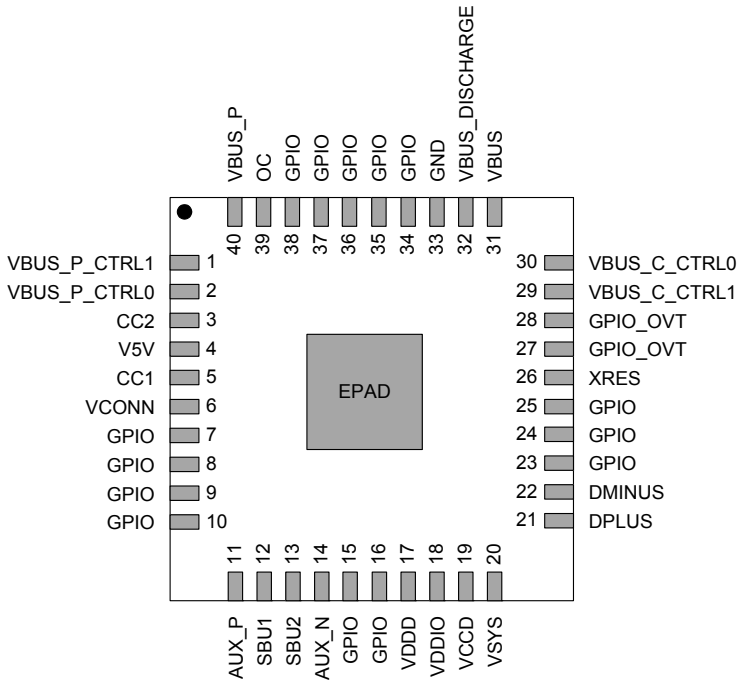


Figure 5. Pinout of 32-QFN Package (Top View)

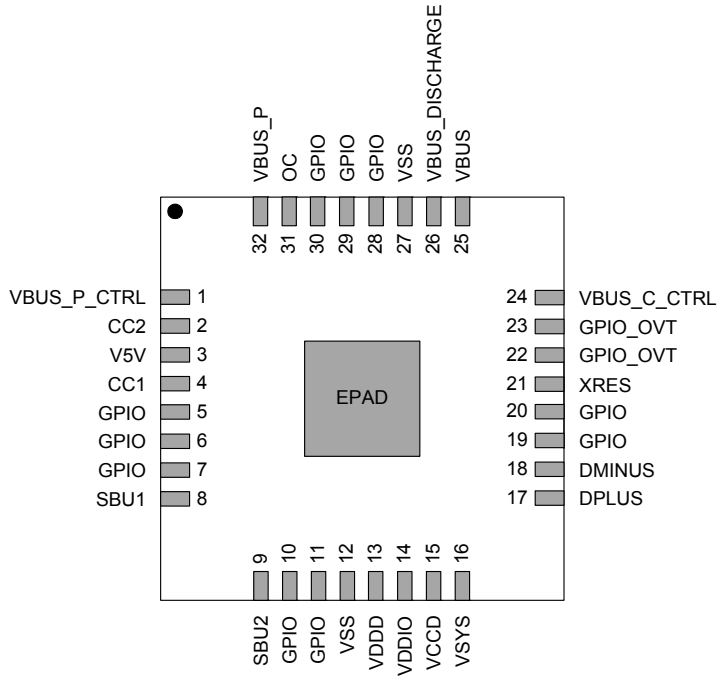
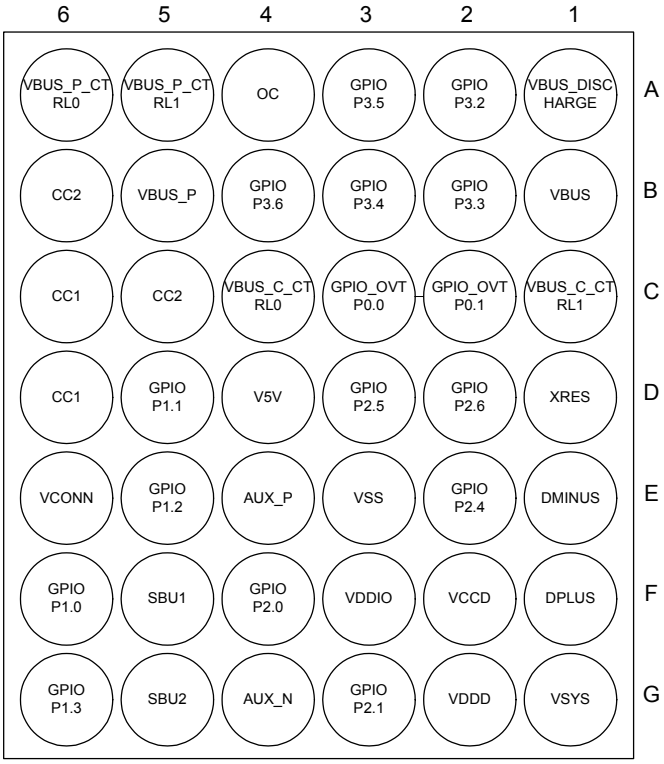


Figure 6. Pinout of 42-WLCSP Bottom (Balls Up) View



Available Firmware and Software Tools

EZ-PD Configuration Utility

The EZ-PD Configuration Utility is a GUI-based Microsoft Windows application developed by Cypress to guide a CCGx user through the process of configuring and programming the chip. The utility allows users to:

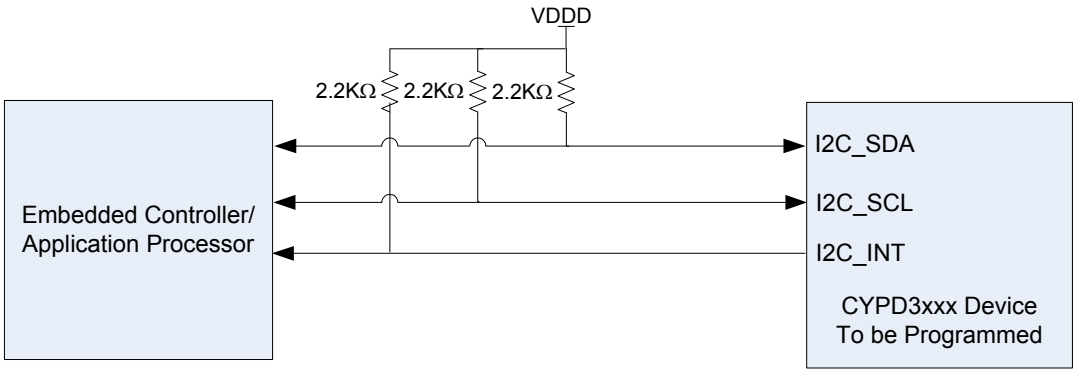
1. Select and configure the parameters they want to modify
2. Program the resulting configuration onto the target CCGx device.

The utility works with the Cypress supplied CCG1, CCG2, CCG3, and CCG4 kits, which host the CCGx controllers along with a USB interface. This version of the EZ-PD Configuration Utility supports configuration and firmware update operations on CCGx controllers implementing EMCA and Display Dongle applications. Support for other applications, such as Power Adapters and Notebook port controllers, will be provided in later versions of the utility.

You can download the EZ-PD Configuration Utility and its associated documentation at the following link:

http://www.cypress.com/documentation/software-and-drivers/ez-pd-configuration-utility

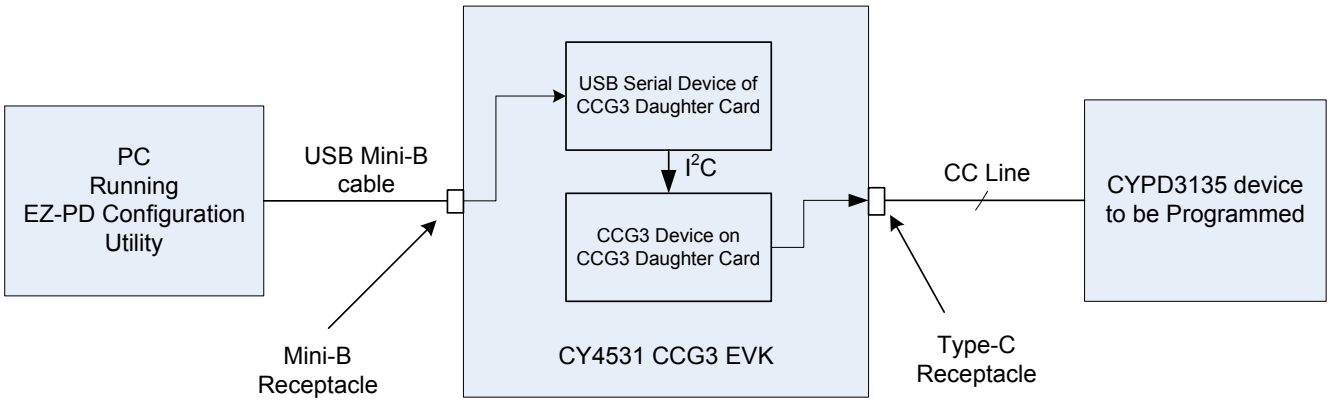
Figure 8. Application Firmware Update over I²C Interface



Application Firmware Update over CC Line

This method primarily applies to CYPD3135 device of the CCG3 family. In these applications, the CY4531 CCG3 EVK can be used to send programming and configuration data as Cypress specific Vendor Defined Messages (VDMs) over the CC line. The CY4531 CCG3 EVK is connected to the system containing CCG3 device on one end and a Windows PC running the EZ-PDTM Configuration Utility as shown in Figure 9 on the other end to program the CCG3 device.

Figure 9. Application Firmware Update over CC Line



Application Firmware Update over USB

This method primarily applies to the CYPD3120 and CYPD3121 devices of the CCG3 family. In these applications, the firmware update can be performed over the D+/D- lines (USB2.0) using various possible options as shown in Figure 10. Option 1 is to have a Windows PC running EZ-PD™ Configuration Utility connected to the device to be programmed via the CY4531 CCG3 EVK. This setup can be avoided using option 2, where the user has a Type-A to Type-C cable. This option requires that the system contain the CCG3 device to be programmed to have a Type-C receptacle. The other option (Option 3) is to have a Windows PC with a native Type-C connector as shown in Figure 10.

Figure 13 illustrates a USB Type-C to DisplayPort (4-lane) adapter application, which enables connectivity between a PC that supports a Type-C port with DisplayPort Alternate Mode support and a legacy monitor that has a DisplayPort interface. The application meets the requirements described in Section 4.2 of the VESA DisplayPort Alt Mode on USB Type-C Standard Version 1.0 (Scenarios 2a and 2b USB Type-C to DisplayPort Cables).

Figure 13. USB Type-C to DisplayPort Adapter Application Diagram

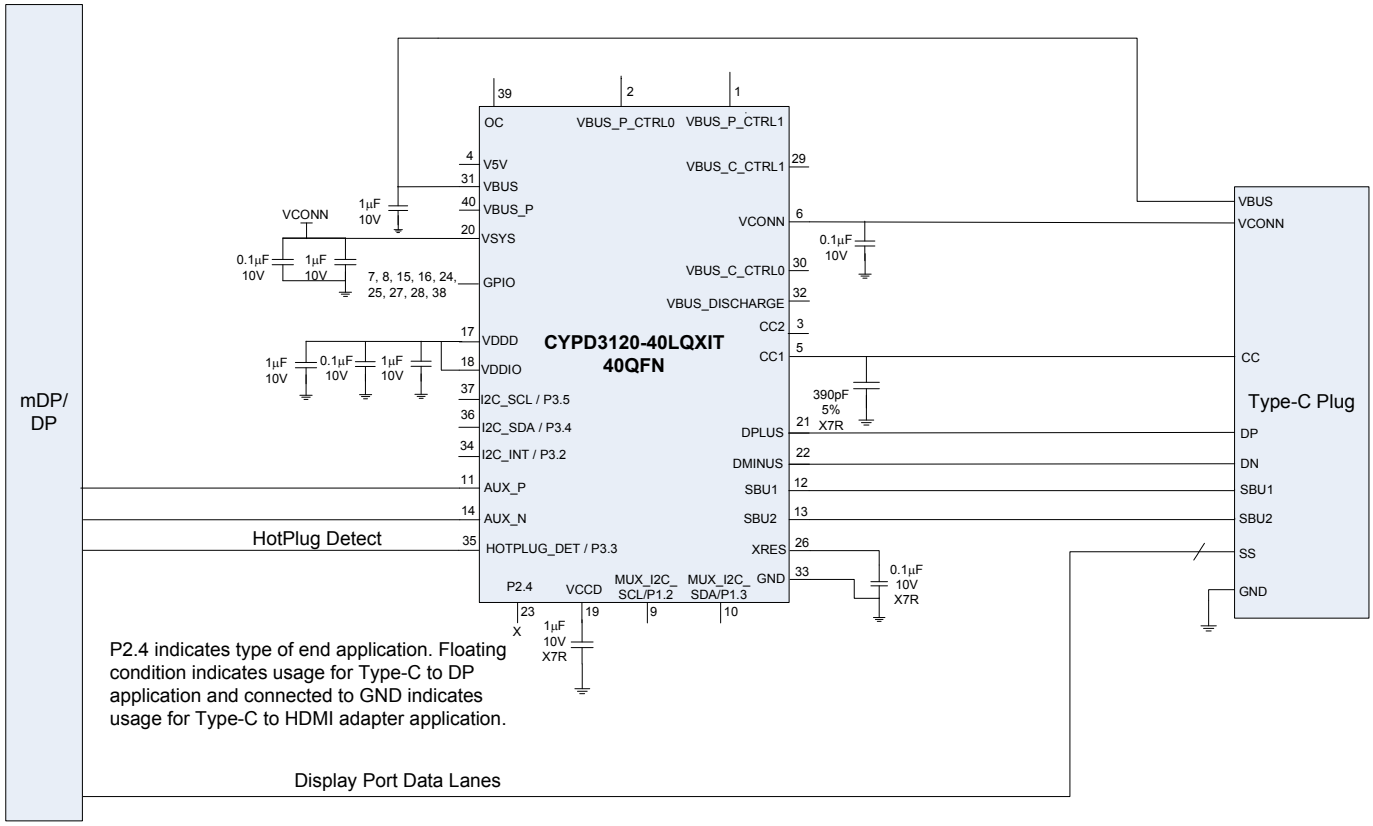


Figure 16 illustrates a CCG3 device based Charge-through Dongle application block diagram. This Charge-through dongle application also implements Cypress's USB SuperSpeed Hub controller HX3 (CYUSB3304-68LTXI) available in 68-QFN package, Low-power single chip USB 3.0 to Gigabit Ethernet Bridge Controller GX3 (CYUSB3610-68LTXC) available in 68-QFN package and the CCG2 (CYPD2122-24LQXI) which acts as an Upstream Facing Port (UFP) and sinks power when connected to USB Type-C chargers.

This application enables connectivity between a USB Type-C Notebook and HDMI Display, legacy USB device and Gigabit Ethernet while also connecting a USB Type-C charging cable. The Charge-Through Dongle solution allows simultaneous HDMI display, Superspeed data transfers, Ethernet connection and charging of a USB Type-C Notebook. Charge-Through Dongle is also widely known as Multiport Adapter. More details including the schematic of the CCG3 device based Charge-through Dongle reference design can be found here.

Figure 16. Charge-through Dongle Application Block Diagram (40-QFN Device)

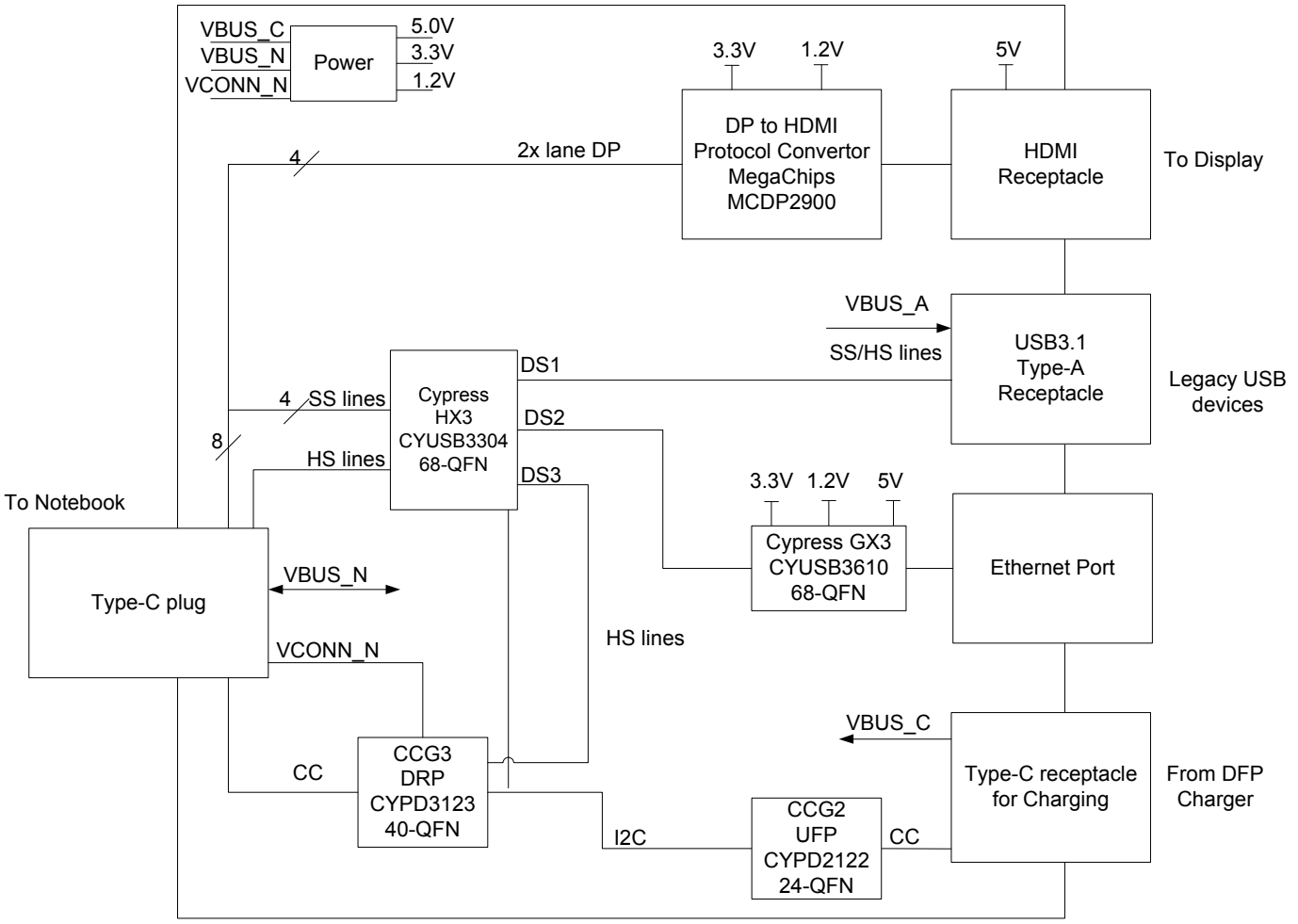


Table 6. I/O DC Specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
OVT							
SID.GIO#46	I_{IHS}	Input current when Pad > VDDIO for OVT inputs	–	–	10.00	µA	Per I^2C specification

Table 7. I/O AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID70	T_{RISEF}	Rise time in Fast Strong mode	2	–	12	ns	3.3 V VDDIO, C_{load} = 25 pF
SID71	T_{FALLF}	Fall time in Fast Strong mode	2	–	12	ns	3.3 V VDDIO, C_{load} = 25 pF

XRES

Table 8. XRES DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.XRES#1	V_{IH_XRES}	Input voltage HIGH threshold on XRES pin	0.7 × VDDIO	–	–	V	CMOS input
SID.XRES#2	V_{IL_XRES}	Input voltage LOW threshold on XRES pin	–	–	0.3 × VDDIO	V	CMOS input
SID.XRES#3	C_{IN_XRES}	Input capacitance on XRES pin	–	–	7	pF	Guaranteed by characterization
SID.XRES#4	$V_{HYSXRES}$	Input voltage hysteresis on XRES pin	–	0.05 × VDDIO	–	mV	Guaranteed by characterization

Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

Pulse Width Modulation (PWM) for GPIO Pins

Table 9. PWM AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.3	$T_{CPWMFREQ}$	Operating frequency	–	–	Fc	MHz	Fc max = CLK_SYS. Maximum = 48 MHz.
SID.TCPWM.4	$T_{PWMENEXT}$	Input trigger pulse width	2/Fc	–	–	ns	For all trigger events
SID.TCPWM.5	T_{PWMEXT}	Output trigger pulse width	2/Fc	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	T_{CRES}	Resolution of counter	1/Fc	–	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWM_{RES}	PWM resolution	1/Fc	–	–	ns	Minimum pulse width of PWM output
SID.TCPWM.5C	Q_{RES}	Quadrature inputs resolution	1/Fc	–	–	ns	Minimum pulse width between quadrature-phase inputs

Table 25. PD DC Specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.PD.8	R_{leak_1}	VCONN leaker for 0.1-µF load	–	–	216	kΩ	Managed Active Cable (MAC) discharge.
SID.PD.9	R_{leak_2}	VCONN leaker for 0.5-µF load	–	–	43.2	kΩ	
SID.PD.10	R_{leak_3}	VCONN leaker for 1.0-µF load	–	–	21.6	kΩ	
SID.PD.11	R_{leak_4}	VCONN leaker for 2.0-µF load	–	–	10.8	kΩ	
SID.PD.12	R_{leak_5}	VCONN leaker for 5.0-µF load	–	–	4.32	kΩ	
SID.PD.13	R_{leak_6}	VCONN leaker for 10-µF load	–	–	2.16	kΩ	
SID.PD.14	I_{leak}	Leaker on VCONN for discharge upon cable detach	150	–	550	µA	–
SID.PD.15	$V_{gndoffset}$	Ground offset tolerated by BMC receiver	–400	–	400	mV	Relative to the remote BMC transmitter. Guaranteed by characterization.

Table 26. CSA Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CSA.1	Out_E_Trim_15_DS	Overall Error at Av = 15 using deep sleep reference	–7.00	–	7.00	%	Guaranteed by characterization.
SID.CSA.2	Out_E_Trim_15_BG	Overall Error at Av = 15 using bandgap reference	–4.50	–	4.50	%	Guaranteed by characterization.
SID.CSA.3	Out_E_Trim_100	Overall Error at Av = 100 using either bandgap or deep sleep reference	–24.50	–	24.50	%	–

Table 27. UV/OV Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.UVOV.1	$V_{THUVOV1}$	Voltage threshold Accuracy, $V_{BUS} \leq 16$ V	–6		6	%	Tested at VBUS = 3.75 V, 4.5 V, 5.25 V, 12 V, 16 V
SID.UVOV.2	$V_{THUVOV2}$	Voltage threshold Accuracy, $V_{BUS} > 16$ V	–10		10	%	Tested at VBUS = 20 V

Gate Driver Specifications

Table 28. Gate Driver DC Specifications

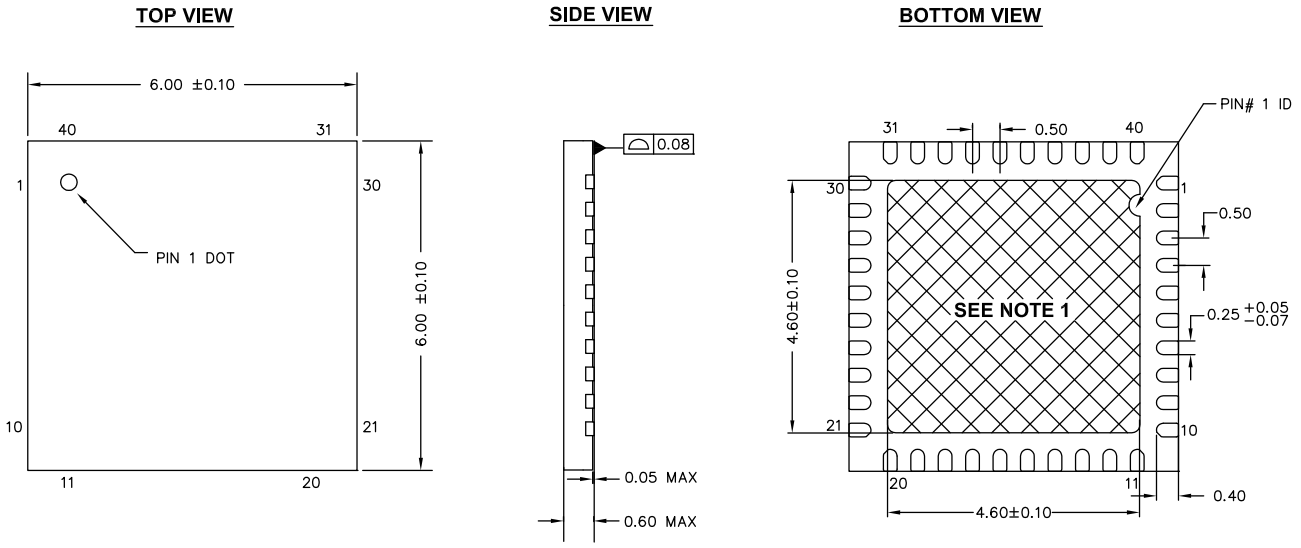
Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
DC.NGDO.1	VGS1	Gate to Source Overdrive	5	–	16.5	V	1. Gate driver Supply Voltage ≥ 5V, where Gate driver supply voltage = VBUS _P for VBUS_P_CTRL_ outputs, and VBUS_C for VBUS_C_CTRL_ outputs. 2. Gate driver current = 0 3. Gate driver configuration = NFET 4. Gate driver pump clock divider = 1
DC.NGDO.2	VGS2	Gate to Source Overdrive	3.75	–	16.5	V	1. Gate driver Supply Voltage ≥ 3.75V, where Gate driver supply voltage = VBUS _P for VBUS_P_CTRL_ outputs, and VBUS_C for VBUS_C_CTRL_ outputs. 2. Gate driver current = 0 3. Gate driver configuration = NFET 4. Gate driver pump clock divider = 1
DC.NGDO.6	R_{PD}	Resistance when “pull down” enabled	–	–	5	kΩ	–

Memory

Table 37. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.MEM#3	FLASH_ERASE	Row erase time	–	–	15.5	ms	–
SID.MEM#4	FLASH_WRITE	Row (Block) write time (erase and program)	–	–	20	ms	–
SID.MEM#8	FLASH_ROW_PGM	Row program time after erase	–	–	7	ms	–
SID178	TBULKERASE	Bulk erase time (64k Bytes)	–	–	35	ms	–
SID180	TDEVPROG	Total device program time	–	–	7.5	s	Guaranteed by characterization
SID182	FRET1	Flash retention, $T_A \le 55$ °C, 100 K P/E cycles	20	–	–	years	Guaranteed by characterization
SID182A	FRET2	Flash retention, $T_A \le 85$ °C, 10 K P/E cycles	10	–	–	years	Guaranteed by characterization
SID182B	FRET3	Flash retention, $T_A \le 105$ °C, 10 K P/E cycles	3	–	–	years	Guaranteed by characterization

Figure 17. 40-pin QFN Package Outline, 001-80659

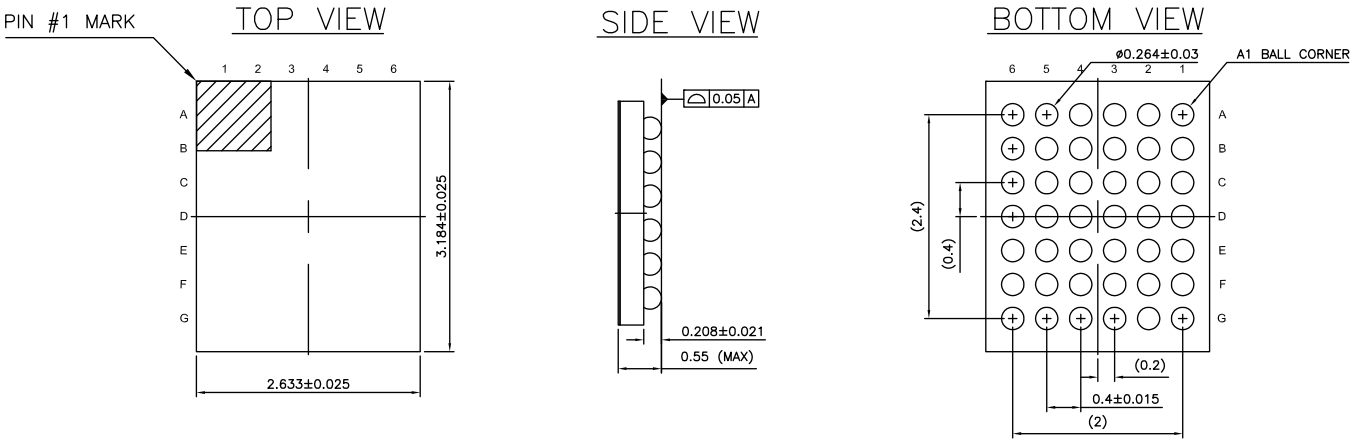


NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT: 68 ±2 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-80659 *A

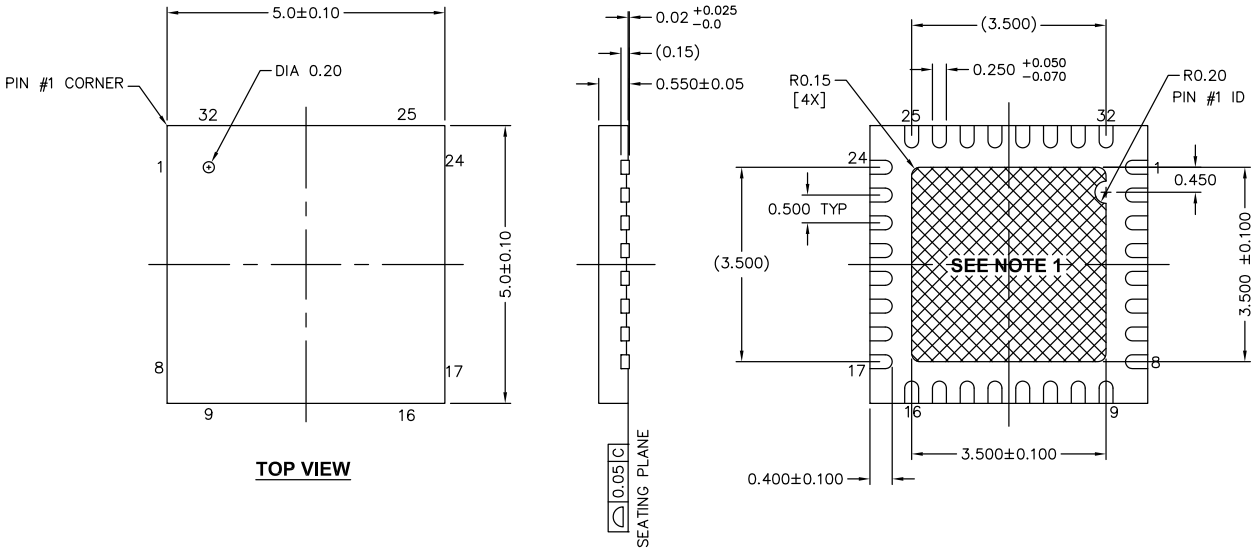
Figure 18. 42-ball CSP Package Outline, 002-04062



002-04062 *A

ALL DIMENSIONS ARE IN MM
JEDEC Publication 95; Design Guide 4.18

Figure 19. 32-pin QFN Package Outline, 001-42168



NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO−248
3. PACKAGE WEIGHT: 0.0388g
4. DIMENSIONS ARE IN MILLIMETERS

001-42168 *E

Document Conventions

Units of Measure

Table 43. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
Hz	hertz
KB	1024 bytes
kHz	kilohertz
kΩ	kilo ohm
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
V	volt

References and Links to Applications Collaterals

Knowledge Base Articles

- Key Differences Among EZ-PD™ CCG1, CCG2, CCG3 and CCG4 - KBA210740
- Programming EZ-PD™ CCG2, EZ-PD™ CCG3 and EZ-PD™ CCG4 Using PSoC® Programmer and MiniProg3 - KBA96477
- CCGX Frequently Asked Questions (FAQs) - KBA97244
- Handling Precautions for CY4501 CCG1 DVK - KBA210560
- Cypress EZ-PD™ CCGx Hardware - KBA204102
- Difference between USB Type-C and USB-PD - KBA204033
- CCGx Programming Methods - KBA97271
- Getting started with Cypress USB Type-C Products - KBA04071
- Type-C to DisplayPort Cable Electrical Requirements
- Dead Battery Charging Implementation in USB Type-C Solutions - KBA97273
- Termination Resistors Required for the USB Type-C Connector – KBA97180
- VBUS Bypass Capacitor Recommendation for Type-C Cable and Type-C to Legacy Cable/Adapter Assemblies – KBA97270
- Need for Regulator and Auxiliary Switch in Type-C to DisplayPort (DP) Cable Solution - KBA97274
- Need for a USB Billboard Device in Type-C Solutions – KBA97146
- CCG1 Devices in Type-C to Legacy Cable/Adapter Assemblies – KBA97145
- Cypress USB Type-C Controller Supported Solutions – KBA97179
- Termination Resistors for Type-C to Legacy Ports – KBA97272
- Handling Instructions for CY4502 CCG2 Development Kit – KBA97916
- Thunderbolt™ Cable Application Using CCG3 Devices - KBA210976
- Power Adapter Application Using CCG3 Devices - KBA210975
- Methods to Upgrade Firmware on CCG3 Devices - KBA210974
- Device Flash Memory Size and Advantages - KBA210973
- Applications of EZ-PD™ CCG4 - KBA210739

Application Notes

- AN96527 - Designing USB Type-C Products Using Cypress's CCG1 Controllers
- AN95615 - Designing USB 3.1 Type-C Cables Using EZ-PD™ CCG2
- AN95599 - Hardware Design Guidelines for EZ-PD™ CCG2
- AN210403 - Hardware Design Guidelines for Dual Role Port Applications Using EZ-PD™ USB Type-C Controllers
- AN210771 - Getting Started with EZ-PD™ CCG4

Reference Designs

- EZ-PD™ CCG2 Electronically Marked Cable Assembly (EMCA) Paddle Card Reference Design
- EZ-PD™ CCG2 USB Type-C to DisplayPort Cable Solution
- CCG1 USB Type-C to DisplayPort Cable Solution
- CCG1 USB Type-C to HDMI/DVI/VGA Adapter Solution
- EZ-PD™ CCG2 USB Type-C to HDMI Adapter Solution
- CCG1 Electronically Marked Cable Assembly (EMCA) Paddle Card Reference Design
- CCG1 USB Type-C to Legacy USB Device Cable Paddle Card Reference Schematics
- EZ-USB GX3 USB Type-C to Gigabit Ethernet Dongle
- EZ-PD™ CCG2 USB Type-C Monitor/Dock Solution
- CCG2 20W Power Adapter Reference Design
- CCG2 18W Power Adapter Reference Design
- EZ-USB GX3 USB Type-A to Gigabit Ethernet Reference Design Kit

Kits

- CY4501 CCG1 Development Kit
- CY4502 EZ-PD™ CCG2 Development Kit
- CY4531 EZ-PD CCG3 Evaluation Kit
- CY4541 EZ-PD™ CCG4 Evaluation Kit

Datasheets

- CCG1 Datasheet: USB Type-C Port Controller with Power Delivery
- CYPD1120 Datasheet: USB Power Delivery Alternate Mode Controller on Type-C
- CCG2: USB Type-C Port Controller Datasheet
- CCG4: Two-Port USB Type-C Controller Datasheet

Document History Page

Document Title: EZ-PD™ CCG3 USB Type-C Port Controller Document Number: 002-03288				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	4905678	VGT	09/11/2015	New data sheet.
*A	4953333	VGT	10/08/2015	Updated General Description: Updated the number of GPIOs to 20. Updated Functional Overview: Updated GPIO: Updated the number of GPIOs to 20. Updated Pinouts: Updated Table 2. Updated Figure 4. Added Figure 6.
*B	5007726	VGT	11/25/2015	Changed status from Advance to Preliminary. Updated Features. Added EZ-PD CCG3 Block Diagram. Updated Functional Overview: Updated USB-PD Subsystem (USBPD SS) (Updated description). Added Full-Speed USB Subsystem. Updated Pinouts: Updated Table 2. Updated Figure 4. Updated Figure 6. Added Applications. Updated Electrical Specifications: Updated Absolute Maximum Ratings: Updated Table 3. Updated Device-Level Specifications: Updated Table 4. Updated Table 5. Updated I/O: Updated Table 6. Updated XRES: Updated Table 8. Updated System Resources: Updated Power-on-Reset (POR) with Brown Out SWD Interface: Updated Table 18. Updated Table 19. Updated Table 20. Updated Internal Main Oscillator: Updated Table 22. Updated Internal Low-Speed OscillatorPower Down: Updated Table 23. Updated Table 24. Updated Internal Low-Speed OscillatorPower Down: Updated Table 25.

Document History Page *(continued)*

Document Title: EZ-PD™ CCG3 USB Type-C Port Controller Document Number: 002-03288				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*E (cont.)	5240836	VGT	04/28/2016	Updated Power Systems Overview: Updated description. Updated Figure 3. Updated Pinouts: Updated Table 2: Updated details in “Description” column corresponding to VDDIO pin. Removed table “CCG3 Pin Description for 16-SOIC Device”. Removed figure “Pinout of 16-SOIC Package (Top View)”. Updated Applications: Removed figure “Power Adapter Application Diagram (16-SOIC Device)”. Added Figure 12. Updated Electrical Specifications: Updated Device-Level Specifications: Updated Table 4. Updated details in “Details/Conditions” column corresponding to “SID.PWR#1_A” Spec ID and “V_{SYS}” parameter. Replaced “V_{DDD}” with “5.5” in “Max” column corresponding to “SID.PWR#13” Spec ID and “V_{DDIO}” parameter. Added “SID.PWR#13_A” Spec ID corresponding to “V_{DDIO}” parameter and its details. Added “SID.PWR#1_C” and “SID.PWR#1_D” Spec IDs corresponding to “V_{SYS}” parameter and its details. Replaced “enabled” with “disabled” in “Details/Conditions” column corresponding to “SID.PwR#28” Spec ID and “V_{BUS}” parameter. Updated details in “Description” and “Details/Conditions” columns corresponding to “SID307” Spec ID and “I_{DD_XR}” parameter. Updated System Resources: Added Gate Driver Specifications, Charger Detect. Updated Ordering Information: Updated part numbers. Updated details in “Application” column corresponding to part number “CYPD3121-40LQXIT”. Updated Ordering Code Definitions Updated Packaging: Removed spec 51-85022 *E. Removed Errata.
*F	5342389	VGT	07/28/2016	Added Available Firmware and Software Tools, CCG3 Programming and Bootloading, and References and Links to Applications Collaterals. Added descriptive notes for the application diagrams. Updated Features, Applications and Timer/Counter/PWM Block (TCPWM). Updated Table 2 through Table 6, Table 18, Table 19, Table 22, Table 23, Table 25, and Table 31 through Table 38. Updated Figure 7, Figure 8, Figure , Figure 11, and Figure 19 (package diagram spec 001-42168 *E). Added Figure 5, Figure 13, and Figure 14. Added Table 26, Table 27, Table 37, and Table 39 through Table 41. Added VDM in Acronyms. Updated Cypress logo and copyright information.
*G	5449433	VGT	09/26/2016	Added Table 34 through Table 36. Updated Table 3, Table 4, Table 6, and Table 37. Updated Copyright and Disclaimer. Added Compliance information in Sales, Solutions, and Legal Information.