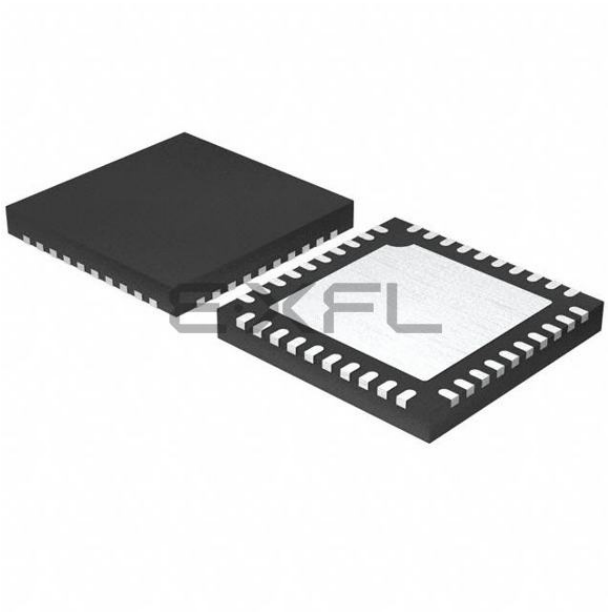

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Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

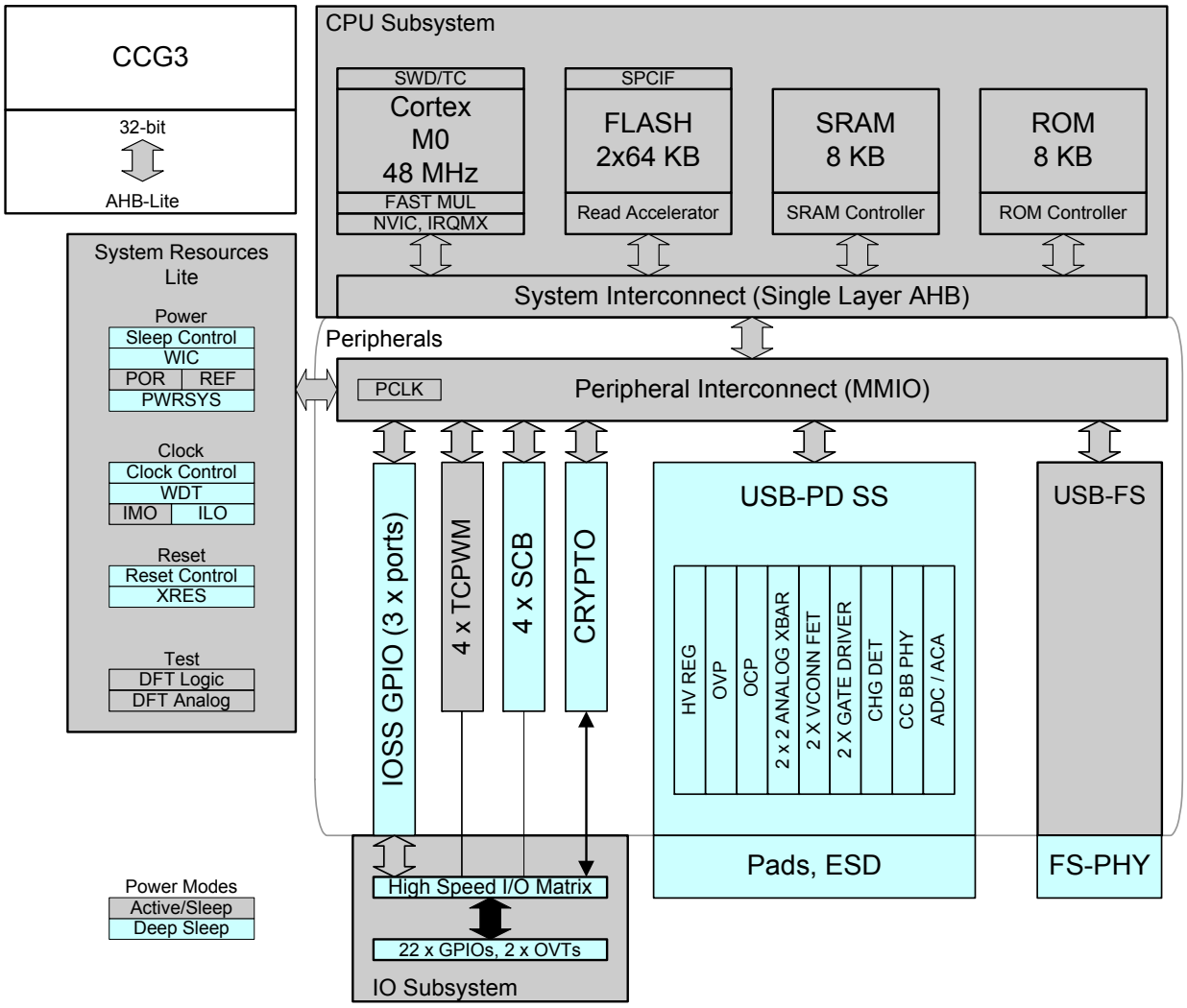
Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	USB Type C
Core Processor	ARM® Cortex®-M0
Program Memory Type	FLASH (128kB)
Controller Series	-
RAM Size	8K x 8
Interface	I²C, SPI, UART/USART, USB
Number of I/O	16
Voltage - Supply	2.7V ~ 21.5V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cypd3123-40lqxi

Contents

EZ-PD CCG3 Block Diagram

Figure 1. EZ-PD CCG3 Block Diagram[1]



Note
1. See Acronyms section for more details.

Functional Overview

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in EZ-PD CCG3 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex-M3 and M4, thus enabling upward compatibility. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor up from the Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a serial wire debug (SWD) interface, which is a two-wire form of JTAG. The debug configuration used for EZ-PD CCG3 has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The EZ-PD CCG3 device has a flash module with two banks of 64 KB flash, a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 1 wait-state (WS) access time at 48 MHz and with 0-WS access time at 24 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

Crypto Block

CCG3 integrates a crypto block for hardware assisted authentication of firmware images. It also supports field upgradeability of firmware in a trusted ecosystem. The CCG3 Crypto block provides cryptography functionality. It includes hardware acceleration blocks for AES (Advanced Encryption Standard) block cipher, SHA-1 (Secure Hash Algorithm) and SHA-2 hash, Cyclic Redundancy Check (CRC) and pseudo random number generation.

Integrated Billboard Device

CCG3 integrates a complete full speed USB 2.0 device controller capable of functioning as a Billboard class device. The USB 2.0 device controller can also support other device classes.

USB-PD Subsystem (USBPD SS)

The USB-PD sub-system contains all of the blocks related to USB Type-C and Power Delivery. The sub-system is comprised of the following:

- BMC PHY: USB-PD Transceiver with Fast Role Swap (FRS) transmit and detect
- VCONN power FETs for the CC lines
- VCONN Ra Termination and Leakers
- Analog Cross-Bar to switch between the SBU1/SBU2 and AUX_P/AUX_N pins
- Programmable Pull-up and Pull-down termination on the AUX_P/AUX_N pins
- HPD Processor
- VBUS_C Regulator (20V LDO)
- Power Switch between VSYS supply and VBUS_C Regulator output
- VBUS_C Over-Voltage (OV) and Under-Voltage (UV) Detectors
- Current Sense Amplifier (CSA) for over current detection
- Gate Drivers for VBUS_P and VBUS_C external Power FETs
- VBUS_C discharge switch
- USB2.0 Full-Speed (FS) PHY with integrated 5.0V to 3.3V regulator
- Charger Detection / Emulation for USB BC1.2 and other proprietary protocols
- 2 instances of 8-bit SAR ADCs
- 8kV IEC ESD Protection on the following pins: VBUS_C, CC1, CC2, SBU1, SBU2, DP, DM

The EZ-PD™ CCG3 USB-PD subsystem interfaces to the pins of a USB Type-C connector. It includes a USB Type-C baseband transceiver and physical-layer logic. This transceiver performs the BMC and the 4b/5b encoding and decoding functions as well as integrating the 1.2V analog front end. This subsystem integrates the required terminations to identify the role of the CCG3 device, including Rp and Rd for UFP/DFP roles and Ra for EMCA/VCONN powered accessories. The programmable VCONN leakers are included in order to discharge VCONN capacitance during a disconnect event. It also integrates power FETs for supplying VCONN power to the CC1/CC2 pins from the V5V pin. The Analog Cross-Bar allows for connecting either of the SBU1/SBU2 pins to either of the AUX_P/AUX_N pins to support DisplayPort sideband signaling. The integrated HPD processor can be used to control or monitor the HPD signal of a DisplayPort source or sink.

The I^2C port on SCB 1-3 blocks of EZ-PD CCG3 are not completely compliant with the I^2C specification in the following aspects:

- The GPIO cells for SCB 1's I^2C port are not overvoltage-tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I^2C system.
- Fast-mode Plus has an I_{OL} specification of 20 mA at a V_{OL} of 0.4V. The GPIO cells can sink a maximum of 8-mA I_{OL} with a V_{OL} maximum of 0.6V.
- Fast-mode and Fast-mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the bus load.

Timer/Counter/PWM Block (TCPWM)

EZ-PD CCG3 has four TCPWM blocks. Each implements a 16-bit timer, counter, pulse-width modulator (PWM), and quadrature decoder functionality.

GPIO

EZ-PD CCG3 has up to 20 GPIOs (these GPIOs can be configured for GPIOs, SCB, SBU, and Aux signals) and SWD pins, which can also be used as GPIOs. The I^2C pins from SCB 0 are overvoltage-tolerant.

The GPIO block implements the following:

- Seven drive strength modes:
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode)
- Selectable slew rates for dV/dt related noise control to improve EMI

During power-on and reset, the I/O pins are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Power Systems Overview

Figure 3 shows an overview of the power system requirement for CCG3. CCG3 shall be able to operate from two possible external supply sources VBUS (4.0 V–21.5 V) or VSYS (2.7 V–5.5 V). The VBUS supply is regulated inside the chip with a low-dropout regulator (LDO) down to 3.3 V level. The chip's internal VDDD rail is intelligently switched between the output of the VBUS regulator and unregulated VSYS. The switched supply, VDDD is either used directly inside some analog blocks or further regulated down to VCCD which powers majority of the core using regulators. Besides Reset mode, CCG3 has three different power modes: Active, Sleep and Deep Sleep, transitions between which are managed by the Power System. A separate power domain VDDIO is provided for the GPIOs. The VDDD and VCCD pins, both the output of regulators are brought out for connecting a 1-µF capacitor for the regulator stability only. These pins are not supported as power supplies. When CCG3 is powered from VSYS that is greater than 3.3 V, the dedicated USB regulator allows USB operation.

Figure 3. EZ-PD CCG3 Power System Block Diagram

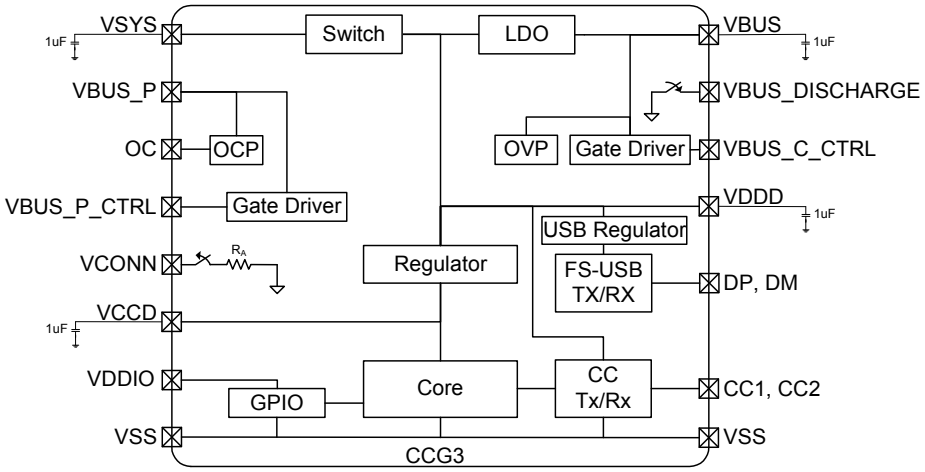


Table 1. CCG3 Power Modes

Mode	Description
RESET	Power is Valid and XRES is not asserted. An internal reset source is asserted or SleepController is sequencing the system out of reset.
ACTIVE	Power is Valid and CPU is executing instructions.
SLEEP	Power is Valid and CPU is not executing instructions. All logic that is not operating is clock gated to save power.
DEEP SLEEP	Main regulator and most hard-IP are shut off. Deep Sleep regulator powers logic, but only low-frequency clock is available.

Figure 4. Pinout of 40-QFN Package (Top View)

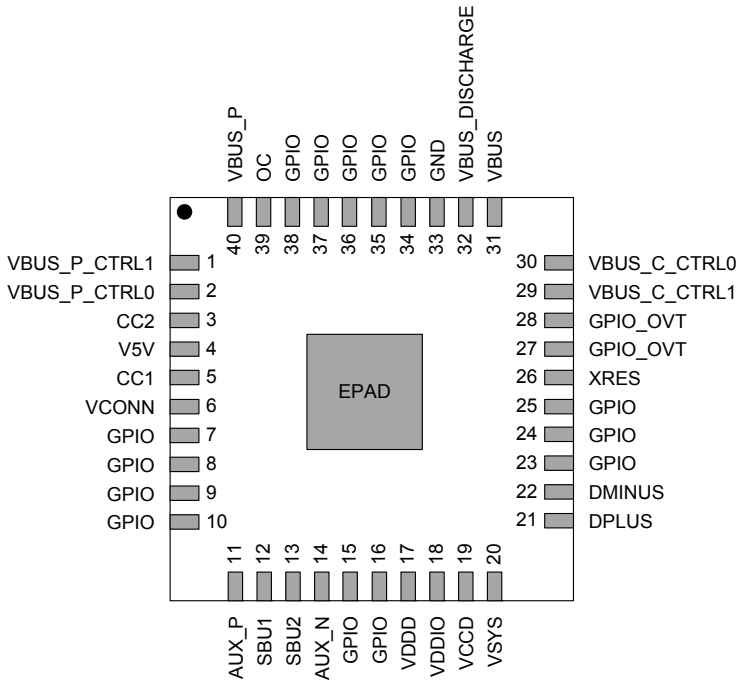
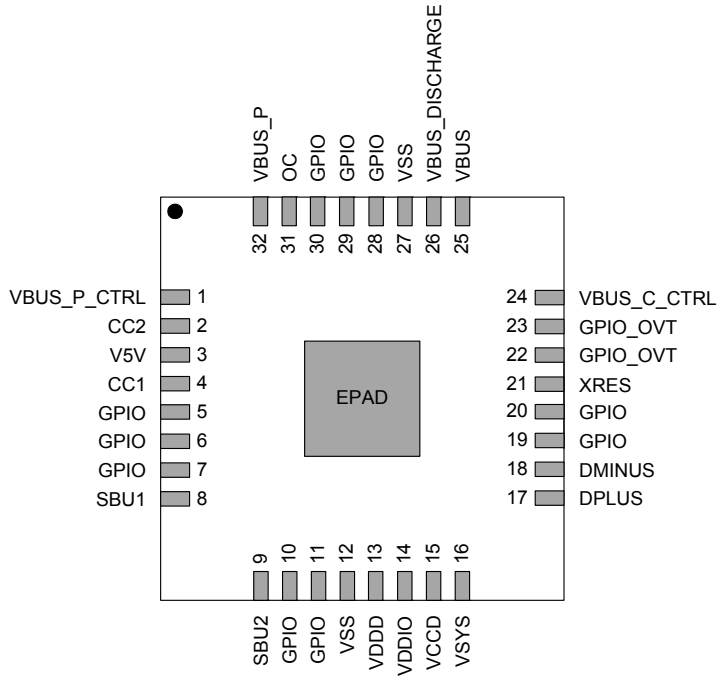


Figure 5. Pinout of 32-QFN Package (Top View)



CCG3 Programming and Bootloading

There are two ways to program application firmware into a CCG3 device:

1. Programming the device flash over SWD Interface
2. Application firmware update over specific interfaces (CC, USB, I^{2}C)

Generally, the CCG3 devices are programmed over SWD interface only during development or during the manufacturing process of the end product. Once the end product is manufactured, the CCG3 device's application firmware can be updated via the appropriate bootloader interface.

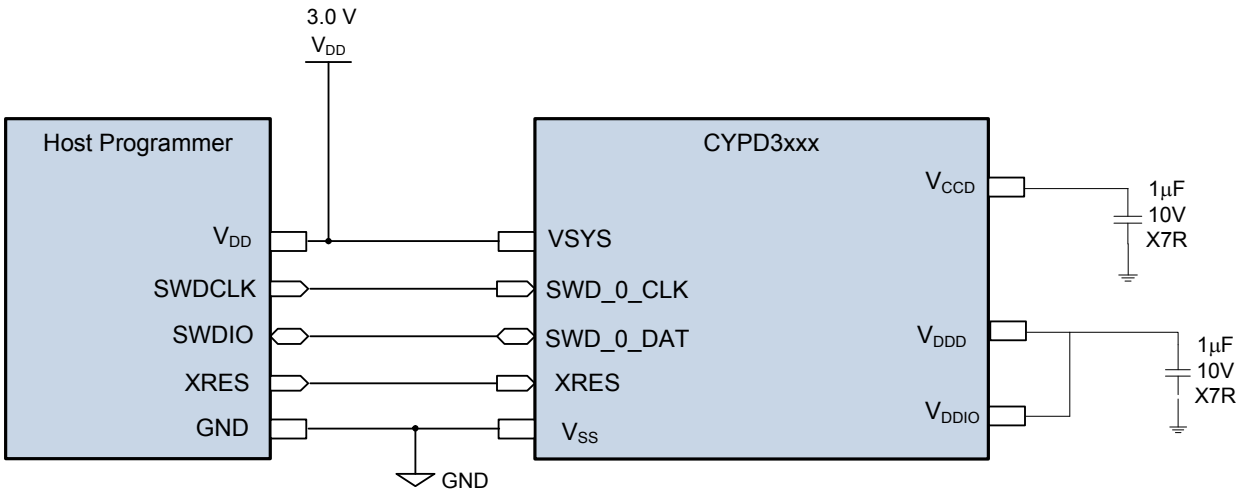
Programming the Device Flash over SWD Interface

CCG3 family of devices can be programmed using the SWD interface. Cypress provides a programming kit (CY8CKIT-002 MiniProg3 Kit) called MiniProg3 which can be used to program the flash as well as debug firmware. The flash is programmed by downloading the information from a hex file. This hex file is a binary file generated as an output of building the firmware project in PSoC Creator Software. Click here for more information on how to use the MiniProg3 programmer. There are many third party programmers that support mass programming in a manufacturing environment.

As shown in the block diagram in Figure 7, the SWD_0_DAT and SWD_0_CLK pins are connected to the host programmer's SWDIO (data) and SWDCLK (clock) pins respectively. During SWD programming, the device can be powered by the host programmer by connecting its VTARG (power supply to the target device) to VSYS pin of CCG3 device. If the CCG3 device is powered using an on-board power supply, it can be programmed using the “Reset Programming” option. For more details, refer to the CYPD3XXX Programming Specifications.

The CYPD3105 device for Thunderbolt cable applications is pre-programmed with a micro-bootloader that allows users to program the flash using the alternate SWD pins (SBU1 for SWD_1_CLK and SBU2 for SWD_1_DAT) that can be connected to the SBU interface of a Type-C connector. Note that this interface can be used to program the flash only once. Subsequent re-programming of this device can be done through the primary SWD interface (SWD_0_CLK and SWD_0_DAT pins). Irrespective of which SWD interface is used for programming the device, once the device is programmed with the hex file provided by Cypress for thunderbolt cable application, subsequent updates to the application firmware can be done over the CC line. Refer to Application Firmware Update over Specific Interfaces (I2C, CC, USB) for more details.

Figure 7. Connecting the Programmer to CYPD3xxx Device



Application Firmware Update over Specific Interfaces (I^{2}C, CC, USB)

The application firmware can be updated over three different interfaces depending on the default firmware programmed into the CCG3 device. Refer to Table 38 for more details on default firmware that various part numbers of the CCG3 family of devices are pre-programmed with (Note that some of the devices have bootloader only and some have bootloader plus application firmware). The application firmware provided by Cypress for all CCG3 applications have dual images. This allows fail-safe update of the alternate image while executing from the current image. For more information, refer to the EZ-PD Configuration Utility User Manual.

Application Firmware Update over I^{2}C Interface

This method primarily applies to CYPD3122, CYPD3125 and CYPD3126 devices of the CCG3 family. In these applications, the CCG3 device interfaces to an on-board application processor or an embedded controller over I^{2}C interface. Refer to Figure 8 for more details. Cypress provides pseudo-code for the host processor for updating the CCG3 device firmware.

Figure 12 illustrates a power bank application diagram using a CCG3 device. In this application, the Type-C receptacle is used for providing as well as consuming power. The consumer path will be active when the battery is charged using a Type-C power source that is connected to the Type-C receptacle in Figure 12. The provider path will be active when the power bank is used for providing power to a sink device connected to the Type-C receptacle. Additionally, a Type-A receptacle can also be provided for providing power to the sinks that have a legacy USB interface.

The CCG3 device negotiates power contracts between the power bank and the sink/source device connected to the Type-C receptacle. The CCG3 device also controls and drives the provider and consumer path FETs and can monitor overcurrent and overvoltage conditions on the Type-C VBUS line.

Figure 12. Power Bank Application Diagram (40-QFN Device)

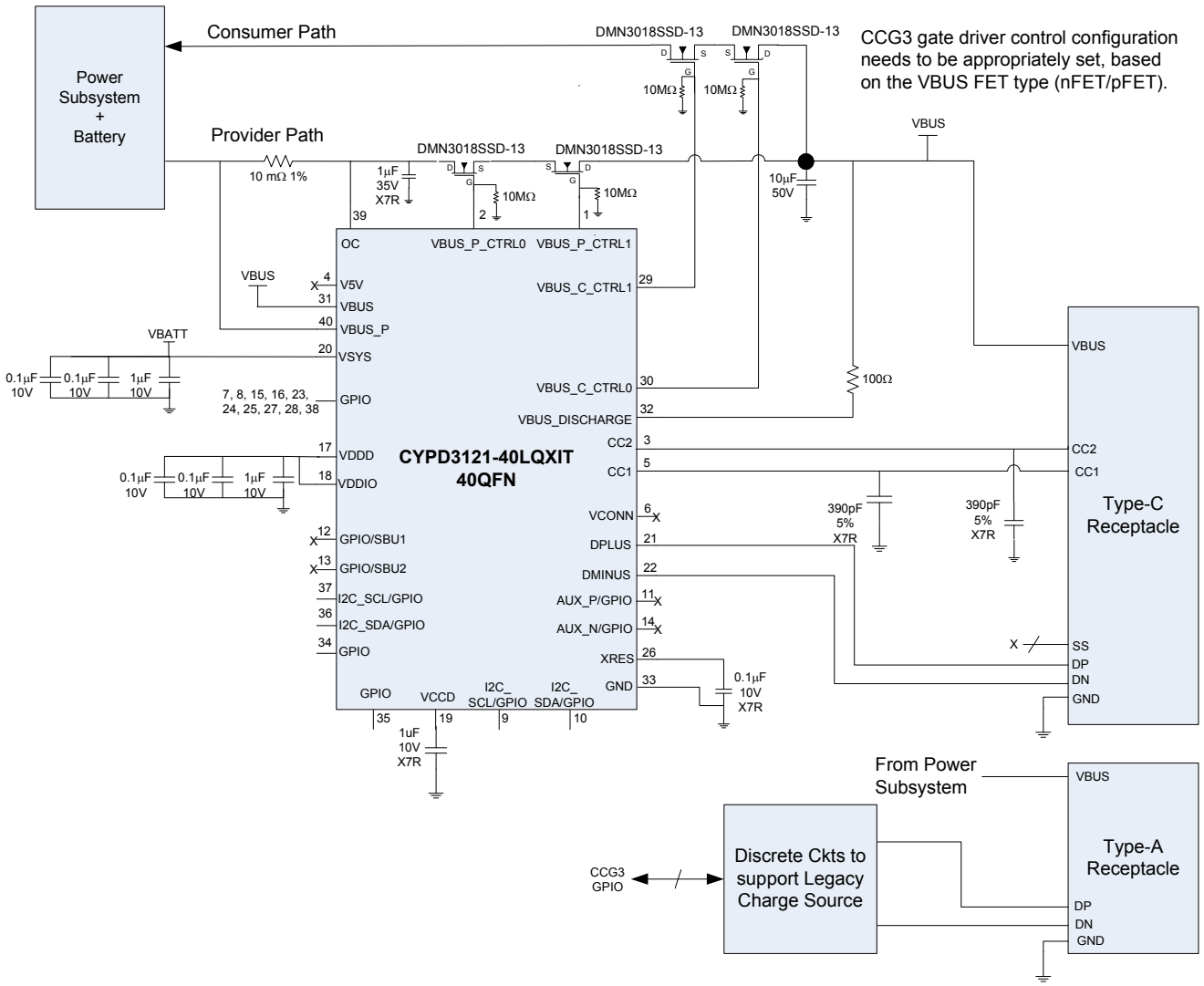


Table 5. AC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#4	F_{CPU}	CPU input frequency	DC	–	48	MHz	All VDDD
SID.PWR#20	T_{SLEEP}	Wakeup from sleep mode	–	0	–	µs	–
SID.PWR#21	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	–	35	µs	–
SID.XRES#5	T_{XRES}	External reset pulse width	5	–	–	µs	All VDDIO
SYS.FES#1	$T_{\_PWR\_RDY}$	Power-up to “Ready to accept I^2C/CC command”	–	5	25	ms	–

I/O

Table 6. I/O DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.GIO#37	V_{IH_CMOS}	Input voltage HIGH threshold	0.7 × VDDIO	–	–	V	CMOS input
SID.GIO#38	V_{IL_CMOS}	Input voltage LOW threshold	–	–	0.3 × VDDIO	V	CMOS input
SID.GIO#39	$V_{IH\_VDDIO2.7-}$	LVTTL input, VDDIO < 2.7 V	0.7× VDDIO	–	–	V	–
SID.GIO#40	$V_{IL\_VDDIO2.7-}$	LVTTL input, VDDIO < 2.7 V	–	–	0.3 × VDDIO	V	–
SID.GIO#41	$V_{IH\_VDDIO2.7+}$	LVTTL input, VDDIO ≥ 2.7 V	2.0	–	–	V	–
SID.GIO#42	$V_{IL\_VDDIO2.7+}$	LVTTL input, VDDIO ≥ 2.7 V	–	–	0.8	V	–
SID.GIO#33	V_{OH_3V}	Output voltage HIGH level	VDDIO –0.6	–	–	V	I_{OH} = 4 mA at 3V VDDIO
SID.GIO#34	$V_{OH\_1.8V}$	Output voltage HIGH level	VDDIO –0.5	–	–	V	I_{OH} = 1 mA at 1.8V VDDIO
SID.GIO#35	$V_{OL\_1.8V}$	Output voltage LOW level	–	–	0.6	V	I_{OL} = 4 mA at 1.8V VDDIO
SID.GIO#36	V_{OL_3V}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 4 mA at 3V VDDIO for SBU and AUX pins
SID.GIO#5	R_{PU}	Pull-up resistor value	3.5	5.6	8.5	kΩ	+25 °C T_A, all VDDIO
SID.GIO#6	R_{PD}	Pull-down resistor value	3.5	5.6	8.5	kΩ	+25 °C T_A, all VDDIO
SID.GIO#16	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	+25 °C T_A, all VDDIO. Guaranteed by characterization.
SID.GIO#17	C_{PIN}	Max pin capacitance	–	3.0	7	pF	All VDDIO, all packages, all I/Os except SBU and AUX. Guaranteed by characterization.
SID.GIO#17A	C_{PIN_SBU}	Max pin capacitance	–	16	18	pF	All VDDIO, all packages, SBU pins only. Guaranteed by characterization.
SID.GIO#17B	C_{PIN_AUX}	Max pin capacitance	–	12	14	pF	All VDDIO, all packages, AUX pins only. Guaranteed by characterization.
SID.GIO#43	V_{HYSTTL}	Input hysteresis, LVTTL VDDIO > 2.7 V	15	40	–	mV	Guaranteed by characterization
SID.GIO#44	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × VDDIO	–	–	mV	VDDIO < 4.5 V. Guaranteed by characterization.
SID69	I_{DIODE}	Current through protection diode to VDDIO/Vss	–	–	100	µA	Guaranteed by characterization
SID.GIO#45	I_{TOT_GPIO}	Maximum total sink chip current	–	–	85	mA	Guaranteed by characterization

Table 6. I/O DC Specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
OVT							
SID.GIO#46	I_{IHS}	Input current when Pad > VDDIO for OVT inputs	–	–	10.00	µA	Per I^2C specification

Table 7. I/O AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID70	T_{RISEF}	Rise time in Fast Strong mode	2	–	12	ns	3.3 V VDDIO, C_{load} = 25 pF
SID71	T_{FALLF}	Fall time in Fast Strong mode	2	–	12	ns	3.3 V VDDIO, C_{load} = 25 pF

XRES

Table 8. XRES DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.XRES#1	V_{IH_XRES}	Input voltage HIGH threshold on XRES pin	0.7 × VDDIO	–	–	V	CMOS input
SID.XRES#2	V_{IL_XRES}	Input voltage LOW threshold on XRES pin	–	–	0.3 × VDDIO	V	CMOS input
SID.XRES#3	C_{IN_XRES}	Input capacitance on XRES pin	–	–	7	pF	Guaranteed by characterization
SID.XRES#4	$V_{HYSXRES}$	Input voltage hysteresis on XRES pin	–	0.05 × VDDIO	–	mV	Guaranteed by characterization

Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

Pulse Width Modulation (PWM) for GPIO Pins

Table 9. PWM AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.3	$T_{CPWMFREQ}$	Operating frequency	–	–	Fc	MHz	Fc max = CLK_SYS. Maximum = 48 MHz.
SID.TCPWM.4	$T_{PWMENEXT}$	Input trigger pulse width	2/Fc	–	–	ns	For all trigger events
SID.TCPWM.5	T_{PWMEXT}	Output trigger pulse width	2/Fc	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	T_{CRES}	Resolution of counter	1/Fc	–	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWM_{RES}	PWM resolution	1/Fc	–	–	ns	Minimum pulse width of PWM output
SID.TCPWM.5C	Q_{RES}	Quadrature inputs resolution	1/Fc	–	–	ns	Minimum pulse width between quadrature-phase inputs

I²C

Table 10. Fixed I²C DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	–	60	µA	–
SID150	I_{I2C2}	Block current consumption at 400 kHz	–	–	185	µA	–
SID151	I_{I2C3}	Block current consumption at 1 Mbps	–	–	390	µA	–
SID152	I_{I2C4}	I²C enabled in Deep Sleep mode	–	–	1.4	µA	–

Table 11. Fixed I²C AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID153	F_{I2C1}	Bit rate	–	–	1	Mbps	–

Table 12. Fixed UART DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID160	I_{UART1}	Block current consumption at 100 Kb/s	–	–	125	µA	–
SID161	I_{UART2}	Block current consumption at 1000 Kb/s	–	–	312	µA	–

Table 13. Fixed UART AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID162	F_{UART}	Bit rate	–	–	1	Mbps	–

Table 14. Fixed SPI DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID163	I_{SPI1}	Block current consumption at 1 Mb/s	–	–	360	µA	–
SID164	I_{SPI2}	Block current consumption at 4 Mb/s	–	–	560	µA	–
SID165	I_{SPI3}	Block current consumption at 8 Mb/s	–	–	600	µA	–

Table 15. Fixed SPI AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID166	F_{SPI}	SPI Operating frequency (Master; 6X oversampling)	–	–	8	MHz	–

Table 16. Fixed SPI Master Mode AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID167	T_{DMO}	MOSI Valid after SClock driving edge	–	–	15	ns	–
SID168	T_{DSI}	MISO Valid before SClock capturing edge	20	–	–	ns	Full clock, late MISO sampling
SID169	T_{HMO}	Previous MOSI data hold time	0	–	–	ns	Referred to slave capturing edge

Internal Main Oscillator

Table 21. IMO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I_{IMO1}	IMO operating current at 48 MHz	–	–	1000	µA	–

Table 22. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#13	F_{IMOTOL}	Frequency variation at 24, 36, and 48 MHz (trimmed)	–	–	±2	%	–25 °C ≤ T_A ≤ 85 °C, all VDDD
SID226	$T_{STARTIMO}$	IMO start-up time	–	–	7	µs	Guaranteed by characterization
SID229	$T_{JITRMSIMO2}$	RMS jitter at 24 MHz	–	145	–	ps	Guaranteed by characterization
SID.CLK#1	F_{IMO}	IMO frequency	24	–	48	MHz	All VDDD

Internal Low-Speed OscillatorPower Down

Table 23. ILO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231	I_{ILO1}	I_{LO} operating current	–	0.3	1.05	µA	–
SID233	$I_{ILOLEAK}$	I_{LO} leakage current	–	2	15	nA	–

Table 24. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234	$T_{STARTILO1}$	I_{LO} start-up time	–	–	2	ms	Guaranteed by characterization
SID238	$T_{ILODUTY}$	I_{LO} duty cycle	40	50	60	%	Guaranteed by characterization
SID.CLK#5	F_{ILO}	I_{LO} frequency	20	40	80	kHz	–

Table 25. PD DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.PD.1	Rp_std	DFP CC termination for default USB Power	64	80	96	µA	–
SID.PD.2	Rp_1.5A	DFP CC termination for 1.5A power	166	180	194.4	µA	–
SID.PD.3	Rp_3.0A	DFP CC termination for 3.0A power	304	330	356.4	µA	–
SID.PD.4	Rd	UFP CC termination	4.59	5.1	5.61	kΩ	–
SID.PD.5	Rd_DB	UFP Dead Battery CC termination on CC1 and CC2, valid for 1.5A and 3.0A Rp termination values	4.08	5.1	6.12	kΩ	UFP Dead Battery CC termination on CC1 and CC2. For Default Rp termination, the voltage on CC1 and CC2 is guaranteed to be <1.32 V.
SID.PD.6	R_A	EMCA cable termination	0.8	1.0	1.2	kΩ	All supplies forced to 0 V and 0.2 V applied at VCONN.
SID.PD.7	Ra_OFF	EMCA cable termination - Disabled	0.4	0.75	–	MΩ	2.7 V applied at VCONN with R_A disabled.

Analog to Digital Converter

Table 32. ADC DC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.ADC.1	Resolution	ADC resolution	–	8	–	Bits	–
SID.ADC.2	INL	Integral non-linearity	–1.5	–	1.5	LSB	–
SID.ADC.3	DNL	Differential non-linearity	–2.5	–	2.5	LSB	–
SID.ADC.4	Gain Error	Gain error	–1	–	1	LSB	–

Table 33. ADC AC Specifications (Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.ADC.5	SLEW_Max	Rate of change of sampled voltage signal	–	–	3	V/ms	–

Table 34. VBUS_C Regulator DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.20vreg.1	VBUSREG	VBUS regulator output voltage measured at VDDD for VBUS = 4.5 V to 21.5 V	3	–	3.6	V	VBUS = 4.5 V - 21.5 V range. VDDD voltage measured with no load and a load of 30 mA.
SID.20vreg.2	VBUSREG2	VBUS regulator output voltage measured at VDDD for VBUS = 3.5 V to 21.5 V	3	–	3.6	V	VBUS = 4.5 V - 21.5 V range. VDDD voltage measured with no load and a load of 15 mA.
SID.20vreg.6	VBUSLINREG	VBUS regulator line regulation for VBUS from 4.5 V to 21.5 V	–	–	0.5	%/V	VBUS supply varied from 4.5 V to 21.5 V and the change in the VDDD measured. Guaranteed by Characterization.
SID.20vreg.8	VBUSLOADREG	VBUS regulator load regulation for VBUS from 4.5 V to 21.5 V	–	–	0.2	%/mA	Supply of 4.5 V - 21.5 V applied on VBUS and the load current swept from 0 to 30 mA. The change in VDDD is measured. Guaranteed by Characterization.

Table 35. VBUS_C Regulator AC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
AC.20vreg.1	T_{START}	Regulator Start-up time	–	–	120	µs	Apply VBUS and measure start time on VDDD pin.
AC.20vreg.2	T_{STOP}	Regulator power down time	–	–	1	µs	Time from assertion of an internal disable signal to for load current on VDDD to decrease from 30 mA to 10 µA.

Table 36. VSYS Switch Specification

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.vddsw.1	Res_sw	Resistance from VSYS supply input to the output supply VDDD	–	–	1.5	Ω	Measured with a load current of 5 mA - 10 mA on VDDD.

Memory

Table 37. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.MEM#3	FLASH_ERASE	Row erase time	–	–	15.5	ms	–
SID.MEM#4	FLASH_WRITE	Row (Block) write time (erase and program)	–	–	20	ms	–
SID.MEM#8	FLASH_ROW_PGM	Row program time after erase	–	–	7	ms	–
SID178	TBULKERASE	Bulk erase time (64k Bytes)	–	–	35	ms	–
SID180	TDEVPROG	Total device program time	–	–	7.5	s	Guaranteed by characterization
SID182	FRET1	Flash retention, $T_A \le 55$ °C, 100 K P/E cycles	20	–	–	years	Guaranteed by characterization
SID182A	FRET2	Flash retention, $T_A \le 85$ °C, 10 K P/E cycles	10	–	–	years	Guaranteed by characterization
SID182B	FRET3	Flash retention, $T_A \le 105$ °C, 10 K P/E cycles	3	–	–	years	Guaranteed by characterization

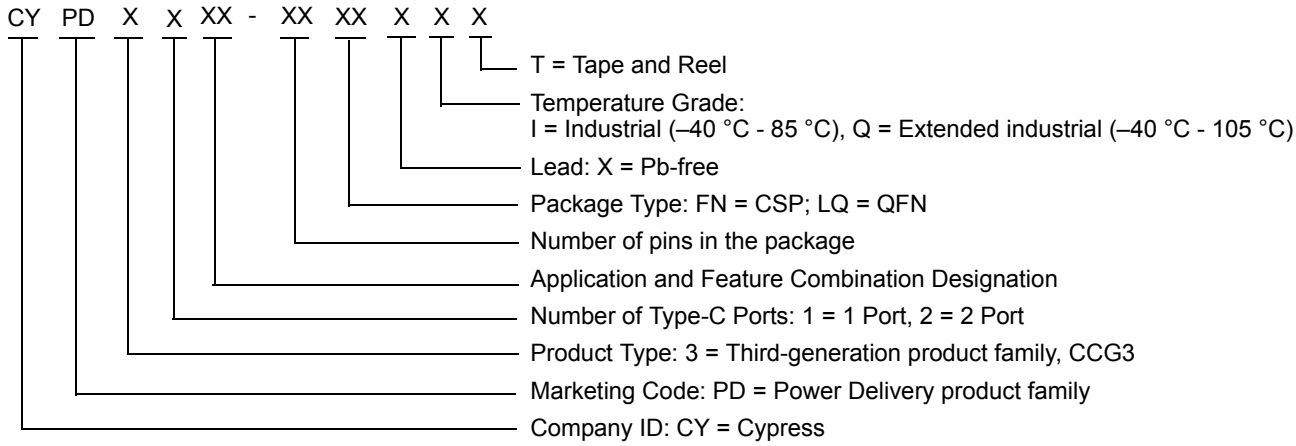
Ordering Information

Table 38 lists the EZ-PD CCG3 part numbers and features.

Table 38. EZ-PD CCG3 Ordering Information

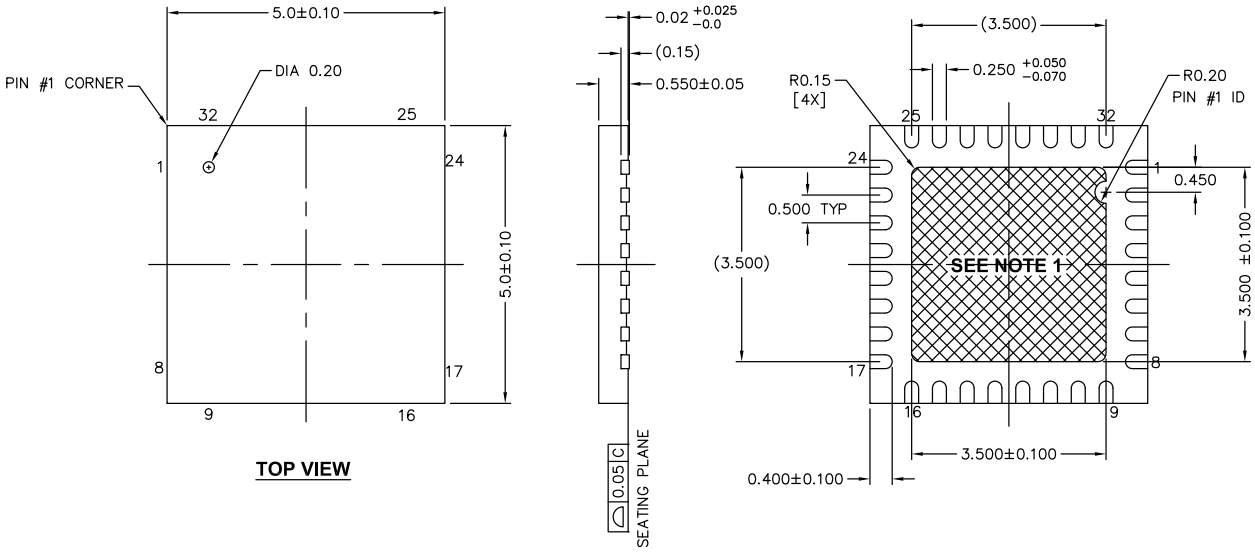
Part Number	Application	Termination Resistor	Role	Default FW	Package	Si ID
CYPD3120-40LQXIT	Dongle	R_P, R_D[4], R_{D_DB}	UFP	USB Bootloader and Application FW	40-QFN	1D00
CYPD3121-40LQXIT	Power Banks	R_P[5], R_D, R_{D_DB}[6]	DRP	USB Bootloader	40-QFN	1D02
CYPD3122-40LQXIT	Monitor (DFP)	R_P, R_D, R_{D_DB}	DFP	I^2C Bootloader	40-QFN	1D03
CYPD3123-40LQXIT	Charge-through Dongle	R_P, R_D, R_{D_DB}	DRP	USB Bootloader and Application FW	40-QFN	1D09
CYPD3125-40LQXIT	Notebooks, Smartphones	R_P, R_D, R_{D_DB}	DRP	I^2C Bootloader	40-QFN	1D04
CYPD3126-42FNXIT	DRP	R_P, R_D[4], R_{D_DB}	DRP	I^2C Bootloader	42-CSP	1D07
CYPD3135-32LQXQT	Power Adapter	R_P	DFP	CC Bootloader and Application FW	32-QFN	1D08
CYPD3135-40LQXIT	Power Adapter	R_P	DFP	CC Bootloader and Application FW	40-QFN	1D05
CYPD3135-40LQXQT	Power Adapter	R_P	DFP	CC Bootloader and Application FW	40-QFN	1D05

Ordering Code Definitions



Notes
3. Termination resistor denoting an EMCA.
4. Termination resistor denoting an upstream facing port.
5. Termination resistor denoting a downstream facing port.
6. Termination resistor denoting dead battery termination.

Figure 19. 32-pin QFN Package Outline, 001-42168



NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO−248
3. PACKAGE WEIGHT: 0.0388g
4. DIMENSIONS ARE IN MILLIMETERS

001-42168 *E

Acronyms

Table 42. Acronyms Used in this Document

Acronym	Description
ADC	analog-to-digital converter
AES	advanced encryption standard
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus
API	application programming interface
ARM®	advanced RISC machine, a CPU architecture
BMC	Biphase Mark Code
CC	configuration channel
CCG3	Cable Controller Generation 3
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
CS	current sense
DFP	downstream facing port
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DRP	dual role port
EEPROM	electrically erasable programmable read-only memory
EMCA	electronically marked cable assembly, a USB cable that includes an IC that reports cable characteristics (e.g., current rating) to the Type-C ports
EMI	electromagnetic interference
ESD	electrostatic discharge
FS	full-speed
GPIO	general-purpose input/output
HPD	hot plug detect
IC	integrated circuit
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
IOSS	input/output subsystem
I/O	input/output, see also GPIO
LDO	low-dropout regulator
LVD	low-voltage detect
LVTTL	low-voltage transistor-transistor logic
MCU	microcontroller unit
MMIO	memory mapped input/output
NC	no connect
NMI	nonmaskable interrupt
NVIC	nested vectored interrupt controller

Table 42. Acronyms Used in this Document *(continued)*

Acronym	Description
opamp	operational amplifier
OCP	overcurrent protection
OVP	overvoltage protection
PCB	printed circuit board
PD	power delivery
PGA	programmable gain amplifier
PHY	physical layer
POR	power-on reset
PRES	precise power-on reset
PSoC®	Programmable System-on-Chip™
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RX	receive
SAR	successive approximation register
SCB	serial communication block
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SHA	secure hash algorithm
SPI	Serial Peripheral Interface, a communications protocol
SRAM	static random access memory
SWD	serial wire debug, a test protocol
TCPWM	timer/counter pulse-width modulator
Thunderbolt™	Trademark of Intel
TX	transmit
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
USB	Universal Serial Bus
USB PD	USB Power Delivery
USB-FS	USB Full-Speed
USBIO	USB input/output, CCG2 pins used to connect to a USB port
USBPD SS	USB PD subsystem
VDM	vendor defined messages
XRES	external reset I/O pin

References and Links to Applications Collaterals

Knowledge Base Articles

- Key Differences Among EZ-PD™ CCG1, CCG2, CCG3 and CCG4 - KBA210740
- Programming EZ-PD™ CCG2, EZ-PD™ CCG3 and EZ-PD™ CCG4 Using PSoC® Programmer and MiniProg3 - KBA96477
- CCGX Frequently Asked Questions (FAQs) - KBA97244
- Handling Precautions for CY4501 CCG1 DVK - KBA210560
- Cypress EZ-PD™ CCGx Hardware - KBA204102
- Difference between USB Type-C and USB-PD - KBA204033
- CCGx Programming Methods - KBA97271
- Getting started with Cypress USB Type-C Products - KBA04071
- Type-C to DisplayPort Cable Electrical Requirements
- Dead Battery Charging Implementation in USB Type-C Solutions - KBA97273
- Termination Resistors Required for the USB Type-C Connector – KBA97180
- VBUS Bypass Capacitor Recommendation for Type-C Cable and Type-C to Legacy Cable/Adapter Assemblies – KBA97270
- Need for Regulator and Auxiliary Switch in Type-C to DisplayPort (DP) Cable Solution - KBA97274
- Need for a USB Billboard Device in Type-C Solutions – KBA97146
- CCG1 Devices in Type-C to Legacy Cable/Adapter Assemblies – KBA97145
- Cypress USB Type-C Controller Supported Solutions – KBA97179
- Termination Resistors for Type-C to Legacy Ports – KBA97272
- Handling Instructions for CY4502 CCG2 Development Kit – KBA97916
- Thunderbolt™ Cable Application Using CCG3 Devices - KBA210976
- Power Adapter Application Using CCG3 Devices - KBA210975
- Methods to Upgrade Firmware on CCG3 Devices - KBA210974
- Device Flash Memory Size and Advantages - KBA210973
- Applications of EZ-PD™ CCG4 - KBA210739

Application Notes

- AN96527 - Designing USB Type-C Products Using Cypress's CCG1 Controllers
- AN95615 - Designing USB 3.1 Type-C Cables Using EZ-PD™ CCG2
- AN95599 - Hardware Design Guidelines for EZ-PD™ CCG2
- AN210403 - Hardware Design Guidelines for Dual Role Port Applications Using EZ-PD™ USB Type-C Controllers
- AN210771 - Getting Started with EZ-PD™ CCG4

Reference Designs

- EZ-PD™ CCG2 Electronically Marked Cable Assembly (EMCA) Paddle Card Reference Design
- EZ-PD™ CCG2 USB Type-C to DisplayPort Cable Solution
- CCG1 USB Type-C to DisplayPort Cable Solution
- CCG1 USB Type-C to HDMI/DVI/VGA Adapter Solution
- EZ-PD™ CCG2 USB Type-C to HDMI Adapter Solution
- CCG1 Electronically Marked Cable Assembly (EMCA) Paddle Card Reference Design
- CCG1 USB Type-C to Legacy USB Device Cable Paddle Card Reference Schematics
- EZ-USB GX3 USB Type-C to Gigabit Ethernet Dongle
- EZ-PD™ CCG2 USB Type-C Monitor/Dock Solution
- CCG2 20W Power Adapter Reference Design
- CCG2 18W Power Adapter Reference Design
- EZ-USB GX3 USB Type-A to Gigabit Ethernet Reference Design Kit

Kits

- CY4501 CCG1 Development Kit
- CY4502 EZ-PD™ CCG2 Development Kit
- CY4531 EZ-PD CCG3 Evaluation Kit
- CY4541 EZ-PD™ CCG4 Evaluation Kit

Datasheets

- CCG1 Datasheet: USB Type-C Port Controller with Power Delivery
- CYPD1120 Datasheet: USB Power Delivery Alternate Mode Controller on Type-C
- CCG2: USB Type-C Port Controller Datasheet
- CCG4: Two-Port USB Type-C Controller Datasheet

Document History Page *(continued)*

Document Title: EZ-PD™ CCG3 USB Type-C Port Controller Document Number: 002-03288				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*E (cont.)	5240836	VGT	04/28/2016	Updated Power Systems Overview: Updated description. Updated Figure 3. Updated Pinouts: Updated Table 2: Updated details in “Description” column corresponding to VDDIO pin. Removed table “CCG3 Pin Description for 16-SOIC Device”. Removed figure “Pinout of 16-SOIC Package (Top View)”. Updated Applications: Removed figure “Power Adapter Application Diagram (16-SOIC Device)”. Added Figure 12. Updated Electrical Specifications: Updated Device-Level Specifications: Updated Table 4. Updated details in “Details/Conditions” column corresponding to “SID.PWR#1_A” Spec ID and “V_{SYS}” parameter. Replaced “V_{DDD}” with “5.5” in “Max” column corresponding to “SID.PWR#13” Spec ID and “V_{DDIO}” parameter. Added “SID.PWR#13_A” Spec ID corresponding to “V_{DDIO}” parameter and its details. Added “SID.PWR#1_C” and “SID.PWR#1_D” Spec IDs corresponding to “V_{SYS}” parameter and its details. Replaced “enabled” with “disabled” in “Details/Conditions” column corresponding to “SID.PwR#28” Spec ID and “V_{BUS}” parameter. Updated details in “Description” and “Details/Conditions” columns corresponding to “SID307” Spec ID and “I_{DD_XR}” parameter. Updated System Resources: Added Gate Driver Specifications, Charger Detect. Updated Ordering Information: Updated part numbers. Updated details in “Application” column corresponding to part number “CYPD3121-40LQXIT”. Updated Ordering Code Definitions Updated Packaging: Removed spec 51-85022 *E. Removed Errata.
*F	5342389	VGT	07/28/2016	Added Available Firmware and Software Tools, CCG3 Programming and Bootloading, and References and Links to Applications Collaterals. Added descriptive notes for the application diagrams. Updated Features, Applications and Timer/Counter/PWM Block (TCPWM). Updated Table 2 through Table 6, Table 18, Table 19, Table 22, Table 23, Table 25, and Table 31 through Table 38. Updated Figure 7, Figure 8, Figure , Figure 11, and Figure 19 (package diagram spec 001-42168 *E). Added Figure 5, Figure 13, and Figure 14. Added Table 26, Table 27, Table 37, and Table 39 through Table 41. Added VDM in Acronyms. Updated Cypress logo and copyright information.
*G	5449433	VGT	09/26/2016	Added Table 34 through Table 36. Updated Table 3, Table 4, Table 6, and Table 37. Updated Copyright and Disclaimer. Added Compliance information in Sales, Solutions, and Legal Information.

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