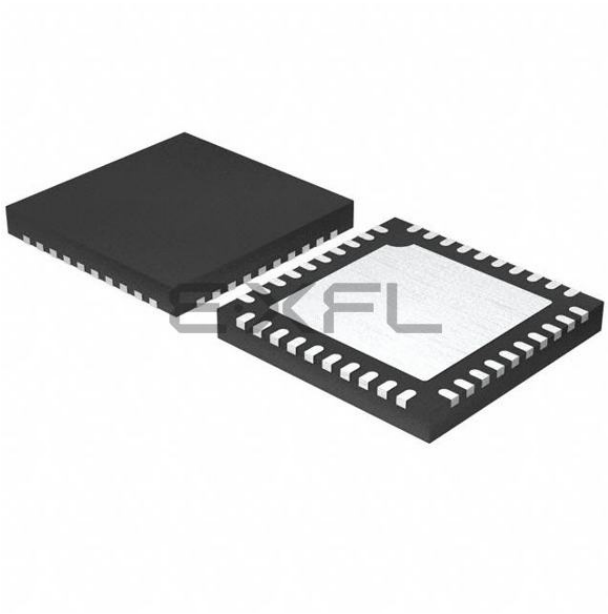

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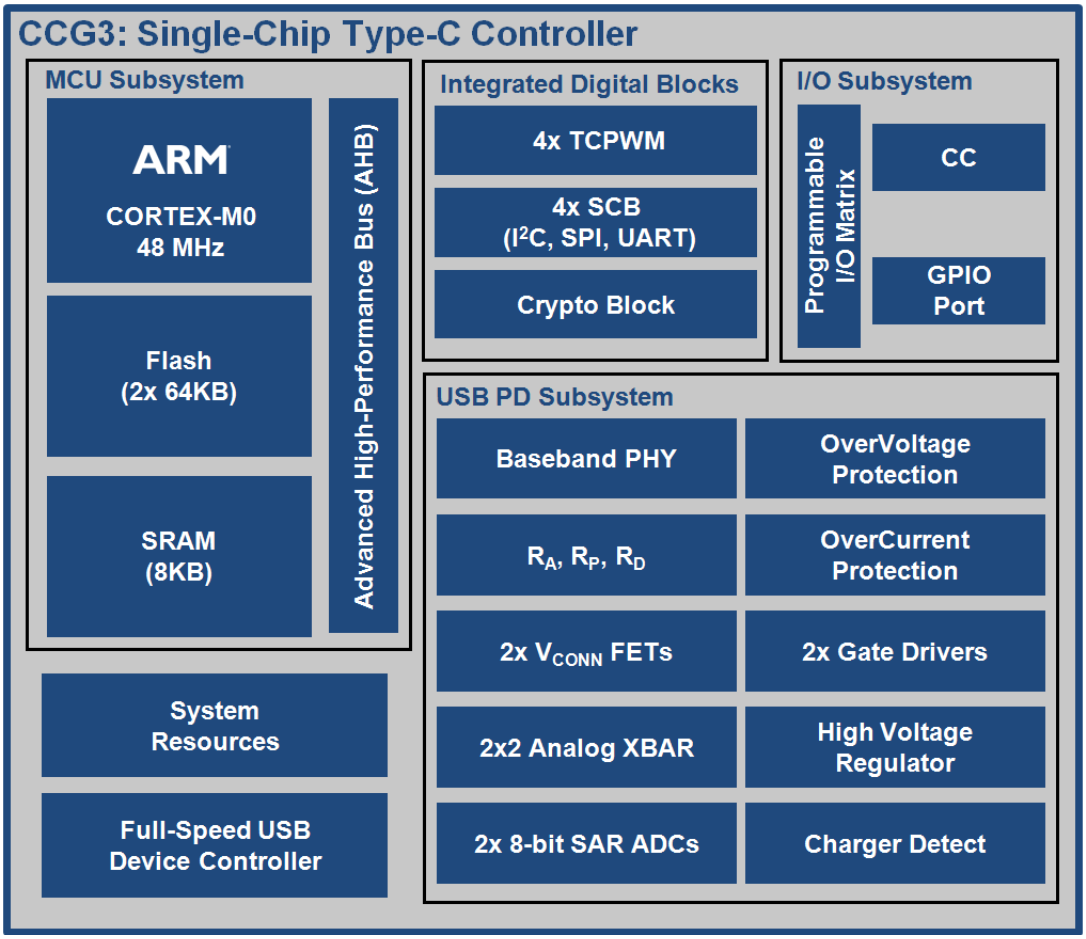
Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

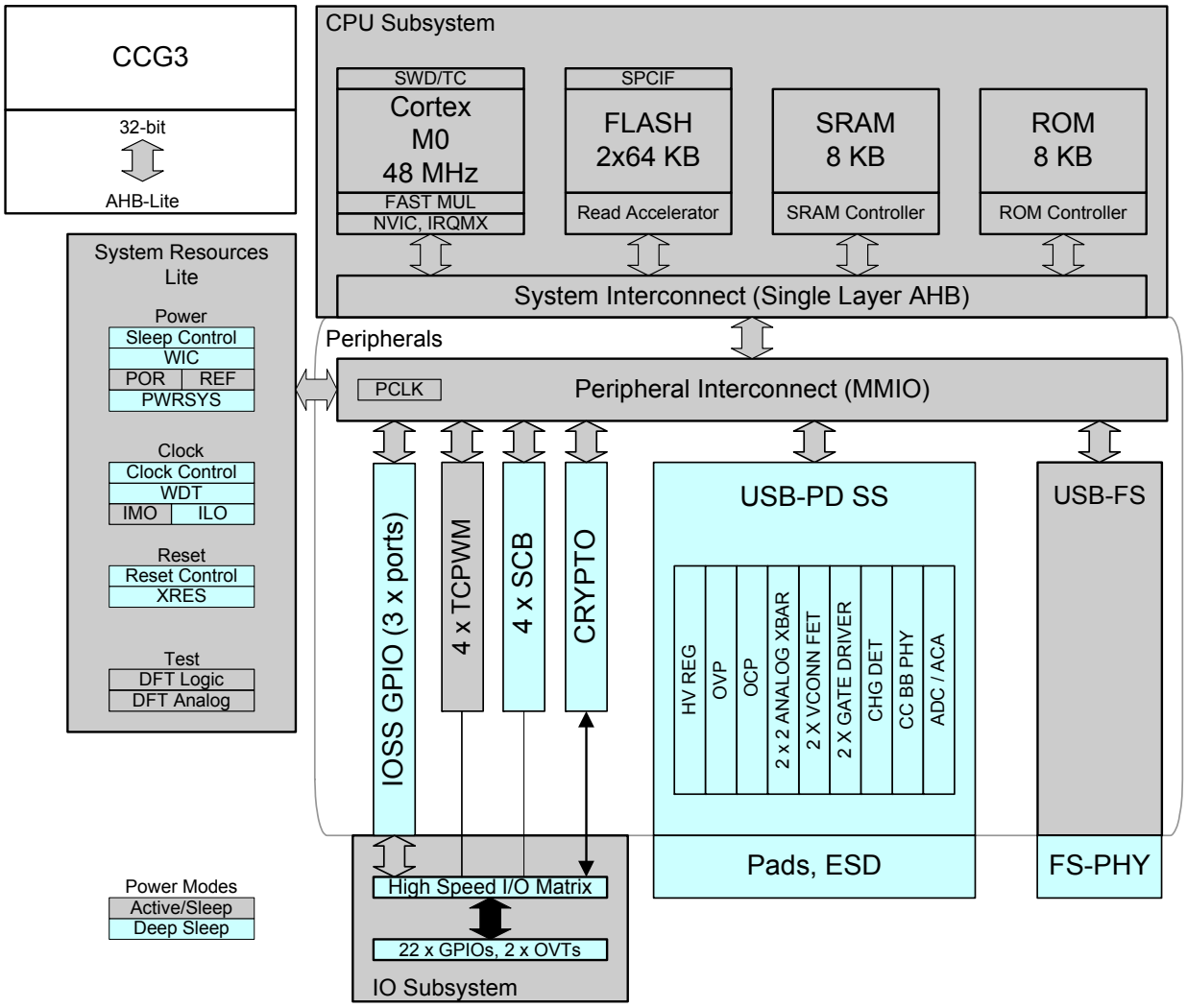
Details	
Product Status	Active
Applications	USB Type C
Core Processor	ARM® Cortex®-M0
Program Memory Type	FLASH (128kB)
Controller Series	-
RAM Size	8K x 8
Interface	I²C, SPI, UART/USART, USB
Number of I/O	16
Voltage - Supply	2.7V ~ 21.5V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cypd3123-40lqxit

Logic Block Diagram



EZ-PD CCG3 Block Diagram

Figure 1. EZ-PD CCG3 Block Diagram[1]

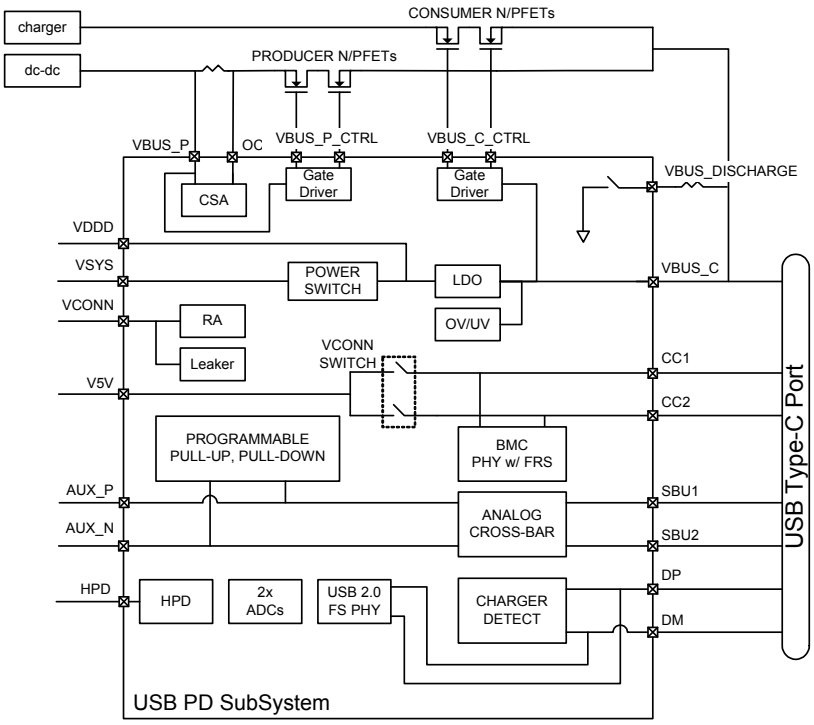


Note
1. See Acronyms section for more details.

The OV/UV (Over-Voltage/Under-Voltage) block monitors the VBUS_C supply for programmable over-voltage and under-voltage conditions. The CSA amplifies the voltage across an external sense resistor, which is proportional to the current being drawn from the external DC-DC VBUS supply converter. The CSA output can either be measured with an ADC or configured to detect an over-current condition. The VBUS_P and VBUS_C gate drivers control the gates of external power FETs for the VBUS_C and VBUS_P supplies. The gate drivers can be configured to support both P and N type external power FETs. The gate drivers are configured by default for nFET devices. In applications using pFETs, the gate drivers must be appropriately configured. The OV/UV and CSA blocks can generate interrupts to automatically turn off the power FETs for the programmed over-voltage and over-current conditions. The VBUS_C discharge switch allows for discharging the VBUS_C line through an external resistor.

The USB-PD sub-system also contains two 8-bit Successive Approximation Register (SAR) ADCs for analog to digital conversions. Each ADC includes an 8-bit DAC and a comparator. The DAC output forms the positive input of the comparator. The negative input of the comparator is from a 4-input multiplexer. The four inputs of the multiplexer are a pair of global analog multiplex busses, an internal bandgap voltage and an internal voltage proportional to the absolute temperature. Each GPIO pin can be connected to the global Analog Multiplex Busses through a switch, which allows either ADC to sample the pin voltage. When sensing the GPIO pin voltage with an ADC, the pin voltage cannot exceed the VDDD or VDDIO supply values.

Figure 2. USB-PD Subsystem



Full-Speed USB Subsystem

The FSUSB subsystem contains a full speed USB device controller as described in the Integrated Billboard Device section.

Peripherals

Serial Communication Blocks (SCB)

EZ-PD CCG3 has four SCBs, which can be configured to implement an I²C, SPI, or UART interface. The hardware I²C blocks implement full multi-master and slave interfaces capable of multimaster arbitration. In the SPI mode, the SCB blocks can be configured to act as master or slave.

In the I²C mode, the SCB blocks are capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and have flexible buffering options to reduce interrupt overhead and latency for the CPU. These blocks also support I²C that creates a mailbox address range in the memory of EZ-PD CCG3 and effectively reduce I²C communication to reading from and writing to an array in memory. In addition, the blocks support 8-deep FIFOs for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduce the need for clock stretching caused by the CPU not having read data on time.

The I²C peripherals are compatible with the I²C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I²C-bus specification and user manual (UM10204).

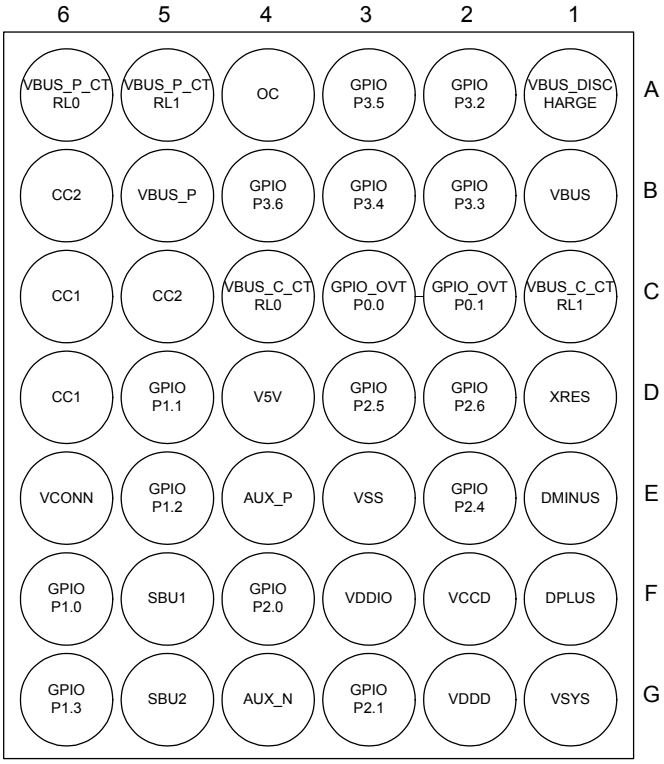
The I²C bus I/Os are implemented with GPIO in open-drain modes.

Pinouts

Table 2. CCG3 Pin Description for 42-CSP, 32-QFN and 40-QFN Devices

Pin Map 42-CSP	Pin Map 32-QFN	Pin Map 40-QFN	Name	Description
A5	N/A	1	VBUS_P_CTRL1	VBUS Gate Driver Control 1 for Producer Switch
A6	1	2	VBUS_P_CTRL0	VBUS Gate Driver Control 0 for Producer Switch
B6	2	3	CC2	USB PD connector detect/Configuration Channel 2
C5	N/A	N/A	CC2	USB PD connector detect/Configuration Channel 2
D4	3	4	V5V	5.0V – 5.5V supply for VCONN FETs
C6	4	5	CC1	USB PD connector detect/Configuration Channel 1
D6	N/A	N/A	CC1	USB PD connector detect/Configuration Channel 1
E6	N/A	6	VCONN	VCONN Input - provides Ra termination for cable applications
F6	5	7	P1.0	GPIO/UART_2_TX / SPI_2_MISO
D5	N/A	8	P1.1	GPIO/UART_2_RX / SPI_2_SEL
E5	6	9	P1.2	GPIO/UART_0_RX/ UART_3_CTS/ SPI_3_MOSI/ I2C_3_SCL / HPD
G6	7	10	P1.3	GPIO/UART_0_TX/ UART_3_RTS/ SPI_3_CLK/ I2C_3_SDA
E4	N/A	11	AUX_P / P1.6	DisplayPort AUX_P signal / GPIO / UART_1_TX / SPI_1_MISO
F5	8	12	SBU1 / P1.4	USB Type-C SBU1 signal / GPIO / UART_3_TX/ SPI_3_MISO/ SWD_1_CLK
G5	9	13	SBU2 / P1.5	USB Type-C SBU2 signal / GPIO / UART_3_RX/ SPI_3_SEL/ SWD_1_DAT
G4	N/A	14	AUX_N / P1.7	DisplayPort AUX_N signal / GPIO / UART_1_RX / SPI_1_SEL
F4	10	15	P2.0	GPIO / UART_1_CTS / SPI_1_CLK/ I2C_1_SCL / SWD_0_DAT
G3	11	16	P2.1	GPIO / UART_1_RTS / SPI_1_MOSI/ I2C_1_SDA / SWD_0_CLK
G2	13	17	VDDD	VDDD Supply Input / Output (2.7 V–5.5 V)
F3	14	18	VDDIO	1.71 V–5.5 V supply for I/Os. This supply also powers the global analog multiplex buses.
F2	15	19	VCCD	1.8V regulator output for filter capacitor
G1	16	20	VSYS	System Power Supply (2.7 V–5.5 V)
F1	17	21	DPLUS	USB 2.0 DP
E1	18	22	DMINUS	USB 2.0 DM
E2	19	23	P2.4	GPIO
D3	20	24	P2.5	GPIO / UART_0_TX/ SPI_0_MOSI
D2	N/A	25	P2.6	GPIO / UART_0_RX/ SPI_0_CLK
D1	21	26	XRES	External Reset Input. Internally pulled-up to VDDIO.
C3	22	27	P0.0	I2C_0_SDA / GPIO_OVT / UART_0_CTS / SPI_0_SEL/ TCPWM0
C2	23	28	P0.1	I2C_0_SCL / GPIO_OVT / UART_0_RTS / SPI_0_MISO/ TCPWM1

Figure 6. Pinout of 42-WLCSP Bottom (Balls Up) View



Available Firmware and Software Tools

EZ-PD Configuration Utility

The EZ-PD Configuration Utility is a GUI-based Microsoft Windows application developed by Cypress to guide a CCGx user through the process of configuring and programming the chip. The utility allows users to:

1. Select and configure the parameters they want to modify
2. Program the resulting configuration onto the target CCGx device.

The utility works with the Cypress supplied CCG1, CCG2, CCG3, and CCG4 kits, which host the CCGx controllers along with a USB interface. This version of the EZ-PD Configuration Utility supports configuration and firmware update operations on CCGx controllers implementing EMCA and Display Dongle applications. Support for other applications, such as Power Adapters and Notebook port controllers, will be provided in later versions of the utility.

You can download the EZ-PD Configuration Utility and its associated documentation at the following link:

http://www.cypress.com/documentation/software-and-drivers/ez-pd-configuration-utility

CCG3 Programming and Bootloading

There are two ways to program application firmware into a CCG3 device:

1. Programming the device flash over SWD Interface
2. Application firmware update over specific interfaces (CC, USB, I^{2}C)

Generally, the CCG3 devices are programmed over SWD interface only during development or during the manufacturing process of the end product. Once the end product is manufactured, the CCG3 device's application firmware can be updated via the appropriate bootloader interface.

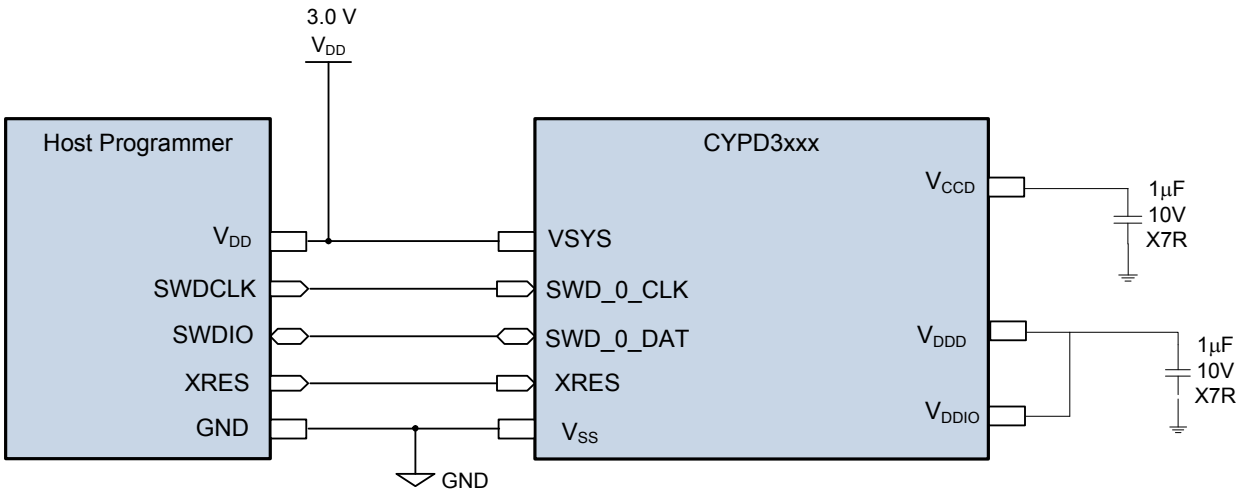
Programming the Device Flash over SWD Interface

CCG3 family of devices can be programmed using the SWD interface. Cypress provides a programming kit (CY8CKIT-002 MiniProg3 Kit) called MiniProg3 which can be used to program the flash as well as debug firmware. The flash is programmed by downloading the information from a hex file. This hex file is a binary file generated as an output of building the firmware project in PSoC Creator Software. Click here for more information on how to use the MiniProg3 programmer. There are many third party programmers that support mass programming in a manufacturing environment.

As shown in the block diagram in Figure 7, the SWD_0_DAT and SWD_0_CLK pins are connected to the host programmer's SWDIO (data) and SWDCLK (clock) pins respectively. During SWD programming, the device can be powered by the host programmer by connecting its VTARG (power supply to the target device) to VSYS pin of CCG3 device. If the CCG3 device is powered using an on-board power supply, it can be programmed using the “Reset Programming” option. For more details, refer to the CYPD3XXX Programming Specifications.

The CYPD3105 device for Thunderbolt cable applications is pre-programmed with a micro-bootloader that allows users to program the flash using the alternate SWD pins (SBU1 for SWD_1_CLK and SBU2 for SWD_1_DAT) that can be connected to the SBU interface of a Type-C connector. Note that this interface can be used to program the flash only once. Subsequent re-programming of this device can be done through the primary SWD interface (SWD_0_CLK and SWD_0_DAT pins). Irrespective of which SWD interface is used for programming the device, once the device is programmed with the hex file provided by Cypress for thunderbolt cable application, subsequent updates to the application firmware can be done over the CC line. Refer to Application Firmware Update over Specific Interfaces (I2C, CC, USB) for more details.

Figure 7. Connecting the Programmer to CYPD3xxx Device



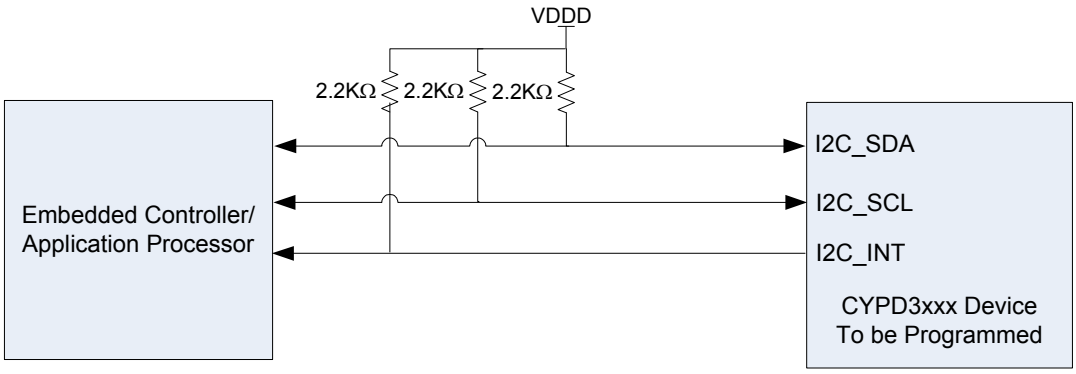
Application Firmware Update over Specific Interfaces (I^{2}C, CC, USB)

The application firmware can be updated over three different interfaces depending on the default firmware programmed into the CCG3 device. Refer to Table 38 for more details on default firmware that various part numbers of the CCG3 family of devices are pre-programmed with (Note that some of the devices have bootloader only and some have bootloader plus application firmware). The application firmware provided by Cypress for all CCG3 applications have dual images. This allows fail-safe update of the alternate image while executing from the current image. For more information, refer to the EZ-PD Configuration Utility User Manual.

Application Firmware Update over I^{2}C Interface

This method primarily applies to CYPD3122, CYPD3125 and CYPD3126 devices of the CCG3 family. In these applications, the CCG3 device interfaces to an on-board application processor or an embedded controller over I^{2}C interface. Refer to Figure 8 for more details. Cypress provides pseudo-code for the host processor for updating the CCG3 device firmware.

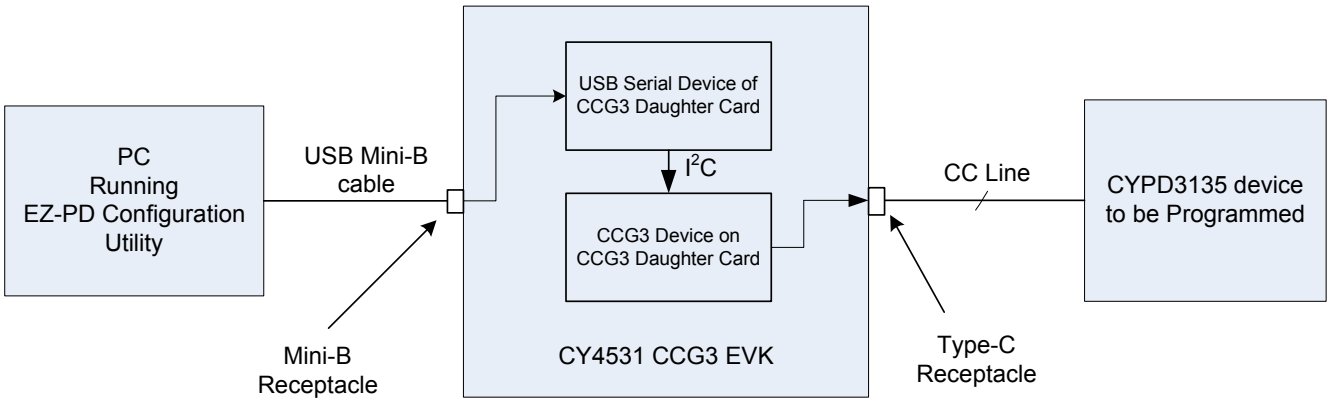
Figure 8. Application Firmware Update over I²C Interface



Application Firmware Update over CC Line

This method primarily applies to CYPD3135 device of the CCG3 family. In these applications, the CY4531 CCG3 EVK can be used to send programming and configuration data as Cypress specific Vendor Defined Messages (VDMs) over the CC line. The CY4531 CCG3 EVK is connected to the system containing CCG3 device on one end and a Windows PC running the EZ-PDTM Configuration Utility as shown in Figure 9 on the other end to program the CCG3 device.

Figure 9. Application Firmware Update over CC Line



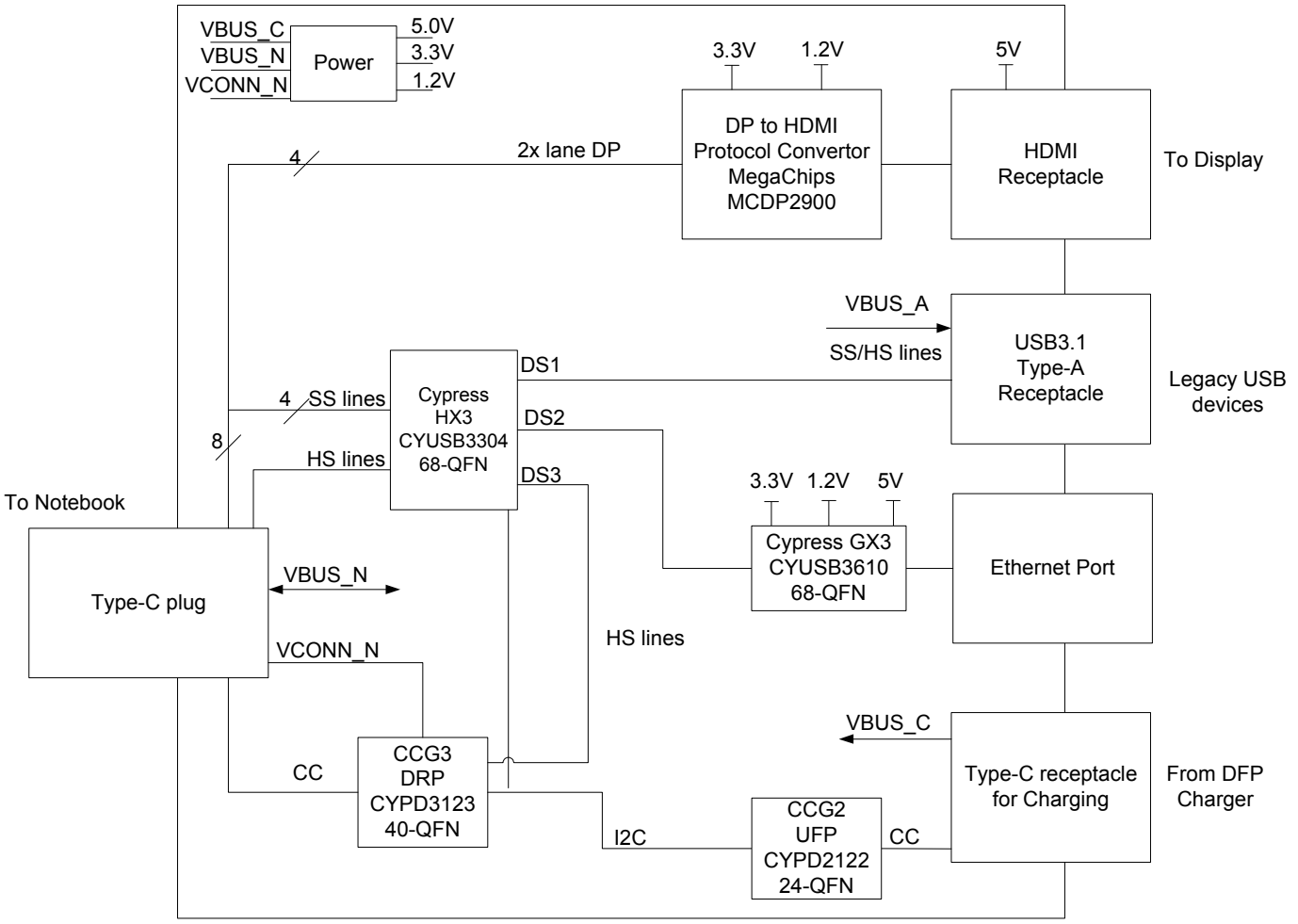
Application Firmware Update over USB

This method primarily applies to the CYPD3120 and CYPD3121 devices of the CCG3 family. In these applications, the firmware update can be performed over the D+/D- lines (USB2.0) using various possible options as shown in Figure 10. Option 1 is to have a Windows PC running EZ-PD™ Configuration Utility connected to the device to be programmed via the CY4531 CCG3 EVK. This setup can be avoided using option 2, where the user has a Type-A to Type-C cable. This option requires that the system contain the CCG3 device to be programmed to have a Type-C receptacle. The other option (Option 3) is to have a Windows PC with a native Type-C connector as shown in Figure 10.

Figure 16 illustrates a CCG3 device based Charge-through Dongle application block diagram. This Charge-through dongle application also implements Cypress's USB SuperSpeed Hub controller HX3 (CYUSB3304-68LTXI) available in 68-QFN package, Low-power single chip USB 3.0 to Gigabit Ethernet Bridge Controller GX3 (CYUSB3610-68LTXC) available in 68-QFN package and the CCG2 (CYPD2122-24LQXI) which acts as an Upstream Facing Port (UFP) and sinks power when connected to USB Type-C chargers.

This application enables connectivity between a USB Type-C Notebook and HDMI Display, legacy USB device and Gigabit Ethernet while also connecting a USB Type-C charging cable. The Charge-Through Dongle solution allows simultaneous HDMI display, Superspeed data transfers, Ethernet connection and charging of a USB Type-C Notebook. Charge-Through Dongle is also widely known as Multiport Adapter. More details including the schematic of the CCG3 device based Charge-through Dongle reference design can be found here.

Figure 16. Charge-through Dongle Application Block Diagram (40-QFN Device)



Electrical Specifications

Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{SYS_MAX}	Digital supply relative to V_{SS}	–0.5	–	6	V	Absolute max
V_{5V}	Max supply voltage relative to V_{SS}	–	–	6	V	
$V_{BUS\_MAX\_ON}$	Max supply voltage relative to V_{SS}, V_{BUS} regulator enabled	–	–	26	V	
$V_{BUS\_MAX\_OFF}$	Max supply voltage relative to V_{SS}, V_{BUS} regulator enabled 100% of the time	–	–	24.5	V	
	Max supply voltage relative to V_{SS}, V_{BUS} regulator enabled 25% of the time	–	–	26	V	
V_{DDIO_MAX}	Max supply voltage relative to V_{SS}	–	–	6	V	
V_{GPIO_ABS}	GPIO voltage	–0.5	–	VDDIO + 0.5	V	
$V_{GPIO\_OVT\_ABS}$	OVT GPIO voltage	–0.5	–	6	V	
I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	
V_{CONN_MAX}	Max voltage relative to V_{SS}	–	–	6	V	
V_{CC_ABS}	Max voltage on CC1 and CC2 pins	–	–	6	V	
$I_{GPIO\_INJECTION}$	GPIO injection current, Max for V_{IH} > VDDD, and Min for V_{IL} < V_{SS}	–0.5	–	0.5	mA	Absolute max, current injected per pin
ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	–
ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	–
LU	Pin current for latch-up	–100	–	100	mA	Tested at 125 °C
ESD_IEC_CON	Electrostatic discharge IEC61000-4-2	8000	–	–	V	Contact discharge on CC1, CC2, VBUS, DPLUS, DMINUS, SBU1 and SBU2 pins
ESD_IEC_AIR	Electrostatic discharge IEC61000-4-2	15000	–	–	V	Air discharge for CC1, CC2, VBUS, DPLUS, DMINUS, SBU1 and SBU2 pins

Device-Level Specifications

All specifications are valid for –40 °C ≤ TA ≤ 105 °C and TJ ≤ 120 °C, except where noted.

Table 4. DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.PWR#1	VSYS	–	2.7	–	5.5	V	UFP Mode.
SID.PWR#1_A	VSYS	–	3	–	5.5	V	DFP/DRP or Gate Driver Modes
SID.PWR#23	VCONN	Power Supply Input Voltage	2.7	–	5.5	V	–
SID.PWR#13	VDDIO	IO Supply Voltage	1.71	–	5.5[2]	V	2.7V < VDDD < 5.5 V
SID.PWR#13_A	VDDIO	IO Supply Voltage for ADC operation	2.7	–	5.5	V	2.7V < VDDD < 5.5 V
SID.PWR24	VCCD	Output Voltage for core Logic	–	1.8	–	V	–
SID.PWR#4	IDD	Supply current	–	25	–	mA	From VSYS or VBUS VBUS = 5V, T_A = 25 °C / VSYS = 5 V, TA = 25 °C FS USB, CC IO in Tx or Rx, no I/O sourcing current, 2 SCBs at 1 Mbps, CPU at 24 MHz.
SID.PWR#1_B	VSYS	Power supply for USB operation	4.5	–	5.5	V	USB configured, USB Regulator enabled
SID.PWR#1_C	VSYS	Power supply for USB operation	3.15	–	3.45	V	USB configured, USB Regulator disabled
SID.PWR#1_D	VSYS	Power supply for charger detect/emulation operation	3.15	–	5.5	V	–40 °C to +85 °C T_A
SID.PWR#27	VBUS	Power supply input voltage	3.5	–	21.5	V	FS USB disabled. Total current consumption from VBUS <15 mA.
SID.PwR#28	VBUS	Power supply input voltage for USB operation	4.5	–	21.5	V	FS USB configured, USB Regulator disabled
SID.PWR#30	VBUS_P	Power supply input voltage	4.00	–	21.5	V	
SID.PWR#15	C_{efc}	External regulator voltage bypass for VCCD	1	1.3	1.6	µF	X5R ceramic or better
SID.PWR#16	C_{exc}	Power supply decoupling capacitor for VSYS	0.8	1	–	µF	X5R ceramic or better
Sleep Mode. VSYS = 2.7 V to 5.5 V. Typical values measured at V_{DD} = 3.3 V and TA = 25 °C.							
SID25A	I_{DD20A}	CC, I^2C, WDT wakeup on. IMO at 48 MHz.	–	3.5	–	mA	VSYS = 3.3 V, T_A = 25 °C, All blocks except CPU are on, CC IO on, USB in Suspend Mode, no I/O sourcing current
Deep Sleep Mode							
SID_DS	I_{DD_DS}	VSYS = 3.0 to 3.6 V. CC Attach, I^2C, WDT Wakeup on.	–	30	–	µA	Power Source = VSYS, DFP Mode, Type-C Not Attached. CC Attach, I^2C and WDT enabled for Wakeup.
XRES Current							
SID307	I_{DD_XR}	Supply current while XRES asserted. This does not include current drawn due to the XRES internal pull-up resistor.	–	30	–	µA	Power Source = VSYS = 3.3 V, Type-C device not attached, T_A = 25 °C

Note

2. If VDDIO > VDDD, GPIO P2.4 cannot be used. It must be left unconnected. See Table 2 for pin numbers.

Table 5. AC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#4	F_{CPU}	CPU input frequency	DC	–	48	MHz	All VDDD
SID.PWR#20	T_{SLEEP}	Wakeup from sleep mode	–	0	–	µs	–
SID.PWR#21	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	–	35	µs	–
SID.XRES#5	T_{XRES}	External reset pulse width	5	–	–	µs	All VDDIO
SYS.FES#1	$T_{\_PWR\_RDY}$	Power-up to “Ready to accept I^2C/CC command”	–	5	25	ms	–

I/O

Table 6. I/O DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.GIO#37	V_{IH_CMOS}	Input voltage HIGH threshold	0.7 × VDDIO	–	–	V	CMOS input
SID.GIO#38	V_{IL_CMOS}	Input voltage LOW threshold	–	–	0.3 × VDDIO	V	CMOS input
SID.GIO#39	$V_{IH\_VDDIO2.7-}$	LVTTL input, VDDIO < 2.7 V	0.7× VDDIO	–	–	V	–
SID.GIO#40	$V_{IL\_VDDIO2.7-}$	LVTTL input, VDDIO < 2.7 V	–	–	0.3 × VDDIO	V	–
SID.GIO#41	$V_{IH\_VDDIO2.7+}$	LVTTL input, VDDIO ≥ 2.7 V	2.0	–	–	V	–
SID.GIO#42	$V_{IL\_VDDIO2.7+}$	LVTTL input, VDDIO ≥ 2.7 V	–	–	0.8	V	–
SID.GIO#33	V_{OH_3V}	Output voltage HIGH level	VDDIO –0.6	–	–	V	I_{OH} = 4 mA at 3V VDDIO
SID.GIO#34	$V_{OH\_1.8V}$	Output voltage HIGH level	VDDIO –0.5	–	–	V	I_{OH} = 1 mA at 1.8V VDDIO
SID.GIO#35	$V_{OL\_1.8V}$	Output voltage LOW level	–	–	0.6	V	I_{OL} = 4 mA at 1.8V VDDIO
SID.GIO#36	V_{OL_3V}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 4 mA at 3V VDDIO for SBU and AUX pins
SID.GIO#5	R_{PU}	Pull-up resistor value	3.5	5.6	8.5	kΩ	+25 °C T_A, all VDDIO
SID.GIO#6	R_{PD}	Pull-down resistor value	3.5	5.6	8.5	kΩ	+25 °C T_A, all VDDIO
SID.GIO#16	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	+25 °C T_A, all VDDIO. Guaranteed by characterization.
SID.GIO#17	C_{PIN}	Max pin capacitance	–	3.0	7	pF	All VDDIO, all packages, all I/Os except SBU and AUX. Guaranteed by characterization.
SID.GIO#17A	C_{PIN_SBU}	Max pin capacitance	–	16	18	pF	All VDDIO, all packages, SBU pins only. Guaranteed by characterization.
SID.GIO#17B	C_{PIN_AUX}	Max pin capacitance	–	12	14	pF	All VDDIO, all packages, AUX pins only. Guaranteed by characterization.
SID.GIO#43	V_{HYSTTL}	Input hysteresis, LVTTL VDDIO > 2.7 V	15	40	–	mV	Guaranteed by characterization
SID.GIO#44	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × VDDIO	–	–	mV	VDDIO < 4.5 V. Guaranteed by characterization.
SID69	I_{DIODE}	Current through protection diode to VDDIO/Vss	–	–	100	µA	Guaranteed by characterization
SID.GIO#45	I_{TOT_GPIO}	Maximum total sink chip current	–	–	85	mA	Guaranteed by characterization

Table 17. Fixed SPI Slave Mode AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID170	T_{DMI}	MOSI Valid before Sclock capturing edge	40	–	–	ns	–
SID171	T_{DSO}	MISO Valid after Sclock driving edge	–	–	42 + 3 × T_{CPU}	ns	T_{CPU} = 1/F_{CPU}
SID171A	T_{DSO_EXT}	MISO Valid after Sclock driving edge in Ext Clk mode	–	–	48	ns	–
SID172	T_{HSO}	Previous MISO data hold time	0	–	–	ns	–
SID172A	$T_{SSELSCK}$	SSEL Valid to first SCK Valid edge	100	–	–	ns	–

System Resources

Power-on-Reset (POR) with Brown Out SWD Interface

Table 18. Imprecise Power On Reset (PRES) (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID185	$V_{RISEIPOR}$	Power-on Reset (POR) rising trip voltage	0.80	–	1.50	V	–
SID186	$V_{FALLIPOR}$	POR falling trip voltage	0.70	–	1.4	V	–

Table 19. Precise Power On Reset (POR) (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190	$V_{FALLPPOR}$	Brown-out Detect (BOD) trip voltage in active/sleep modes	1.48	–	1.62	V	–
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep mode	1.1	–	1.5	V	–

Table 20. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.SWD#1	F_SWDCLK1	3.3 V ≤ VDDIO ≤ 5.5 V	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#2	F_SWDCLK2	1.8 V ≤ VDDIO ≤ 3.3 V	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#3	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 × T	–	–	ns	Guaranteed by characterization
SID.SWD#4	T_SWDI_HOLD	T = 1/f SWDCLK	0.25 × T	–	–	ns	Guaranteed by characterization
SID.SWD#5	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.50 × T	ns	Guaranteed by characterization
SID.SWD#6	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	Guaranteed by characterization

Table 25. PD DC Specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.PD.8	R_{leak_1}	VCONN leaker for 0.1-µF load	–	–	216	kΩ	Managed Active Cable (MAC) discharge.
SID.PD.9	R_{leak_2}	VCONN leaker for 0.5-µF load	–	–	43.2	kΩ	
SID.PD.10	R_{leak_3}	VCONN leaker for 1.0-µF load	–	–	21.6	kΩ	
SID.PD.11	R_{leak_4}	VCONN leaker for 2.0-µF load	–	–	10.8	kΩ	
SID.PD.12	R_{leak_5}	VCONN leaker for 5.0-µF load	–	–	4.32	kΩ	
SID.PD.13	R_{leak_6}	VCONN leaker for 10-µF load	–	–	2.16	kΩ	
SID.PD.14	I_{leak}	Leaker on VCONN for discharge upon cable detach	150	–	550	µA	–
SID.PD.15	$V_{gndoffset}$	Ground offset tolerated by BMC receiver	–400	–	400	mV	Relative to the remote BMC transmitter. Guaranteed by characterization.

Table 26. CSA Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CSA.1	Out_E_Trim_15_DS	Overall Error at Av = 15 using deep sleep reference	–7.00	–	7.00	%	Guaranteed by characterization.
SID.CSA.2	Out_E_Trim_15_BG	Overall Error at Av = 15 using bandgap reference	–4.50	–	4.50	%	Guaranteed by characterization.
SID.CSA.3	Out_E_Trim_100	Overall Error at Av = 100 using either bandgap or deep sleep reference	–24.50	–	24.50	%	–

Table 27. UV/OV Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.UVOV.1	$V_{THUVOV1}$	Voltage threshold Accuracy, $V_{BUS} \leq 16$ V	–6		6	%	Tested at VBUS = 3.75 V, 4.5 V, 5.25 V, 12 V, 16 V
SID.UVOV.2	$V_{THUVOV2}$	Voltage threshold Accuracy, $V_{BUS} > 16$ V	–10		10	%	Tested at VBUS = 20 V

Gate Driver Specifications

Table 28. Gate Driver DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
DC.NGDO.1	VGS1	Gate to Source Overdrive	5	–	16.5	V	1. Gate driver Supply Voltage ≥ 5V, where Gate driver supply voltage = VBUS _P for VBUS_P_CTRL_ outputs, and VBUS_C for VBUS_C_CTRL_ outputs. 2. Gate driver current = 0 3. Gate driver configuration = NFET 4. Gate driver pump clock divider = 1
DC.NGDO.2	VGS2	Gate to Source Overdrive	3.75	–	16.5	V	1. Gate driver Supply Voltage ≥ 3.75V, where Gate driver supply voltage = VBUS _P for VBUS_P_CTRL_ outputs, and VBUS_C for VBUS_C_CTRL_ outputs. 2. Gate driver current = 0 3. Gate driver configuration = NFET 4. Gate driver pump clock divider = 1
DC.NGDO.6	R_{PD}	Resistance when “pull down” enabled	–	–	5	kΩ	–

Table 29. Gate Driver AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
AC.NGDO.1	T_{ON}	Gate turn-on time to gate_driver_supply_voltage + 5V for supply voltage ≥ 5V and VBUS * 2 for supply voltage < 5V	–	–	1	ms	1. Gate driver configuration = NFET 2. Load = The gate of a SI9936 MOSFET

SBU

Table 30. Analog Crossbar Switch Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.SBU.1	Ron_sw	Switch ON Resistance	–	–	10	Ω	Voltage input from 0 V to 3.6 V
SID.SBU.2	Rpu_aux_1	AUX_P/N Pull-up Resistance – 100k	80	–	120	kΩ	–
SID.SBU.3	Rpu_aux_2	AUX_P/N Pull-up Resistance – 1M	0.8	–	1.2	MΩ	–
SID.SBU.4	Rpd_aux_1	AUX_P/N Pull-down Resistance – 100k	80	–	120	kΩ	–
SID.SBU.5	Rpd_aux_2	AUX_P/N Pull-down Resistance – 1M	0.8	–	1.2	MΩ	–
SID.SBU.6	Rpd_aux_3	AUX_P/N Pull-down Resistance – 470k	329	–	611	kΩ	–
SID.SBU.7	Rpd_aux_4	AUX_P/N Pull-down Resistance – 4.7M	3.29	–	6.11	MΩ	–

Charger Detect

Table 31. Charger Detect Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CD.1	VDAT_REF	BC1.2 Data Detect Voltage Threshold	250	–	400	mV	–
SID.CD.2	VDM_SRC	BC1.2 DM Voltage Source	500	–	700	mV	With current sink of 25 µA–175 µA
SID.CD.3	VDP_SRC	BC1.2 DP Voltage Source	500	–	700	mV	With current sink of 25 µA–175 µA
SID.CD.4	IDM_SINK	BC1.2 DM Current Sink	25	–	175	µA	–
SID.CD.5	IDP_SINK	BC1.2 DP Current Sink	25	–	175	µA	–
SID.CD.6	IDP_SRC	BC1.2 DP DCD Current Source	7	–	13	µA	–
SID.CD.7	RDP_UP	USB FS DP Pull-up Termination	0.9	–	1.575	kΩ	–
SID.CD.8	RDM_UP	USB FS DM Pull-up Termination	0.9	–	1.575	kΩ	–
SID.CD.9	RDP_DWN	USB FS DP Pull-down Termination	14.25	–	24.8	kΩ	–
SID.CD.10	RDM_DWN	USB FS DM Pull-down Termination	14.25	–	24.8	kΩ	–
SID.CD.11	RDAT_LKG	DP/DM Data Line Leakage Termination	300	–	500	kΩ	The charger detect function and data line leakage is enabled.
SID.CD.12	RDCP_DAT	BC1.2 DCP Port Resistance between DP and DM	–	–	40	Ω	–
SID.CD.13	VSETH	USB FS Logic Threshold	1.26	–	1.54	V	–

Memory

Table 37. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.MEM#3	FLASH_ERASE	Row erase time	–	–	15.5	ms	–
SID.MEM#4	FLASH_WRITE	Row (Block) write time (erase and program)	–	–	20	ms	–
SID.MEM#8	FLASH_ROW_PGM	Row program time after erase	–	–	7	ms	–
SID178	TBULKERASE	Bulk erase time (64k Bytes)	–	–	35	ms	–
SID180	TDEVPROG	Total device program time	–	–	7.5	s	Guaranteed by characterization
SID182	FRET1	Flash retention, $T_A \le 55$ °C, 100 K P/E cycles	20	–	–	years	Guaranteed by characterization
SID182A	FRET2	Flash retention, $T_A \le 85$ °C, 10 K P/E cycles	10	–	–	years	Guaranteed by characterization
SID182B	FRET3	Flash retention, $T_A \le 105$ °C, 10 K P/E cycles	3	–	–	years	Guaranteed by characterization

Document History Page

Document Title: EZ-PD™ CCG3 USB Type-C Port Controller Document Number: 002-03288				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	4905678	VGT	09/11/2015	New data sheet.
*A	4953333	VGT	10/08/2015	Updated General Description: Updated the number of GPIOs to 20. Updated Functional Overview: Updated GPIO: Updated the number of GPIOs to 20. Updated Pinouts: Updated Table 2. Updated Figure 4. Added Figure 6.
*B	5007726	VGT	11/25/2015	Changed status from Advance to Preliminary. Updated Features. Added EZ-PD CCG3 Block Diagram. Updated Functional Overview: Updated USB-PD Subsystem (USBPD SS) (Updated description). Added Full-Speed USB Subsystem. Updated Pinouts: Updated Table 2. Updated Figure 4. Updated Figure 6. Added Applications. Updated Electrical Specifications: Updated Absolute Maximum Ratings: Updated Table 3. Updated Device-Level Specifications: Updated Table 4. Updated Table 5. Updated I/O: Updated Table 6. Updated XRES: Updated Table 8. Updated System Resources: Updated Power-on-Reset (POR) with Brown Out SWD Interface: Updated Table 18. Updated Table 19. Updated Table 20. Updated Internal Main Oscillator: Updated Table 22. Updated Internal Low-Speed OscillatorPower Down: Updated Table 23. Updated Table 24. Updated Internal Low-Speed OscillatorPower Down: Updated Table 25.

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Document Title: EZ-PD™ CCG3 USB Type-C Port Controller Document Number: 002-03288				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*B (cont.)	5007726	VGT	11/25/2015	Updated Analog to Digital Converter: Updated Table 32. Updated Table 33. Updated Packaging: Added Figure 18 (spec 002-04062 *A).
*C	5080470	VGT	01/11/2016	Updated General Description. Updated Features. Updated Logic Block Diagram. Updated Power Systems Overview. Updated Pinouts: Updated Table 2. Added table “CCG3 Pin Description for 16-SOIC Device”. Added figure “Pinout of 16-SOIC Package (Top View)”. Updated Applications: Updated Figure . Updated Figure 11. Updated figure “Power Adapter Application Diagram (16-SOIC Device)”. Updated Figure 15. Updated Ordering Information. Updated Packaging: Added spec 51-85022 *E. Added Errata.
*D	5137796	VGT	03/09/2016	Updated Pinouts: Updated table “CCG3 Pin Description for 16-SOIC Device”. Updated figure “Pinout of 16-SOIC Package (Top View)”. Updated Applications: Updated Figure 11. Updated Figure 12. Updated Ordering Information Updated Errata. Updated to new template.
*E	5240836	VGT	04/28/2016	Updated General Description: Updated description. Updated Features: Updated Type-C and USB-PD Support: Updated description. Updated Packages: Updated description. Updated Logic Block Diagram. Updated Functional Overview: Updated Integrated Billboard Device: Updated description. Updated USB-PD Subsystem (USBPD SS): Updated description. Added Figure 2 and Figure 5.

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Document Title: EZ-PD™ CCG3 USB Type-C Port Controller Document Number: 002-03288				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*E (cont.)	5240836	VGT	04/28/2016	Updated Power Systems Overview: Updated description. Updated Figure 3. Updated Pinouts: Updated Table 2: Updated details in “Description” column corresponding to VDDIO pin. Removed table “CCG3 Pin Description for 16-SOIC Device”. Removed figure “Pinout of 16-SOIC Package (Top View)”. Updated Applications: Removed figure “Power Adapter Application Diagram (16-SOIC Device)”. Added Figure 12. Updated Electrical Specifications: Updated Device-Level Specifications: Updated Table 4. Updated details in “Details/Conditions” column corresponding to “SID.PWR#1_A” Spec ID and “V_{SYS}” parameter. Replaced “V_{DDD}” with “5.5” in “Max” column corresponding to “SID.PWR#13” Spec ID and “V_{DDIO}” parameter. Added “SID.PWR#13_A” Spec ID corresponding to “V_{DDIO}” parameter and its details. Added “SID.PWR#1_C” and “SID.PWR#1_D” Spec IDs corresponding to “V_{SYS}” parameter and its details. Replaced “enabled” with “disabled” in “Details/Conditions” column corresponding to “SID.PwR#28” Spec ID and “V_{BUS}” parameter. Updated details in “Description” and “Details/Conditions” columns corresponding to “SID307” Spec ID and “I_{DD_XR}” parameter. Updated System Resources: Added Gate Driver Specifications, Charger Detect. Updated Ordering Information: Updated part numbers. Updated details in “Application” column corresponding to part number “CYPD3121-40LQXIT”. Updated Ordering Code Definitions Updated Packaging: Removed spec 51-85022 *E. Removed Errata.
*F	5342389	VGT	07/28/2016	Added Available Firmware and Software Tools, CCG3 Programming and Bootloading, and References and Links to Applications Collaterals. Added descriptive notes for the application diagrams. Updated Features, Applications and Timer/Counter/PWM Block (TCPWM). Updated Table 2 through Table 6, Table 18, Table 19, Table 22, Table 23, Table 25, and Table 31 through Table 38. Updated Figure 7, Figure 8, Figure , Figure 11, and Figure 19 (package diagram spec 001-42168 *E). Added Figure 5, Figure 13, and Figure 14. Added Table 26, Table 27, Table 37, and Table 39 through Table 41. Added VDM in Acronyms. Updated Cypress logo and copyright information.
*G	5449433	VGT	09/26/2016	Added Table 34 through Table 36. Updated Table 3, Table 4, Table 6, and Table 37. Updated Copyright and Disclaimer. Added Compliance information in Sales, Solutions, and Legal Information.

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Document Title: EZ-PD™ CCG3 USB Type-C Port Controller Document Number: 002-03288				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*H	5514508	VGT	01/13/2017	Removed Preliminary document status. Updated Sales information and Copyright details. Added Gate Driver Specifications in Table 28 and Table 29. Updated Applications. Added Figure 16. Updated Ordering Information: Added “CYPD3123-40LQXIT” part number. Removed “CYPD3105-42FNXIT” part number.