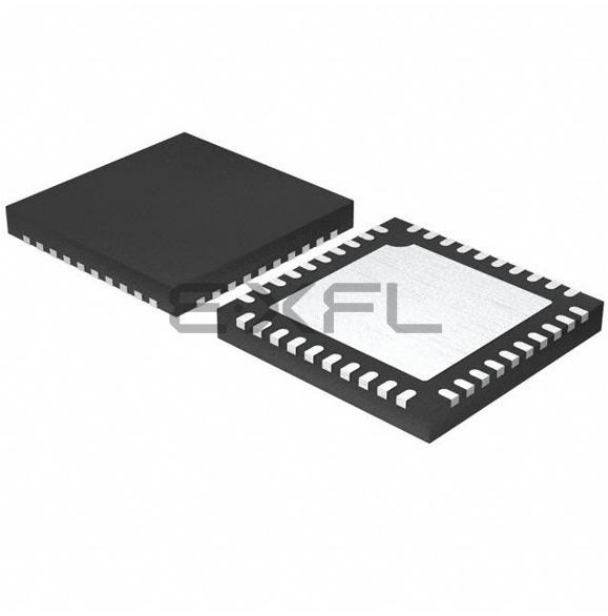

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Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

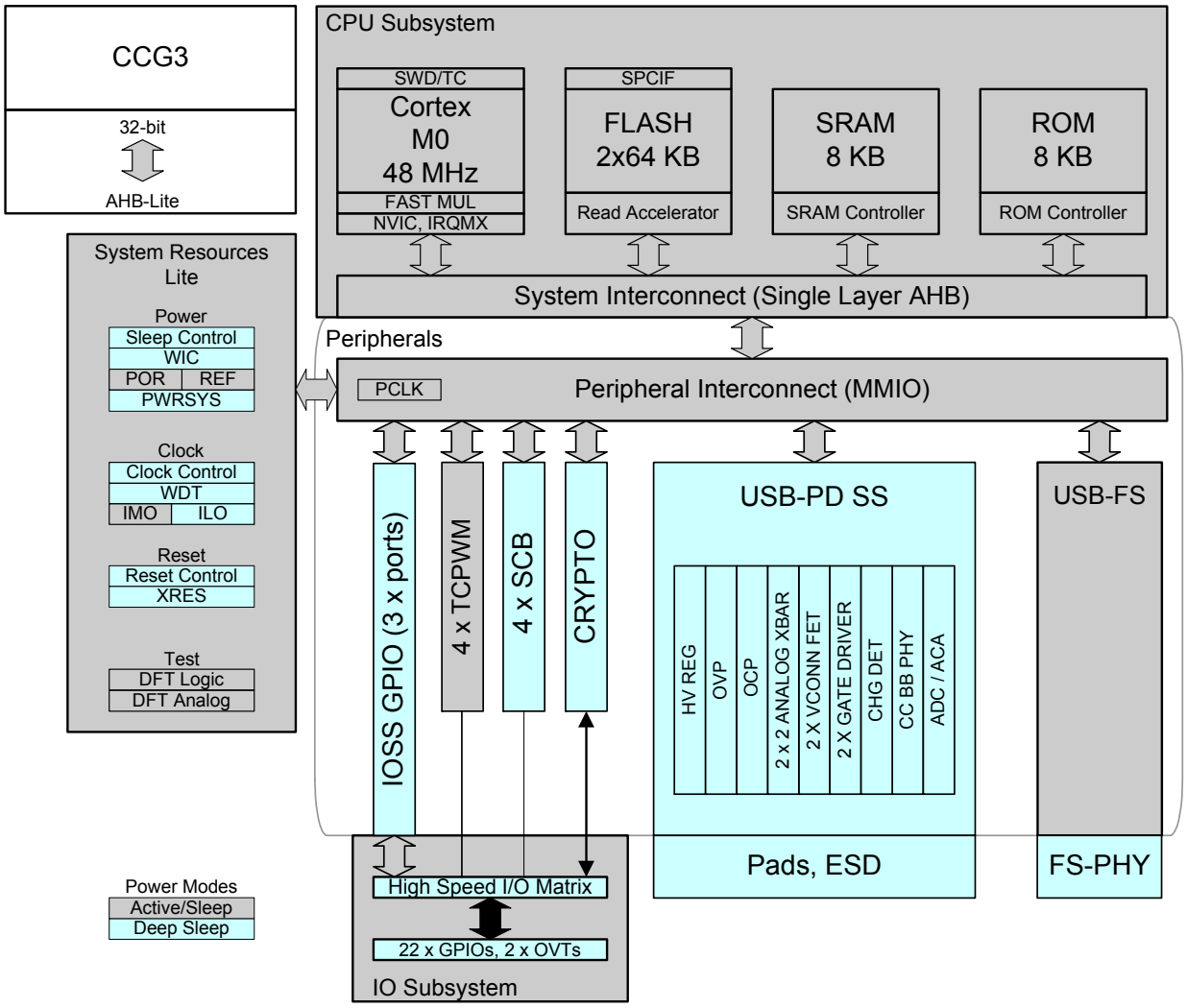
Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	USB Type C
Core Processor	ARM® Cortex®-M0
Program Memory Type	FLASH (128kB)
Controller Series	-
RAM Size	8K x 8
Interface	I²C, SPI, UART/USART, USB
Number of I/O	20
Voltage - Supply	2.7V ~ 5.5V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cypd3125-40lqxi

Contents

EZ-PD CCG3 Block Diagram

Figure 1. EZ-PD CCG3 Block Diagram[1]



Note
1. See Acronyms section for more details.

Functional Overview

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in EZ-PD CCG3 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex-M3 and M4, thus enabling upward compatibility. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor up from the Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a serial wire debug (SWD) interface, which is a two-wire form of JTAG. The debug configuration used for EZ-PD CCG3 has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The EZ-PD CCG3 device has a flash module with two banks of 64 KB flash, a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 1 wait-state (WS) access time at 48 MHz and with 0-WS access time at 24 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

Crypto Block

CCG3 integrates a crypto block for hardware assisted authentication of firmware images. It also supports field upgradeability of firmware in a trusted ecosystem. The CCG3 Crypto block provides cryptography functionality. It includes hardware acceleration blocks for AES (Advanced Encryption Standard) block cipher, SHA-1 (Secure Hash Algorithm) and SHA-2 hash, Cyclic Redundancy Check (CRC) and pseudo random number generation.

Integrated Billboard Device

CCG3 integrates a complete full speed USB 2.0 device controller capable of functioning as a Billboard class device. The USB 2.0 device controller can also support other device classes.

USB-PD Subsystem (USBPD SS)

The USB-PD sub-system contains all of the blocks related to USB Type-C and Power Delivery. The sub-system is comprised of the following:

- BMC PHY: USB-PD Transceiver with Fast Role Swap (FRS) transmit and detect
- VCONN power FETs for the CC lines
- VCONN Ra Termination and Leakers
- Analog Cross-Bar to switch between the SBU1/SBU2 and AUX_P/AUX_N pins
- Programmable Pull-up and Pull-down termination on the AUX_P/AUX_N pins
- HPD Processor
- VBUS_C Regulator (20V LDO)
- Power Switch between VSYS supply and VBUS_C Regulator output
- VBUS_C Over-Voltage (OV) and Under-Voltage (UV) Detectors
- Current Sense Amplifier (CSA) for over current detection
- Gate Drivers for VBUS_P and VBUS_C external Power FETs
- VBUS_C discharge switch
- USB2.0 Full-Speed (FS) PHY with integrated 5.0V to 3.3V regulator
- Charger Detection / Emulation for USB BC1.2 and other proprietary protocols
- 2 instances of 8-bit SAR ADCs
- 8kV IEC ESD Protection on the following pins: VBUS_C, CC1, CC2, SBU1, SBU2, DP, DM

The EZ-PD™ CCG3 USB-PD subsystem interfaces to the pins of a USB Type-C connector. It includes a USB Type-C baseband transceiver and physical-layer logic. This transceiver performs the BMC and the 4b/5b encoding and decoding functions as well as integrating the 1.2V analog front end. This subsystem integrates the required terminations to identify the role of the CCG3 device, including Rp and Rd for UFP/DFP roles and Ra for EMCA/VCONN powered accessories. The programmable VCONN leakers are included in order to discharge VCONN capacitance during a disconnect event. It also integrates power FETs for supplying VCONN power to the CC1/CC2 pins from the V5V pin. The Analog Cross-Bar allows for connecting either of the SBU1/SBU2 pins to either of the AUX_P/AUX_N pins to support DisplayPort sideband signaling. The integrated HPD processor can be used to control or monitor the HPD signal of a DisplayPort source or sink.

Power Systems Overview

Figure 3 shows an overview of the power system requirement for CCG3. CCG3 shall be able to operate from two possible external supply sources VBUS (4.0 V–21.5 V) or VSYS (2.7 V–5.5 V). The VBUS supply is regulated inside the chip with a low-dropout regulator (LDO) down to 3.3 V level. The chip's internal VDDD rail is intelligently switched between the output of the VBUS regulator and unregulated VSYS. The switched supply, VDDD is either used directly inside some analog blocks or further regulated down to VCCD which powers majority of the core using regulators. Besides Reset mode, CCG3 has three different power modes: Active, Sleep and Deep Sleep, transitions between which are managed by the Power System. A separate power domain VDDIO is provided for the GPIOs. The VDDD and VCCD pins, both the output of regulators are brought out for connecting a 1-µF capacitor for the regulator stability only. These pins are not supported as power supplies. When CCG3 is powered from VSYS that is greater than 3.3 V, the dedicated USB regulator allows USB operation.

Figure 3. EZ-PD CCG3 Power System Block Diagram

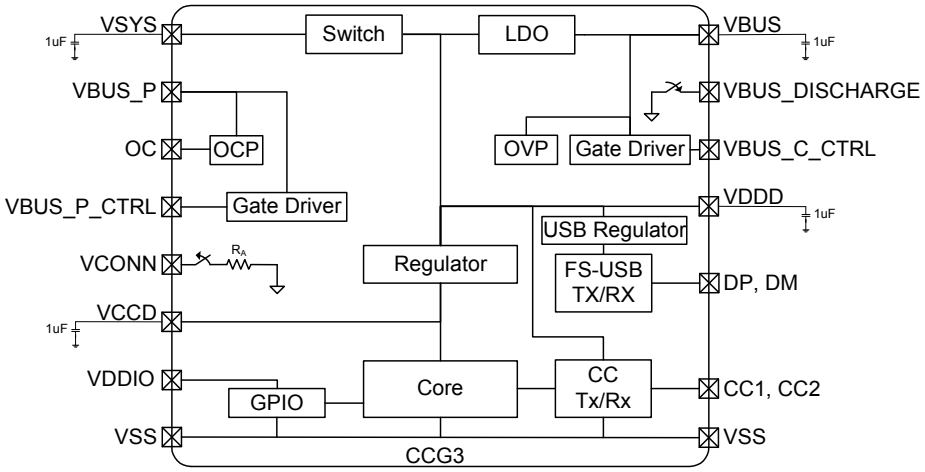


Table 1. CCG3 Power Modes

Mode	Description
RESET	Power is Valid and XRES is not asserted. An internal reset source is asserted or SleepController is sequencing the system out of reset.
ACTIVE	Power is Valid and CPU is executing instructions.
SLEEP	Power is Valid and CPU is not executing instructions. All logic that is not operating is clock gated to save power.
DEEP SLEEP	Main regulator and most hard-IP are shut off. Deep Sleep regulator powers logic, but only low-frequency clock is available.

Figure 6. Pinout of 42-WLCSP Bottom (Balls Up) View

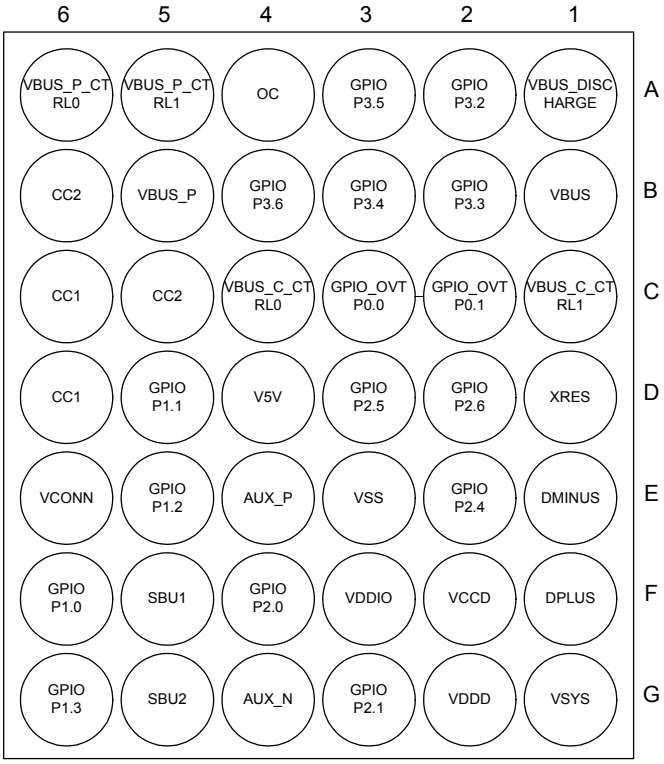


Figure 10. Application Firmware Update over USB

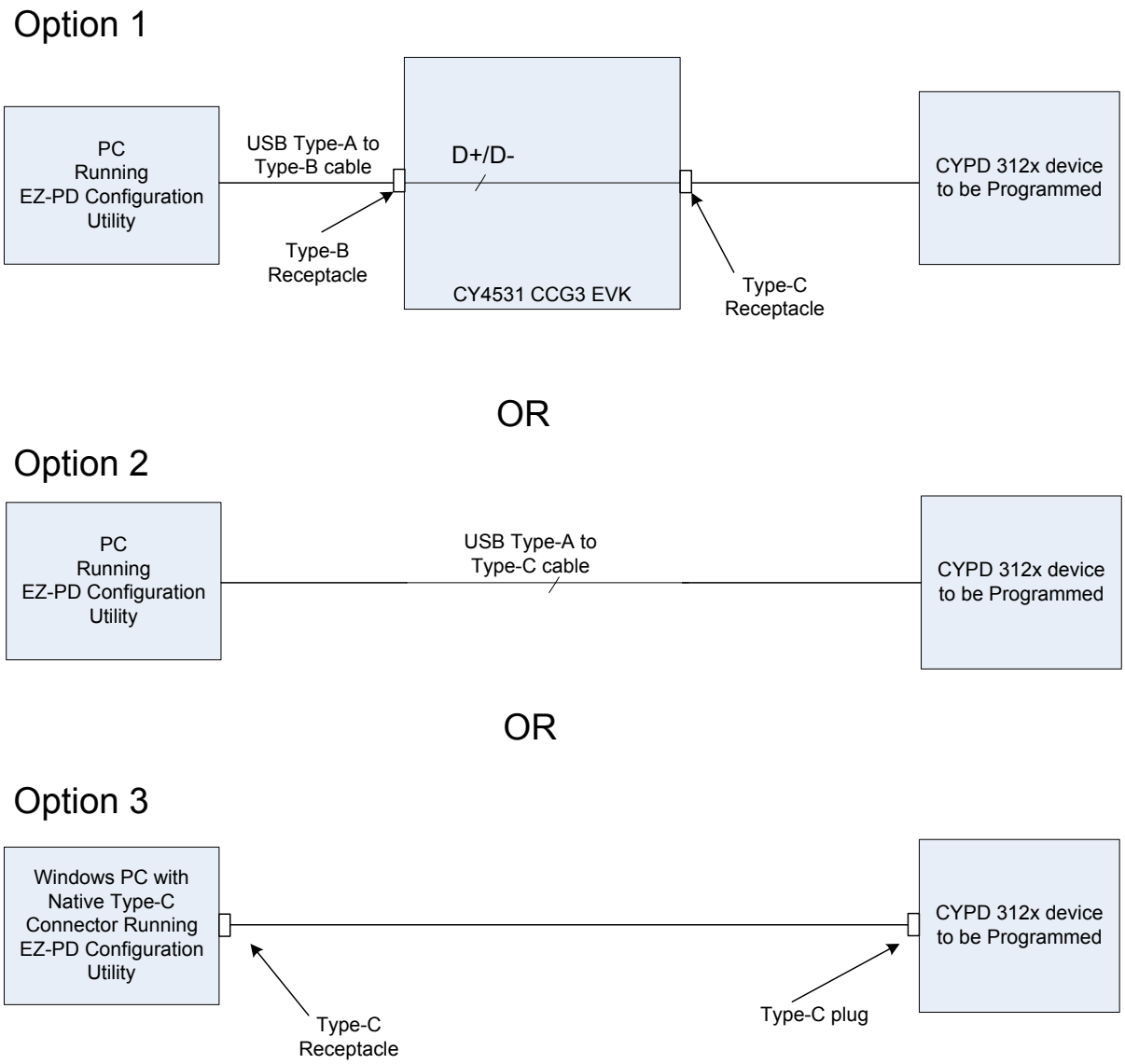


Figure 12 illustrates a power bank application diagram using a CCG3 device. In this application, the Type-C receptacle is used for providing as well as consuming power. The consumer path will be active when the battery is charged using a Type-C power source that is connected to the Type-C receptacle in Figure 12. The provider path will be active when the power bank is used for providing power to a sink device connected to the Type-C receptacle. Additionally, a Type-A receptacle can also be provided for providing power to the sinks that have a legacy USB interface.

The CCG3 device negotiates power contracts between the power bank and the sink/source device connected to the Type-C receptacle. The CCG3 device also controls and drives the provider and consumer path FETs and can monitor overcurrent and overvoltage conditions on the Type-C VBUS line.

Figure 12. Power Bank Application Diagram (40-QFN Device)

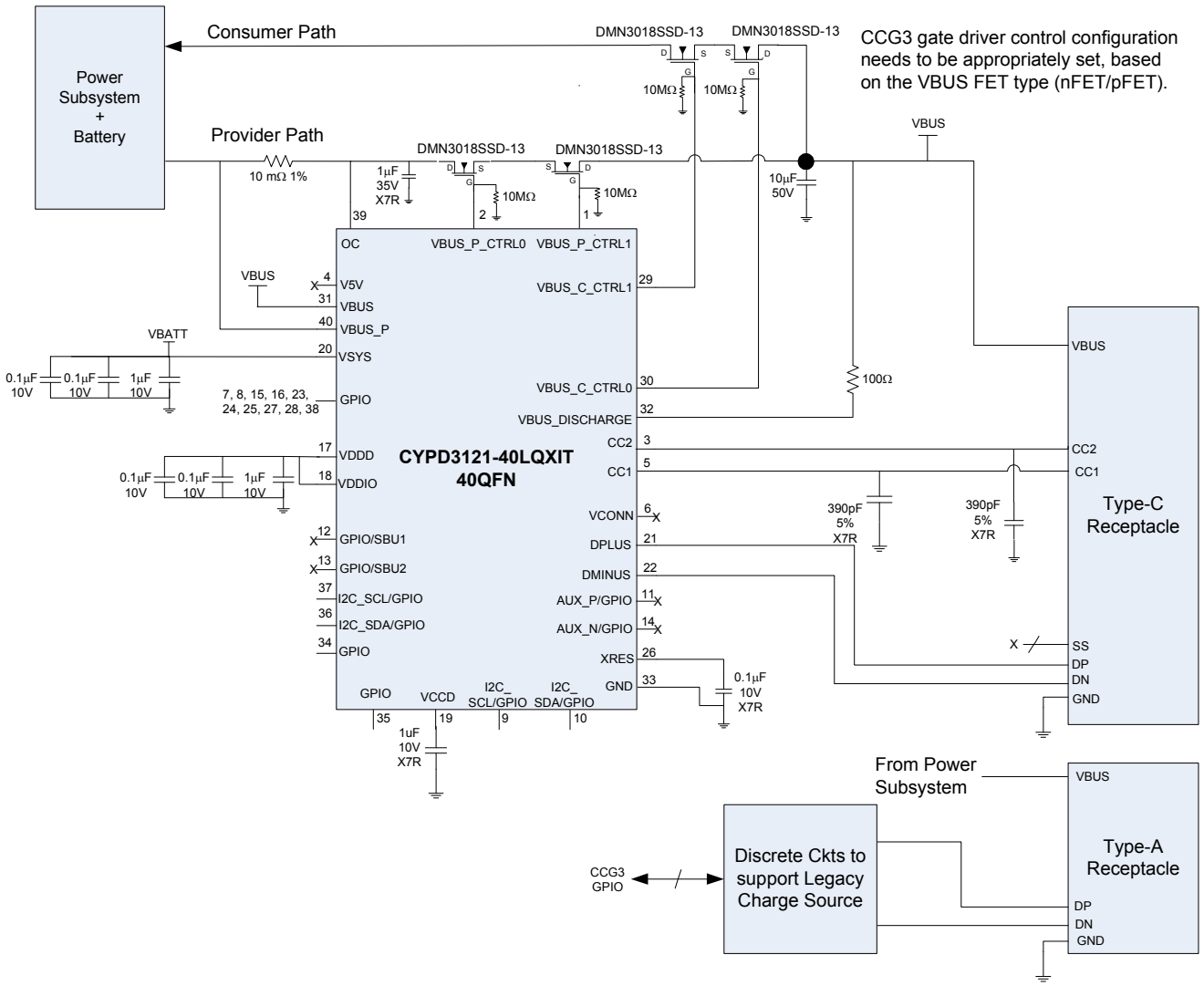


Figure 14 illustrates a USB Type-C to HDMI adapter application, which enables connectivity between a PC that supports a Type-C port with DisplayPort Alternate Mode support and a legacy monitor that has HDMI interface. It enables users of any Notebook that implements USB-Type C to connect to other display types.

This application meets the requirements described in Section 4.3 of the VESA DisplayPort Alt Mode on USB Type-C Standard Version 1.0. This application supports display output at a resolution of up to 4K Ultra HD (3840x2160) at 60 Hz.

Figure 14. USB Type-C to HDMI Adapter Application

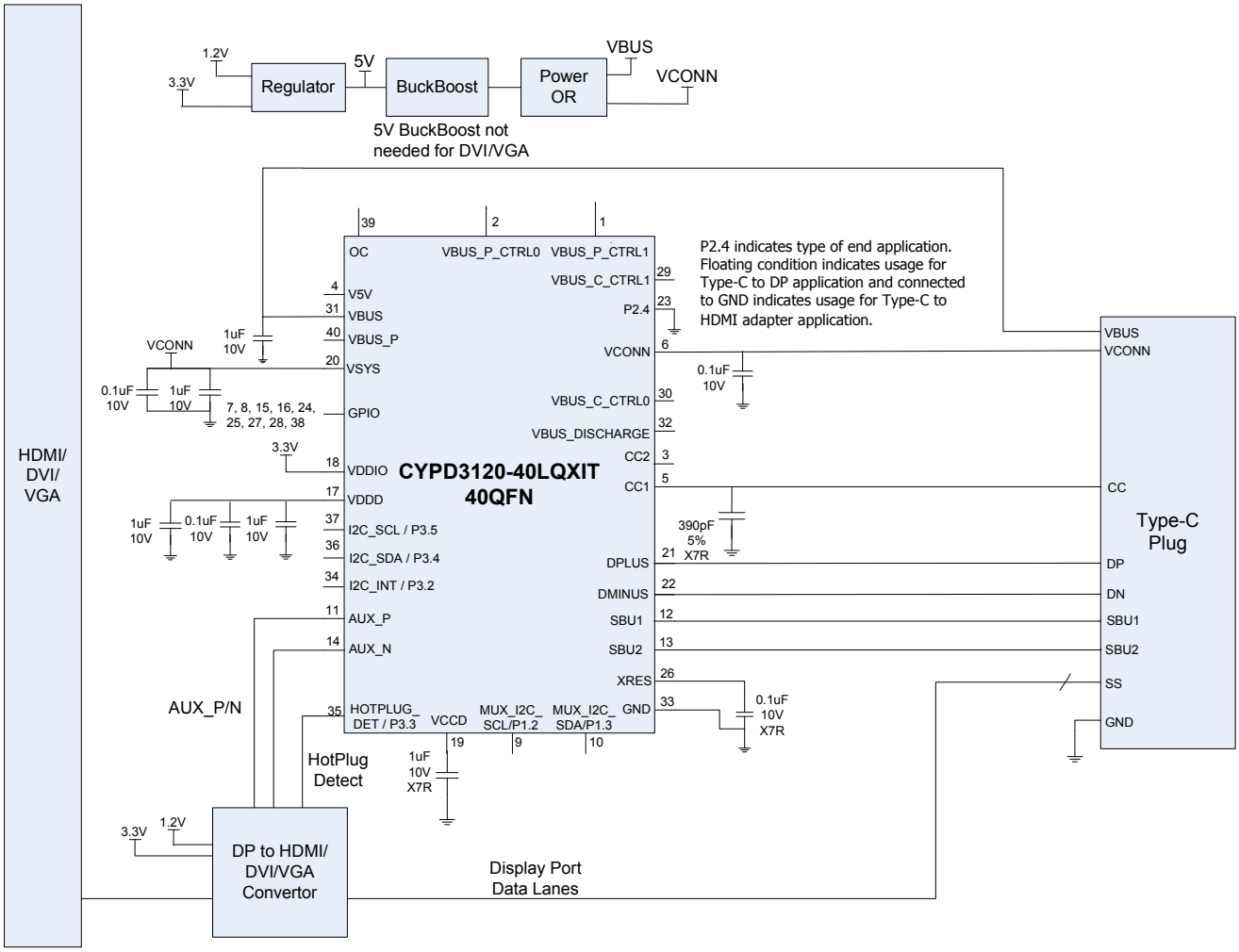
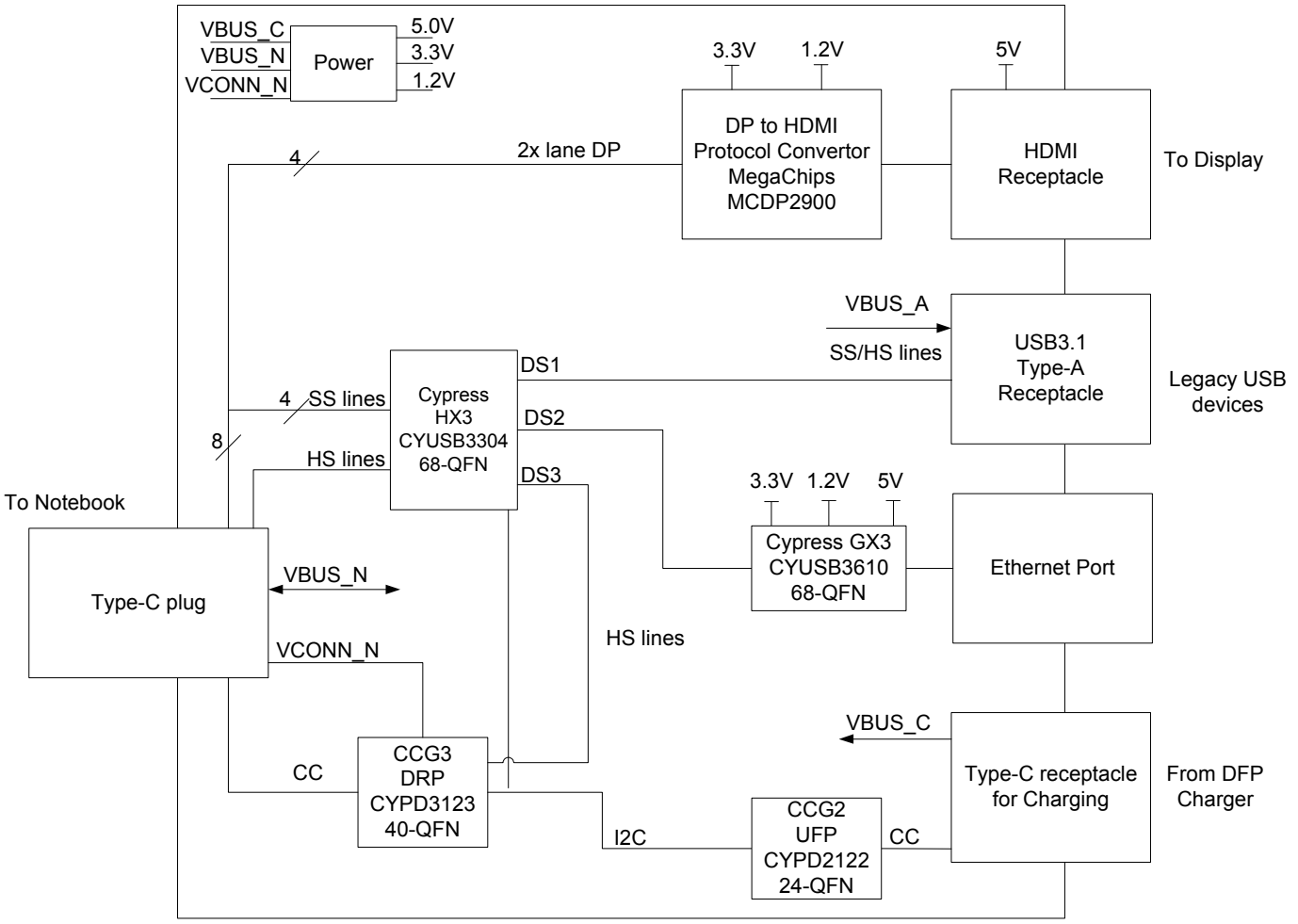


Figure 16 illustrates a CCG3 device based Charge-through Dongle application block diagram. This Charge-through dongle application also implements Cypress's USB SuperSpeed Hub controller HX3 (CYUSB3304-68LTXI) available in 68-QFN package, Low-power single chip USB 3.0 to Gigabit Ethernet Bridge Controller GX3 (CYUSB3610-68LTXC) available in 68-QFN package and the CCG2 (CYPD2122-24LQXI) which acts as an Upstream Facing Port (UFP) and sinks power when connected to USB Type-C chargers.

This application enables connectivity between a USB Type-C Notebook and HDMI Display, legacy USB device and Gigabit Ethernet while also connecting a USB Type-C charging cable. The Charge-Through Dongle solution allows simultaneous HDMI display, Superspeed data transfers, Ethernet connection and charging of a USB Type-C Notebook. Charge-Through Dongle is also widely known as Multiport Adapter. More details including the schematic of the CCG3 device based Charge-through Dongle reference design can be found here.

Figure 16. Charge-through Dongle Application Block Diagram (40-QFN Device)



Electrical Specifications

Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{SYS_MAX}	Digital supply relative to V_{SS}	–0.5	–	6	V	Absolute max
V_{5V}	Max supply voltage relative to V_{SS}	–	–	6	V	
$V_{BUS\_MAX\_ON}$	Max supply voltage relative to V_{SS}, V_{BUS} regulator enabled	–	–	26	V	
$V_{BUS\_MAX\_OFF}$	Max supply voltage relative to V_{SS}, V_{BUS} regulator enabled 100% of the time	–	–	24.5	V	
	Max supply voltage relative to V_{SS}, V_{BUS} regulator enabled 25% of the time	–	–	26	V	
V_{DDIO_MAX}	Max supply voltage relative to V_{SS}	–	–	6	V	
V_{GPIO_ABS}	GPIO voltage	–0.5	–	VDDIO + 0.5	V	
$V_{GPIO\_OVT\_ABS}$	OVT GPIO voltage	–0.5	–	6	V	
I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	
V_{CONN_MAX}	Max voltage relative to V_{SS}	–	–	6	V	
V_{CC_ABS}	Max voltage on CC1 and CC2 pins	–	–	6	V	
$I_{GPIO\_INJECTION}$	GPIO injection current, Max for V_{IH} > VDDD, and Min for V_{IL} < V_{SS}	–0.5	–	0.5	mA	Absolute max, current injected per pin
ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	–
ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	–
LU	Pin current for latch-up	–100	–	100	mA	Tested at 125 °C
ESD_IEC_CON	Electrostatic discharge IEC61000-4-2	8000	–	–	V	Contact discharge on CC1, CC2, VBUS, DPLUS, DMINUS, SBU1 and SBU2 pins
ESD_IEC_AIR	Electrostatic discharge IEC61000-4-2	15000	–	–	V	Air discharge for CC1, CC2, VBUS, DPLUS, DMINUS, SBU1 and SBU2 pins

Table 5. AC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#4	F_{CPU}	CPU input frequency	DC	–	48	MHz	All VDDD
SID.PWR#20	T_{SLEEP}	Wakeup from sleep mode	–	0	–	µs	–
SID.PWR#21	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	–	35	µs	–
SID.XRES#5	T_{XRES}	External reset pulse width	5	–	–	µs	All VDDIO
SYS.FES#1	$T_{\_PWR\_RDY}$	Power-up to “Ready to accept I^2C/CC command”	–	5	25	ms	–

I/O

Table 6. I/O DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.GIO#37	V_{IH_CMOS}	Input voltage HIGH threshold	0.7 × VDDIO	–	–	V	CMOS input
SID.GIO#38	V_{IL_CMOS}	Input voltage LOW threshold	–	–	0.3 × VDDIO	V	CMOS input
SID.GIO#39	$V_{IH\_VDDIO2.7-}$	LVTTL input, VDDIO < 2.7 V	0.7× VDDIO	–	–	V	–
SID.GIO#40	$V_{IL\_VDDIO2.7-}$	LVTTL input, VDDIO < 2.7 V	–	–	0.3 × VDDIO	V	–
SID.GIO#41	$V_{IH\_VDDIO2.7+}$	LVTTL input, VDDIO ≥ 2.7 V	2.0	–	–	V	–
SID.GIO#42	$V_{IL\_VDDIO2.7+}$	LVTTL input, VDDIO ≥ 2.7 V	–	–	0.8	V	–
SID.GIO#33	V_{OH_3V}	Output voltage HIGH level	VDDIO –0.6	–	–	V	I_{OH} = 4 mA at 3V VDDIO
SID.GIO#34	$V_{OH\_1.8V}$	Output voltage HIGH level	VDDIO –0.5	–	–	V	I_{OH} = 1 mA at 1.8V VDDIO
SID.GIO#35	$V_{OL\_1.8V}$	Output voltage LOW level	–	–	0.6	V	I_{OL} = 4 mA at 1.8V VDDIO
SID.GIO#36	V_{OL_3V}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 4 mA at 3V VDDIO for SBU and AUX pins
SID.GIO#5	R_{PU}	Pull-up resistor value	3.5	5.6	8.5	kΩ	+25 °C T_A, all VDDIO
SID.GIO#6	R_{PD}	Pull-down resistor value	3.5	5.6	8.5	kΩ	+25 °C T_A, all VDDIO
SID.GIO#16	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	+25 °C T_A, all VDDIO. Guaranteed by characterization.
SID.GIO#17	C_{PIN}	Max pin capacitance	–	3.0	7	pF	All VDDIO, all packages, all I/Os except SBU and AUX. Guaranteed by characterization.
SID.GIO#17A	C_{PIN_SBU}	Max pin capacitance	–	16	18	pF	All VDDIO, all packages, SBU pins only. Guaranteed by characterization.
SID.GIO#17B	C_{PIN_AUX}	Max pin capacitance	–	12	14	pF	All VDDIO, all packages, AUX pins only. Guaranteed by characterization.
SID.GIO#43	V_{HYSTTL}	Input hysteresis, LVTTL VDDIO > 2.7 V	15	40	–	mV	Guaranteed by characterization
SID.GIO#44	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × VDDIO	–	–	mV	VDDIO < 4.5 V. Guaranteed by characterization.
SID69	I_{DIODE}	Current through protection diode to VDDIO/Vss	–	–	100	µA	Guaranteed by characterization
SID.GIO#45	I_{TOT_GPIO}	Maximum total sink chip current	–	–	85	mA	Guaranteed by characterization

Table 6. I/O DC Specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
OVT							
SID.GIO#46	I_{IHS}	Input current when Pad > VDDIO for OVT inputs	–	–	10.00	µA	Per I^2C specification

Table 7. I/O AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID70	T_{RISEF}	Rise time in Fast Strong mode	2	–	12	ns	3.3 V VDDIO, C_{load} = 25 pF
SID71	T_{FALLF}	Fall time in Fast Strong mode	2	–	12	ns	3.3 V VDDIO, C_{load} = 25 pF

XRES

Table 8. XRES DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.XRES#1	V_{IH_XRES}	Input voltage HIGH threshold on XRES pin	0.7 × VDDIO	–	–	V	CMOS input
SID.XRES#2	V_{IL_XRES}	Input voltage LOW threshold on XRES pin	–	–	0.3 × VDDIO	V	CMOS input
SID.XRES#3	C_{IN_XRES}	Input capacitance on XRES pin	–	–	7	pF	Guaranteed by characterization
SID.XRES#4	$V_{HYSXRES}$	Input voltage hysteresis on XRES pin	–	0.05 × VDDIO	–	mV	Guaranteed by characterization

Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

Pulse Width Modulation (PWM) for GPIO Pins

Table 9. PWM AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.3	$T_{CPWMFREQ}$	Operating frequency	–	–	Fc	MHz	Fc max = CLK_SYS. Maximum = 48 MHz.
SID.TCPWM.4	$T_{PWMENEXT}$	Input trigger pulse width	2/Fc	–	–	ns	For all trigger events
SID.TCPWM.5	T_{PWMEXT}	Output trigger pulse width	2/Fc	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	T_{CRES}	Resolution of counter	1/Fc	–	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWM_{RES}	PWM resolution	1/Fc	–	–	ns	Minimum pulse width of PWM output
SID.TCPWM.5C	Q_{RES}	Quadrature inputs resolution	1/Fc	–	–	ns	Minimum pulse width between quadrature-phase inputs

Table 17. Fixed SPI Slave Mode AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID170	T_{DMI}	MOSI Valid before Sclock capturing edge	40	–	–	ns	–
SID171	T_{DSO}	MISO Valid after Sclock driving edge	–	–	42 + 3 × T_{CPU}	ns	T_{CPU} = 1/F_{CPU}
SID171A	T_{DSO_EXT}	MISO Valid after Sclock driving edge in Ext Clk mode	–	–	48	ns	–
SID172	T_{HSO}	Previous MISO data hold time	0	–	–	ns	–
SID172A	$T_{SSELSCK}$	SSEL Valid to first SCK Valid edge	100	–	–	ns	–

System Resources

Power-on-Reset (POR) with Brown Out SWD Interface

Table 18. Imprecise Power On Reset (PRES) (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID185	$V_{RISEIPOR}$	Power-on Reset (POR) rising trip voltage	0.80	–	1.50	V	–
SID186	$V_{FALLIPOR}$	POR falling trip voltage	0.70	–	1.4	V	–

Table 19. Precise Power On Reset (POR) (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190	$V_{FALLPPOR}$	Brown-out Detect (BOD) trip voltage in active/sleep modes	1.48	–	1.62	V	–
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep mode	1.1	–	1.5	V	–

Table 20. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.SWD#1	F_SWDCLK1	3.3 V ≤ VDDIO ≤ 5.5 V	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#2	F_SWDCLK2	1.8 V ≤ VDDIO ≤ 3.3 V	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#3	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 × T	–	–	ns	Guaranteed by characterization
SID.SWD#4	T_SWDI_HOLD	T = 1/f SWDCLK	0.25 × T	–	–	ns	Guaranteed by characterization
SID.SWD#5	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.50 × T	ns	Guaranteed by characterization
SID.SWD#6	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	Guaranteed by characterization

Table 25. PD DC Specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.PD.8	R_{leak_1}	VCONN leaker for 0.1-µF load	–	–	216	kΩ	Managed Active Cable (MAC) discharge.
SID.PD.9	R_{leak_2}	VCONN leaker for 0.5-µF load	–	–	43.2	kΩ	
SID.PD.10	R_{leak_3}	VCONN leaker for 1.0-µF load	–	–	21.6	kΩ	
SID.PD.11	R_{leak_4}	VCONN leaker for 2.0-µF load	–	–	10.8	kΩ	
SID.PD.12	R_{leak_5}	VCONN leaker for 5.0-µF load	–	–	4.32	kΩ	
SID.PD.13	R_{leak_6}	VCONN leaker for 10-µF load	–	–	2.16	kΩ	
SID.PD.14	I_{leak}	Leaker on VCONN for discharge upon cable detach	150	–	550	µA	–
SID.PD.15	$V_{gndoffset}$	Ground offset tolerated by BMC receiver	–400	–	400	mV	Relative to the remote BMC transmitter. Guaranteed by characterization.

Table 26. CSA Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CSA.1	Out_E_Trim_15_DS	Overall Error at Av = 15 using deep sleep reference	–7.00	–	7.00	%	Guaranteed by characterization.
SID.CSA.2	Out_E_Trim_15_BG	Overall Error at Av = 15 using bandgap reference	–4.50	–	4.50	%	Guaranteed by characterization.
SID.CSA.3	Out_E_Trim_100	Overall Error at Av = 100 using either bandgap or deep sleep reference	–24.50	–	24.50	%	–

Table 27. UV/OV Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.UVOV.1	$V_{THUVOV1}$	Voltage threshold Accuracy, $V_{BUS} \leq 16$ V	–6		6	%	Tested at VBUS = 3.75 V, 4.5 V, 5.25 V, 12 V, 16 V
SID.UVOV.2	$V_{THUVOV2}$	Voltage threshold Accuracy, $V_{BUS} > 16$ V	–10		10	%	Tested at VBUS = 20 V

Gate Driver Specifications

Table 28. Gate Driver DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
DC.NGDO.1	VGS1	Gate to Source Overdrive	5	–	16.5	V	1. Gate driver Supply Voltage ≥ 5V, where Gate driver supply voltage = VBUS _P for VBUS_P_CTRL_ outputs, and VBUS_C for VBUS_C_CTRL_ outputs. 2. Gate driver current = 0 3. Gate driver configuration = NFET 4. Gate driver pump clock divider = 1
DC.NGDO.2	VGS2	Gate to Source Overdrive	3.75	–	16.5	V	1. Gate driver Supply Voltage ≥ 3.75V, where Gate driver supply voltage = VBUS _P for VBUS_P_CTRL_ outputs, and VBUS_C for VBUS_C_CTRL_ outputs. 2. Gate driver current = 0 3. Gate driver configuration = NFET 4. Gate driver pump clock divider = 1
DC.NGDO.6	R_{PD}	Resistance when “pull down” enabled	–	–	5	kΩ	–

Table 29. Gate Driver AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
AC.NGDO.1	T_{ON}	Gate turn-on time to gate_driver_supply_voltage + 5V for supply voltage ≥ 5V and VBUS * 2 for supply voltage < 5V	–	–	1	ms	1. Gate driver configuration = NFET 2. Load = The gate of a SI9936 MOSFET

SBU

Table 30. Analog Crossbar Switch Specifications

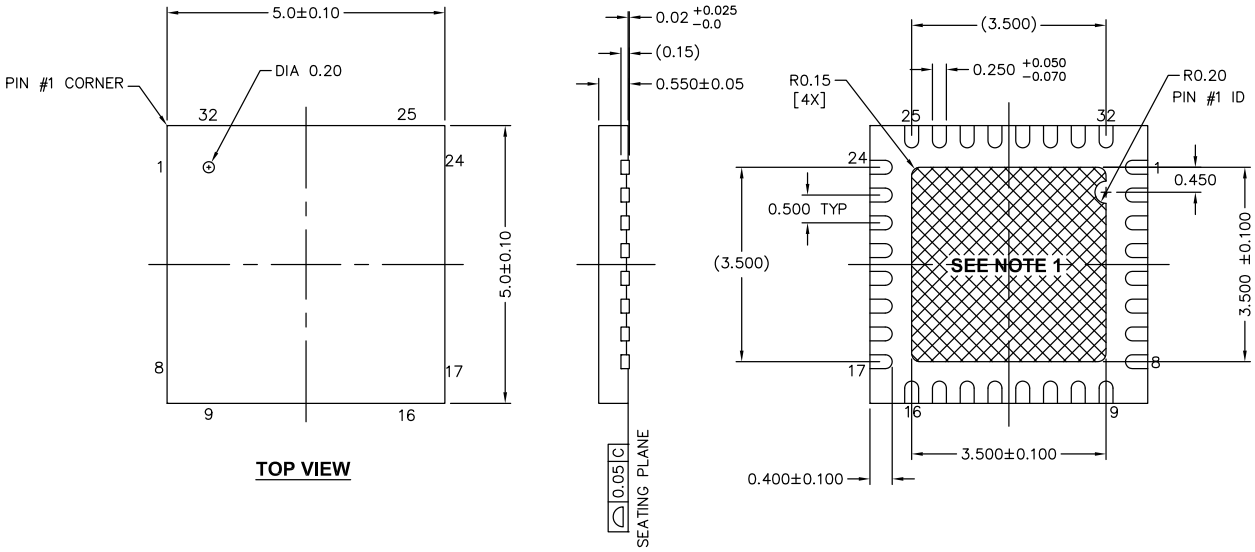
Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.SBU.1	Ron_sw	Switch ON Resistance	–	–	10	Ω	Voltage input from 0 V to 3.6 V
SID.SBU.2	Rpu_aux_1	AUX_P/N Pull-up Resistance – 100k	80	–	120	kΩ	–
SID.SBU.3	Rpu_aux_2	AUX_P/N Pull-up Resistance – 1M	0.8	–	1.2	MΩ	–
SID.SBU.4	Rpd_aux_1	AUX_P/N Pull-down Resistance – 100k	80	–	120	kΩ	–
SID.SBU.5	Rpd_aux_2	AUX_P/N Pull-down Resistance – 1M	0.8	–	1.2	MΩ	–
SID.SBU.6	Rpd_aux_3	AUX_P/N Pull-down Resistance – 470k	329	–	611	kΩ	–
SID.SBU.7	Rpd_aux_4	AUX_P/N Pull-down Resistance – 4.7M	3.29	–	6.11	MΩ	–

Charger Detect

Table 31. Charger Detect Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CD.1	VDAT_REF	BC1.2 Data Detect Voltage Threshold	250	–	400	mV	–
SID.CD.2	VDM_SRC	BC1.2 DM Voltage Source	500	–	700	mV	With current sink of 25 µA–175 µA
SID.CD.3	VDP_SRC	BC1.2 DP Voltage Source	500	–	700	mV	With current sink of 25 µA–175 µA
SID.CD.4	IDM_SINK	BC1.2 DM Current Sink	25	–	175	µA	–
SID.CD.5	IDP_SINK	BC1.2 DP Current Sink	25	–	175	µA	–
SID.CD.6	IDP_SRC	BC1.2 DP DCD Current Source	7	–	13	µA	–
SID.CD.7	RDP_UP	USB FS DP Pull-up Termination	0.9	–	1.575	kΩ	–
SID.CD.8	RDM_UP	USB FS DM Pull-up Termination	0.9	–	1.575	kΩ	–
SID.CD.9	RDP_DWN	USB FS DP Pull-down Termination	14.25	–	24.8	kΩ	–
SID.CD.10	RDM_DWN	USB FS DM Pull-down Termination	14.25	–	24.8	kΩ	–
SID.CD.11	RDAT_LKG	DP/DM Data Line Leakage Termination	300	–	500	kΩ	The charger detect function and data line leakage is enabled.
SID.CD.12	RDCP_DAT	BC1.2 DCP Port Resistance between DP and DM	–	–	40	Ω	–
SID.CD.13	VSETH	USB FS Logic Threshold	1.26	–	1.54	V	–

Figure 19. 32-pin QFN Package Outline, 001-42168



NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO−248
3. PACKAGE WEIGHT: 0.0388g
4. DIMENSIONS ARE IN MILLIMETERS

001-42168 *E

Acronyms

Table 42. Acronyms Used in this Document

Acronym	Description
ADC	analog-to-digital converter
AES	advanced encryption standard
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus
API	application programming interface
ARM®	advanced RISC machine, a CPU architecture
BMC	Biphase Mark Code
CC	configuration channel
CCG3	Cable Controller Generation 3
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
CS	current sense
DFP	downstream facing port
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DRP	dual role port
EEPROM	electrically erasable programmable read-only memory
EMCA	electronically marked cable assembly, a USB cable that includes an IC that reports cable characteristics (e.g., current rating) to the Type-C ports
EMI	electromagnetic interference
ESD	electrostatic discharge
FS	full-speed
GPIO	general-purpose input/output
HPD	hot plug detect
IC	integrated circuit
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
IOSS	input/output subsystem
I/O	input/output, see also GPIO
LDO	low-dropout regulator
LVD	low-voltage detect
LVTTL	low-voltage transistor-transistor logic
MCU	microcontroller unit
MMIO	memory mapped input/output
NC	no connect
NMI	nonmaskable interrupt
NVIC	nested vectored interrupt controller

Table 42. Acronyms Used in this Document *(continued)*

Acronym	Description
opamp	operational amplifier
OCP	overcurrent protection
OVP	overvoltage protection
PCB	printed circuit board
PD	power delivery
PGA	programmable gain amplifier
PHY	physical layer
POR	power-on reset
PRES	precise power-on reset
PSoC®	Programmable System-on-Chip™
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RX	receive
SAR	successive approximation register
SCB	serial communication block
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SHA	secure hash algorithm
SPI	Serial Peripheral Interface, a communications protocol
SRAM	static random access memory
SWD	serial wire debug, a test protocol
TCPWM	timer/counter pulse-width modulator
Thunderbolt™	Trademark of Intel
TX	transmit
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
USB	Universal Serial Bus
USB PD	USB Power Delivery
USB-FS	USB Full-Speed
USBIO	USB input/output, CCG2 pins used to connect to a USB port
USBPD SS	USB PD subsystem
VDM	vendor defined messages
XRES	external reset I/O pin

Document Conventions

Units of Measure

Table 43. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
Hz	hertz
KB	1024 bytes
kHz	kilohertz
kΩ	kilo ohm
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
V	volt

Document History Page *(continued)*

Document Title: EZ-PD™ CCG3 USB Type-C Port Controller Document Number: 002-03288				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*B (cont.)	5007726	VGT	11/25/2015	Updated Analog to Digital Converter: Updated Table 32. Updated Table 33. Updated Packaging: Added Figure 18 (spec 002-04062 *A).
*C	5080470	VGT	01/11/2016	Updated General Description. Updated Features. Updated Logic Block Diagram. Updated Power Systems Overview. Updated Pinouts: Updated Table 2. Added table “CCG3 Pin Description for 16-SOIC Device”. Added figure “Pinout of 16-SOIC Package (Top View)”. Updated Applications: Updated Figure . Updated Figure 11. Updated figure “Power Adapter Application Diagram (16-SOIC Device)”. Updated Figure 15. Updated Ordering Information. Updated Packaging: Added spec 51-85022 *E. Added Errata.
*D	5137796	VGT	03/09/2016	Updated Pinouts: Updated table “CCG3 Pin Description for 16-SOIC Device”. Updated figure “Pinout of 16-SOIC Package (Top View)”. Updated Applications: Updated Figure 11. Updated Figure 12. Updated Ordering Information Updated Errata. Updated to new template.
*E	5240836	VGT	04/28/2016	Updated General Description: Updated description. Updated Features: Updated Type-C and USB-PD Support: Updated description. Updated Packages: Updated description. Updated Logic Block Diagram. Updated Functional Overview: Updated Integrated Billboard Device: Updated description. Updated USB-PD Subsystem (USBPD SS): Updated description. Added Figure 2 and Figure 5.

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