Infineon Technologies - CY8C4125AXI-M445 Datasheet

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I²C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, CapSense, LCD, LVD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b SAR; 2xIDAC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4125axi-m445

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article KBA86521, How to Design with PSoC 3, PSoC 4, and PSoC 5LP. Following is an abbreviated list for PSoC 4:

- Overview: PSoC Portfolio, PSoC Roadmap
- Product Selectors: PSoC 1, PSoC 3, PSoC 4, PSoC 5LP
  In addition, PSoC Creator includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 4 are:
  - AN79953: Getting Started With PSoC 4
  - AN88619: PSoC 4 Hardware Design Considerations
  - AN86439: Using PSoC 4 GPIO Pins
  - AN57821: Mixed Signal Circuit Board Layout
  - AN81623: Digital Design Best Practices
  - AN73854: Introduction To Bootloaders
  - AN89610: ARM Cortex Code Optimization
- Technical Reference Manual (TRM) is in two documents:
  - Architecture TRM details each PSoC 4 functional block.
  - Registers TRM describes each of the PSoC 4 registers.
- Development Kits:
  - CY8CKIT-042, PSoC 4 Pioneer Kit, is an easy-to-use and inexpensive development platform. This kit includes connectors for Arduino™ compatible shields and Digilent® Pmod™ daughter cards.
  - CY8CKIT-049 is a very low-cost prototyping platform. It is a low-cost alternative to sampling PSoC 4 devices.
  - CY8CKIT-001 is a common development platform for any one of the PSoC 1, PSoC 3, PSoC 4, or PSoC 5LP families of devices.

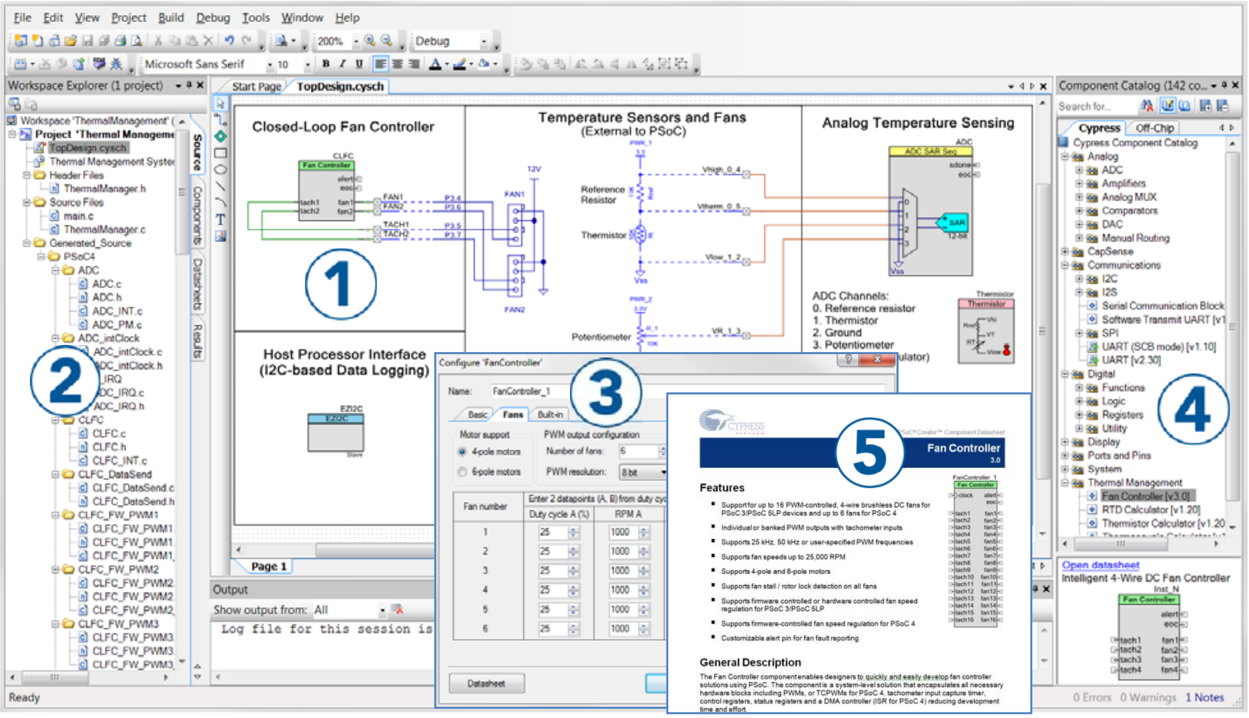
The MiniProg3 device provides an interface for flash programming and debug.

PSoC Creator

PSoC Creator is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC 3, PSoC 4, and PSoC 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC Components; see the list of component datasheets. With PSoC Creator, you can:

1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

Figure 1. Multiple-Sensor Example Project in PSoC Creator



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Log file for this session is
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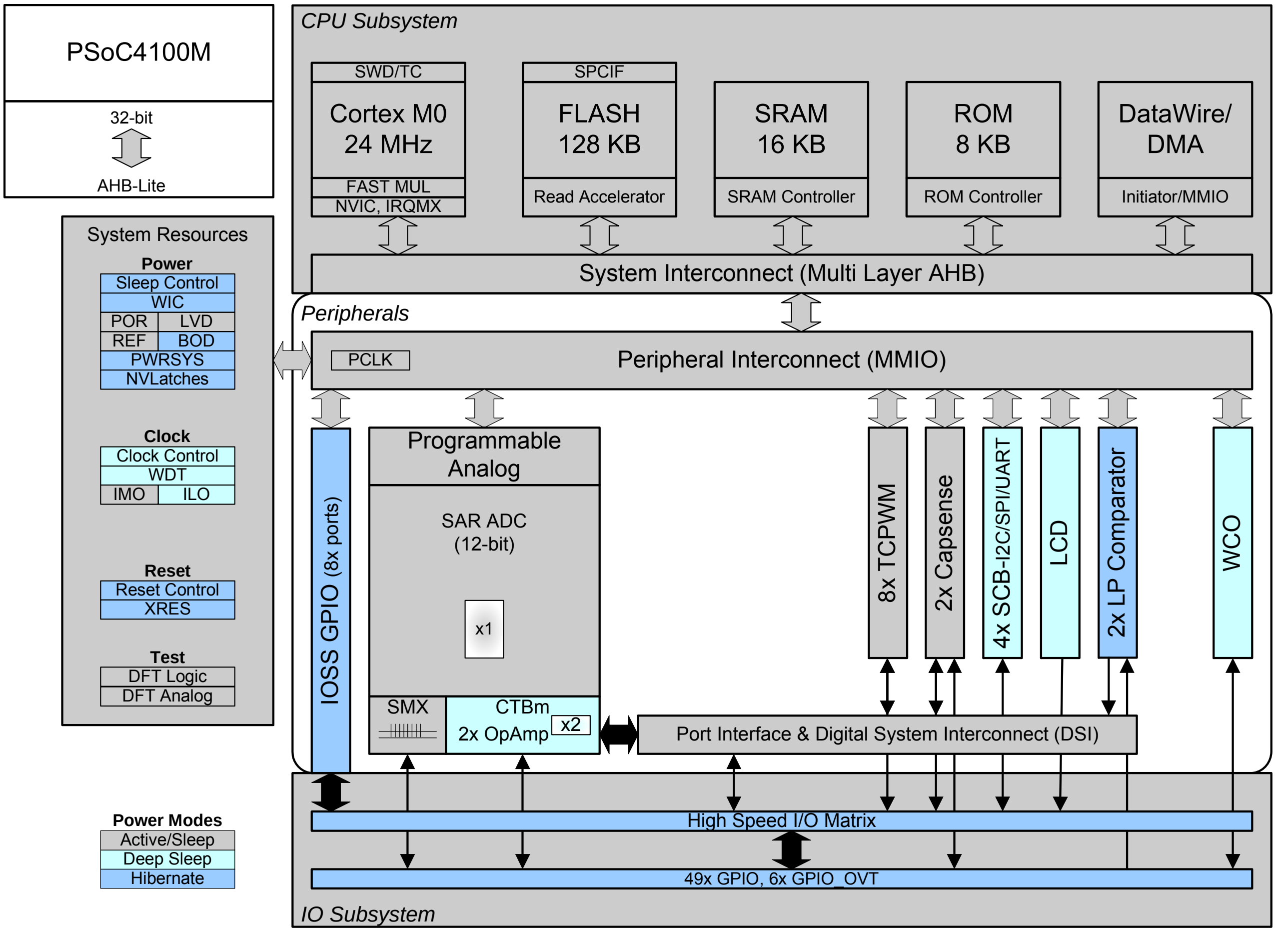
Contents

PSoC 4100M Block Diagram



The PSoC 4100-M devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The ARM Serial_Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator Integrated Development Environment (IDE) provides fully integrated programming and debug support for PSoC 4100-M devices. The SWD interface is fully compatible with industry-standard third-party tools. The PSoC 4100-M family provides a level of security not possible with multi-chip application solutions or with microcontrollers. This is due to its ability to disable debug features, robust flash protection, and because it allows customer-proprietary functionality to be implemented in on-chip programmable blocks.

The debug circuits are enabled by default and can only be disabled in firmware. If not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. Because all programming, debug, and test interfaces are disabled when maximum device security is enabled, PSoC 4100-M with device security enabled may not be returned for failure analysis. This is a trade-off the PSoC 4100-M allows the customer to make.

Pinouts

The following is the pin list for the PSoC 4100M. This shows the power supply and port pins (for example, P0.0 is Pin 0 of Port 0).

68-QFN		64-TQFP		48-TQFP		44-TQFP	
Pin	**Name**	**Pin**	**Name**	**Pin**	**Name**	**Pin**	**Name**
42	P0.0	39	P0.0	28	P0.0	24	P0.0
43	P0.1	40	P0.1	29	P0.1	25	P0.1
44	P0.2	41	P0.2	30	P0.2	26	P0.2
45	P0.3	42	P0.3	31	P0.3	27	P0.3
46	P0.4	43	P0.4	32	P0.4	28	P0.4
47	P0.5	44	P0.5	33	P0.5	29	P0.5
48	P0.6	45	P0.6	34	P0.6	30	P0.6
49	P0.7	46	P0.7	35	P0.7	31	P0.7
50	XRES	47	XRES	36	XRES	32	XRES
51	VCCD	48	VCCD	37	VCCD	33	VCCD
52	VSSD	49	VSSD	38	VSSD	DN	VSSD
53	VDDD	50	VDDD	39	VDDD	34	VDDD
				40	VDDA	35	VDDA
54	P5.0	51	P5.0				
55	P5.1	52	P5.1				
56	P5.2	53	P5.2				
57	P5.3	54	P5.3				
58	P5.4						
59	P5.5	55	P5.5				
60	VDDA	56	VDDA	40	VDDA	35	VDDA
61	VSSA	57	VSSA	41	VSSA	36	VSSA
62	P1.0	58	P1.0	42	P1.0	37	P1.0
63	P1.1	59	P1.1	43	P1.1	38	P1.1
64	P1.2	60	P1.2	44	P1.2	39	P1.2
65	P1.3	61	P1.3	45	P1.3	40	P1.3
66	P1.4	62	P1.4	46	P1.4	41	P1.4
67	P1.5	63	P1.5	47	P1.5	42	P1.5
68	P1.6	64	P1.6	48	P1.6	43	P1.6
1	P1.7/VREF	1	P1.7/VREF	1	P1.7/VREF	44	P1.7/VREF
						1	VSSD
2	P2.0	2	P2.0	2	P2.0	2	P2.0
3	P2.1	3	P2.1	3	P2.1	3	P2.1
4	P2.2	4	P2.2	4	P2.2	4	P2.2
5	P2.3	5	P2.3	5	P2.3	5	P2.3
6	P2.4	6	P2.4	6	P2.4	6	P2.4
7	P2.5	7	P2.5	7	P2.5	7	P2.5

68-QFN		64-TQFP		48-TQFP		44-TQFP	
Pin	**Name**	**Pin**	**Name**	**Pin**	**Name**	**Pin**	**Name**
8	P2.6	8	P2.6	8	P2.6	8	P2.6
9	P2.7	9	P2.7	9	P2.7	9	P2.7
10	VSSA	10	VSSA	10	VSSD	10	VSSD
11	VDDA	11	VDDA				
12	P6.0	12	P6.0				
13	P6.1	13	P6.1				
14	P6.2	14	P6.2				
15	P6.3						
16	P6.4	15	P6.4				
17	P6.5	16	P6.5				
18	VSSIO	17	VSSIO	10	VSSD	10	VSSD
19	P3.0	18	P3.0	12	P3.0	11	P3.0
20	P3.1	19	P3.1	13	P3.1	12	P3.1
21	P3.2	20	P3.2	14	P3.2	13	P3.2
22	P3.3	21	P3.3	16	P3.3	14	P3.3
23	P3.4	22	P3.4	17	P3.4	15	P3.4
24	P3.5	23	P3.5	18	P3.5	16	P3.5
25	P3.6	24	P3.6	19	P3.6	17	P3.6
26	P3.7	25	P3.7	20	P3.7	18	P3.7
27	VDDIO	26	VDDIO	21	VDDIO	19	VDDD
28	P4.0	27	P4.0	22	P4.0	20	P4.0
29	P4.1	28	P4.1	23	P4.1	21	P4.1
30	P4.2	29	P4.2	24	P4.2	22	P4.2
31	P4.3	30	P4.3	25	P4.3	23	P4.3
32	P4.4	31	P4.4				
33	P4.5	32	P4.5				
34	P4.6	33	P4.6				
35	P4.7						
39	P7.0	37	P7.0	26	P7.0		
40	P7.1	38	P7.1	27	P7.1		
41	P7.2						

The pins of Port 6 are overvoltage-tolerant. Pins 36, 37, and 38 are No-Connects on the 68-pin QFN. Pins 34, 35, and 36 are No-Connects on the 64-pin TQFP. Pins 11 and 15 are No-connects in the 48-pin TQFP. All VSS pins must be tied together.

The output drivers of I/O Ports P0 and P7 are connected to VDDD. Output drivers of I/O Ports 1, 2, and 5 are connected to VDDA. Output drivers of I/O Ports 3, 4, and 6 are connected to VDDIO.

Each of the pins shown in the previous table can have multiple programmable functions as shown in the following table. Column headings refer to Analog and Alternate pin functions:

Port/Pin	Analog	Alt. Function 1	Alt. Function 2	Alt. Function 3	Alt. Function 4	Alt. Function 5
P0.0	lpcomp.in_p[0]					scb[0].spi_select1:0
P0.1	lpcomp.in_n[0]					scb[0].spi_select2:0
P0.2	lpcomp.in_p[1]					scb[0].spi_select3:0
P0.3	lpcomp.in_n[1]					
P0.4	wco_in		scb[1].uart_rx:0		scb[1].i2c_scl:0	scb[1].spi_mosi:1
P0.5	wco_out		scb[1].uart_tx:0		scb[1].i2c_sda:0	scb[1].spi_miso:1
P0.6		ext_clk:0	scb[1].uart_cts:0			scb[1].spi_clk:1
P0.7			scb[1].uart_rts:0		wakeup	scb[1].spi_select0:1
P5.0	ctb1.oa0.inp	tcpwm.line[4]:2	scb[2].uart_rx:0		scb[2].i2c_scl:0	scb[2].spi_mosi:0
P5.1	ctb1.oa0.inm	tcpwm.line_compl[4]:2	scb[2].uart_tx:0		scb[2].i2c_sda:0	scb[2].spi_miso:0
P5.2	ctb1.oa0.out	tcpwm.line[5]:2	scb[2].uart_cts:0		lpcomp.comp[0]:1	scb[2].spi_clk:0
P5.3	ctb1.oa1.out	tcpwm.line_compl[5]:2	scb[2].uart_rts:0		lpcomp.comp[1]:1	scb[2].spi_select0:0
P5.4	ctb1.oa1.inm	tcpwm.line[6]:2				scb[2].spi_select1:0
P5.5	ctb1.oa1.inp	tcpwm.line_compl[6]:2				scb[2].spi_select2:0
P5.6	ctb1.oa0.inp_alt	tcpwm.line[7]:0				scb[2].spi_select3:0
P5.7	ctb1.oa1.inp_alt	tcpwm.line_compl[7]:0				
P1.0	ctb0.oa0.inp	tcpwm.line[2]:1	scb[0].uart_rx:1		scb[0].i2c_scl:0	scb[0].spi_mosi:1
P1.1	ctb0.oa0.inm	tcpwm.line_compl[2]:1	scb[0].uart_tx:1		scb[0].i2c_sda:0	scb[0].spi_miso:1
P1.2	ctb0.oa0.out	tcpwm.line[3]:1	scb[0].uart_cts:1			scb[0].spi_clk:1
P1.3	ctb0.oa1.out	tcpwm.line_compl[3]:1	scb[0].uart_rts:1			scb[0].spi_select0:1
P1.4	ctb0.oa1.inm	tcpwm.line[6]:1				scb[0].spi_select1:1
P1.5	ctb0.oa1.inp	tcpwm.line_compl[6]:1				scb[0].spi_select2:1
P1.6	ctb0.oa0.inp_alt	tcpwm.line[7]:1				scb[0].spi_select3:1
P1.7	ctb0.oa1.inp_alt	tcpwm.line_compl[7]:1				
P2.0	sarmux.0	tcpwm.line[4]:1			scb[1].i2c_scl:1	scb[1].spi_mosi:2
P2.1	sarmux.1	tcpwm.line_compl[4]:1			scb[1].i2c_sda:1	scb[1].spi_miso:2
P2.2	sarmux.2	tcpwm.line[5]:1				scb[1].spi_clk:2
P2.3	sarmux.3	tcpwm.line_compl[5]:1				scb[1].spi_select0:2
P2.4	sarmux.4	tcpwm.line[0]:1				scb[1].spi_select1:1
P2.5	sarmux.5	tcpwm.line_compl[0]:1				scb[1].spi_select2:1
P2.6	sarmux.6	tcpwm.line[1]:1				scb[1].spi_select3:1
P2.7	sarmux.7	tcpwm.line_compl[1]:1				scb[3].spi_select0:1

Table 4. GPIO DC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID65A	I_{IL_CTBM}	Input leakage current (absolute value) for CTBM pins	–	–	4	nA	Guaranteed by characterization
SID66	C_{IN}	Input capacitance	–	–	7	pF	
SID67	V_{HYSTTL}	Input hysteresis LVTTL	25	40	–	mV	$V_{DDD} \geq 2.7$ V
SID68	$V_{HYSCMOS}$	Input hysteresis CMOS	$0.05 \times V_{DDD}$	–	–	mV	
SID69	I_{DIODE}	Current through protection diode to V_{DD}/Vss	–	–	100	µA	Guaranteed by characterization
SID69A	I_{TOT_GPIO}	Maximum Total Source or Sink Chip Current	–	–	200	mA	Guaranteed by characterization

Table 5. GPIO AC Specifications

(Guaranteed by Characterization)[3]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID70	T_{RISEF}	Rise time in fast strong mode	2	–	12	ns	3.3 V V_{DDD}, Cload = 25 pF
SID71	T_{FALLF}	Fall time in fast strong mode	2	–	12	ns	3.3 V V_{DDD}, Cload = 25 pF
SID72	T_{RISES}	Rise time in slow strong mode	10	–	60	ns	3.3 V V_{DDD}, Cload = 25 pF
SID73	T_{FALLS}	Fall time in slow strong mode	10	–	60	ns	3.3 V V_{DDD}, Cload = 25 pF
SID74	$F_{GPIOUT1}$	GPIO Fout;3.3 V ≤ V_{DDD} ≤ 5.5 V. Fast strong mode.	–	–	24	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID75	$F_{GPIOUT2}$	GPIO Fout;1.7 V≤ V_{DDD}≤ 3.3 V. Fast strong mode.	–	–	16.7	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID76	$F_{GPIOUT3}$	GPIO Fout;3.3 V ≤ V_{DDD} ≤ 5.5 V. Slow strong mode.	–	–	7	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID245	$F_{GPIOUT4}$	GPIO Fout;1.7 V ≤ V_{DDD} ≤ 3.3 V. Slow strong mode.	–	–	3.5	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID246	F_{GPIOIN}	GPIO input operating frequency; 1.71 V ≤ V_{DDD} ≤ 5.5 V	–	–	48	MHz	90/10% V_{IO}

Note

[3] Simultaneous switching transitions on many fully-loaded GPIO pins may cause ground perturbations depending on several factors including PCB and decoupling capacitor design. For applications that are very sensitive to ground perturbations, the slower GPIO slew rate setting may be used.

XRES

Table 6. XRES DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID77	V_{IH}	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS Input
SID78	V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DDD}	V	CMOS Input
SID79	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID80	C_{IN}	Input capacitance	–	3	–	pF	
SID81	$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	Guaranteed by characterization
SID82	I_{DIODE}	Current through protection diode to V_{DDD}/V_{SS}	–	–	100	µA	Guaranteed by characterization

Table 7. XRES AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID83	$T_{RESETWIDTH}$	Reset pulse width	1	–	–	µs	Guaranteed by characterization

Analog Peripherals

Opamp

Table 8. Opamp Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
	I_{DD}	Opamp block current. No load.	–	–	–	–	
SID269	I_{DD_HI}	Power = high	–	1100	1850	µA	
SID270	I_{DD_MED}	Power = medium	–	550	950	µA	
SID271	I_{DD_LOW}	Power = low	–	150	350	µA	
	GBW	Load = 20 pF, 0.1 mA. V_{DDA} = 2.7 V	–	–	–	–	
SID272	GBW_HI	Power = high	6	–	–	MHz	
SID273	GBW_MED	Power = medium	4	–	–	MHz	
SID274	GBW_LO	Power = low	–	1	–	MHz	
	I_{OUT_MAX}	$V_{DDA} \geq 2.7$ V, 500 mV from rail	–	–	–	–	
SID275	$I_{OUT\_MAX\_HI}$	Power = high	10	–	–	mA	
SID276	$I_{OUT\_MAX\_MID}$	Power = medium	10	–	–	mA	
SID277	$I_{OUT\_MAX\_LO}$	Power = low	–	5	–	mA	
	I_{OUT}	V_{DDA} = 1.71 V, 500 mV from rail	–	–	–	–	
SID278	$I_{OUT\_MAX\_HI}$	Power = high	4	–	–	mA	
SID279	$I_{OUT\_MAX\_MID}$	Power = medium	4	–	–	mA	
SID280	$I_{OUT\_MAX\_LO}$	Power = low	–	2	–	mA	
SID281	V_{IN}	Input voltage range	–0.05	–	VDDA – 0.2	V	Charge-pump on, $V_{DDA} \geq 2.7$ V
SID282	V_{CM}	Input common mode voltage	–0.05	–	VDDA – 0.2	V	Charge-pump on, $V_{DDA} \geq 2.7$ V
	V_{OUT}	$V_{DDA} \geq 2.7$ V	–	–	–		
SID283	V_{OUT_1}	Power = high, Iload=10 mA	0.5	–	VDDA – 0.5	V	
SID284	V_{OUT_2}	Power = high, Iload=1 mA	0.2	–	VDDA – 0.2	V	
SID285	V_{OUT_3}	Power = medium, Iload=1 mA	0.2	–	VDDA – 0.2	V	
SID286	V_{OUT_4}	Power = low, Iload=0.1 mA	0.2	–	VDDA – 0.2	V	
SID288	V_{OS_TR}	Offset voltage, trimmed	1	±0.5	1	mV	High mode
SID288A	V_{OS_TR}	Offset voltage, trimmed	–	±1	–	mV	Medium mode
SID288B	V_{OS_TR}	Offset voltage, trimmed	–	±2	–	mV	Low mode
SID290	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–10	±3	10	µV/°C	High mode. $T_A \leq 85$ °C.
SID290Q	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	15	±3	15	µV/°C	High mode. $T_A \leq 105$ °C
SID290A	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	µV/°C	Medium mode
SID290B	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	µV/°C	Low mode
SID291	CMRR	DC Common mode rejection ratio. High-power mode. Common Model voltage range from 0.5 V to VDDA - 0.5 V.	60	70	–	dB	V_{DDD} = 3.6 V
SID292	PSRR	At 1 kHz, 100-mV ripple	70	85	–	dB	V_{DDD} = 3.6 V
	Noise		–	–	–	–	

Table 8. Opamp Specifications

(Guaranteed by Characterization) *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID_DS_18	VOS_LOW_M2	Mode 2, Low current	–	5	–	mV	With trim 25 °C, 0.2 V to V_{DDA}-1.5 V
SID_DS_19	IOUT_HI_M1	Mode 1, High current	–	10	–	mA	Output is 0.5 V to VDDA-0.5 V
SID_DS_20	IOUT_MED_M1	Mode 1, Medium current	–	10	–	mA	Output is 0.5 V to VDDA-0.5 V
SID_DS_21	IOUT_LOW_M1	Mode 1, Low current	–	4	–	mA	Output is 0.5 V to VDDA-0.5 V
SID_DS_22	IOUT_HI_M2	Mode 2, High current	–	1	–	mA	Output is 0.5 V to V_{DDA}-0.5 V
SID_DS_23	IOUT_MED_M2	Mode 2, Medium current	–	1	–	mA	Output is 0.5 V to V_{DDA}-0.5 V
SID_DS_24	IOUT_LOW_M2	Mode 2, Low current	–	0.5	–	mA	Output is 0.5 V to V_{DDA}-0.5 V

Comparator

Table 9. Comparator DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID85	$V_{OFFSET2}$	Input offset voltage, Common Mode voltage range from 0 to V_{DD}-1	–	–	±4	mV	
SID85A	$V_{OFFSET3}$	Input offset voltage. Ultra low-power mode ($V_{DDD} \geq 2.2$ V for Temp < 0 °C, $V_{DDD} \geq 1.8$ V for Temp > 0 °C).	–	±12	–	mV	
SID86	V_{HYST}	Hysteresis when enabled, Common Mode voltage range from 0 to V_{DD} -1.	–	10	35	mV	Guaranteed by characterization
SID87	V_{ICM1}	Input common mode voltage in normal mode	0	–	$V_{DDD} - 0.1$	V	Modes 1 and 2.
SID247	V_{ICM2}	Input common mode voltage in low power mode	0	–	V_{DDD}	V	
SID247A	V_{ICM3}	Input common mode voltage in ultra low power mode ($V_{DDD} \geq 2.2$ V for Temp < 0 °C, $V_{DDD} \geq 1.8$ V for Temp > 0 °C)	0	–	V_{DDD} – 1.15	V	
SID88	CMRR	Common mode rejection ratio	50	–	–	dB	$V_{DDD} \geq 2.7$ V. Guaranteed by characterization
SID88A	CMRR	Common mode rejection ratio	42	–	–	dB	$V_{DDD} < 2.7$ V. Guaranteed by characterization
SID89	I_{CMP1}	Block current, normal mode	–	–	400	µA	Guaranteed by characterization
SID248	I_{CMP2}	Block current, low power mode	–	–	100	µA	Guaranteed by characterization
SID259	I_{CMP3}	Block current, ultra low power mode ($V_{DDD} \geq 2.2$ V for Temp < 0 °C, V_{DDD} ≥ 1.8 V for Temp > 0 °C)	–	6	28	µA	Guaranteed by characterization
SID90	Z_{CMP}	DC input impedance of comparator	35	–	–	MΩ	Guaranteed by characterization

Table 10. Comparator AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID91	T_{RESP1}	Response time, normal mode	–	–	110	ns	50-mV overdrive
SID258	T_{RESP2}	Response time, low power mode	–	–	200	ns	50-mV overdrive
SID92	T_{RESP3}	Response time, ultra low power mode (V_{DDD} ≥ 2.2 V for Temp < 0 °C, V_{DDD} ≥ 1.8 V for Temp > 0 °C)	–	–	15	µs	200-mV overdrive

Temperature Sensor

Table 11. Temperature Sensor Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID93	$T_{SENSACC}$	Temperature sensor accuracy	–5	±1	+5	°C	–40 to +85 °C

SAR ADC

Table 12. SAR ADC DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID94	A_RES	Resolution	–	–	12	bits	
SID95	A_CHNIS_S	Number of channels - single ended	–	–	16		8 full speed
SID96	A-CHNKS_D	Number of channels - differential	–	–	8		Diff inputs use neighboring I/O
SID97	A-MONO	Monotonicity	–	–	–		Yes. Based on characterization
SID98	A_GAINERR	Gain error	–	–	±0.1	%	With external reference.
SID99	A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V $V_{REF.}$
SID100	A_ISAR	Current consumption	–	–	1	mA	
SID101	A_VINS	Input voltage range - single ended	V_{SS}	–	V_{DDA}	V	Based on device characterization
SID102	A_VIND	Input voltage range - differential	V_{SS}	–	V_{DDA}	V	Based on device characterization
SID103	A_INRES	Input resistance	–	–	2.2	KΩ	Based on device characterization
SID104	A_INCAP	Input capacitance	–	–	10	pF	Based on device characterization

Table 13. SAR ADC AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID106	A_PSRR	Power supply rejection ratio	70	–	–	dB	
SID107	A_CMRR	Common mode rejection ratio	66	–	–	dB	Measured at 1 V
SID108	A_SAMP_1	Sample rate with external reference bypass cap	–	–	806	ksps	

Table 13. SAR ADC AC Specifications

(Guaranteed by Characterization) *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID108A	A_SAMP_2	Sample rate with no bypass cap. Reference = V_{DD}	–	–	500	ksps	
SID108B	A_SAMP_3	Sample rate with no bypass cap. Internal reference	–	–	100	ksps	
SID109	A_SNDR	Signal-to-noise and distortion ratio (SINAD)	66	–	–	dB	F_{IN} = 10 kHz
SID111	A_INL	Integral non linearity	–1.4	–	+1.4	LSB	V_{DD} = 1.71 to 5.5, 806 Ksps, Vref = 1 to 5.5.
SID111A	A_INL	Integral non linearity	–1.4	–	+1.4	LSB	V_{DDD} = 1.71 to 3.6, 806 Ksps, Vref = 1.71 to V_{DDD}.
SID111B	A_INL	Integral non linearity	–1.4	–	+1.4	LSB	V_{DDD} = 1.71 to 5.5, 500 Ksps, Vref = 1 to 5.5.
SID112	A_DNL	Differential non linearity	–0.9	–	+1.35	LSB	V_{DDD} = 1.71 to 5.5, 806 Ksps, Vref = 1 to 5.5.
SID112A	A_DNL	Differential non linearity	–0.9	–	+1.35	LSB	V_{DDD} = 1.71 to 3.6, 806 Ksps, Vref = 1.71 to V_{DDD}.
SID112B	A_DNL	Differential non linearity	–0.9	–	+1.35	LSB	V_{DDD} = 1.71 to 5.5, 500 Ksps, Vref = 1 to 5.5.
SID113	A_THD	Total harmonic distortion	–	–	–65	dB	F_{IN} = 10 kHz.

CSD

Table 14. CSD Block Specification

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
CSD Specification							
SID308	VCSD	Voltage range of operation	1.71	–	5.5	V	
SID309	IDAC1	DNL for 8-bit resolution	–1	–	1	LSB	
SID310	IDAC1	INL for 8-bit resolution	–3	–	3	LSB	
SID311	IDAC2	DNL for 7-bit resolution	–1	–	1	LSB	
SID312	IDAC2	INL for 7-bit resolution	–3	–	3	LSB	
SID313	SNR	Ratio of counts of finger to noise. Guaranteed by characterization	5	–	–	Ratio	Capacitance range of 9 to 35 pF, 0.1 pF sensitivity
SID314	IDAC1_CRT1	Output current of Idac1 (8-bits) in High range	–	612	–	µA	
SID314A	IDAC1_CRT2	Output current of Idac1(8-bits) in Low range	–	306	–	µA	
SID315	IDAC2_CRT1	Output current of Idac2 (7-bits) in High range	–	304.8	–	µA	
SID315A	IDAC2_CRT2	Output current of Idac2 (7-bits) in Low range	–	152.4	–	µA	

Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripheral in timer mode.

Timer/Counter/PWM

Table 15. TCPWM Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.1	ITCPWM1	Block current consumption at 3 MHz	–	–	45	µA	All modes (Timer/Counter/PWM)
SID.TCPWM.2	ITCPWM2	Block current consumption at 12 MHz	–	–	155	µA	All modes (Timer/Counter/PWM)
SID.TCPWM.2A	ITCPWM3	Block current consumption at 48 MHz	–	–	650	µA	All modes (Timer/Counter/PWM)
SID.TCPWM.3	TCPWMFREQ	Operating frequency	–	–	Fc	MHz	Fc max = Fcpu. Maximum = 24 MHz
SID.TCPWM.4	TPWMENEXT	Input Trigger Pulse Width for all Trigger Events	2/Fc	–	–	ns	Trigger Events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.
SID.TCPWM.5	TPWMEXT	Output Trigger Pulse widths	2/Fc	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) trigger outputs
SID.TCPWM.5A	TCRES	Resolution of Counter	1/Fc	–	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWMRES	PWM Resolution	1/Fc	–	–	ns	Minimum pulse width of PWM Output
SID.TCPWM.5C	QRES	Quadrature inputs resolution	1/Fc	–	–	ns	Minimum pulse width between Quadrature phase inputs.

I^{2}C

Table 16. Fixed I^{2}C DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	–	50	µA	
SID150	I_{I2C2}	Block current consumption at 400 kHz	–	–	135	µA	
SID151	I_{I2C3}	Block current consumption at 1 Mbps	–	–	310	µA	
SID152	I_{I2C4}	I^{2}C enabled in Deep Sleep mode	–	–	1.4	µA	

Table 17. Fixed I^{2}C AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID153	F_{I2C1}	Bit rate	–	–	1	Mbps	

LCD Direct Drive

Table 18. LCD Direct Drive DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID154	I_{LCDLOW}	Operating current in low power mode	–	5	–	µA	16 × 4 small segment disp. at 50 Hz
SID155	C_{LCDCAP}	LCD capacitance per segment/common driver	–	500	5000	pF	Guaranteed by Design
SID156	LCD_{OFFSET}	Long-term segment offset	–	20	–	mV	
SID157	I_{LCDOP1}	PWM Mode current. 5-V bias. 24-MHz IMO	–	0.6	–	mA	32 × 4 segments. 50 Hz, 25 °C
SID158	I_{LCDOP2}	PWM Mode current. 3.3-V bias. 24-MHz IMO.	–	0.5	–	mA	32 × 4 segments. 50 Hz, 25 °C

Table 19. LCD Direct Drive AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID159	F_{LCD}	LCD frame rate	10	50	150	Hz	

Table 20. Fixed UART DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID160	I_{UART1}	Block current consumption at 100 Kbits/sec	–	–	55	µA	
SID161	I_{UART2}	Block current consumption at 1000 Kbits/sec	–	–	312	µA	

Table 21. Fixed UART AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID162	F_{UART}	Bit rate	–	–	1	Mbps	

SPI Specifications

Table 22. Fixed SPI DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID163	I_{SPI1}	Block current consumption at 1 Mbits/sec	–	–	360	µA	
SID164	I_{SPI2}	Block current consumption at 4 Mbits/sec	–	–	560	µA	
SID165	I_{SPI3}	Block current consumption at 8 Mbits/sec	–	–	600	µA	

Table 23. Fixed SPI AC Specifications

(Guaranteed by Characterization)

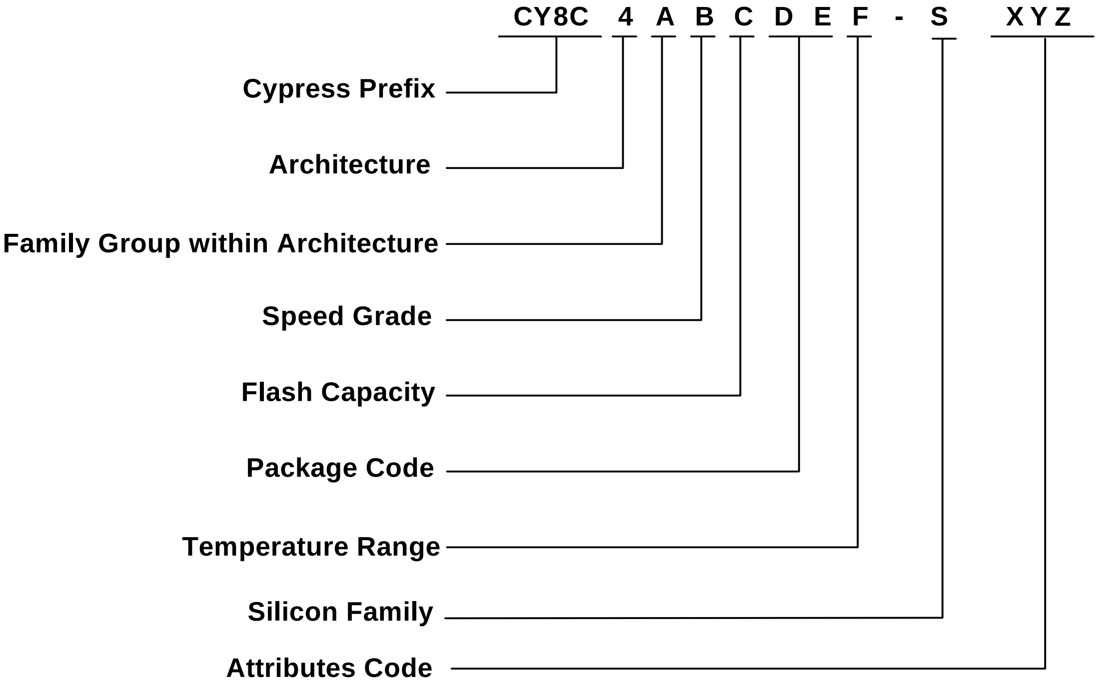
Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID166	F_{SPI}	SPI operating frequency (master; 6X oversampling)	–	–	8	MHz	

The nomenclature used in the preceding table is based on the following part numbering convention:

Field	Description	Values	Meaning
CY8C	Cypress Prefix		
4	Architecture	4	PSoC 4
A	Family	1	4100 Family
B	CPU Speed	4	48 MHz
C	Flash Capacity	4	16 KB
		5	32 KB
		6	64 KB
		7	128 KB
DE	Package Code	AX, AZ	TQFP
		LQ	QFN
		BU	BGA
		FD	CSP
F	Temperature Range	I	Industrial
		Q	Extended Industrial
S	Silicon Family	N/A	PSoC 4 Base Series
		L	PSoC 4 L-Series
		BL	PSoC 4 BLE
		M	PSoC 4 M-Series
XYZ	Attributes Code	000-999	Code of feature set in the specific family

Part Numbering Conventions

The part number fields are defined as follows.



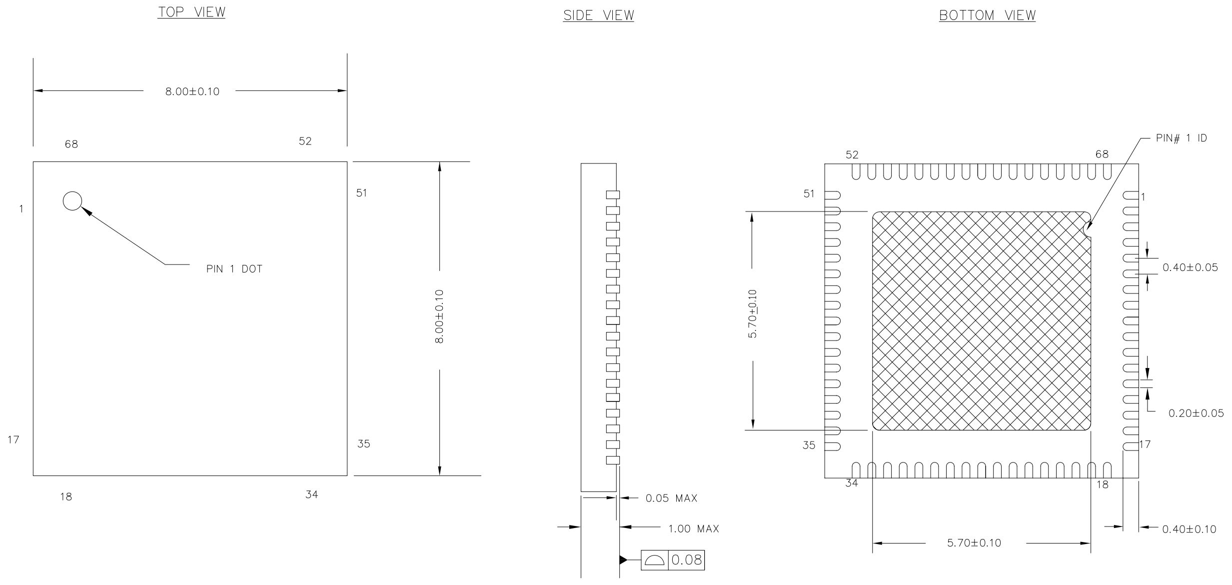
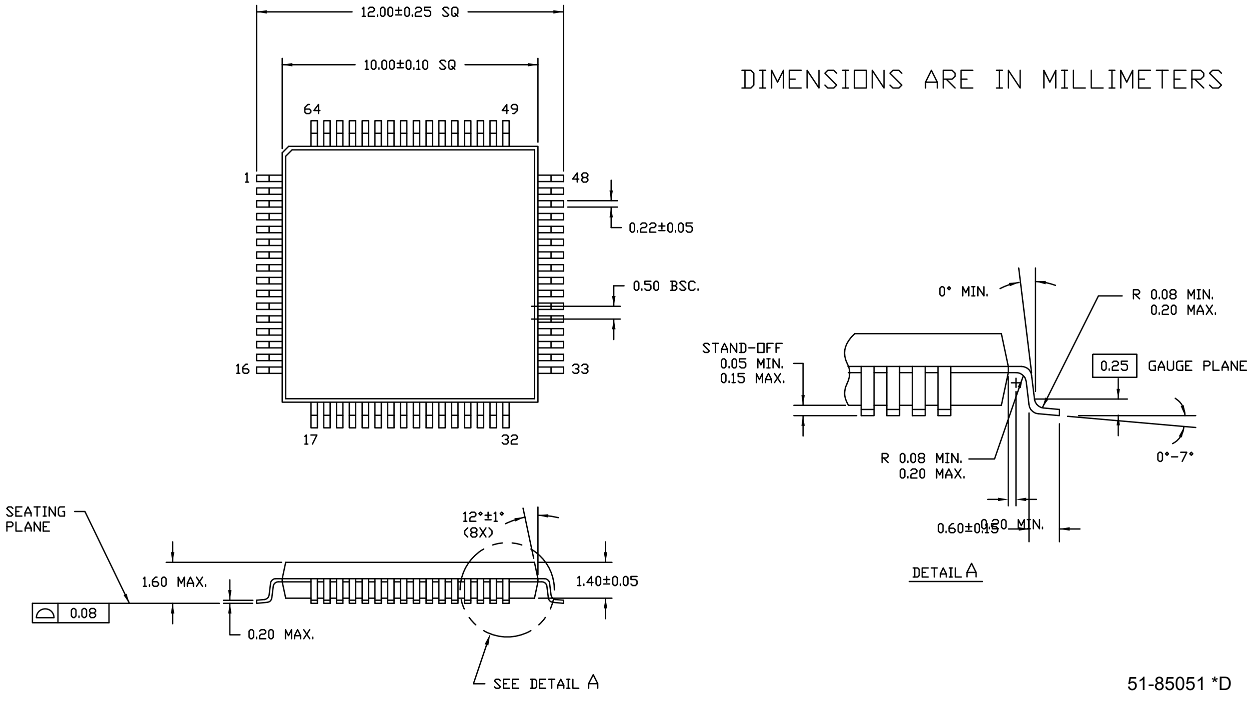


Figure 5. 68-Pin 8 × 8 × 1.0 mm QFN Package Outline

NOTES:

1. ▨ HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 17 ± 2mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-09618 *E



DIMENSIONS ARE IN MILLIMETERS

Figure 6. 64-Pin 10 × 10 × 1.4 mm TQFP Package Outline

51-85051 *D

Acronyms

Table 43. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
ARM®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I^{2}C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD
PC	program counter
PCB	printed circuit board

Document Conventions

Units of Measure

Table 44. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

Revision History

Description Title: PSoC® 4: PSoC 4100M Family Datasheet Programmable System-on-Chip (PSoC®)
Document Number: 001-96519

Revision	ECN	Orig. of Change	Submission Date	Description of Change
*A	4765455	WKA	05/20/2015	Release to web.
*B	4815539	WKA	06/29/2015	Removed note regarding hardware handshaking in the UART Mode section. Changed max value of SID51A to 2 ms. Added “Guaranteed by characterization” note for SID65 and SID65A Updated Ordering Information.
*C	4941619	WKA	09/30/2015	Updated CapSense section. Updated the note at the end of the Pinout table. Removed Conditions for spec SID237.
*D	5026805	WKA	11/26/2015	Added Comparator ULP mode range restrictions and corrected typos.
*E	5408936	WKA	08/19/2016	Added extended industrial temperature range. Added specs SID290Q, SID182A, and SID299A. Updated conditions for SID290, SID223, and SID237. Added 44-pin TQFP package details. Updated Ordering Information

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