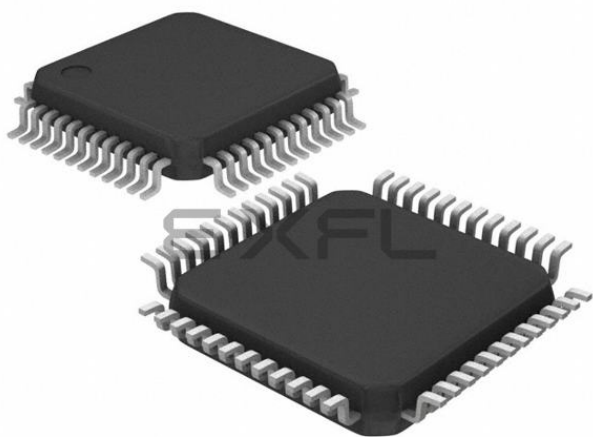




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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I ² C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, CapSense, LCD, LVD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b SAR; 2xIDAC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4125azi-m433

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article [KBA86521, How to Design with PSoC 3, PSoC 4, and PSoC 5LP](#). Following is an abbreviated list for PSoC 4:

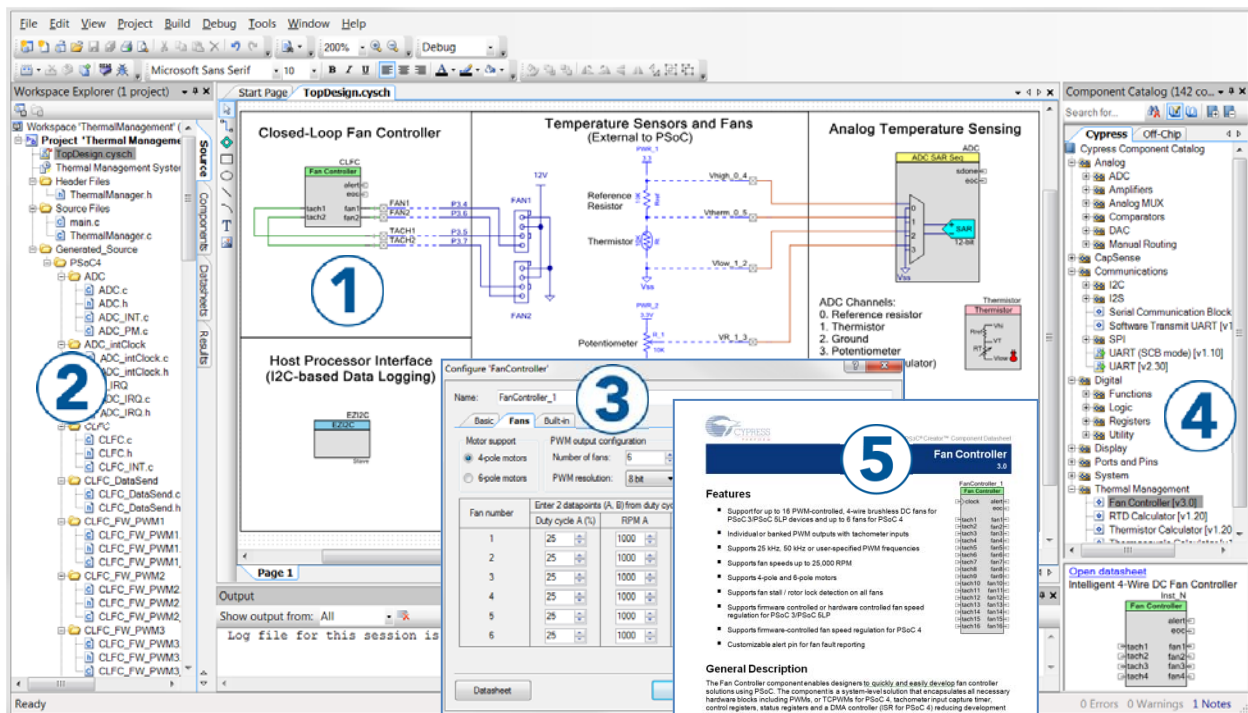
- Overview: [PSoC Portfolio](#), [PSoC Roadmap](#)
 - Product Selectors: [PSoC 1](#), [PSoC 3](#), [PSoC 4](#), [PSoC 5LP](#)
In addition, PSoC Creator includes a device selection tool.
 - Application notes: Cypress offers a large number of PSoC application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 4 are:
 - [AN79953](#): Getting Started With PSoC 4
 - [AN88619](#): PSoC 4 Hardware Design Considerations
 - [AN86439](#): Using PSoC 4 GPIO Pins
 - [AN57821](#): Mixed Signal Circuit Board Layout
 - [AN81623](#): Digital Design Best Practices
 - [AN73854](#): Introduction To Bootloaders
 - [AN89610](#): ARM Cortex Code Optimization
 - Technical Reference Manual (TRM) is in two documents:
 - [Architecture TRM](#) details each PSoC 4 functional block.
 - [Registers TRM](#) describes each of the PSoC 4 registers.
 - Development Kits:
 - [CY8CKIT-042](#), PSoC 4 Pioneer Kit, is an easy-to-use and inexpensive development platform. This kit includes connectors for Arduino™ compatible shields and Digilent® Pmod™ daughter cards.
 - [CY8CKIT-049](#) is a very low-cost prototyping platform. It is a low-cost alternative to sampling PSoC 4 devices.
 - [CY8CKIT-001](#) is a common development platform for any one of the PSoC 1, PSoC 3, PSoC 4, or PSoC 5LP families of devices.
- The [MiniProg3](#) device provides an interface for flash programming and debug.

PSoC Creator

PSoC Creator is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC 3, PSoC 4, and PSoC 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC Components; see the [list of component datasheets](#). With PSoC Creator, you can:

1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

Figure 1. Multiple-Sensor Example Project in PSoC Creator



Contents

PSoC 4100M Block Diagram	4	Analog Peripherals	19
Functional Definition	5	Digital Peripherals	24
CPU and Memory Subsystem	5	Memory	26
System Resources	5	System Resources	27
Analog Blocks.....	6	Ordering Information	30
Fixed Function Digital	7	Part Numbering Conventions	31
GPIO	8	Packaging	32
Special Function Peripherals.....	8	Acronyms	35
Pinouts	9	Document Conventions	37
Power	13	Units of Measure	37
Unregulated External Supply.....	13	Revision History	38
Regulated External Supply	13	Sales, Solutions, and Legal Information	39
Development Support	14	Worldwide Sales and Design Support.....	39
Documentation	14	Products	39
Online	14	PSoC® Solutions	39
Tools.....	14	Cypress Developer Community.....	39
Electrical Specifications	15	Technical Support	39
Absolute Maximum Ratings.....	15		
Device Level Specifications.....	15		

Watchdog Timer

A watchdog timer is implemented in the clock block running from the low-frequency clock; this allows watchdog operation during Deep Sleep and generates a watchdog reset or an interrupt if not serviced before the timeout occurs. The watchdog reset is recorded in the Reset Cause register.

Reset

The PSoC 4100M can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset to avoid complications with configuration and multiple pin functions during power-on or reconfiguration.

Voltage Reference

The PSoC 4100M reference system generates all internally required references. A 1% voltage reference spec is provided for the 12-bit ADC. To allow better signal-to-noise ratios (SNR) and better absolute accuracy, it is possible to add an external bypass capacitor to the internal reference using a GPIO pin or to use an external reference for the SAR.

Analog Blocks

12-bit SAR ADC

The 12-bit SAR ADC can operate at a maximum sample rate of 806 Ksamples/second.

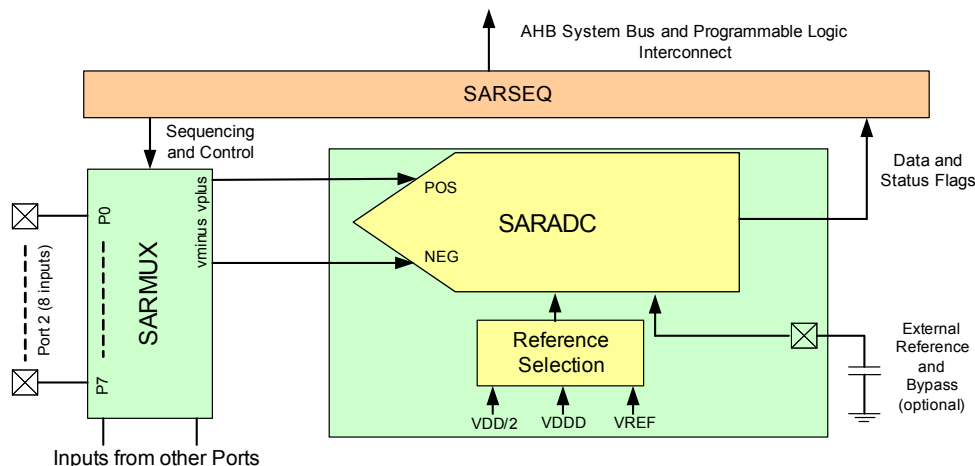
The block functionality is augmented for the user by adding a reference buffer to it (trimmable to $\pm 1\%$) and by providing the choice of three internal voltage references: V_{DD} , $V_{DD}/2$, and

V_{REF} (nominally 1.024 V) as well as an external reference through a GPIO pin. The Sample-and-Hold (S/H) aperture is programmable allowing the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. The system performance will be 65 dB for true 12-bit precision if appropriate references are used and system noise levels permit. To improve performance in noisy conditions, it is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer (expandable to 16 inputs). The sequencer cycles through selected channels autonomously (sequencer scan) and does so with zero switching overhead (that is, the aggregate sampling bandwidth is equal to 1 Msps, whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware-driven switching. A feature provided by the sequencer is buffering of each channel to reduce CPU interrupt service requirements. To accommodate signals with varying source impedance and frequency, it is possible to have different sample times programmable for each channel. In addition, the signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without the necessity of having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is able to digitize the output of the on-board temperature sensor for calibration and other temperature-dependent functions. The SAR is not available in Deep Sleep and Hibernate modes as it requires a high-speed clock. The SAR operating range is 1.71 to 5.5 V.

Figure 3. SAR ADC System Diagram



Pinouts

The following is the pin list for the PSoC 4100M. This shows the power supply and port pins (for example, P0.0 is Pin 0 of Port 0).

68-QFN		64-TQFP		48-TQFP		44-TQFP	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
42	P0.0	39	P0.0	28	P0.0	24	P0.0
43	P0.1	40	P0.1	29	P0.1	25	P0.1
44	P0.2	41	P0.2	30	P0.2	26	P0.2
45	P0.3	42	P0.3	31	P0.3	27	P0.3
46	P0.4	43	P0.4	32	P0.4	28	P0.4
47	P0.5	44	P0.5	33	P0.5	29	P0.5
48	P0.6	45	P0.6	34	P0.6	30	P0.6
49	P0.7	46	P0.7	35	P0.7	31	P0.7
50	XRES	47	XRES	36	XRES	32	XRES
51	VCCD	48	VCCD	37	VCCD	33	VCCD
52	VSSD	49	VSSD	38	VSSD	DN	VSSD
53	VDDD	50	VDDD	39	VDDD	34	VDDD
				40	VDDA	35	VDDA
54	P5.0	51	P5.0				
55	P5.1	52	P5.1				
56	P5.2	53	P5.2				
57	P5.3	54	P5.3				
58	P5.4						
59	P5.5	55	P5.5				
60	VDDA	56	VDDA	40	VDDA	35	VDDA
61	VSSA	57	VSSA	41	VSSA	36	VSSA
62	P1.0	58	P1.0	42	P1.0	37	P1.0
63	P1.1	59	P1.1	43	P1.1	38	P1.1
64	P1.2	60	P1.2	44	P1.2	39	P1.2
65	P1.3	61	P1.3	45	P1.3	40	P1.3
66	P1.4	62	P1.4	46	P1.4	41	P1.4
67	P1.5	63	P1.5	47	P1.5	42	P1.5
68	P1.6	64	P1.6	48	P1.6	43	P1.6
1	P1.7/VREF	1	P1.7/VREF	1	P1.7/VREF	44	P1.7/VREF
						1	VSSD
2	P2.0	2	P2.0	2	P2.0	2	P2.0
3	P2.1	3	P2.1	3	P2.1	3	P2.1
4	P2.2	4	P2.2	4	P2.2	4	P2.2
5	P2.3	5	P2.3	5	P2.3	5	P2.3
6	P2.4	6	P2.4	6	P2.4	6	P2.4
7	P2.5	7	P2.5	7	P2.5	7	P2.5

Each of the pins shown in the previous table can have multiple programmable functions as shown in the following table. Column headings refer to Analog and Alternate pin functions:

Port/Pin	Analog	Alt. Function 1	Alt. Function 2	Alt. Function 3	Alt. Function 4	Alt. Function 5
P0.0	lpcomp.in_p[0]					scb[0].spi_select1:0
P0.1	lpcomp.in_n[0]					scb[0].spi_select2:0
P0.2	lpcomp.in_p[1]					scb[0].spi_select3:0
P0.3	lpcomp.in_n[1]					
P0.4	wco_in		scb[1].uart_rx:0		scb[1].i2c_scl:0	scb[1].spi_mosi:1
P0.5	wco_out		scb[1].uart_tx:0		scb[1].i2c_sda:0	scb[1].spi_miso:1
P0.6		ext_clk:0	scb[1].uart_cts:0			scb[1].spi_clk:1
P0.7			scb[1].uart_rts:0		wakeup	scb[1].spi_select0:1
P5.0	ctb1.oa0.inp	tcpwm.line[4]:2	scb[2].uart_rx:0		scb[2].i2c_scl:0	scb[2].spi_mosi:0
P5.1	ctb1.oa0.inm	tcpwm.line_compl[4]:2	scb[2].uart_tx:0		scb[2].i2c_sda:0	scb[2].spi_miso:0
P5.2	ctb1.oa0.out	tcpwm.line[5]:2	scb[2].uart_cts:0		lpcomp.comp[0]:1	scb[2].spi_clk:0
P5.3	ctb1.oa1.out	tcpwm.line_compl[5]:2	scb[2].uart_rts:0		lpcomp.comp[1]:1	scb[2].spi_select0:0
P5.4	ctb1.oa1.inm	tcpwm.line[6]:2				scb[2].spi_select1:0
P5.5	ctb1.oa1.inp	tcpwm.line_compl[6]:2				scb[2].spi_select2:0
P5.6	ctb1.oa0.inp_alt	tcpwm.line[7]:0				scb[2].spi_select3:0
P5.7	ctb1.oa1.inp_alt	tcpwm.line_compl[7]:0				
P1.0	ctb0.oa0.inp	tcpwm.line[2]:1	scb[0].uart_rx:1		scb[0].i2c_scl:0	scb[0].spi_mosi:1
P1.1	ctb0.oa0.inm	tcpwm.line_compl[2]:1	scb[0].uart_tx:1		scb[0].i2c_sda:0	scb[0].spi_miso:1
P1.2	ctb0.oa0.out	tcpwm.line[3]:1	scb[0].uart_cts:1			scb[0].spi_clk:1
P1.3	ctb0.oa1.out	tcpwm.line_compl[3]:1	scb[0].uart_rts:1			scb[0].spi_select0:1
P1.4	ctb0.oa1.inm	tcpwm.line[6]:1				scb[0].spi_select1:1
P1.5	ctb0.oa1.inp	tcpwm.line_compl[6]:1				scb[0].spi_select2:1
P1.6	ctb0.oa0.inp_alt	tcpwm.line[7]:1				scb[0].spi_select3:1
P1.7	ctb0.oa1.inp_alt	tcpwm.line_compl[7]:1				
P2.0	sarmux.0	tcpwm.line[4]:1			scb[1].i2c_scl:1	scb[1].spi_mosi:2
P2.1	sarmux.1	tcpwm.line_compl[4]:1			scb[1].i2c_sda:1	scb[1].spi_miso:2
P2.2	sarmux.2	tcpwm.line[5]:1				scb[1].spi_clk:2
P2.3	sarmux.3	tcpwm.line_compl[5]:1				scb[1].spi_select0:2
P2.4	sarmux.4	tcpwm.line[0]:1				scb[1].spi_select1:1
P2.5	sarmux.5	tcpwm.line_compl[0]:1				scb[1].spi_select2:1
P2.6	sarmux.6	tcpwm.line[1]:1				scb[1].spi_select3:1
P2.7	sarmux.7	tcpwm.line_compl[1]:1				scb[3].spi_select0:1

Port/Pin	Analog	Alt. Function 1	Alt. Function 2	Alt. Function 3	Alt. Function 4	Alt. Function 5
P6.0		tcpwm.line[4]:0	scb[3].uart_rx:0		scb[3].i2c_scl:0	scb[3].spi_mosi:0
P6.1		tcpwm.line_compl[4]:0	scb[3].uart_tx:0		scb[3].i2c_sda:0	scb[3].spi_miso:0
P6.2		tcpwm.line[5]:0	scb[3].uart_cts:0			scb[3].spi_clk:0
P6.3		tcpwm.line_compl[5]:0	scb[3].uart_rts:0			scb[3].spi_select0:0
P6.4		tcpwm.line[6]:0				scb[3].spi_select1:0
P6.5		tcpwm.line_compl[6]:0				scb[3].spi_select2:0
P3.0		tcpwm.line[0]:0	scb[1].uart_rx:1		scb[1].i2c_scl:2	scb[1].spi_mosi:0
P3.1		tcpwm.line_compl[0]:0	scb[1].uart_tx:1		scb[1].i2c_sda:2	scb[1].spi_miso:0
P3.2		tcpwm.line[1]:0	scb[1].uart_cts:1		swd_data	scb[1].spi_clk:0
P3.3		tcpwm.line_compl[1]:0	scb[1].uart_rts:1		swd_clk	scb[1].spi_select0:0
P3.4		tcpwm.line[2]:0				scb[1].spi_select1:0
P3.5		tcpwm.line_compl[2]:0				scb[1].spi_select2:0
P3.6		tcpwm.line[3]:0				scb[1].spi_select3:0
P3.7		tcpwm.line_compl[3]:0				
P4.0			scb[0].uart_rx:0		scb[0].i2c_scl:1	scb[0].spi_mosi:0
P4.1			scb[0].uart_tx:0		scb[0].i2c_sda:1	scb[0].spi_miso:0
P4.2	csd[0].c_mod		scb[0].uart_cts:0		lpcomp.comp[0]:0	scb[0].spi_clk:0
P4.3	csd[0].c_sh_tank		scb[0].uart_rts:0		lpcomp.comp[1]:0	scb[0].spi_select0:0
P4.4						scb[0].spi_select1:2
P4.5						scb[0].spi_select2:2
P4.6						scb[0].spi_select3:2
P4.7						
P7.0		tcpwm.line[0]:2	scb[3].uart_rx:1		scb[3].i2c_scl:1	scb[3].spi_mosi:1
P7.1		tcpwm.line_compl[0]:2	scb[3].uart_tx:1		scb[3].i2c_sda:1	scb[3].spi_miso:1
P7.2		tcpwm.line[1]:2	scb[3].uart_cts:1			scb[3].spi_clk:1

Descriptions of the power pin functions are as follows:

VDDD: Power supply for both analog and digital sections (where there is no V_{DDA} pin).

VDDA: Analog V_{DD} pin where package pins allow; shorted to V_{DDD} otherwise.

VDDIO: I/O pin power domain.

VSSA: Analog ground pin where package pins allow; shorted to VSS otherwise

VSS: Ground pin.

VCCD: Regulated Digital supply (1.8 V $\pm$ 5%).

Port Pins can all be used as LCD Commons, LCD Segment drivers, or CSD sense and shield pins can be connected to AMUXBUS A or B or can all be used as GPIO pins that can be driven by firmware or DSI signals.

XRES

Table 6. XRES DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID77	V_{IH}	Input voltage high threshold	$0.7 \times V_{DD}$	–	–	V	CMOS Input
SID78	V_{IL}	Input voltage low threshold	–	–	$0.3 \times V_{DD}$	V	CMOS Input
SID79	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	k Ω	
SID80	C_{IN}	Input capacitance	–	3	–	pF	
SID81	$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	Guaranteed by characterization
SID82	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	μ A	Guaranteed by characterization

Table 7. XRES AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID83	$T_{RESETWIDTH}$	Reset pulse width	1	–	–	μ s	Guaranteed by characterization

Analog Peripherals

Opamp

Table 8. Opamp Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
	I _{DD}	Opamp block current. No load.	–	–	–	–	
SID269	I _{DD_HI}	Power = high	–	1100	1850	μA	
SID270	I _{DD_MED}	Power = medium	–	550	950	μA	
SID271	I _{DD_LOW}	Power = low	–	150	350	μA	
	GBW	Load = 20 pF, 0.1 mA. V _{DDA} = 2.7 V	–	–	–	–	
SID272	GBW_HI	Power = high	6	–	–	MHz	
SID273	GBW_MED	Power = medium	4	–	–	MHz	
SID274	GBW_LO	Power = low	–	1	–	MHz	
	I _{OUT_MAX}	V _{DDA} ≥ 2.7 V, 500 mV from rail	–	–	–	–	
SID275	I _{OUT_MAX_HI}	Power = high	10	–	–	mA	
SID276	I _{OUT_MAX_MID}	Power = medium	10	–	–	mA	
SID277	I _{OUT_MAX_LO}	Power = low	–	5	–	mA	
	I _{OUT}	V _{DDA} = 1.71 V, 500 mV from rail	–	–	–	–	
SID278	I _{OUT_MAX_HI}	Power = high	4	–	–	mA	
SID279	I _{OUT_MAX_MID}	Power = medium	4	–	–	mA	
SID280	I _{OUT_MAX_LO}	Power = low	–	2	–	mA	
SID281	V _{IN}	Input voltage range	–0.05	–	V _{DDA} – 0.2	V	Charge-pump on, V _{DDA} ≥ 2.7 V
SID282	V _{CM}	Input common mode voltage	–0.05	–	V _{DDA} – 0.2	V	Charge-pump on, V _{DDA} ≥ 2.7 V
	V _{OUT}	V _{DDA} ≥ 2.7 V	–	–	–	–	
SID283	V _{OUT_1}	Power = high, I _{load} =10 mA	0.5	–	V _{DDA} – 0.5	V	
SID284	V _{OUT_2}	Power = high, I _{load} =1 mA	0.2	–	V _{DDA} – 0.2	V	
SID285	V _{OUT_3}	Power = medium, I _{load} =1 mA	0.2	–	V _{DDA} – 0.2	V	
SID286	V _{OUT_4}	Power = low, I _{load} =0.1 mA	0.2	–	V _{DDA} – 0.2	V	
SID288	V _{OS_TR}	Offset voltage, trimmed	1	±0.5	1	mV	High mode
SID288A	V _{OS_TR}	Offset voltage, trimmed	–	±1	–	mV	Medium mode
SID288B	V _{OS_TR}	Offset voltage, trimmed	–	±2	–	mV	Low mode
SID290	V _{OS_DR_TR}	Offset voltage drift, trimmed	–10	±3	10	μV/°C	High mode. T _A ≤ 85 °C.
SID290Q	V _{OS_DR_TR}	Offset voltage drift, trimmed	15	±3	15	μV/°C	High mode. T _A ≤ 105 °C
SID290A	V _{OS_DR_TR}	Offset voltage drift, trimmed	–	±10	–	μV/°C	Medium mode
SID290B	V _{OS_DR_TR}	Offset voltage drift, trimmed	–	±10	–	μV/°C	Low mode
SID291	CMRR	DC Common mode rejection ratio. High-power mode. Common Mode voltage range from 0.5 V to V _{DDA} – 0.5 V.	60	70	–	dB	V _{DD} = 3.6 V
SID292	PSRR	At 1 kHz, 100-mV ripple	70	85	–	dB	V _{DD} = 3.6 V
	Noise		–	–	–	–	

Table 8. Opamp Specifications

(Guaranteed by Characterization) (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID293	V _{N1}	Input referred, 1 Hz - 1GHz, power = high	–	94	–	μVrms	
SID294	V _{N2}	Input referred, 1 kHz, power = high	–	72	–	nV/rtHz	
SID295	V _{N3}	Input referred, 10kHz, power = high	–	28	–	nV/rtHz	
SID296	V _{N4}	Input referred, 100kHz, power = high	–	15	–	nV/rtHz	
SID297	Cload	Stable up to maximum load. Performance specs at 50 pF.	–	–	125	pF	
SID298	Slew_rate	Cload = 50 pF, Power = High, V _{DDA} ≥ 2.7 V	6	–	–	V/μs	
SID299	T _{op_wake}	From disable to enable, no external RC dominating	–	25	–	μs	
SID299A	OL_GAIN	Open Loop Gain	–	90	–	dB	
	Comp_mode	Comparator mode; 50 mV drive, Trise = Tfall (approx.)	–	–	–		
SID300	T _{PD1}	Response time; power = high	–	150	–	ns	
SID301	T _{PD2}	Response time; power = medium	–	400	–	ns	
SID302	T _{PD3}	Response time; power = low	–	2000	–	ns	
SID303	V _{hyst_op}	Hysteresis	–	10	–	mV	
Deep Sleep Mode		Mode 2 is lowest current range. Mode 1 has higher GBW.					Deep Sleep mode. V _{DDA} ≥ 2.7 V.
SID_DS_1	IDD_HI_M1	Mode 1, High current	–	1400	–	uA	25 °C
SID_DS_2	IDD_MED_M1	Mode 1, Medium current	–	700	–	uA	25 °C
SID_DS_3	IDD_LOW_M1	Mode 1, Low current	–	200	–	uA	25 °C
SID_DS_4	IDD_HI_M2	Mode 2, High current	–	120	–	uA	25 °C
SID_DS_5	IDD_MED_M2	Mode 2, Medium current	–	60	–	uA	25 °C
SID_DS_6	IDD_LOW_M2	Mode 2, Low current	–	15	–	uA	25 °C
SID_DS_7	GBW_HI_M1	Mode 1, High current	–	4	–	MHz	25 °C
SID_DS_8	GBW_MED_M1	Mode 1, Medium current	–	2	–	MHz	25 °C
SID_DS_9	GBW_LOW_M1	Mode 1, Low current	–	0.5	–	MHz	25 °C
SID_DS_10	GBW_HI_M2	Mode 2, High current	–	0.5	–	MHz	20-pF load, no DC load 0.2 V to V _{DDA} -1.5 V
SID_DS_11	GBW_MED_M2	Mode 2, Medium current	–	0.2	–	MHz	20-pF load, no DC load 0.2 V to V _{DDA} -1.5 V
SID_DS_12	GBW_LOW_M2	Mode 2, Low current	–	0.1	–	MHz	20-pF load, no DC load 0.2 V to V _{DDA} -1.5 V
SID_DS_13	VOS_HI_M1	Mode 1, High current	–	5	–	mV	With trim 25 °C, 0.2 V to V _{DDA} -1.5 V
SID_DS_14	VOS_MED_M1	Mode 1, Medium current	–	5	–	mV	With trim 25 °C, 0.2 V to V _{DDA} -1.5 V
SID_DS_15	VOS_LOW_M1	Mode 1, Low current	–	5	–	mV	With trim 25 °C, 0.2 V to V _{DDA} -1.5 V
SID_DS_16	VOS_HI_M2	Mode 2, High current	–	5	–	mV	With trim 25 °C, 0.2 V to V _{DDA} -1.5 V
SID_DS_17	VOS_MED_M2	Mode 2, Medium current	–	5	–	mV	With trim 25 °C, 0.2 V to V _{DDA} -1.5 V

Table 8. Opamp Specifications

(Guaranteed by Characterization) (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID_DS_18	VOS_LOW_M2	Mode 2, Low current	–	5	–	mV	With trim 25 °C, 0.2 V to V _{DDA} -1.5 V
SID_DS_19	IOUT_HI_M1	Mode 1, High current	–	10	–	mA	Output is 0.5 V to V _{DDA} -0.5 V
SID_DS_20	IOUT_MED_M1	Mode 1, Medium current	–	10	–	mA	Output is 0.5 V to V _{DDA} -0.5 V
SID_DS_21	IOUT_LOW_M1	Mode 1, Low current	–	4	–	mA	Output is 0.5 V to V _{DDA} -0.5 V
SID_DS_22	IOUT_HI_M2	Mode 2, High current	–	1	–	mA	Output is 0.5 V to V _{DDA} -0.5 V
SID_DS_23	IOUT_MED_M2	Mode 2, Medium current	–	1	–	mA	Output is 0.5 V to V _{DDA} -0.5 V
SID_DS_24	IOUT_LOW_M2	Mode 2, Low current	–	0.5	–	mA	Output is 0.5 V to V _{DDA} -0.5 V

Comparator

Table 9. Comparator DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID85	V _{OFFSET2}	Input offset voltage, Common Mode voltage range from 0 to V _{DD} -1	–	–	±4	mV	
SID85A	V _{OFFSET3}	Input offset voltage. Ultra low-power mode (V _{DDD} ≥ 2.2 V for Temp < 0 °C, V _{DDD} ≥ 1.8 V for Temp > 0 °C).	–	±12	–	mV	
SID86	V _{HYST}	Hysteresis when enabled, Common Mode voltage range from 0 to V _{DD} -1.	–	10	35	mV	Guaranteed by characterization
SID87	V _{ICM1}	Input common mode voltage in normal mode	0	–	V _{DDD} -0.1	V	Modes 1 and 2.
SID247	V _{ICM2}	Input common mode voltage in low power mode	0	–	V _{DDD}	V	
SID247A	V _{ICM3}	Input common mode voltage in ultra low power mode (V _{DDD} ≥ 2.2 V for Temp < 0 °C, V _{DDD} ≥ 1.8 V for Temp > 0 °C)	0	–	V _{DDD} -1.15	V	
SID88	CMRR	Common mode rejection ratio	50	–	–	dB	V _{DDD} ≥ 2.7 V. Guaranteed by characterization
SID88A	CMRR	Common mode rejection ratio	42	–	–	dB	V _{DDD} < 2.7 V. Guaranteed by characterization
SID89	I _{CMP1}	Block current, normal mode	–	–	400	μA	Guaranteed by characterization
SID248	I _{CMP2}	Block current, low power mode	–	–	100	μA	Guaranteed by characterization
SID259	I _{CMP3}	Block current, ultra low power mode (V _{DDD} ≥ 2.2 V for Temp < 0 °C, V _{DDD} ≥ 1.8 V for Temp > 0 °C)	–	6	28	μA	Guaranteed by characterization
SID90	Z _{CMP}	DC input impedance of comparator	35	–	–	MΩ	Guaranteed by characterization

Table 10. Comparator AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID91	T _{RESP1}	Response time, normal mode	–	–	110	ns	50-mV overdrive
SID258	T _{RESP2}	Response time, low power mode	–	–	200	ns	50-mV overdrive
SID92	T _{RESP3}	Response time, ultra low power mode (V _{DDD} ≥ 2.2 V for Temp < 0 °C, V _{DDD} ≥ 1.8 V for Temp > 0 °C)	–	–	15	µs	200-mV overdrive

Temperature Sensor

Table 11. Temperature Sensor Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID93	T _{SENSACC}	Temperature sensor accuracy	–5	±1	+5	°C	–40 to +85 °C

SAR ADC

Table 12. SAR ADC DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID94	A_RES	Resolution	–	–	12	bits	
SID95	A_CHNIS_S	Number of channels - single ended	–	–	16		8 full speed
SID96	A-CHNKS_D	Number of channels - differential	–	–	8		Diff inputs use neighboring I/O
SID97	A-MONO	Monotonicity	–	–	–		Yes. Based on characterization
SID98	A_GAINERR	Gain error	–	–	±0.1	%	With external reference.
SID99	A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V V _{REF} .
SID100	A_ISAR	Current consumption	–	–	1	mA	
SID101	A_VINS	Input voltage range - single ended	V _{SS}	–	V _{DDA}	V	Based on device characterization
SID102	A_VIND	Input voltage range - differential	V _{SS}	–	V _{DDA}	V	Based on device characterization
SID103	A_INRES	Input resistance	–	–	2.2	KΩ	Based on device characterization
SID104	A_INCAP	Input capacitance	–	–	10	pF	Based on device characterization

Table 13. SAR ADC AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID106	A_PSR	Power supply rejection ratio	70	–	–	dB	
SID107	A_CMRR	Common mode rejection ratio	66	–	–	dB	Measured at 1 V
SID108	A_SAMP_1	Sample rate with external reference bypass cap	–	–	806	ksps	

Table 13. SAR ADC AC Specifications

(Guaranteed by Characterization) (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID108A	A_SAMP_2	Sample rate with no bypass cap. Reference = V_{DD}	–	–	500	ksps	
SID108B	A_SAMP_3	Sample rate with no bypass cap. Internal reference	–	–	100	ksps	
SID109	A_SNR	Signal-to-noise and distortion ratio (SINAD)	66	–	–	dB	$F_{IN} = 10 \text{ kHz}$
SID111	A_INL	Integral non linearity	–1.4	–	+1.4	LSB	$V_{DD} = 1.71 \text{ to } 5.5$, 806 Ksps, $V_{ref} = 1 \text{ to } 5.5$.
SID111A	A_INL	Integral non linearity	–1.4	–	+1.4	LSB	$V_{DDD} = 1.71 \text{ to } 3.6$, 806 Ksps, $V_{ref} = 1.71 \text{ to } V_{DDD}$.
SID111B	A_INL	Integral non linearity	–1.4	–	+1.4	LSB	$V_{DDD} = 1.71 \text{ to } 5.5$, 500 Ksps, $V_{ref} = 1 \text{ to } 5.5$.
SID112	A_DNL	Differential non linearity	–0.9	–	+1.35	LSB	$V_{DDD} = 1.71 \text{ to } 5.5$, 806 Ksps, $V_{ref} = 1 \text{ to } 5.5$.
SID112A	A_DNL	Differential non linearity	–0.9	–	+1.35	LSB	$V_{DDD} = 1.71 \text{ to } 3.6$, 806 Ksps, $V_{ref} = 1.71 \text{ to } V_{DDD}$.
SID112B	A_DNL	Differential non linearity	–0.9	–	+1.35	LSB	$V_{DDD} = 1.71 \text{ to } 5.5$, 500 Ksps, $V_{ref} = 1 \text{ to } 5.5$.
SID113	A_THD	Total harmonic distortion	–	–	–65	dB	$F_{IN} = 10 \text{ kHz}$.

CSD

Table 14. CSD Block Specification

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
CSD Specification							
SID308	VCSD	Voltage range of operation	1.71	–	5.5	V	
SID309	IDAC1	DNL for 8-bit resolution	–1	–	1	LSB	
SID310	IDAC1	INL for 8-bit resolution	–3	–	3	LSB	
SID311	IDAC2	DNL for 7-bit resolution	–1	–	1	LSB	
SID312	IDAC2	INL for 7-bit resolution	–3	–	3	LSB	
SID313	SNR	Ratio of counts of finger to noise. Guaranteed by characterization	5	–	–	Ratio	Capacitance range of 9 to 35 pF, 0.1 pF sensitivity
SID314	IDAC1_CRT1	Output current of Idac1 (8-bits) in High range	–	612	–	μA	
SID314A	IDAC1_CRT2	Output current of Idac1(8-bits) in Low range	–	306	–	μA	
SID315	IDAC2_CRT1	Output current of Idac2 (7-bits) in High range	–	304.8	–	μA	
SID315A	IDAC2_CRT2	Output current of Idac2 (7-bits) in Low range	–	152.4	–	μA	

SWD Interface

Table 32. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID213	F_SWCLK1	$3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	–	–	14	MHz	SWDCLK $\leq$ 1/3 CPU clock frequency
SID214	F_SWCLK2	$1.71\text{ V} \leq V_{DD} \leq 3.3\text{ V}$	–	–	7	MHz	SWDCLK $\leq$ 1/3 CPU clock frequency
SID215	T_SWDI_SETUP	$T = 1/f_{\text{SWDCLK}}$	0.25*T	–	–	ns	Guaranteed by characterization
SID216	T_SWDI_HOLD	$T = 1/f_{\text{SWDCLK}}$	0.25*T	–	–	ns	Guaranteed by characterization
SID217	T_SWDO_VALID	$T = 1/f_{\text{SWDCLK}}$	–	–	0.5*T	ns	Guaranteed by characterization
SID217A	T_SWDO_HOLD	$T = 1/f_{\text{SWDCLK}}$	1	–	–	ns	Guaranteed by characterization

Internal Main Oscillator

Table 33. IMO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I_IMO1	IMO operating current at 48 MHz	–	–	1000	μA	
SID219	I_IMO2	IMO operating current at 24 MHz	–	–	325	μA	
SID220	I_IMO3	IMO operating current at 12 MHz	–	–	225	μA	
SID221	I_IMO4	IMO operating current at 6 MHz	–	–	180	μA	
SID222	I_IMO5	IMO operating current at 3 MHz	–	–	150	μA	

Table 34. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	F_IMOTOL1	Frequency variation from 3 to 48 MHz	–	–	±2	%	±3% if $T_A > 85^\circ\text{C}$ and IMO frequency < 24 MHz
SID226	T_STARTIMO	IMO startup time	–	–	12	μs	
SID227	T_JITRMSIMO1	RMS Jitter at 3 MHz	–	156	–	ps	
SID228	T_JITRMSIMO2	RMS Jitter at 24 MHz	–	145	–	ps	
SID229	T_JITRMSIMO3	RMS Jitter at 48 MHz	–	139	–	ps	

Internal Low-Speed Oscillator

Table 35. ILO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231	I_ILO1	ILO operating current at 32 kHz	–	0.3	1.05	μA	Guaranteed by Characterization
SID233	I_ILOLEAK	ILO leakage current	–	2	15	nA	Guaranteed by Design

Packaging

The description of the PSoC4100M package dimensions follows.

Spec ID#	Package	Description	Package Dwg #
PKG_1	68-pin QFN	68 QFN, 8 mm x 8 mm x 1.0 mm height with 0.4 mm pitch	001-09618
PKG_2	64-pin TQFP	64 TQFP, 10 mm x10 mm x 1.4 mm height with 0.5 mm pitch	51-85051
PKG_4	64-pin TQFP	64 TQFP, 14 mm x14 mm x 1.4 mm height with 0.8 mm pitch	51-85046
PKG_5	48-pin TQFP	48 TQFP, 7 mm x 7 mm x 1.4 mm height with 0.5 mm pitch	51-85135
PKG_6	44-pin TQFP	44 TQFP, 10 mm x 10 mm x 1.4 mm height with 0.8 mm pitch	51-85064

Table 40. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T _A	Operating ambient temperature		–40	25	85	°C
T _J	Operating junction temperature		–40	–	100	°C
T _{JA}	Package θ_{JA} (68-pin QFN)		–	16.8	–	°C/Watt
T _{JC}	Package θ_{JC} (68-pin QFN)		–	2.9	–	°C/Watt
T _{JA}	Package θ_{JA} (64-pin TQFP, 0.5-mm pitch)		–	56	–	°C/Watt
T _{JC}	Package θ_{JC} (64-pin TQFP, 0.5-mm pitch)		–	19.5	–	°C/Watt
T _{JA}	Package θ_{JA} (64-pin TQFP, 0.8-mm pitch)		–	66.4	–	°C/Watt
T _{JC}	Package θ_{JC} (64-pin TQFP, 0.8-mm pitch)		–	18.2	–	°C/Watt
T _{JA}	Package θ_{JA} (48-pin TQFP, 0.5-mm pitch)		–	67.3	–	°C/Watt
T _{JC}	Package θ_{JC} (48-pin TQFP, 0.5-mm pitch)		–	30.4	–	°C/Watt
T _{JA}	Package θ_{JA} (44-pin TQFP, 0.8-mm pitch)		–	57	–	°C/Watt
T _{JC}	Package θ_{JC} (44-pin TQFP, 0.8-mm pitch)		–	25.9	–	°C/Watt

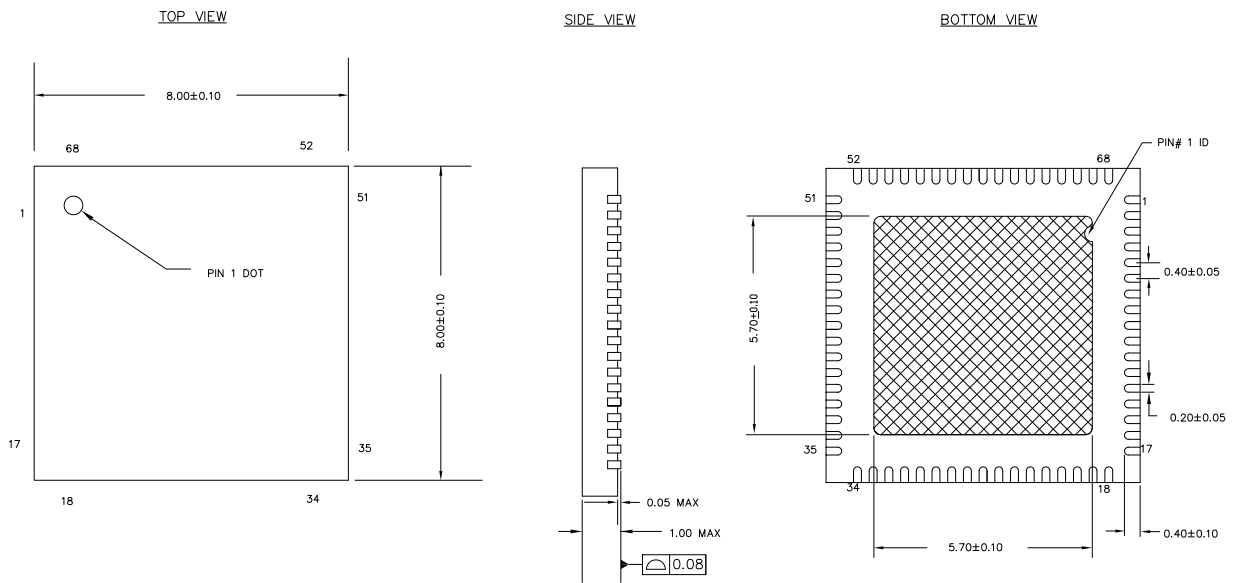
Table 41. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
All packages	260 °C	30 seconds

Table 42. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
All packages	MSL 3

Figure 5. 68-Pin 8 × 8 × 1.0 mm QFN Package Outline

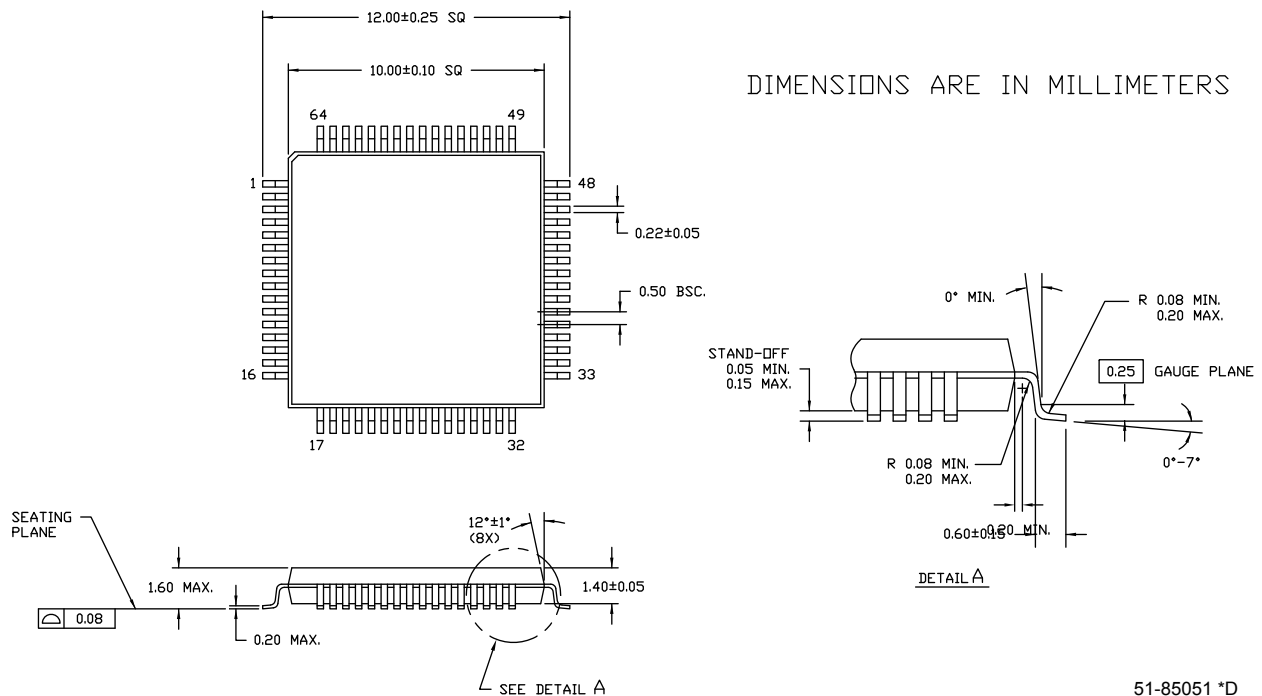


NOTES:

1.  HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 17 ± 2mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-09618 *E

Figure 6. 64-Pin 10 × 10 × 1.4 mm TQFP Package Outline



51-85051 *D

Figure 7. 64-Pin 14 × 14 × 1.4 mm TQFP Package Outline

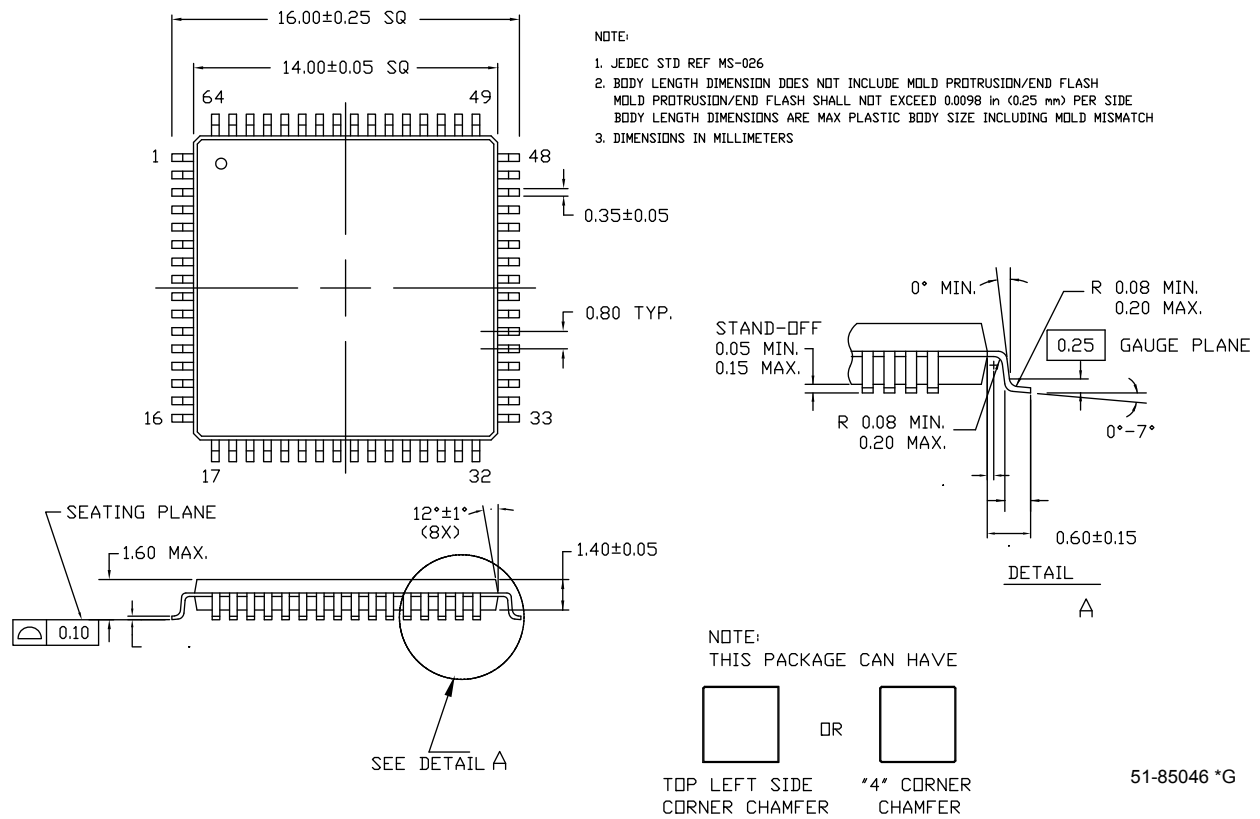


Figure 8. 48-Pin 7 × 7 × 1.4 mm TQFP Package Outline

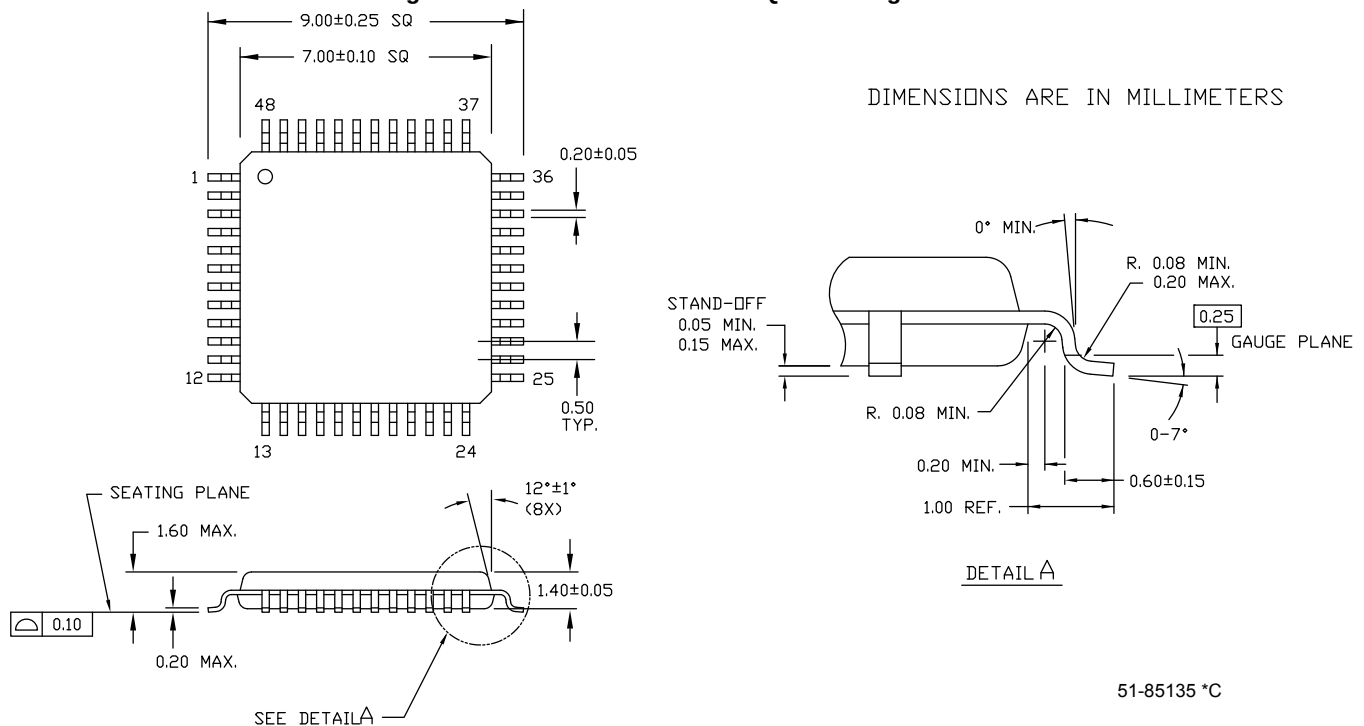
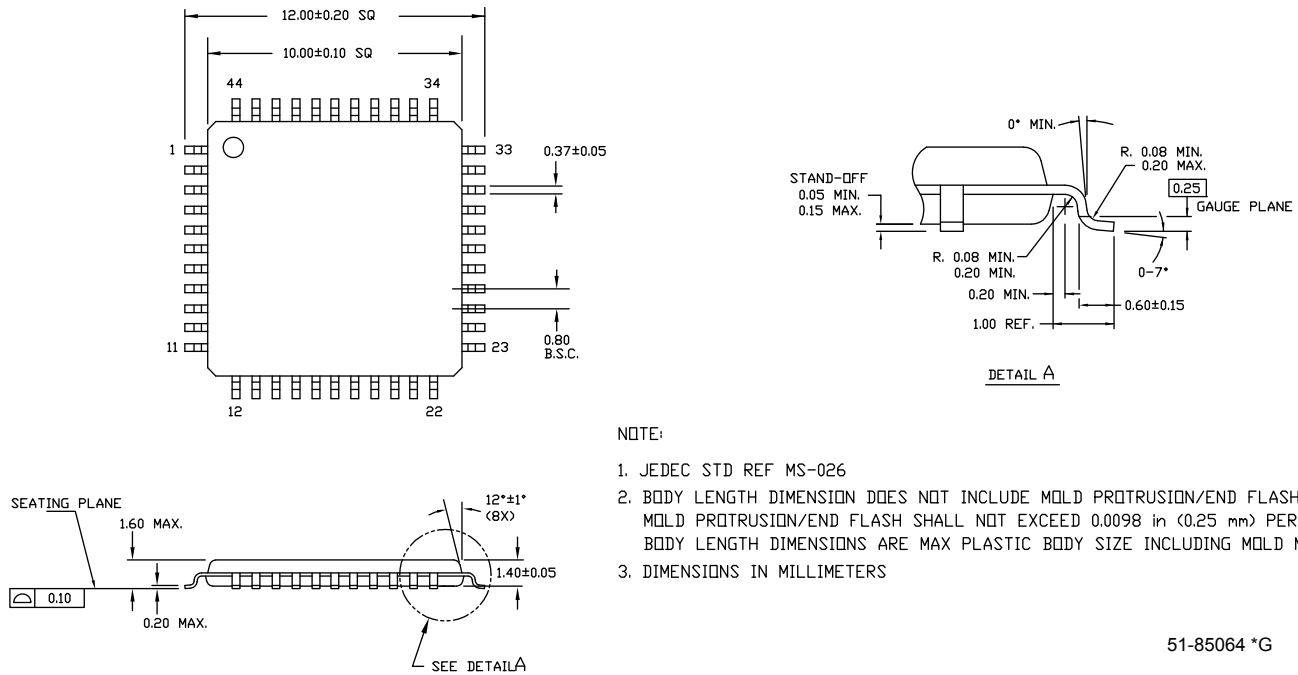


Figure 9. 44-Pin 10 × 10 × 1.4 mm TQFP Package Outline



51-85064 *G

Document Conventions

Units of Measure

Table 44. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
μA	microampere
μF	microfarad
μH	microhenry
μs	microsecond
μV	microvolt
μW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

Revision History

Description Title: PSoC® 4: PSoC 4100M Family Datasheet Programmable System-on-Chip (PSoC®) Document Number: 001-96519				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
*A	4765455	WKA	05/20/2015	Release to web.
*B	4815539	WKA	06/29/2015	Removed note regarding hardware handshaking in the UART Mode section. Changed max value of SID51A to 2 ms. Added "Guaranteed by characterization" note for SID65 and SID65A Updated Ordering Information.
*C	4941619	WKA	09/30/2015	Updated CapSense section. Updated the note at the end of the Pinout table. Removed Conditions for spec SID237.
*D	5026805	WKA	11/26/2015	Added Comparator ULP mode range restrictions and corrected typos.
*E	5408936	WKA	08/19/2016	Added extended industrial temperature range. Added specs SID290Q, SID182A, and SID299A. Updated conditions for SID290, SID223, and SID237. Added 44-pin TQFP package details. Updated Ordering Information

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