



Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I ² C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, CapSense, LCD, LVD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b SAR; 2xIDAC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4126axi-m445

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article [KBA86521, How to Design with PSoC 3, PSoC 4, and PSoC 5LP](#). Following is an abbreviated list for PSoC 4:

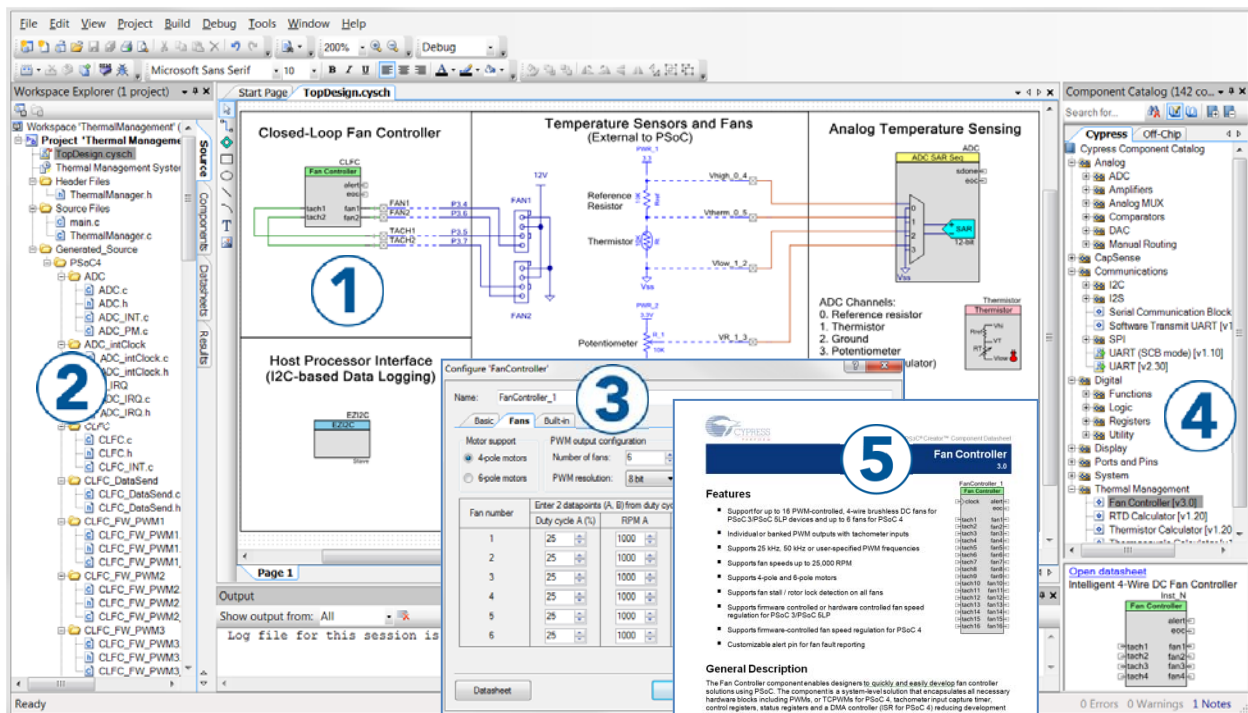
- Overview: [PSoC Portfolio](#), [PSoC Roadmap](#)
 - Product Selectors: [PSoC 1](#), [PSoC 3](#), [PSoC 4](#), [PSoC 5LP](#)
In addition, PSoC Creator includes a device selection tool.
 - Application notes: Cypress offers a large number of PSoC application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 4 are:
 - [AN79953](#): Getting Started With PSoC 4
 - [AN88619](#): PSoC 4 Hardware Design Considerations
 - [AN86439](#): Using PSoC 4 GPIO Pins
 - [AN57821](#): Mixed Signal Circuit Board Layout
 - [AN81623](#): Digital Design Best Practices
 - [AN73854](#): Introduction To Bootloaders
 - [AN89610](#): ARM Cortex Code Optimization
 - Technical Reference Manual (TRM) is in two documents:
 - [Architecture TRM](#) details each PSoC 4 functional block.
 - [Registers TRM](#) describes each of the PSoC 4 registers.
 - Development Kits:
 - [CY8CKIT-042](#), PSoC 4 Pioneer Kit, is an easy-to-use and inexpensive development platform. This kit includes connectors for Arduino™ compatible shields and Digilent® Pmod™ daughter cards.
 - [CY8CKIT-049](#) is a very low-cost prototyping platform. It is a low-cost alternative to sampling PSoC 4 devices.
 - [CY8CKIT-001](#) is a common development platform for any one of the PSoC 1, PSoC 3, PSoC 4, or PSoC 5LP families of devices.
- The [MiniProg3](#) device provides an interface for flash programming and debug.

PSoC Creator

PSoC Creator is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC 3, PSoC 4, and PSoC 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC Components; see the [list of component datasheets](#). With PSoC Creator, you can:

1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

Figure 1. Multiple-Sensor Example Project in PSoC Creator



Contents

PSoC 4100M Block Diagram	4	Analog Peripherals	19
Functional Definition	5	Digital Peripherals	24
CPU and Memory Subsystem	5	Memory	26
System Resources	5	System Resources	27
Analog Blocks.....	6	Ordering Information	30
Fixed Function Digital	7	Part Numbering Conventions	31
GPIO	8	Packaging	32
Special Function Peripherals.....	8	Acronyms	35
Pinouts	9	Document Conventions	37
Power	13	Units of Measure	37
Unregulated External Supply.....	13	Revision History	38
Regulated External Supply	13	Sales, Solutions, and Legal Information	39
Development Support	14	Worldwide Sales and Design Support.....	39
Documentation	14	Products	39
Online	14	PSoC® Solutions	39
Tools.....	14	Cypress Developer Community.....	39
Electrical Specifications	15	Technical Support	39
Absolute Maximum Ratings.....	15		
Device Level Specifications.....	15		

Functional Definition

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in the PSoC 4100-M is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and execute a subset of the Thumb-2 instruction set. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC), which can wake the processor up from the Deep Sleep mode allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a 2-wire form of JTAG; the debug configuration used for PSoC 4100-M has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The PSoC 4100-M has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

SRAM

SRAM memory is retained during Hibernate.

SRoM

A supervisory ROM that contains boot and configuration routines is provided.

DMA

A DMA engine, with eight channels, is provided that can do 32-bit transfers and has chainable ping-pong descriptors.

System Resources

Power System

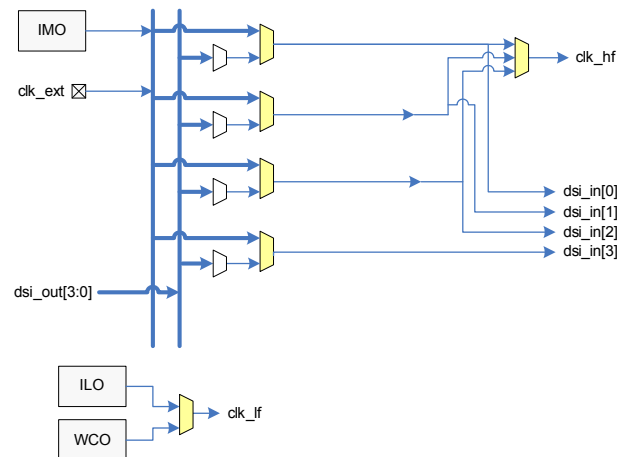
The power system is described in detail in the section [Power on page 13](#). It provides assurance that voltage levels are as required for each respective mode and either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (brown-out detect (BOD)) or interrupts (low voltage detect (LVD)). The PSoC 4100M operates with a single external supply over the range of 1.71 to 5.5 V and has five different power modes, transitions between which are managed by the power system. The PSoC 4100M provides Sleep, Deep Sleep, Hibernate, and Stop low-power modes.

Clock System

The PSoC 4100-M clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that no meta-stable conditions occur.

The clock system for the PSoC 4100-M consists of a Watch Crystal Oscillator (WCO) running at 32 kHz, the IMO (3 to 48 MHz) and the ILO (32-kHz nominal) internal oscillators, and provision for an external clock.

Figure 2. PSoC 4100M MCU Clocking Architecture



The clk_hf signal can be divided down to generate synchronous clocks for the analog and digital peripherals. There are a total of 16 clock dividers for the PSoC 4100-M, each with 16-bit divide capability. The analog clock leads the digital clocks to allow analog events to occur before digital clock-related noise is generated. The 16-bit capability allows a lot of flexibility in generating fine-grained frequency values and is fully supported in PSoC Creator.

IMO Clock Source

The IMO is the primary source of internal clocking in the PSoC 4100M. It is trimmed during testing to achieve the specified accuracy. Trim values are stored in nonvolatile memory. Trimming can also be done on the fly to allow in-field calibration. The IMO default frequency is 24 MHz and it can be adjusted between 3 to 48 MHz in steps of 1 MHz. IMO tolerance with Cypress-provided calibration settings is $\pm 2\%$.

ILO Clock Source

The ILO is a very low power oscillator, nominally 32 kHz, which is primarily used to generate clocks for peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

Crystal Oscillator

The PSoC 4100M clock subsystem also includes a low-frequency crystal oscillator (32-kHz WCO) that is available during the Deep Sleep mode and can be used for Real-Time Clock (RTC) and Watchdog Timer applications.

Pinouts

The following is the pin list for the PSoC 4100M. This shows the power supply and port pins (for example, P0.0 is Pin 0 of Port 0).

68-QFN		64-TQFP		48-TQFP		44-TQFP	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
42	P0.0	39	P0.0	28	P0.0	24	P0.0
43	P0.1	40	P0.1	29	P0.1	25	P0.1
44	P0.2	41	P0.2	30	P0.2	26	P0.2
45	P0.3	42	P0.3	31	P0.3	27	P0.3
46	P0.4	43	P0.4	32	P0.4	28	P0.4
47	P0.5	44	P0.5	33	P0.5	29	P0.5
48	P0.6	45	P0.6	34	P0.6	30	P0.6
49	P0.7	46	P0.7	35	P0.7	31	P0.7
50	XRES	47	XRES	36	XRES	32	XRES
51	VCCD	48	VCCD	37	VCCD	33	VCCD
52	VSSD	49	VSSD	38	VSSD	DN	VSSD
53	VDDD	50	VDDD	39	VDDD	34	VDDD
				40	VDDA	35	VDDA
54	P5.0	51	P5.0				
55	P5.1	52	P5.1				
56	P5.2	53	P5.2				
57	P5.3	54	P5.3				
58	P5.4						
59	P5.5	55	P5.5				
60	VDDA	56	VDDA	40	VDDA	35	VDDA
61	VSSA	57	VSSA	41	VSSA	36	VSSA
62	P1.0	58	P1.0	42	P1.0	37	P1.0
63	P1.1	59	P1.1	43	P1.1	38	P1.1
64	P1.2	60	P1.2	44	P1.2	39	P1.2
65	P1.3	61	P1.3	45	P1.3	40	P1.3
66	P1.4	62	P1.4	46	P1.4	41	P1.4
67	P1.5	63	P1.5	47	P1.5	42	P1.5
68	P1.6	64	P1.6	48	P1.6	43	P1.6
1	P1.7/VREF	1	P1.7/VREF	1	P1.7/VREF	44	P1.7/VREF
						1	VSSD
2	P2.0	2	P2.0	2	P2.0	2	P2.0
3	P2.1	3	P2.1	3	P2.1	3	P2.1
4	P2.2	4	P2.2	4	P2.2	4	P2.2
5	P2.3	5	P2.3	5	P2.3	5	P2.3
6	P2.4	6	P2.4	6	P2.4	6	P2.4
7	P2.5	7	P2.5	7	P2.5	7	P2.5

68-QFN		64-TQFP		48-TQFP		44-TQFP	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
8	P2.6	8	P2.6	8	P2.6	8	P2.6
9	P2.7	9	P2.7	9	P2.7	9	P2.7
10	VSSA	10	VSSA	10	VSSD	10	VSSD
11	VDDA	11	VDDA				
12	P6.0	12	P6.0				
13	P6.1	13	P6.1				
14	P6.2	14	P6.2				
15	P6.3						
16	P6.4	15	P6.4				
17	P6.5	16	P6.5				
18	VSSIO	17	VSSIO	10	VSSD	10	VSSD
19	P3.0	18	P3.0	12	P3.0	11	P3.0
20	P3.1	19	P3.1	13	P3.1	12	P3.1
21	P3.2	20	P3.2	14	P3.2	13	P3.2
22	P3.3	21	P3.3	16	P3.3	14	P3.3
23	P3.4	22	P3.4	17	P3.4	15	P3.4
24	P3.5	23	P3.5	18	P3.5	16	P3.5
25	P3.6	24	P3.6	19	P3.6	17	P3.6
26	P3.7	25	P3.7	20	P3.7	18	P3.7
27	VDDIO	26	VDDIO	21	VDDIO	19	VDDD
28	P4.0	27	P4.0	22	P4.0	20	P4.0
29	P4.1	28	P4.1	23	P4.1	21	P4.1
30	P4.2	29	P4.2	24	P4.2	22	P4.2
31	P4.3	30	P4.3	25	P4.3	23	P4.3
32	P4.4	31	P4.4				
33	P4.5	32	P4.5				
34	P4.6	33	P4.6				
35	P4.7						
39	P7.0	37	P7.0	26	P7.0		
40	P7.1	38	P7.1	27	P7.1		
41	P7.2						

The pins of Port 6 are overvoltage-tolerant. Pins 36, 37, and 38 are No-Connects on the 68-pin QFN. Pins 34, 35, and 36 are No-Connects on the 64-pin TQFP. Pins 11 and 15 are No-connects in the 48-pin TQFP. All VSS pins must be tied together.

The output drivers of I/O Ports P0 and P7 are connected to VDDD. Output drivers of I/O Ports 1, 2, and 5 are connected to VDDA. Output drivers of I/O Ports 3, 4, and 6 are connected to VDDIO.

Each of the pins shown in the previous table can have multiple programmable functions as shown in the following table. Column headings refer to Analog and Alternate pin functions:

Port/Pin	Analog	Alt. Function 1	Alt. Function 2	Alt. Function 3	Alt. Function 4	Alt. Function 5
P0.0	lpcomp.in_p[0]					scb[0].spi_select1:0
P0.1	lpcomp.in_n[0]					scb[0].spi_select2:0
P0.2	lpcomp.in_p[1]					scb[0].spi_select3:0
P0.3	lpcomp.in_n[1]					
P0.4	wco_in		scb[1].uart_rx:0		scb[1].i2c_scl:0	scb[1].spi_mosi:1
P0.5	wco_out		scb[1].uart_tx:0		scb[1].i2c_sda:0	scb[1].spi_miso:1
P0.6		ext_clk:0	scb[1].uart_cts:0			scb[1].spi_clk:1
P0.7			scb[1].uart_rts:0		wakeup	scb[1].spi_select0:1
P5.0	ctb1.oa0.inp	tcpwm.line[4]:2	scb[2].uart_rx:0		scb[2].i2c_scl:0	scb[2].spi_mosi:0
P5.1	ctb1.oa0.inm	tcpwm.line_compl[4]:2	scb[2].uart_tx:0		scb[2].i2c_sda:0	scb[2].spi_miso:0
P5.2	ctb1.oa0.out	tcpwm.line[5]:2	scb[2].uart_cts:0		lpcomp.comp[0]:1	scb[2].spi_clk:0
P5.3	ctb1.oa1.out	tcpwm.line_compl[5]:2	scb[2].uart_rts:0		lpcomp.comp[1]:1	scb[2].spi_select0:0
P5.4	ctb1.oa1.inm	tcpwm.line[6]:2				scb[2].spi_select1:0
P5.5	ctb1.oa1.inp	tcpwm.line_compl[6]:2				scb[2].spi_select2:0
P5.6	ctb1.oa0.inp_alt	tcpwm.line[7]:0				scb[2].spi_select3:0
P5.7	ctb1.oa1.inp_alt	tcpwm.line_compl[7]:0				
P1.0	ctb0.oa0.inp	tcpwm.line[2]:1	scb[0].uart_rx:1		scb[0].i2c_scl:0	scb[0].spi_mosi:1
P1.1	ctb0.oa0.inm	tcpwm.line_compl[2]:1	scb[0].uart_tx:1		scb[0].i2c_sda:0	scb[0].spi_miso:1
P1.2	ctb0.oa0.out	tcpwm.line[3]:1	scb[0].uart_cts:1			scb[0].spi_clk:1
P1.3	ctb0.oa1.out	tcpwm.line_compl[3]:1	scb[0].uart_rts:1			scb[0].spi_select0:1
P1.4	ctb0.oa1.inm	tcpwm.line[6]:1				scb[0].spi_select1:1
P1.5	ctb0.oa1.inp	tcpwm.line_compl[6]:1				scb[0].spi_select2:1
P1.6	ctb0.oa0.inp_alt	tcpwm.line[7]:1				scb[0].spi_select3:1
P1.7	ctb0.oa1.inp_alt	tcpwm.line_compl[7]:1				
P2.0	sarmux.0	tcpwm.line[4]:1			scb[1].i2c_scl:1	scb[1].spi_mosi:2
P2.1	sarmux.1	tcpwm.line_compl[4]:1			scb[1].i2c_sda:1	scb[1].spi_miso:2
P2.2	sarmux.2	tcpwm.line[5]:1				scb[1].spi_clk:2
P2.3	sarmux.3	tcpwm.line_compl[5]:1				scb[1].spi_select0:2
P2.4	sarmux.4	tcpwm.line[0]:1				scb[1].spi_select1:1
P2.5	sarmux.5	tcpwm.line_compl[0]:1				scb[1].spi_select2:1
P2.6	sarmux.6	tcpwm.line[1]:1				scb[1].spi_select3:1
P2.7	sarmux.7	tcpwm.line_compl[1]:1				scb[3].spi_select0:1

Power

The supply voltage range is 1.71 to 5.5 V with all functions and circuits operating over that range.

The PSoC 4100M family allows two distinct modes of power supply operation: Unregulated External Supply and Regulated External Supply modes.

Unregulated External Supply

In this mode, the PSoC 4100M is powered by an External Power Supply that can be anywhere in the range of 1.8 to 5.5 V. This range is also designed for battery-powered operation, for instance, the chip can be powered from a battery system that starts at 3.5V and works down to 1.8 V. In this mode, the internal regulator of the PSoC 4100M supplies the internal logic and the VCCD output of the PSoC 4100M must be bypassed to ground via an external Capacitor (in the range of 1 to 1.6 μ F; X5R ceramic or better).

The grounds, VSSA and VSS, must be shorted together. Bypass capacitors must be used from VDDD and VDPA to ground, typical practice for systems in this frequency range is to use a capacitor in the 1 μ F range in parallel with a smaller capacitor (0.1 μ F, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the Bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

Power Supply	Bypass Capacitors
VDDD–VSS and VDDIO–VSS	0.1 μ F ceramic at each pin plus bulk capacitor 1 to 10 μ F.
VDPA–VSSA	0.1 μ F ceramic at pin. Additional 1 μ F to 10 μ F bulk capacitor
VCCD–VSS	1 μ F ceramic capacitor at the VCCD pin
VREF–VSSA (optional)	The internal bandgap may be bypassed with a 1 μ F to 10 μ F capacitor for better ADC performance.

Regulated External Supply

In this mode, the PSoC 4100M is powered by an external power supply that must be within the range of 1.71 to 1.89 V ($1.8 \pm 5\%$); note that this range needs to include power supply ripple. VCCD and VDDD pins are shorted together and bypassed. The internal regulator is disabled in firmware.

Table 3. AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID48	F _{CPU}	CPU frequency	DC	–	24	MHz	1.71 ≤ V _{DD} ≤ 5.5
SID49	T _{SLEEP}	Wakeup from sleep mode	–	0	–	μs	Guaranteed by characterization
SID50	T _{DEEPSLEEP}	Wakeup from Deep Sleep mode	–	–	25	μs	24 MHz IMO. Guaranteed by characterization
SID51	T _{HIBERNATE}	Wakeup from Hibernate mode	–	–	0.7	ms	Guaranteed by characterization
SID51A	T _{STOP}	Wakeup from Stop mode	–	–	2	ms	Guaranteed by characterization
SID52	T _{RESETWIDTH}	External reset pulse width	1	–	–	μs	Guaranteed by characterization

GPIO

Table 4. GPIO DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID57	V _{IH} ^[2]	Input voltage high threshold	0.7 × V _{DDD}	–	–	V	CMOS Input
SID57A	I _{IHS}	Input current when Pad > V _{DDIO} for OVT inputs	–	–	10	μA	Per I ² C Spec
SID58	V _{IL}	Input voltage low threshold	–	–	0.3 × V _{DDD}	V	CMOS Input
SID241	V _{IH} ^[2]	LVTTL input, V _{DDD} < 2.7 V	0.7 × V _{DDD}	–	–	V	
SID242	V _{IL}	LVTTL input, V _{DDD} < 2.7 V	–	–	0.3 × V _{DDD}	V	
SID243	V _{IH} ^[2]	LVTTL input, V _{DDD} ≥ 2.7 V	2.0	–	–	V	
SID244	V _{IL}	LVTTL input, V _{DDD} ≥ 2.7 V	–	–	0.8	V	
SID59	V _{OH}	Output voltage high level	V _{DDD} – 0.6	–	–	V	I _{OH} = 4 mA at 3 V V _{DDD}
SID60	V _{OH}	Output voltage high level	V _{DDD} – 0.5	–	–	V	I _{OH} = 1 mA at 1.8 V V _{DDD}
SID61	V _{OL}	Output voltage low level	–	–	0.6	V	I _{OL} = 4 mA at 1.8 V V _{DDD}
SID62	V _{OL}	Output voltage low level	–	–	0.6	V	I _{OL} = 8 mA at 3 V V _{DDD}
SID62A	V _{OL}	Output voltage low level	–	–	0.4	V	I _{OL} = 3 mA at 3 V V _{DDD}
SID63	R _{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID64	R _{PULLDOWN}	Pull-down resistor	3.5	5.6	8.5	kΩ	
SID65	I _{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V _{DDD} = 3.0 V. Guaranteed by characterization

Note

 2. V_{IH} must not exceed V_{DDD} + 0.2 V.

Table 4. GPIO DC Specifications (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID65A	I_{IL_CTBM}	Input leakage current (absolute value) for CTBM pins	–	–	4	nA	Guaranteed by characterization
SID66	C_{IN}	Input capacitance	–	–	7	pF	
SID67	V_{HYSTTL}	Input hysteresis LVTTTL	25	40	–	mV	$V_{DD} \geq 2.7\text{ V}$
SID68	$V_{HYSCMOS}$	Input hysteresis CMOS	$0.05 \times V_{DD}$	–	–	mV	
SID69	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	μA	Guaranteed by characterization
SID69A	I_{TOT_GPIO}	Maximum Total Source or Sink Chip Current	–	–	200	mA	Guaranteed by characterization

Table 5. GPIO AC Specifications

(Guaranteed by Characterization)^[3]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID70	T_{RISEF}	Rise time in fast strong mode	2	–	12	ns	3.3 V V_{DD} , Load = 25 pF
SID71	T_{FALLF}	Fall time in fast strong mode	2	–	12	ns	3.3 V V_{DD} , Load = 25 pF
SID72	T_{RISES}	Rise time in slow strong mode	10	–	60	ns	3.3 V V_{DD} , Load = 25 pF
SID73	T_{FALLS}	Fall time in slow strong mode	10	–	60	ns	3.3 V V_{DD} , Load = 25 pF
SID74	$F_{GPIOUT1}$	GPIO Fout; 3.3 V $\leq V_{DD} \leq 5.5\text{ V}$. Fast strong mode.	–	–	24	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID75	$F_{GPIOUT2}$	GPIO Fout; 1.7 V $\leq V_{DD} \leq 3.3\text{ V}$. Fast strong mode.	–	–	16.7	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID76	$F_{GPIOUT3}$	GPIO Fout; 3.3 V $\leq V_{DD} \leq 5.5\text{ V}$. Slow strong mode.	–	–	7	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID245	$F_{GPIOUT4}$	GPIO Fout; 1.7 V $\leq V_{DD} \leq 3.3\text{ V}$. Slow strong mode.	–	–	3.5	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID246	F_{GPIOIN}	GPIO input operating frequency; 1.71 V $\leq V_{DD} \leq 5.5\text{ V}$	–	–	48	MHz	90/10% V_{IO}

Note

3. Simultaneous switching transitions on many fully-loaded GPIO pins may cause ground perturbations depending on several factors including PCB and decoupling capacitor design. For applications that are very sensitive to ground perturbations, the slower GPIO slew rate setting may be used.

XRES

Table 6. XRES DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID77	V_{IH}	Input voltage high threshold	$0.7 \times V_{DD}$	–	–	V	CMOS Input
SID78	V_{IL}	Input voltage low threshold	–	–	$0.3 \times V_{DD}$	V	CMOS Input
SID79	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	k Ω	
SID80	C_{IN}	Input capacitance	–	3	–	pF	
SID81	$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	Guaranteed by characterization
SID82	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	μ A	Guaranteed by characterization

Table 7. XRES AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID83	$T_{RESETWIDTH}$	Reset pulse width	1	–	–	μ s	Guaranteed by characterization

Table 10. Comparator AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID91	T _{RESP1}	Response time, normal mode	–	–	110	ns	50-mV overdrive
SID258	T _{RESP2}	Response time, low power mode	–	–	200	ns	50-mV overdrive
SID92	T _{RESP3}	Response time, ultra low power mode (V _{DDD} ≥ 2.2 V for Temp < 0 °C, V _{DDD} ≥ 1.8 V for Temp > 0 °C)	–	–	15	µs	200-mV overdrive

Temperature Sensor

Table 11. Temperature Sensor Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID93	T _{SENSACC}	Temperature sensor accuracy	–5	±1	+5	°C	–40 to +85 °C

SAR ADC

Table 12. SAR ADC DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID94	A_RES	Resolution	–	–	12	bits	
SID95	A_CHNIS_S	Number of channels - single ended	–	–	16		8 full speed
SID96	A-CHNKS_D	Number of channels - differential	–	–	8		Diff inputs use neighboring I/O
SID97	A-MONO	Monotonicity	–	–	–		Yes. Based on characterization
SID98	A_GAINERR	Gain error	–	–	±0.1	%	With external reference.
SID99	A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V V _{REF} .
SID100	A_ISAR	Current consumption	–	–	1	mA	
SID101	A_VINS	Input voltage range - single ended	V _{SS}	–	V _{DDA}	V	Based on device characterization
SID102	A_VIND	Input voltage range - differential	V _{SS}	–	V _{DDA}	V	Based on device characterization
SID103	A_INRES	Input resistance	–	–	2.2	KΩ	Based on device characterization
SID104	A_INCAP	Input capacitance	–	–	10	pF	Based on device characterization

Table 13. SAR ADC AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID106	A_PSR	Power supply rejection ratio	70	–	–	dB	
SID107	A_CMRR	Common mode rejection ratio	66	–	–	dB	Measured at 1 V
SID108	A_SAMP_1	Sample rate with external reference bypass cap	–	–	806	ksps	

Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripheral in timer mode.

Timer/Counter/PWM

Table 15. TCPWM Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.1	ITCPWM1	Block current consumption at 3 MHz	–	–	45	μA	All modes (Timer/Counter/PWM)
SID.TCPWM.2	ITCPWM2	Block current consumption at 12 MHz	–	–	155	μA	All modes (Timer/Counter/PWM)
SID.TCPWM.2A	ITCPWM3	Block current consumption at 48 MHz	–	–	650	μA	All modes (Timer/Counter/PWM)
SID.TCPWM.3	TCPWMFREQ	Operating frequency	–	–	Fc	MHz	Fc max = Fcpu. Maximum = 24 MHz
SID.TCPWM.4	TPWMENEXT	Input Trigger Pulse Width for all Trigger Events	2/Fc	–	–	ns	Trigger Events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.
SID.TCPWM.5	TPWMEXT	Output Trigger Pulse widths	2/Fc	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) trigger outputs
SID.TCPWM.5A	TCRES	Resolution of Counter	1/Fc	–	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWMRES	PWM Resolution	1/Fc	–	–	ns	Minimum pulse width of PWM Output
SID.TCPWM.5C	QRES	Quadrature inputs resolution	1/Fc	–	–	ns	Minimum pulse width between Quadrature phase inputs.

I²C

Table 16. Fixed I²C DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID149	I _{I2C1}	Block current consumption at 100 kHz	–	–	50	μA	
SID150	I _{I2C2}	Block current consumption at 400 kHz	–	–	135	μA	
SID151	I _{I2C3}	Block current consumption at 1 Mbps	–	–	310	μA	
SID152	I _{I2C4}	I ² C enabled in Deep Sleep mode	–	–	1.4	μA	

Table 17. Fixed I²C AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID153	F _{I2C1}	Bit rate	–	–	1	Mbps	

Table 24. Fixed SPI Master mode AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID167	T _{DMO}	MOSI valid after Scklock driving edge	–	–	15	ns	
SID168	T _{DSI}	MISO valid before Scklock capturing edge. Full clock, late MISO Sampling used	20	–	–	ns	
SID169	T _{HMO}	Previous MOSI data hold time with respect to capturing edge at Slave	0	–	–	ns	

Table 25. Fixed SPI Slave mode AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID170	T _{DMI}	MOSI valid before Scklock capturing edge	40	–	–	ns	
SID171	T _{DSO}	MISO valid after Scklock driving edge	–	–	42 + 3 × (1/FCPU)	ns	
SID171A	T _{DSO_ext}	MISO valid after Scklock driving edge in Ext. Clock mode	–	–	48	ns	
SID172	T _{HSO}	Previous MISO data hold time	0	–	–	ns	
SID172A	T _{SSELSCK}	SSEL Valid to first SCK Valid edge	100	–	–	ns	

Memory

Table 26. Flash DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID173	V _{PE}	Erase and program voltage	1.71	–	5.5	V	

Table 27. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID174	T _{ROWWRITE}	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 128 bytes
SID175	T _{ROWERASE}	Row erase time	–	–	13	ms	
SID176	T _{ROWPROGRAM}	Row program time after erase	–	–	7	ms	
SID178	T _{BULKERASE}	Bulk erase time (128 KB)	–	–	35	ms	
SID179	T _{SECTORERASE}	Sector erase time (8 KB)	–	–	15	ms	
SID180	T _{DEVPROG}	Total device program time	–	–	15	seconds	Guaranteed by characterization
SID181	F _{END}	Flash endurance	100 K	–	–	cycles	Guaranteed by characterization
SID182	F _{RET}	Flash retention. T _A ≤ 55 °C, 100 K P/E cycles	20	–	–	years	Guaranteed by characterization
SID182A		Flash retention. T _A ≤ 85 °C, 10 K P/E cycles	10	–	–	years	Guaranteed by characterization
SID182B	F _{RETQ}	Flash retention. T _A ≤ 105 °C, 10K P/E cycles, ≤ three years at T _A ≥ 85 °C	10	20	–	years	Guaranteed by characterization.

System Resources

Power-on-Reset (POR) with Brown Out

Table 28. Imprecise Power On Reset (PRES)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID185	V _{RISEIPOR}	Rising trip voltage	0.80	–	1.45	V	Guaranteed by characterization
SID186	V _{FALLIPOR}	Falling trip voltage	0.75	–	1.4	V	Guaranteed by characterization
SID187	V _{IPORHYST}	Hysteresis	15	–	200	mV	Guaranteed by characterization

Table 29. Precise Power On Reset (POR)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190	V _{FALLPPOR}	BOD trip voltage in active and sleep modes	1.64	–	–	V	Guaranteed by characterization
SID192	V _{FALLDPSLP}	BOD trip voltage in Deep Sleep	1.4	–	–	V	Guaranteed by characterization

Voltage Monitors

Table 30. Voltage Monitors DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID195	V _{LVI1}	LVI_A/D_SEL[3:0] = 0000b	1.71	1.75	1.79	V	
SID196	V _{LVI2}	LVI_A/D_SEL[3:0] = 0001b	1.76	1.80	1.85	V	
SID197	V _{LVI3}	LVI_A/D_SEL[3:0] = 0010b	1.85	1.90	1.95	V	
SID198	V _{LVI4}	LVI_A/D_SEL[3:0] = 0011b	1.95	2.00	2.05	V	
SID199	V _{LVI5}	LVI_A/D_SEL[3:0] = 0100b	2.05	2.10	2.15	V	
SID200	V _{LVI6}	LVI_A/D_SEL[3:0] = 0101b	2.15	2.20	2.26	V	
SID201	V _{LVI7}	LVI_A/D_SEL[3:0] = 0110b	2.24	2.30	2.36	V	
SID202	V _{LVI8}	LVI_A/D_SEL[3:0] = 0111b	2.34	2.40	2.46	V	
SID203	V _{LVI9}	LVI_A/D_SEL[3:0] = 1000b	2.44	2.50	2.56	V	
SID204	V _{LVI10}	LVI_A/D_SEL[3:0] = 1001b	2.54	2.60	2.67	V	
SID205	V _{LVI11}	LVI_A/D_SEL[3:0] = 1010b	2.63	2.70	2.77	V	
SID206	V _{LVI12}	LVI_A/D_SEL[3:0] = 1011b	2.73	2.80	2.87	V	
SID207	V _{LVI13}	LVI_A/D_SEL[3:0] = 1100b	2.83	2.90	2.97	V	
SID208	V _{LVI14}	LVI_A/D_SEL[3:0] = 1101b	2.93	3.00	3.08	V	
SID209	V _{LVI15}	LVI_A/D_SEL[3:0] = 1110b	3.12	3.20	3.28	V	
SID210	V _{LVI16}	LVI_A/D_SEL[3:0] = 1111b	4.39	4.50	4.61	V	
SID211	LVI_IDD	Block current	–	–	100	μA	Guaranteed by characterization

Table 31. Voltage Monitors AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID212	T _{MONTRIP}	Voltage monitor trip time	–	–	1	μs	Guaranteed by characterization

Table 36. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234	T _{STARTILO1}	ILO startup time	–	–	2	ms	Guaranteed by characterization
SID236	T _{ILODUTY}	ILO duty cycle	40	50	60	%	Guaranteed by characterization
SID237	F _{ILOTRIM1}	32 kHz trimmed frequency	15	32	50	kHz	Max ILO frequency is 70 kHz if T _A > 85 °C

Table 37. External Clock Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID305	ExtClkFreq	External Clock input Frequency	0	–	48	MHz	Guaranteed by characterization
SID306	ExtClkDuty	Duty cycle; Measured at V _{DD/2}	45	–	55	%	Guaranteed by characterization

Table 38. Watch Crystal Oscillator (WCO) Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
IMO WCO-PLL calibrated mode							
SID330	IMO _{WCO1}	Frequency variation with IMO set to 3 MHz	–0.6	–	0.6	%	Does not include WCO tolerance
SID331	IMO _{WCO2}	Frequency variation with IMO set to 5 MHz	–0.4	–	0.4	%	Does not include WCO tolerance
SID332	IMO _{WCO3}	Frequency variation with IMO set to 7 MHz or 9 MHz	–0.3	–	0.3	%	Does not include WCO tolerance
SID333	IMO _{WCO4}	All other IMO frequency settings	–0.2	–	0.2	%	Does not include WCO tolerance
WCO Specifications							
SID398	F _{WCO}	Crystal frequency	–	32.768		kHz	
SID399	F _{TOL}	Frequency tolerance	–	50	250	ppm	With 20-ppm crystal.
SID400	ESR	Equivalent series resistance	–	50	–	kΩ	
SID401	PD	Drive level	–	–	1	μW	
SID402	T _{START}	Startup time	–	–	500	ms	
SID403	C _L	Crystal load capacitance	6	–	12.5	pF	
SID404	C ₀	Crystal shunt capacitance	–	1.35	–	pF	
SID405	I _{WCO1}	Operating current (high power mode)	–	–	8	uA	

Table 39. Block Specs

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID257	T _{WS24} *	Number of wait states at 24 MHz	1	–	–		CPU execution from Flash
SID260	V _{REFSAR}	Trimmed internal reference to SAR	–1	–	+1	%	Percentage of V _{bg} (1.024 V). Guaranteed by characterization
SID261	F _{SARINTREF}	SAR operating speed without external reference bypass	–	–	100	ksps	12-bit resolution. Guaranteed by characterization
SID262	T _{CLKSWITCH}	Clock switching from clk1 to clk2 in clk1 periods	3	–	4	Periods	Guaranteed by design

* T_{WS24} is guaranteed by design

Ordering Information

The PSoC 4100M family part numbers and features are listed in the following table.

Category	MPN	Features														Package				
		Max CPU Speed (MHz)	Flash (KB)	SRAM (KB)	UDB	Opamp (CTBm)	CSD	IDAC (1X7-Bit, 1-8-Bit)	Direct LCD Drive	12-bit SAR ADC	LP Comparators	TCPWM Blocks	SCB Blocks	CAN	GPIO	44-TQFP	48-TQFP	64-TQFP (0.5-mm pitch)	64-TQFP (0.8-mm pitch)	68-QFN
4125	CY8C4125AZI-M433	24	32	4	0	2	–	–	–	806 ksp/s	2	8	4	–	38	–	✓	–	–	–
	CY8C4125AZI-M443	24	32	4	0	2	✓	–	✓	806 ksp/s	2	8	4	–	38	–	✓	–	–	–
	CY8C4125AZI-M445	24	32	4	0	2	✓	–	✓	806 ksp/s	2	8	4	–	51	–	–	✓	–	–
	CY8C4125LTI-M445	24	32	4	0	2	✓	–	✓	806 ksp/s	2	8	4	–	55	–	–	–	–	✓
	CY8C4125AXI-M445	24	32	4	0	2	✓	–	✓	806 ksp/s	2	8	4	–	51	–	–	–	✓	–
4126	CY8C4126AZI-M443	24	64	8	0	2	✓	–	✓	806 ksp/s	2	8	4	–	38	–	✓	–	–	–
	CY8C4126AXI-M443	24	64	8	0	2	✓	–	✓	806 ksp/s	2	8	4	–	36	✓	–	–	–	–
	CY8C4126AZI-M445	24	64	8	0	2	✓	–	✓	806 ksp/s	2	8	4	–	51	–	–	✓	–	–
	CY8C4126AZI-M475	24	64	8	0	4	–	✓	–	806 ksp/s	2	8	4	–	51	–	–	✓	–	–
	CY8C4126LTI-M445	24	64	8	0	2	✓	–	✓	806 ksp/s	2	8	4	–	55	–	–	–	–	✓
	CY8C4126LTI-M475	24	64	8	0	4	–	✓	–	806 ksp/s	2	8	4	–	55	–	–	–	–	✓
	CY8C4126AXI-M445	24	64	8	0	2	✓	–	✓	806 ksp/s	2	8	4	–	51	–	–	–	✓	–
4127	CY8C4127LTI-M475	24	128	16	0	4	✓	✓	–	806 ksp/s	2	8	4	–	55	–	–	–	–	✓
	CY8C4127AZI-M475	24	128	16	0	4	–	✓	–	806 ksp/s	2	8	4	–	51	–	–	✓	–	–
	CY8C4127AZI-M485	24	128	16	0	4	✓	✓	✓	806 ksp/s	2	8	4	–	51	–	–	✓	–	–
	CY8C4127AXI-M485	24	128	16	0	4	✓	✓	✓	806 ksp/s	2	8	4	–	51	–	–	–	✓	–

The nomenclature used in the preceding table is based on the following part numbering convention:

Field	Description	Values	Meaning
CY8C	Cypress Prefix		
4	Architecture	4	PSoC 4
A	Family	1	4100 Family
B	CPU Speed	4	48 MHz
C	Flash Capacity	4	16 KB
		5	32 KB
		6	64 KB
		7	128 KB
DE	Package Code	AX, AZ	TQFP
		LQ	QFN
		BU	BGA
		FD	CSP
F	Temperature Range	I	Industrial
		Q	Extended Industrial
S	Silicon Family	N/A	PSoC 4 Base Series
		L	PSoC 4 L-Series
		BL	PSoC 4 BLE
		M	PSoC 4 M-Series
XYZ	Attributes Code	000-999	Code of feature set in the specific family

Part Numbering Conventions

The part number fields are defined as follows.

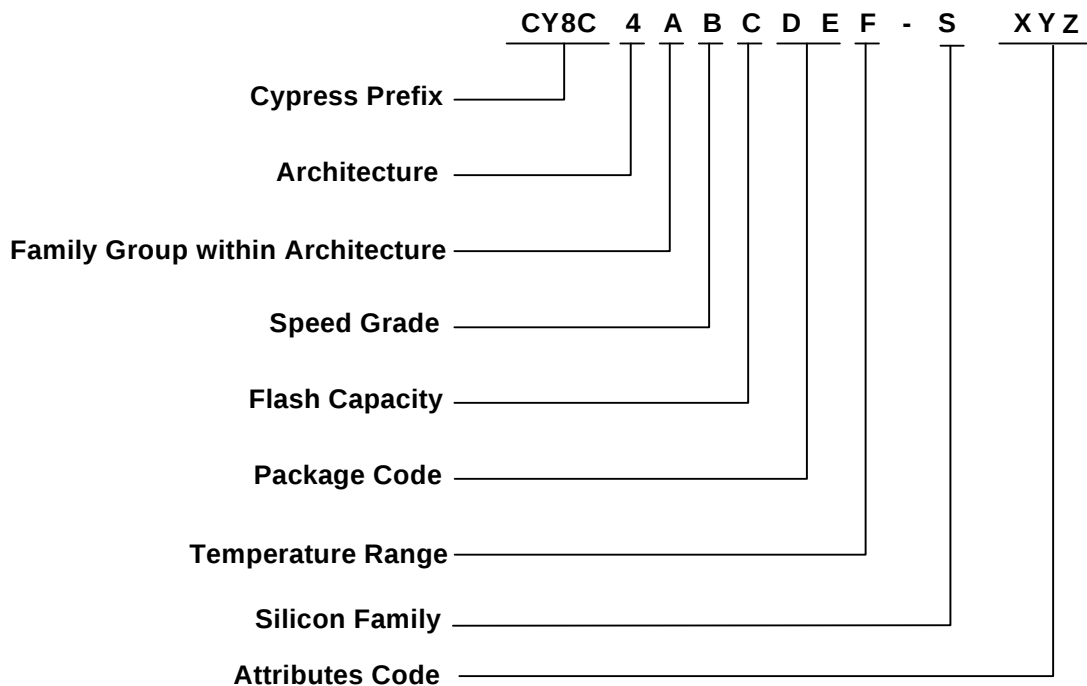
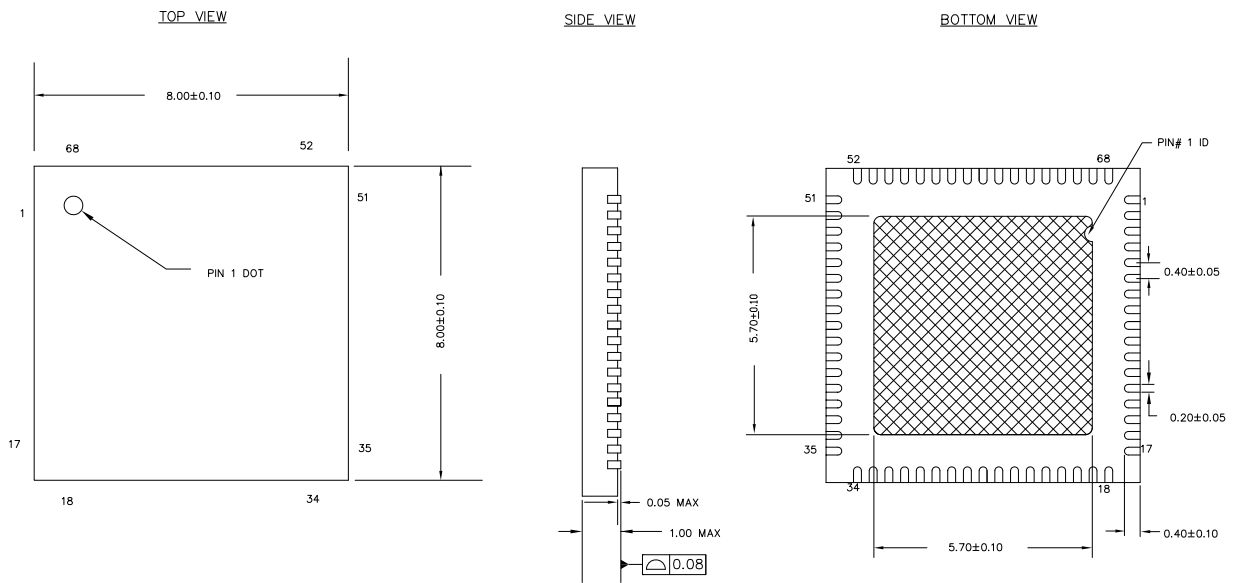


Figure 5. 68-Pin 8 × 8 × 1.0 mm QFN Package Outline

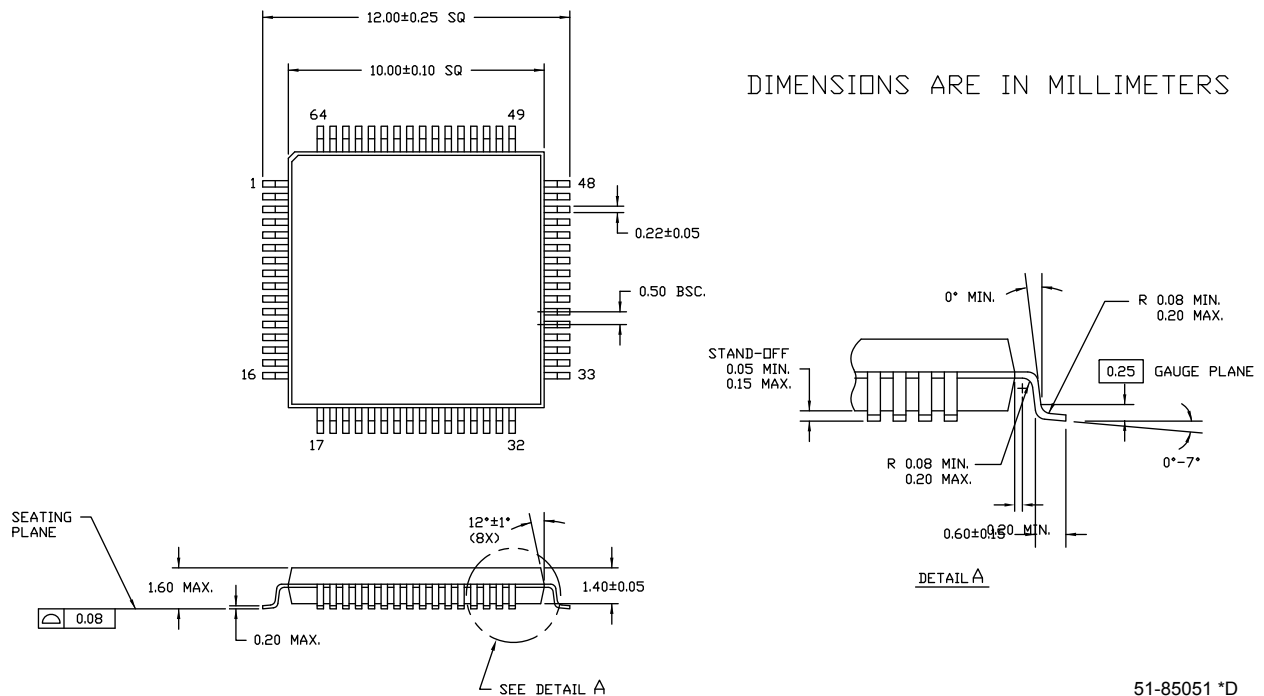


NOTES:

1.  HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 17 ± 2mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-09618 *E

Figure 6. 64-Pin 10 × 10 × 1.4 mm TQFP Package Outline



51-85051 *D

Figure 7. 64-Pin 14 × 14 × 1.4 mm TQFP Package Outline

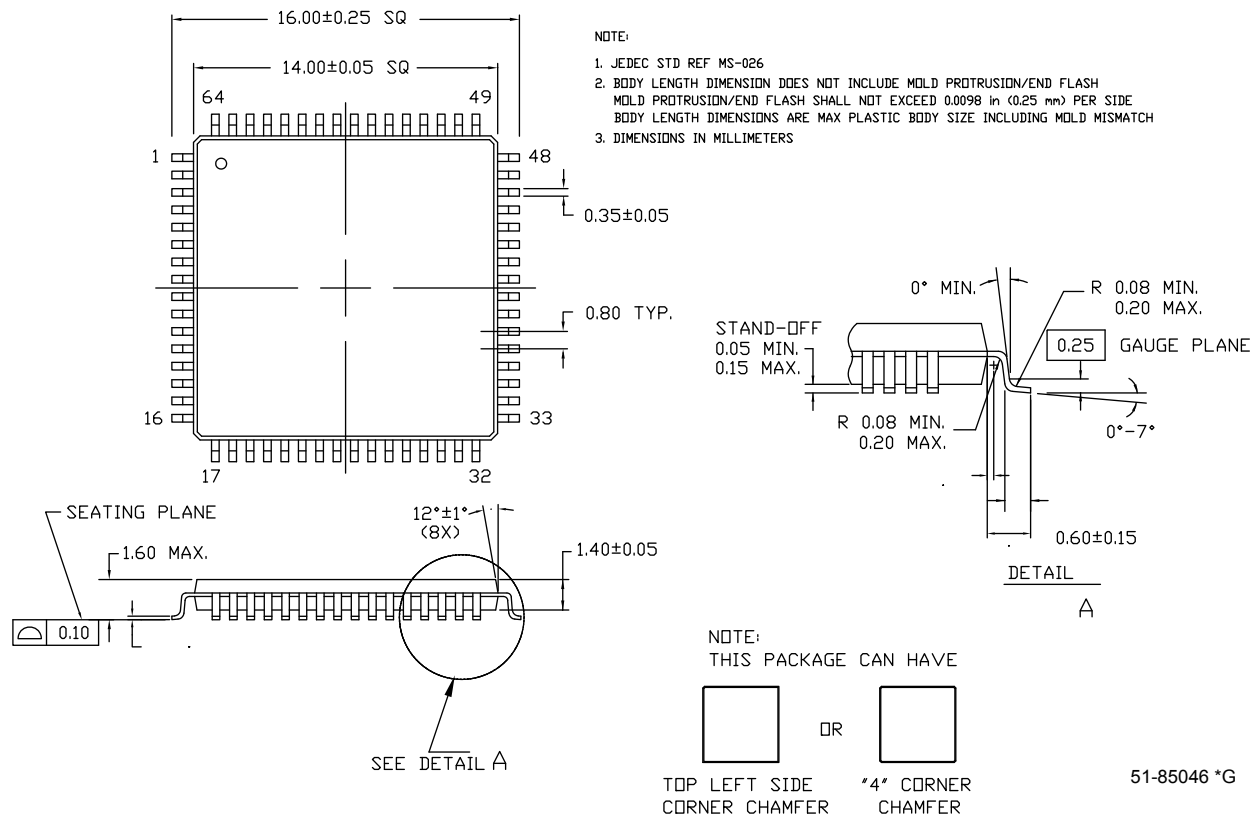


Figure 8. 48-Pin 7 × 7 × 1.4 mm TQFP Package Outline

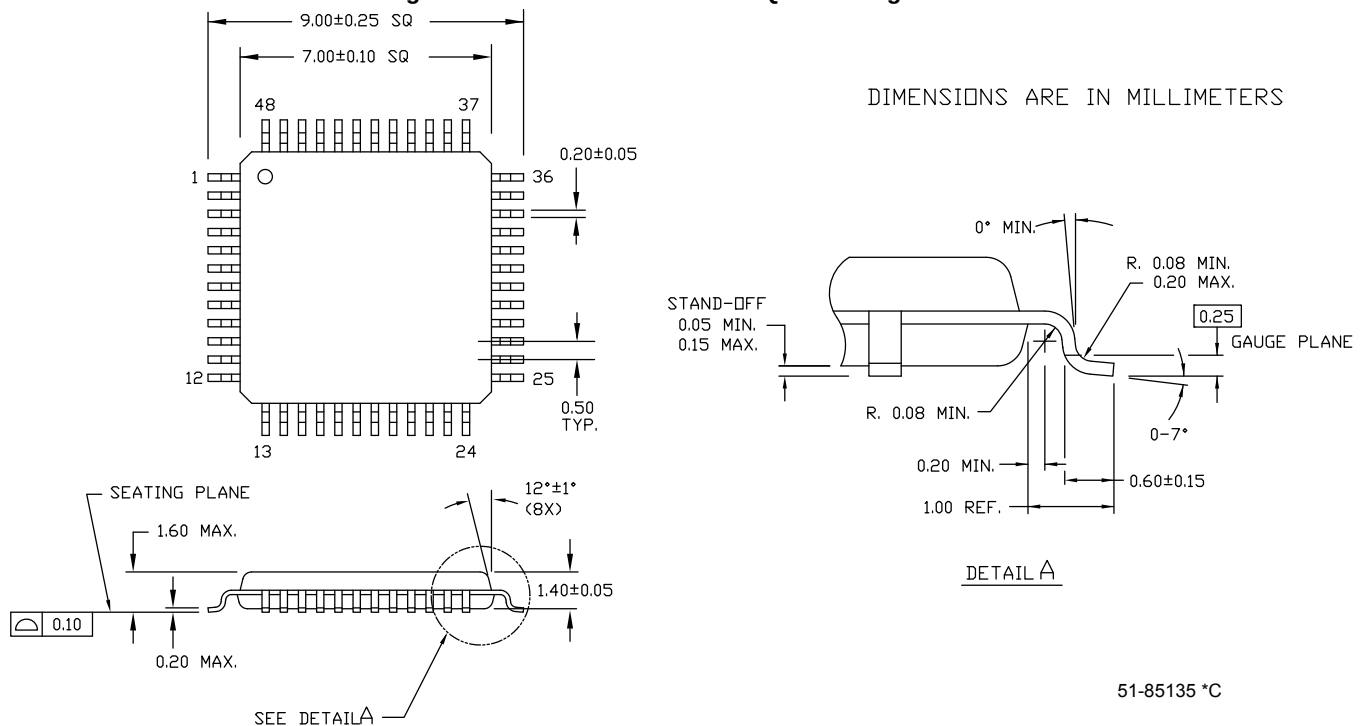
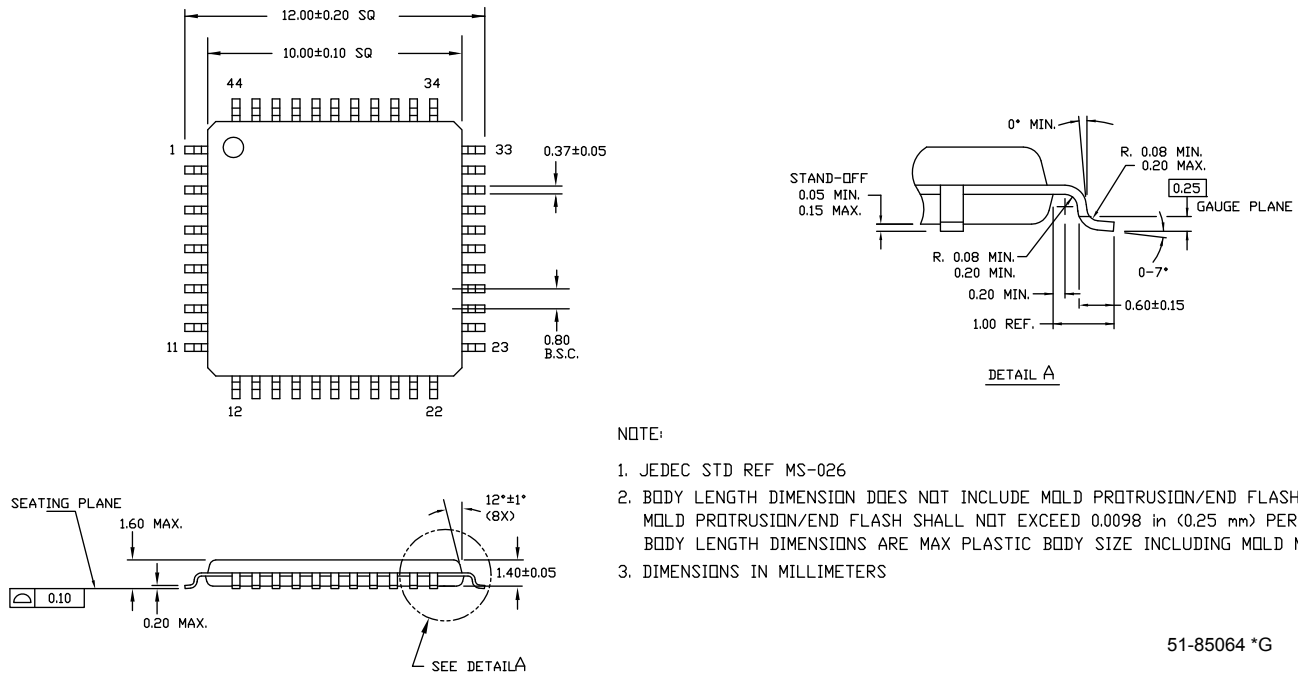


Figure 9. 44-Pin 10 × 10 × 1.4 mm TQFP Package Outline



NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85064 *G