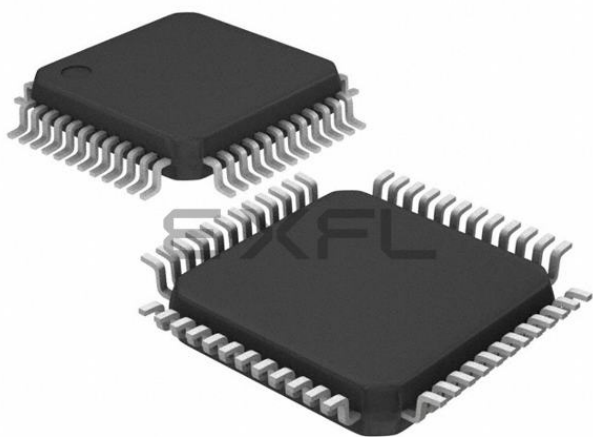




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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I ² C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, CapSense, LCD, LVD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b SAR; 2xIDAC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4126azi-m443

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article [KBA86521](#), [How to Design with PSoC 3](#), [PSoC 4](#), and [PSoC 5LP](#). Following is an abbreviated list for PSoC 4:

- Overview: [PSoC Portfolio](#), [PSoC Roadmap](#)
- Product Selectors: [PSoC 1](#), [PSoC 3](#), [PSoC 4](#), [PSoC 5LP](#)
In addition, PSoC Creator includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 4 are:
 - [AN79953](#): Getting Started With PSoC 4
 - [AN88619](#): PSoC 4 Hardware Design Considerations
 - [AN86439](#): Using PSoC 4 GPIO Pins
 - [AN57821](#): Mixed Signal Circuit Board Layout
 - [AN81623](#): Digital Design Best Practices
 - [AN73854](#): Introduction To Bootloaders
 - [AN89610](#): ARM Cortex Code Optimization
- Technical Reference Manual (TRM) is in two documents:
 - [Architecture TRM](#) details each PSoC 4 functional block.
 - [Registers TRM](#) describes each of the PSoC 4 registers.
- Development Kits:
 - [CY8CKIT-042](#), PSoC 4 Pioneer Kit, is an easy-to-use and inexpensive development platform. This kit includes connectors for Arduino™ compatible shields and Digilent® Pmod™ daughter cards.
 - [CY8CKIT-049](#) is a very low-cost prototyping platform. It is a low-cost alternative to sampling PSoC 4 devices.
 - [CY8CKIT-001](#) is a common development platform for any one of the PSoC 1, PSoC 3, PSoC 4, or PSoC 5LP families of devices.

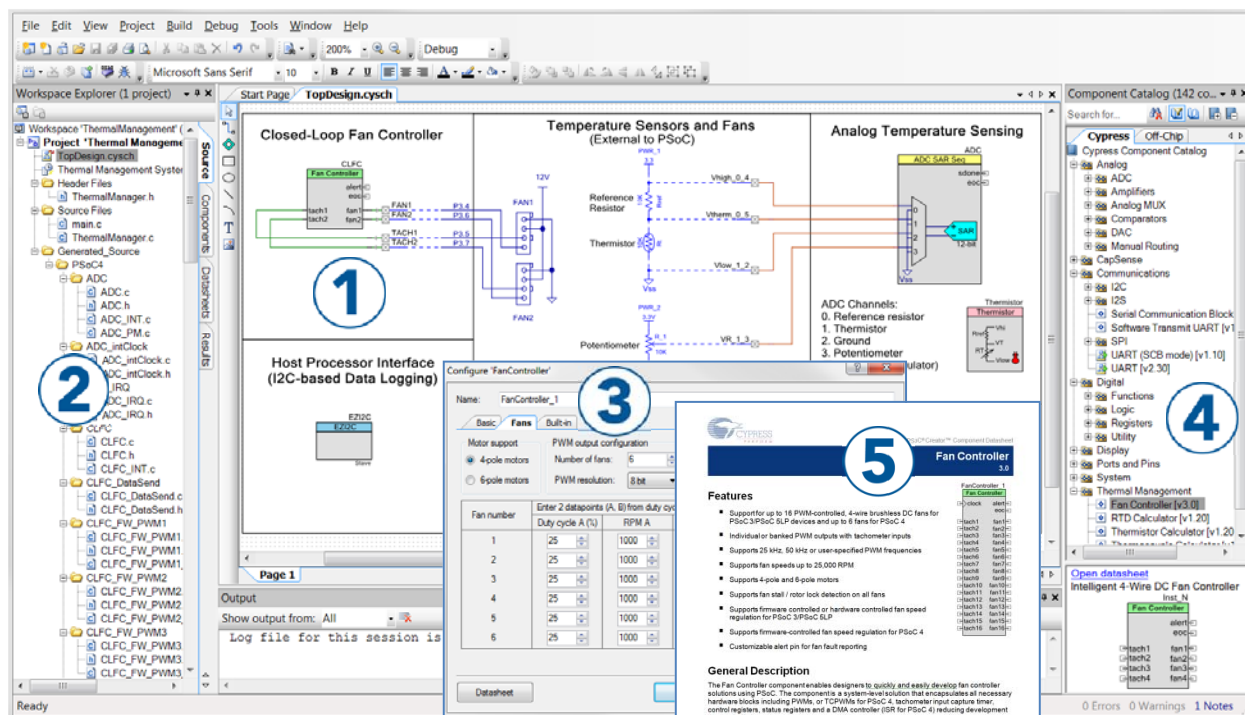
The [MiniProg3](#) device provides an interface for flash programming and debug.

PSoC Creator

[PSoC Creator](#) is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC 3, PSoC 4, and PSoC 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC Components; see the [list of component datasheets](#). With PSoC Creator, you can:

1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

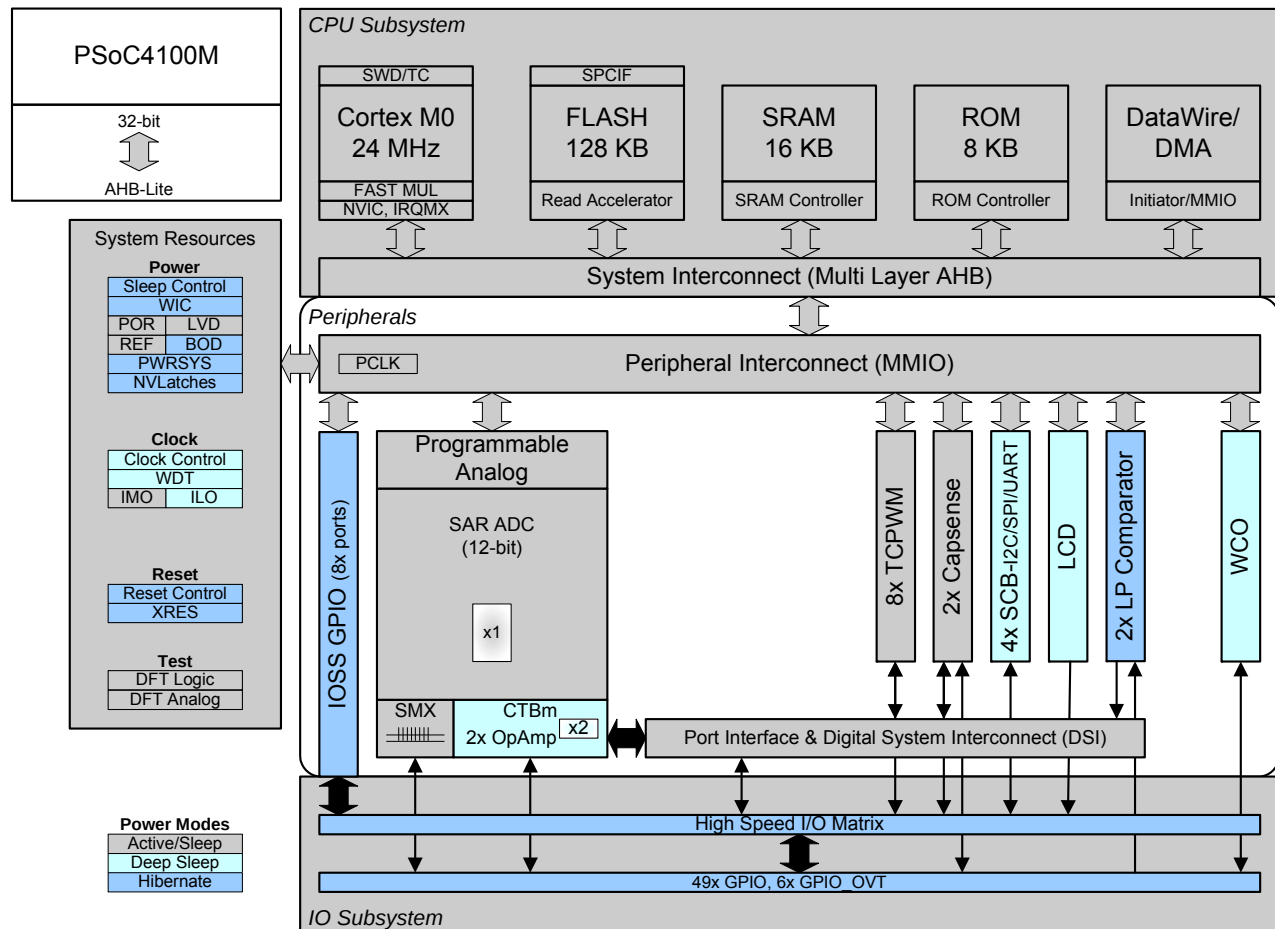
Figure 1. Multiple-Sensor Example Project in PSoC Creator



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PSoC 4100M Block Diagram



The PSoC 4100-M devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The ARM Serial_Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator Integrated Development Environment (IDE) provides fully integrated programming and debug support for PSoC 4100-M devices. The SWD interface is fully compatible with industry-standard third-party tools. The PSoC 4100-M family provides a level of security not possible with multi-chip application solutions or with microcontrollers. This is due to its ability to disable debug features, robust flash protection, and

because it allows customer-proprietary functionality to be implemented in on-chip programmable blocks.

The debug circuits are enabled by default and can only be disabled in firmware. If not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. Because all programming, debug, and test interfaces are disabled when maximum device security is enabled, PSoC 4100-M with device security enabled may not be returned for failure analysis. This is a trade-off the PSoC 4100-M allows the customer to make.

68-QFN		64-TQFP		48-TQFP		44-TQFP	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
8	P2.6	8	P2.6	8	P2.6	8	P2.6
9	P2.7	9	P2.7	9	P2.7	9	P2.7
10	VSSA	10	VSSA	10	VSSD	10	VSSD
11	VDDA	11	VDDA				
12	P6.0	12	P6.0				
13	P6.1	13	P6.1				
14	P6.2	14	P6.2				
15	P6.3						
16	P6.4	15	P6.4				
17	P6.5	16	P6.5				
18	VSSIO	17	VSSIO	10	VSSD	10	VSSD
19	P3.0	18	P3.0	12	P3.0	11	P3.0
20	P3.1	19	P3.1	13	P3.1	12	P3.1
21	P3.2	20	P3.2	14	P3.2	13	P3.2
22	P3.3	21	P3.3	16	P3.3	14	P3.3
23	P3.4	22	P3.4	17	P3.4	15	P3.4
24	P3.5	23	P3.5	18	P3.5	16	P3.5
25	P3.6	24	P3.6	19	P3.6	17	P3.6
26	P3.7	25	P3.7	20	P3.7	18	P3.7
27	VDDIO	26	VDDIO	21	VDDIO	19	VDDD
28	P4.0	27	P4.0	22	P4.0	20	P4.0
29	P4.1	28	P4.1	23	P4.1	21	P4.1
30	P4.2	29	P4.2	24	P4.2	22	P4.2
31	P4.3	30	P4.3	25	P4.3	23	P4.3
32	P4.4	31	P4.4				
33	P4.5	32	P4.5				
34	P4.6	33	P4.6				
35	P4.7						
39	P7.0	37	P7.0	26	P7.0		
40	P7.1	38	P7.1	27	P7.1		
41	P7.2						

The pins of Port 6 are overvoltage-tolerant. Pins 36, 37, and 38 are No-Connects on the 68-pin QFN. Pins 34, 35, and 36 are No-Connects on the 64-pin TQFP. Pins 11 and 15 are No-connects in the 48-pin TQFP. All VSS pins must be tied together.

The output drivers of I/O Ports P0 and P7 are connected to VDDD. Output drivers of I/O Ports 1, 2, and 5 are connected to VDDA. Output drivers of I/O Ports 3, 4, and 6 are connected to VDDIO.

Development Support

The PSoC 4100M family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit www.cypress.com/go/psoc4 to find out more.

Documentation

A suite of documentation supports the PSoC 4100M family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

Software User Guide: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

Component Datasheets: The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

Application Notes: PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

Technical Reference Manual: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers.

Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

Tools

With industry standard cores, programming, and debugging interfaces, the PSoC 4100M family is part of a development tool ecosystem. Visit us at www.cypress.com/go/psoccreator for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

Table 3. AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID48	F _{CPU}	CPU frequency	DC	–	24	MHz	1.71 ≤ V _{DD} ≤ 5.5
SID49	T _{SLEEP}	Wakeup from sleep mode	–	0	–	μs	Guaranteed by characterization
SID50	T _{DEEPSLEEP}	Wakeup from Deep Sleep mode	–	–	25	μs	24 MHz IMO. Guaranteed by characterization
SID51	T _{HIBERNATE}	Wakeup from Hibernate mode	–	–	0.7	ms	Guaranteed by characterization
SID51A	T _{STOP}	Wakeup from Stop mode	–	–	2	ms	Guaranteed by characterization
SID52	T _{RESETWIDTH}	External reset pulse width	1	–	–	μs	Guaranteed by characterization

GPIO

Table 4. GPIO DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID57	V _{IH} ^[2]	Input voltage high threshold	0.7 × V _{DDD}	–	–	V	CMOS Input
SID57A	I _{IHS}	Input current when Pad > V _{DDIO} for OVT inputs	–	–	10	μA	Per I ² C Spec
SID58	V _{IL}	Input voltage low threshold	–	–	0.3 × V _{DDD}	V	CMOS Input
SID241	V _{IH} ^[2]	LVTTL input, V _{DDD} < 2.7 V	0.7 × V _{DDD}	–	–	V	
SID242	V _{IL}	LVTTL input, V _{DDD} < 2.7 V	–	–	0.3 × V _{DDD}	V	
SID243	V _{IH} ^[2]	LVTTL input, V _{DDD} ≥ 2.7 V	2.0	–	–	V	
SID244	V _{IL}	LVTTL input, V _{DDD} ≥ 2.7 V	–	–	0.8	V	
SID59	V _{OH}	Output voltage high level	V _{DDD} – 0.6	–	–	V	I _{OH} = 4 mA at 3 V V _{DDD}
SID60	V _{OH}	Output voltage high level	V _{DDD} – 0.5	–	–	V	I _{OH} = 1 mA at 1.8 V V _{DDD}
SID61	V _{OL}	Output voltage low level	–	–	0.6	V	I _{OL} = 4 mA at 1.8 V V _{DDD}
SID62	V _{OL}	Output voltage low level	–	–	0.6	V	I _{OL} = 8 mA at 3 V V _{DDD}
SID62A	V _{OL}	Output voltage low level	–	–	0.4	V	I _{OL} = 3 mA at 3 V V _{DDD}
SID63	R _{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID64	R _{PULLDOWN}	Pull-down resistor	3.5	5.6	8.5	kΩ	
SID65	I _{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V _{DDD} = 3.0 V. Guaranteed by characterization

Note

 2. V_{IH} must not exceed V_{DDD} + 0.2 V.

Table 4. GPIO DC Specifications (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID65A	I_{IL_CTBM}	Input leakage current (absolute value) for CTBM pins	–	–	4	nA	Guaranteed by characterization
SID66	C_{IN}	Input capacitance	–	–	7	pF	
SID67	V_{HYSTTL}	Input hysteresis LVTTTL	25	40	–	mV	$V_{DD} \geq 2.7\text{ V}$
SID68	$V_{HYSCMOS}$	Input hysteresis CMOS	$0.05 \times V_{DD}$	–	–	mV	
SID69	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	μA	Guaranteed by characterization
SID69A	I_{TOT_GPIO}	Maximum Total Source or Sink Chip Current	–	–	200	mA	Guaranteed by characterization

Table 5. GPIO AC Specifications

(Guaranteed by Characterization)^[3]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID70	T_{RISEF}	Rise time in fast strong mode	2	–	12	ns	3.3 V V_{DD} , Load = 25 pF
SID71	T_{FALLF}	Fall time in fast strong mode	2	–	12	ns	3.3 V V_{DD} , Load = 25 pF
SID72	T_{RISES}	Rise time in slow strong mode	10	–	60	ns	3.3 V V_{DD} , Load = 25 pF
SID73	T_{FALLS}	Fall time in slow strong mode	10	–	60	ns	3.3 V V_{DD} , Load = 25 pF
SID74	$F_{GPIOUT1}$	GPIO Fout; 3.3 V $\leq V_{DD} \leq 5.5\text{ V}$. Fast strong mode.	–	–	24	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID75	$F_{GPIOUT2}$	GPIO Fout; 1.7 V $\leq V_{DD} \leq 3.3\text{ V}$. Fast strong mode.	–	–	16.7	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID76	$F_{GPIOUT3}$	GPIO Fout; 3.3 V $\leq V_{DD} \leq 5.5\text{ V}$. Slow strong mode.	–	–	7	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID245	$F_{GPIOUT4}$	GPIO Fout; 1.7 V $\leq V_{DD} \leq 3.3\text{ V}$. Slow strong mode.	–	–	3.5	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID246	F_{GPIOIN}	GPIO input operating frequency; 1.71 V $\leq V_{DD} \leq 5.5\text{ V}$	–	–	48	MHz	90/10% V_{IO}

Note

3. Simultaneous switching transitions on many fully-loaded GPIO pins may cause ground perturbations depending on several factors including PCB and decoupling capacitor design. For applications that are very sensitive to ground perturbations, the slower GPIO slew rate setting may be used.

XRES

Table 6. XRES DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID77	V_{IH}	Input voltage high threshold	$0.7 \times V_{DD}$	–	–	V	CMOS Input
SID78	V_{IL}	Input voltage low threshold	–	–	$0.3 \times V_{DD}$	V	CMOS Input
SID79	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	k Ω	
SID80	C_{IN}	Input capacitance	–	3	–	pF	
SID81	$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	Guaranteed by characterization
SID82	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	μ A	Guaranteed by characterization

Table 7. XRES AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID83	$T_{RESETWIDTH}$	Reset pulse width	1	–	–	μ s	Guaranteed by characterization

Table 8. Opamp Specifications

(Guaranteed by Characterization) (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID293	V _{N1}	Input referred, 1 Hz - 1GHz, power = high	–	94	–	μVrms	
SID294	V _{N2}	Input referred, 1 kHz, power = high	–	72	–	nV/rtHz	
SID295	V _{N3}	Input referred, 10kHz, power = high	–	28	–	nV/rtHz	
SID296	V _{N4}	Input referred, 100kHz, power = high	–	15	–	nV/rtHz	
SID297	Cload	Stable up to maximum load. Performance specs at 50 pF.	–	–	125	pF	
SID298	Slew_rate	Cload = 50 pF, Power = High, V _{DDA} ≥ 2.7 V	6	–	–	V/μs	
SID299	T _{op_wake}	From disable to enable, no external RC dominating	–	25	–	μs	
SID299A	OL_GAIN	Open Loop Gain	–	90	–	dB	
	Comp_mode	Comparator mode; 50 mV drive, Trise = Tfall (approx.)	–	–	–		
SID300	T _{PD1}	Response time; power = high	–	150	–	ns	
SID301	T _{PD2}	Response time; power = medium	–	400	–	ns	
SID302	T _{PD3}	Response time; power = low	–	2000	–	ns	
SID303	V _{hyst_op}	Hysteresis	–	10	–	mV	
Deep Sleep Mode		Mode 2 is lowest current range. Mode 1 has higher GBW.					Deep Sleep mode. V _{DDA} ≥ 2.7 V.
SID_DS_1	IDD_HI_M1	Mode 1, High current	–	1400	–	uA	25 °C
SID_DS_2	IDD_MED_M1	Mode 1, Medium current	–	700	–	uA	25 °C
SID_DS_3	IDD_LOW_M1	Mode 1, Low current	–	200	–	uA	25 °C
SID_DS_4	IDD_HI_M2	Mode 2, High current	–	120	–	uA	25 °C
SID_DS_5	IDD_MED_M2	Mode 2, Medium current	–	60	–	uA	25 °C
SID_DS_6	IDD_LOW_M2	Mode 2, Low current	–	15	–	uA	25 °C
SID_DS_7	GBW_HI_M1	Mode 1, High current	–	4	–	MHz	25 °C
SID_DS_8	GBW_MED_M1	Mode 1, Medium current	–	2	–	MHz	25 °C
SID_DS_9	GBW_LOW_M1	Mode 1, Low current	–	0.5	–	MHz	25 °C
SID_DS_10	GBW_HI_M2	Mode 2, High current	–	0.5	–	MHz	20-pF load, no DC load 0.2 V to V _{DDA} -1.5 V
SID_DS_11	GBW_MED_M2	Mode 2, Medium current	–	0.2	–	MHz	20-pF load, no DC load 0.2 V to V _{DDA} -1.5 V
SID_DS_12	GBW_LOW_M2	Mode 2, Low current	–	0.1	–	MHz	20-pF load, no DC load 0.2 V to V _{DDA} -1.5 V
SID_DS_13	VOS_HI_M1	Mode 1, High current	–	5	–	mV	With trim 25 °C, 0.2 V to V _{DDA} -1.5 V
SID_DS_14	VOS_MED_M1	Mode 1, Medium current	–	5	–	mV	With trim 25 °C, 0.2 V to V _{DDA} -1.5 V
SID_DS_15	VOS_LOW_M1	Mode 1, Low current	–	5	–	mV	With trim 25 °C, 0.2 V to V _{DDA} -1.5 V
SID_DS_16	VOS_HI_M2	Mode 2, High current	–	5	–	mV	With trim 25 °C, 0.2 V to V _{DDA} -1.5 V
SID_DS_17	VOS_MED_M2	Mode 2, Medium current	–	5	–	mV	With trim 25 °C, 0.2 V to V _{DDA} -1.5 V

Table 8. Opamp Specifications

(Guaranteed by Characterization) (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID_DS_18	VOS_LOW_M2	Mode 2, Low current	–	5	–	mV	With trim 25 °C, 0.2 V to V _{DDA} -1.5 V
SID_DS_19	IOUT_HI_M1	Mode 1, High current	–	10	–	mA	Output is 0.5 V to V _{DDA} -0.5 V
SID_DS_20	IOUT_MED_M1	Mode 1, Medium current	–	10	–	mA	Output is 0.5 V to V _{DDA} -0.5 V
SID_DS_21	IOUT_LOW_M1	Mode 1, Low current	–	4	–	mA	Output is 0.5 V to V _{DDA} -0.5 V
SID_DS_22	IOUT_HI_M2	Mode 2, High current	–	1	–	mA	Output is 0.5 V to V _{DDA} -0.5 V
SID_DS_23	IOUT_MED_M2	Mode 2, Medium current	–	1	–	mA	Output is 0.5 V to V _{DDA} -0.5 V
SID_DS_24	IOUT_LOW_M2	Mode 2, Low current	–	0.5	–	mA	Output is 0.5 V to V _{DDA} -0.5 V

Comparator

Table 9. Comparator DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID85	V _{OFFSET2}	Input offset voltage, Common Mode voltage range from 0 to V _{DD} -1	–	–	±4	mV	
SID85A	V _{OFFSET3}	Input offset voltage. Ultra low-power mode (V _{DDD} ≥ 2.2 V for Temp < 0 °C, V _{DDD} ≥ 1.8 V for Temp > 0 °C).	–	±12	–	mV	
SID86	V _{HYST}	Hysteresis when enabled, Common Mode voltage range from 0 to V _{DD} -1.	–	10	35	mV	Guaranteed by characterization
SID87	V _{ICM1}	Input common mode voltage in normal mode	0	–	V _{DDD} -0.1	V	Modes 1 and 2.
SID247	V _{ICM2}	Input common mode voltage in low power mode	0	–	V _{DDD}	V	
SID247A	V _{ICM3}	Input common mode voltage in ultra low power mode (V _{DDD} ≥ 2.2 V for Temp < 0 °C, V _{DDD} ≥ 1.8 V for Temp > 0 °C)	0	–	V _{DDD} -1.15	V	
SID88	CMRR	Common mode rejection ratio	50	–	–	dB	V _{DDD} ≥ 2.7 V. Guaranteed by characterization
SID88A	CMRR	Common mode rejection ratio	42	–	–	dB	V _{DDD} < 2.7 V. Guaranteed by characterization
SID89	I _{CMP1}	Block current, normal mode	–	–	400	μA	Guaranteed by characterization
SID248	I _{CMP2}	Block current, low power mode	–	–	100	μA	Guaranteed by characterization
SID259	I _{CMP3}	Block current, ultra low power mode (V _{DDD} ≥ 2.2 V for Temp < 0 °C, V _{DDD} ≥ 1.8 V for Temp > 0 °C)	–	6	28	μA	Guaranteed by characterization
SID90	Z _{CMP}	DC input impedance of comparator	35	–	–	MΩ	Guaranteed by characterization

Table 13. SAR ADC AC Specifications

(Guaranteed by Characterization) (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID108A	A_SAMP_2	Sample rate with no bypass cap. Reference = V_{DD}	–	–	500	ksps	
SID108B	A_SAMP_3	Sample rate with no bypass cap. Internal reference	–	–	100	ksps	
SID109	A_SNR	Signal-to-noise and distortion ratio (SINAD)	66	–	–	dB	$F_{IN} = 10 \text{ kHz}$
SID111	A_INL	Integral non linearity	–1.4	–	+1.4	LSB	$V_{DD} = 1.71 \text{ to } 5.5$, 806 Ksps, $V_{ref} = 1 \text{ to } 5.5$.
SID111A	A_INL	Integral non linearity	–1.4	–	+1.4	LSB	$V_{DDD} = 1.71 \text{ to } 3.6$, 806 Ksps, $V_{ref} = 1.71$ to V_{DDD} .
SID111B	A_INL	Integral non linearity	–1.4	–	+1.4	LSB	$V_{DDD} = 1.71 \text{ to } 5.5$, 500 Ksps, $V_{ref} = 1 \text{ to } 5.5$.
SID112	A_DNL	Differential non linearity	–0.9	–	+1.35	LSB	$V_{DDD} = 1.71 \text{ to } 5.5$, 806 Ksps, $V_{ref} = 1 \text{ to } 5.5$.
SID112A	A_DNL	Differential non linearity	–0.9	–	+1.35	LSB	$V_{DDD} = 1.71 \text{ to } 3.6$, 806 Ksps, $V_{ref} = 1.71$ to V_{DDD} .
SID112B	A_DNL	Differential non linearity	–0.9	–	+1.35	LSB	$V_{DDD} = 1.71 \text{ to } 5.5$, 500 Ksps, $V_{ref} = 1 \text{ to } 5.5$.
SID113	A_THD	Total harmonic distortion	–	–	–65	dB	$F_{IN} = 10 \text{ kHz}$.

CSD

Table 14. CSD Block Specification

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
CSD Specification							
SID308	VCSD	Voltage range of operation	1.71	–	5.5	V	
SID309	IDAC1	DNL for 8-bit resolution	–1	–	1	LSB	
SID310	IDAC1	INL for 8-bit resolution	–3	–	3	LSB	
SID311	IDAC2	DNL for 7-bit resolution	–1	–	1	LSB	
SID312	IDAC2	INL for 7-bit resolution	–3	–	3	LSB	
SID313	SNR	Ratio of counts of finger to noise. Guaranteed by characterization	5	–	–	Ratio	Capacitance range of 9 to 35 pF, 0.1 pF sensitivity
SID314	IDAC1_CRT1	Output current of Idac1 (8-bits) in High range	–	612	–	μA	
SID314A	IDAC1_CRT2	Output current of Idac1(8-bits) in Low range	–	306	–	μA	
SID315	IDAC2_CRT1	Output current of Idac2 (7-bits) in High range	–	304.8	–	μA	
SID315A	IDAC2_CRT2	Output current of Idac2 (7-bits) in Low range	–	152.4	–	μA	

Table 24. Fixed SPI Master mode AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID167	T _{DMO}	MOSI valid after Scklock driving edge	–	–	15	ns	
SID168	T _{DSI}	MISO valid before Scklock capturing edge. Full clock, late MISO Sampling used	20	–	–	ns	
SID169	T _{HMO}	Previous MOSI data hold time with respect to capturing edge at Slave	0	–	–	ns	

Table 25. Fixed SPI Slave mode AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID170	T _{DMI}	MOSI valid before Scklock capturing edge	40	–	–	ns	
SID171	T _{DSO}	MISO valid after Scklock driving edge	–	–	42 + 3 × (1/FCPU)	ns	
SID171A	T _{DSO_ext}	MISO valid after Scklock driving edge in Ext. Clock mode	–	–	48	ns	
SID172	T _{HSO}	Previous MISO data hold time	0	–	–	ns	
SID172A	T _{SSELSCK}	SSEL Valid to first SCK Valid edge	100	–	–	ns	

Memory

Table 26. Flash DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID173	V _{PE}	Erase and program voltage	1.71	–	5.5	V	

Table 27. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID174	T _{ROWWRITE}	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 128 bytes
SID175	T _{ROWERASE}	Row erase time	–	–	13	ms	
SID176	T _{ROWPROGRAM}	Row program time after erase	–	–	7	ms	
SID178	T _{BULKERASE}	Bulk erase time (128 KB)	–	–	35	ms	
SID179	T _{SECTORERASE}	Sector erase time (8 KB)	–	–	15	ms	
SID180	T _{DEVPROG}	Total device program time	–	–	15	seconds	Guaranteed by characterization
SID181	F _{END}	Flash endurance	100 K	–	–	cycles	Guaranteed by characterization
SID182	F _{RET}	Flash retention. T _A ≤ 55 °C, 100 K P/E cycles	20	–	–	years	Guaranteed by characterization
SID182A		Flash retention. T _A ≤ 85 °C, 10 K P/E cycles	10	–	–	years	Guaranteed by characterization
SID182B	F _{RETQ}	Flash retention. T _A ≤ 105 °C, 10K P/E cycles, ≤ three years at T _A ≥ 85 °C	10	20	–	years	Guaranteed by characterization.

System Resources

Power-on-Reset (POR) with Brown Out

Table 28. Imprecise Power On Reset (PRES)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID185	V _{RISEIPOR}	Rising trip voltage	0.80	–	1.45	V	Guaranteed by characterization
SID186	V _{FALLIPOR}	Falling trip voltage	0.75	–	1.4	V	Guaranteed by characterization
SID187	V _{IPORHYST}	Hysteresis	15	–	200	mV	Guaranteed by characterization

Table 29. Precise Power On Reset (POR)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190	V _{FALLPPOR}	BOD trip voltage in active and sleep modes	1.64	–	–	V	Guaranteed by characterization
SID192	V _{FALLDPSLP}	BOD trip voltage in Deep Sleep	1.4	–	–	V	Guaranteed by characterization

Voltage Monitors

Table 30. Voltage Monitors DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID195	V _{LVI1}	LVI_A/D_SEL[3:0] = 0000b	1.71	1.75	1.79	V	
SID196	V _{LVI2}	LVI_A/D_SEL[3:0] = 0001b	1.76	1.80	1.85	V	
SID197	V _{LVI3}	LVI_A/D_SEL[3:0] = 0010b	1.85	1.90	1.95	V	
SID198	V _{LVI4}	LVI_A/D_SEL[3:0] = 0011b	1.95	2.00	2.05	V	
SID199	V _{LVI5}	LVI_A/D_SEL[3:0] = 0100b	2.05	2.10	2.15	V	
SID200	V _{LVI6}	LVI_A/D_SEL[3:0] = 0101b	2.15	2.20	2.26	V	
SID201	V _{LVI7}	LVI_A/D_SEL[3:0] = 0110b	2.24	2.30	2.36	V	
SID202	V _{LVI8}	LVI_A/D_SEL[3:0] = 0111b	2.34	2.40	2.46	V	
SID203	V _{LVI9}	LVI_A/D_SEL[3:0] = 1000b	2.44	2.50	2.56	V	
SID204	V _{LVI10}	LVI_A/D_SEL[3:0] = 1001b	2.54	2.60	2.67	V	
SID205	V _{LVI11}	LVI_A/D_SEL[3:0] = 1010b	2.63	2.70	2.77	V	
SID206	V _{LVI12}	LVI_A/D_SEL[3:0] = 1011b	2.73	2.80	2.87	V	
SID207	V _{LVI13}	LVI_A/D_SEL[3:0] = 1100b	2.83	2.90	2.97	V	
SID208	V _{LVI14}	LVI_A/D_SEL[3:0] = 1101b	2.93	3.00	3.08	V	
SID209	V _{LVI15}	LVI_A/D_SEL[3:0] = 1110b	3.12	3.20	3.28	V	
SID210	V _{LVI16}	LVI_A/D_SEL[3:0] = 1111b	4.39	4.50	4.61	V	
SID211	LVI_IDD	Block current	–	–	100	μA	Guaranteed by characterization

Table 31. Voltage Monitors AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID212	T _{MONTRIP}	Voltage monitor trip time	–	–	1	μs	Guaranteed by characterization

Ordering Information

The PSoC 4100M family part numbers and features are listed in the following table.

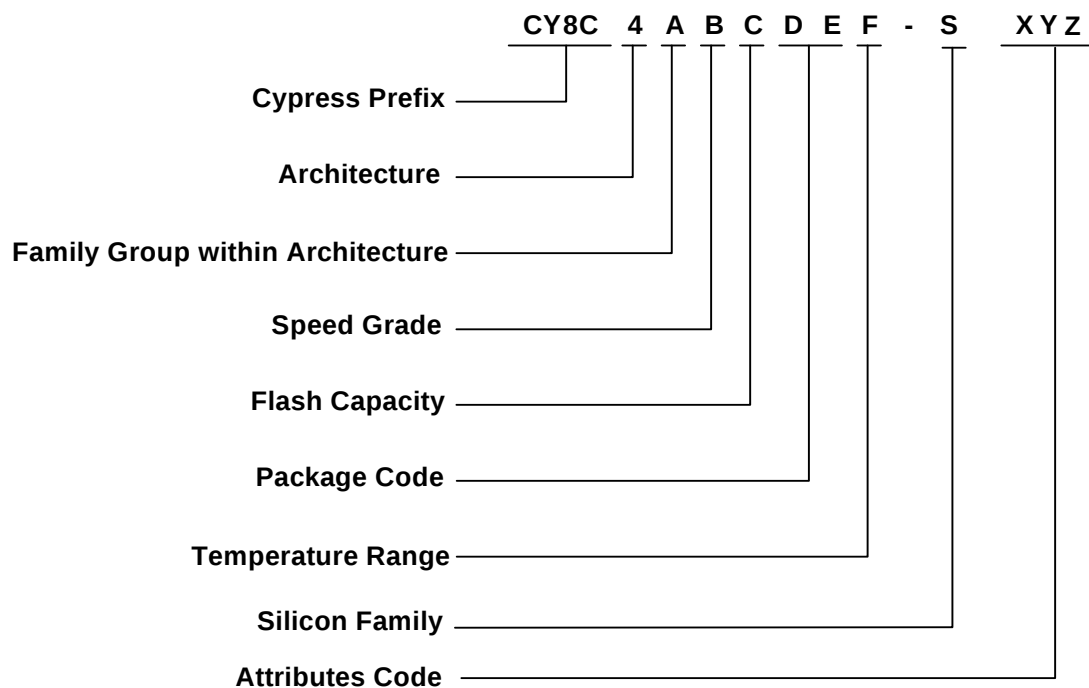
Category	MPN	Features														Package				
		Max CPU Speed (MHz)	Flash (KB)	SRAM (KB)	UDB	Opamp (CTBm)	CSD	IDAC (1X7-Bit, 1-8-Bit)	Direct LCD Drive	12-bit SAR ADC	LP Comparators	TCPWM Blocks	SCB Blocks	CAN	GPIO	44-TQFP	48-TQFP	64-TQFP (0.5-mm pitch)	64-TQFP (0.8-mm pitch)	68-QFN
4125	CY8C4125AZI-M433	24	32	4	0	2	–	–	–	806 ksp/s	2	8	4	–	38	–	✓	–	–	–
	CY8C4125AZI-M443	24	32	4	0	2	✓	–	✓	806 ksp/s	2	8	4	–	38	–	✓	–	–	–
	CY8C4125AZI-M445	24	32	4	0	2	✓	–	✓	806 ksp/s	2	8	4	–	51	–	–	✓	–	–
	CY8C4125LTI-M445	24	32	4	0	2	✓	–	✓	806 ksp/s	2	8	4	–	55	–	–	–	–	✓
	CY8C4125AXI-M445	24	32	4	0	2	✓	–	✓	806 ksp/s	2	8	4	–	51	–	–	–	✓	–
4126	CY8C4126AZI-M443	24	64	8	0	2	✓	–	✓	806 ksp/s	2	8	4	–	38	–	✓	–	–	–
	CY8C4126AXI-M443	24	64	8	0	2	✓	–	✓	806 ksp/s	2	8	4	–	36	✓	–	–	–	–
	CY8C4126AZI-M445	24	64	8	0	2	✓	–	✓	806 ksp/s	2	8	4	–	51	–	–	✓	–	–
	CY8C4126AZI-M475	24	64	8	0	4	–	✓	–	806 ksp/s	2	8	4	–	51	–	–	✓	–	–
	CY8C4126LTI-M445	24	64	8	0	2	✓	–	✓	806 ksp/s	2	8	4	–	55	–	–	–	–	✓
	CY8C4126LTI-M475	24	64	8	0	4	–	✓	–	806 ksp/s	2	8	4	–	55	–	–	–	–	✓
	CY8C4126AXI-M445	24	64	8	0	2	✓	–	✓	806 ksp/s	2	8	4	–	51	–	–	–	✓	–
4127	CY8C4127LTI-M475	24	128	16	0	4	✓	✓	–	806 ksp/s	2	8	4	–	55	–	–	–	–	✓
	CY8C4127AZI-M475	24	128	16	0	4	–	✓	–	806 ksp/s	2	8	4	–	51	–	–	✓	–	–
	CY8C4127AZI-M485	24	128	16	0	4	✓	✓	✓	806 ksp/s	2	8	4	–	51	–	–	✓	–	–
	CY8C4127AXI-M485	24	128	16	0	4	✓	✓	✓	806 ksp/s	2	8	4	–	51	–	–	–	✓	–

The nomenclature used in the preceding table is based on the following part numbering convention:

Field	Description	Values	Meaning
CY8C	Cypress Prefix		
4	Architecture	4	PSoC 4
A	Family	1	4100 Family
B	CPU Speed	4	48 MHz
C	Flash Capacity	4	16 KB
		5	32 KB
		6	64 KB
		7	128 KB
DE	Package Code	AX, AZ	TQFP
		LQ	QFN
		BU	BGA
		FD	CSP
F	Temperature Range	I	Industrial
		Q	Extended Industrial
S	Silicon Family	N/A	PSoC 4 Base Series
		L	PSoC 4 L-Series
		BL	PSoC 4 BLE
		M	PSoC 4 M-Series
XYZ	Attributes Code	000-999	Code of feature set in the specific family

Part Numbering Conventions

The part number fields are defined as follows.



Packaging

The description of the PSoC4100M package dimensions follows.

Spec ID#	Package	Description	Package Dwg #
PKG_1	68-pin QFN	68 QFN, 8 mm x 8 mm x 1.0 mm height with 0.4 mm pitch	001-09618
PKG_2	64-pin TQFP	64 TQFP, 10 mm x10 mm x 1.4 mm height with 0.5 mm pitch	51-85051
PKG_4	64-pin TQFP	64 TQFP, 14 mm x14 mm x 1.4 mm height with 0.8 mm pitch	51-85046
PKG_5	48-pin TQFP	48 TQFP, 7 mm x 7 mm x 1.4 mm height with 0.5 mm pitch	51-85135
PKG_6	44-pin TQFP	44 TQFP, 10 mm x 10 mm x 1.4 mm height with 0.8 mm pitch	51-85064

Table 40. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T _A	Operating ambient temperature		–40	25	85	°C
T _J	Operating junction temperature		–40	–	100	°C
T _{JA}	Package θ_{JA} (68-pin QFN)		–	16.8	–	°C/Watt
T _{JC}	Package θ_{JC} (68-pin QFN)		–	2.9	–	°C/Watt
T _{JA}	Package θ_{JA} (64-pin TQFP, 0.5-mm pitch)		–	56	–	°C/Watt
T _{JC}	Package θ_{JC} (64-pin TQFP, 0.5-mm pitch)		–	19.5	–	°C/Watt
T _{JA}	Package θ_{JA} (64-pin TQFP, 0.8-mm pitch)		–	66.4	–	°C/Watt
T _{JC}	Package θ_{JC} (64-pin TQFP, 0.8-mm pitch)		–	18.2	–	°C/Watt
T _{JA}	Package θ_{JA} (48-pin TQFP, 0.5-mm pitch)		–	67.3	–	°C/Watt
T _{JC}	Package θ_{JC} (48-pin TQFP, 0.5-mm pitch)		–	30.4	–	°C/Watt
T _{JA}	Package θ_{JA} (44-pin TQFP, 0.8-mm pitch)		–	57	–	°C/Watt
T _{JC}	Package θ_{JC} (44-pin TQFP, 0.8-mm pitch)		–	25.9	–	°C/Watt

Table 41. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
All packages	260 °C	30 seconds

Table 42. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
All packages	MSL 3

Figure 7. 64-Pin 14 × 14 × 1.4 mm TQFP Package Outline

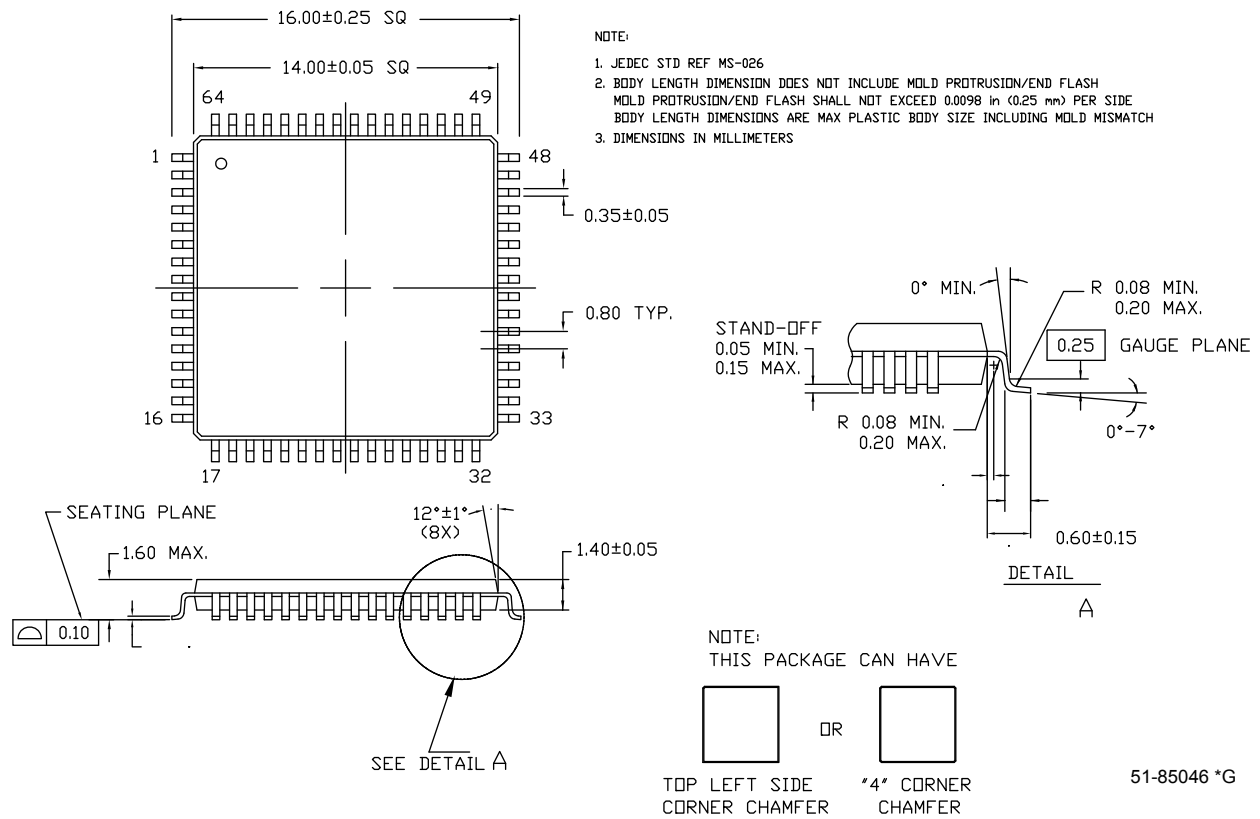


Figure 8. 48-Pin 7 × 7 × 1.4 mm TQFP Package Outline

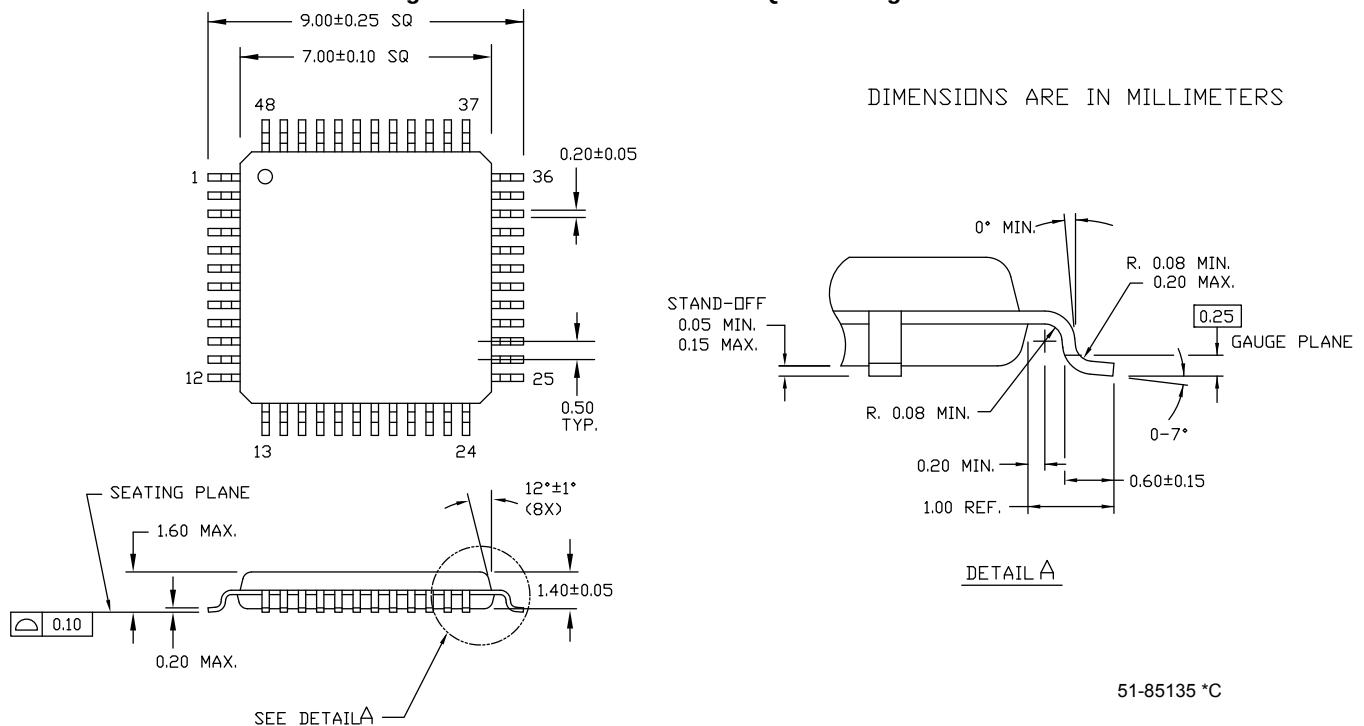
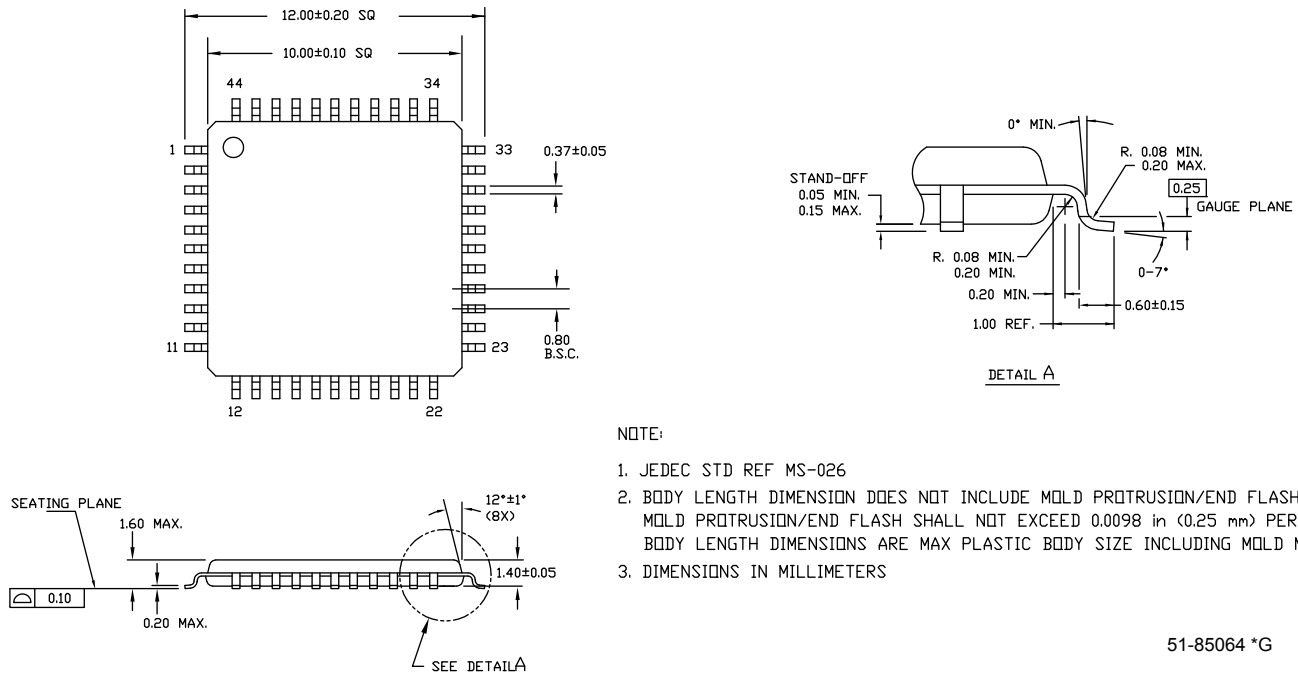


Figure 9. 44-Pin 10 × 10 × 1.4 mm TQFP Package Outline



51-85064 *G

Acronyms

Table 43. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
ARM®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge

Table 43. Acronyms Used in this Document *(continued)*

Acronym	Description
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I ² C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD
PC	program counter
PCB	printed circuit board

Table 43. Acronyms Used in this Document *(continued)*

Acronym	Description
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I ² C serial clock
SDA	I ² C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA

Table 43. Acronyms Used in this Document *(continued)*

Acronym	Description
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal