Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I²C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, CapSense, LCD, LVD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b SAR; 2xIDAC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4127azi-m485

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article KBA86521, How to Design with PSoC 3, PSoC 4, and PSoC 5LP. Following is an abbreviated list for PSoC 4:

- Overview: PSoC Portfolio, PSoC Roadmap
- Product Selectors: PSoC 1, PSoC 3, PSoC 4, PSoC 5LP
  In addition, PSoC Creator includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 4 are:
  - AN79953: Getting Started With PSoC 4
  - AN88619: PSoC 4 Hardware Design Considerations
  - AN86439: Using PSoC 4 GPIO Pins
  - AN57821: Mixed Signal Circuit Board Layout
  - AN81623: Digital Design Best Practices
  - AN73854: Introduction To Bootloaders
  - AN89610: ARM Cortex Code Optimization
- Technical Reference Manual (TRM) is in two documents:
  - Architecture TRM details each PSoC 4 functional block.
  - Registers TRM describes each of the PSoC 4 registers.
- Development Kits:
  - CY8CKIT-042, PSoC 4 Pioneer Kit, is an easy-to-use and inexpensive development platform. This kit includes connectors for Arduino™ compatible shields and Digilent® Pmod™ daughter cards.
  - CY8CKIT-049 is a very low-cost prototyping platform. It is a low-cost alternative to sampling PSoC 4 devices.
  - CY8CKIT-001 is a common development platform for any one of the PSoC 1, PSoC 3, PSoC 4, or PSoC 5LP families of devices.

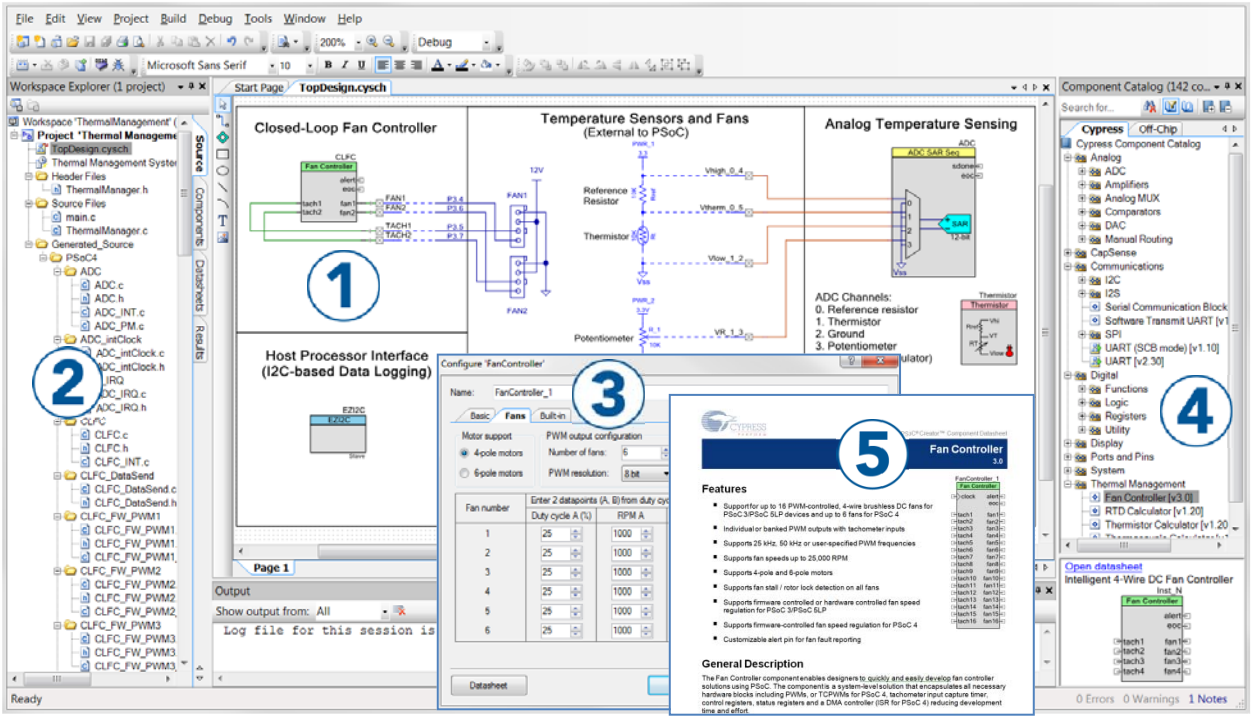
The MiniProg3 device provides an interface for flash programming and debug.

PSoC Creator

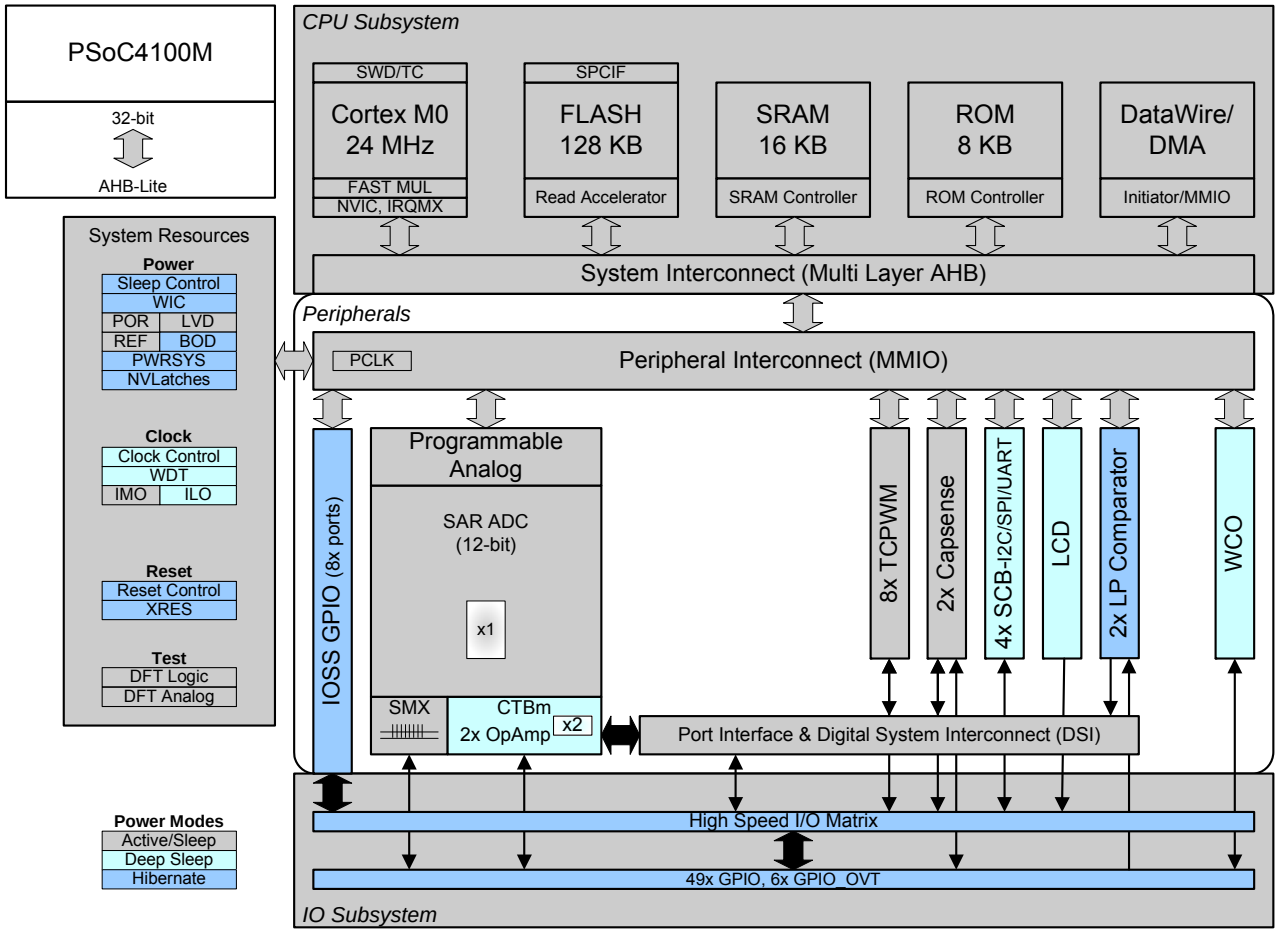
PSoC Creator is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC 3, PSoC 4, and PSoC 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC Components; see the list of component datasheets. With PSoC Creator, you can:

1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

Figure 1. Multiple-Sensor Example Project in PSoC Creator



PSoC 4100M Block Diagram



The PSoC 4100-M devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The ARM Serial_Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator Integrated Development Environment (IDE) provides fully integrated programming and debug support for PSoC 4100-M devices. The SWD interface is fully compatible with industry-standard third-party tools. The PSoC 4100-M family provides a level of security not possible with multi-chip application solutions or with microcontrollers. This is due to its ability to disable debug features, robust flash protection, and because it allows customer-proprietary functionality to be implemented in on-chip programmable blocks.

The debug circuits are enabled by default and can only be disabled in firmware. If not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. Because all programming, debug, and test interfaces are disabled when maximum device security is enabled, PSoC 4100-M with device security enabled may not be returned for failure analysis. This is a trade-off the PSoC 4100-M allows the customer to make.

Pinouts

The following is the pin list for the PSoC 4100M. This shows the power supply and port pins (for example, P0.0 is Pin 0 of Port 0).

68-QFN		64-TQFP		48-TQFP		44-TQFP	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
42	P0.0	39	P0.0	28	P0.0	24	P0.0
43	P0.1	40	P0.1	29	P0.1	25	P0.1
44	P0.2	41	P0.2	30	P0.2	26	P0.2
45	P0.3	42	P0.3	31	P0.3	27	P0.3
46	P0.4	43	P0.4	32	P0.4	28	P0.4
47	P0.5	44	P0.5	33	P0.5	29	P0.5
48	P0.6	45	P0.6	34	P0.6	30	P0.6
49	P0.7	46	P0.7	35	P0.7	31	P0.7
50	XRES	47	XRES	36	XRES	32	XRES
51	VCCD	48	VCCD	37	VCCD	33	VCCD
52	VSSD	49	VSSD	38	VSSD	DN	VSSD
53	VDDD	50	VDDD	39	VDDD	34	VDDD
				40	VDDA	35	VDDA
54	P5.0	51	P5.0				
55	P5.1	52	P5.1				
56	P5.2	53	P5.2				
57	P5.3	54	P5.3				
58	P5.4						
59	P5.5	55	P5.5				
60	VDDA	56	VDDA	40	VDDA	35	VDDA
61	VSSA	57	VSSA	41	VSSA	36	VSSA
62	P1.0	58	P1.0	42	P1.0	37	P1.0
63	P1.1	59	P1.1	43	P1.1	38	P1.1
64	P1.2	60	P1.2	44	P1.2	39	P1.2
65	P1.3	61	P1.3	45	P1.3	40	P1.3
66	P1.4	62	P1.4	46	P1.4	41	P1.4
67	P1.5	63	P1.5	47	P1.5	42	P1.5
68	P1.6	64	P1.6	48	P1.6	43	P1.6
1	P1.7/VREF	1	P1.7/VREF	1	P1.7/VREF	44	P1.7/VREF
						1	VSSD
2	P2.0	2	P2.0	2	P2.0	2	P2.0
3	P2.1	3	P2.1	3	P2.1	3	P2.1
4	P2.2	4	P2.2	4	P2.2	4	P2.2
5	P2.3	5	P2.3	5	P2.3	5	P2.3
6	P2.4	6	P2.4	6	P2.4	6	P2.4
7	P2.5	7	P2.5	7	P2.5	7	P2.5

Port/Pin	Analog	Alt. Function 1	Alt. Function 2	Alt. Function 3	Alt. Function 4	Alt. Function 5
P6.0		tcpwm.line[4]:0	scb[3].uart_rx:0		scb[3].i2c_scl:0	scb[3].spi_mosi:0
P6.1		tcpwm.line_compl[4]:0	scb[3].uart_tx:0		scb[3].i2c_sda:0	scb[3].spi_miso:0
P6.2		tcpwm.line[5]:0	scb[3].uart_cts:0			scb[3].spi_clk:0
P6.3		tcpwm.line_compl[5]:0	scb[3].uart_rts:0			scb[3].spi_select0:0
P6.4		tcpwm.line[6]:0				scb[3].spi_select1:0
P6.5		tcpwm.line_compl[6]:0				scb[3].spi_select2:0
P3.0		tcpwm.line[0]:0	scb[1].uart_rx:1		scb[1].i2c_scl:2	scb[1].spi_mosi:0
P3.1		tcpwm.line_compl[0]:0	scb[1].uart_tx:1		scb[1].i2c_sda:2	scb[1].spi_miso:0
P3.2		tcpwm.line[1]:0	scb[1].uart_cts:1		swd_data	scb[1].spi_clk:0
P3.3		tcpwm.line_compl[1]:0	scb[1].uart_rts:1		swd_clk	scb[1].spi_select0:0
P3.4		tcpwm.line[2]:0				scb[1].spi_select1:0
P3.5		tcpwm.line_compl[2]:0				scb[1].spi_select2:0
P3.6		tcpwm.line[3]:0				scb[1].spi_select3:0
P3.7		tcpwm.line_compl[3]:0				
P4.0			scb[0].uart_rx:0		scb[0].i2c_scl:1	scb[0].spi_mosi:0
P4.1			scb[0].uart_tx:0		scb[0].i2c_sda:1	scb[0].spi_miso:0
P4.2	csd[0].c_mod		scb[0].uart_cts:0		lpcomp.comp[0]:0	scb[0].spi_clk:0
P4.3	csd[0].c_sh_tank		scb[0].uart_rts:0		lpcomp.comp[1]:0	scb[0].spi_select0:0
P4.4						scb[0].spi_select1:2
P4.5						scb[0].spi_select2:2
P4.6						scb[0].spi_select3:2
P4.7						
P7.0		tcpwm.line[0]:2	scb[3].uart_rx:1		scb[3].i2c_scl:1	scb[3].spi_mosi:1
P7.1		tcpwm.line_compl[0]:2	scb[3].uart_tx:1		scb[3].i2c_sda:1	scb[3].spi_miso:1
P7.2		tcpwm.line[1]:2	scb[3].uart_cts:1			scb[3].spi_clk:1

Descriptions of the power pin functions are as follows:

VDDD: Power supply for both analog and digital sections (where there is no V_{DDA} pin).

VDDA: Analog V_{DD} pin where package pins allow; shorted to V_{DDD} otherwise.

VDDIO: I/O pin power domain.

VSSA: Analog ground pin where package pins allow; shorted to VSS otherwise

VSS: Ground pin.

VCCD: Regulated Digital supply (1.8 V ±5%).

Port Pins can all be used as LCD Commons, LCD Segment drivers, or CSD sense and shield pins can be connected to AMUXBUS A or B or can all be used as GPIO pins that can be driven by firmware or DSI signals.

Power

The supply voltage range is 1.71 to 5.5 V with all functions and circuits operating over that range.

The PSoC 4100M family allows two distinct modes of power supply operation: Unregulated External Supply and Regulated External Supply modes.

Unregulated External Supply

In this mode, the PSoC 4100M is powered by an External Power Supply that can be anywhere in the range of 1.8 to 5.5 V. This range is also designed for battery-powered operation, for instance, the chip can be powered from a battery system that starts at 3.5V and works down to 1.8 V. In this mode, the internal regulator of the PSoC 4100M supplies the internal logic and the VCCD output of the PSoC 4100M must be bypassed to ground via an external Capacitor (in the range of 1 to 1.6 µF; X5R ceramic or better).

The grounds, VSSA and VSS, must be shorted together. Bypass capacitors must be used from VDDD and VDDA to ground, typical practice for systems in this frequency range is to use a capacitor in the 1 µF range in parallel with a smaller capacitor (0.1 µF, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the Bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

Power Supply	Bypass Capacitors
VDDD–VSS and VDDIO-VSS	0.1 µF ceramic at each pin plus bulk capacitor 1 to 10 µF.
VDDA–VSSA	0.1 µF ceramic at pin. Additional 1 µF to 10 µF bulk capacitor
VCCD–VSS	1 µF ceramic capacitor at the VCCD pin
VREF–VSSA (optional)	The internal bandgap may be bypassed with a 1 µF to 10 µF capacitor for better ADC performance.

Regulated External Supply

In this mode, the PSoC 4100M is powered by an external power supply that must be within the range of 1.71 to 1.89 V (1.8 ±5%); note that this range needs to include power supply ripple. VCCD and VDDD pins are shorted together and bypassed. The internal regulator is disabled in firmware.

Electrical Specifications

Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings[1]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID1	V_{DD_ABS}	Analog or digital supply relative to V_{SS} ($V_{SSD} = V_{SSA}$)	–0.5	–	6	V	Absolute maximum
SID2	V_{CCD_ABS}	Direct digital core voltage input relative to V_{SSD}	–0.5	–	1.95	V	Absolute maximum
SID3	V_{GPIO_ABS}	GPIO voltage; V_{DDD} or V_{DDA}	–0.5	–	V_{DD}+0.5	V	Absolute maximum
SID4	I_{GPIO_ABS}	Current per GPIO	–25	–	25	mA	Absolute maximum
SID5	$I_{G\text{-}PIO\_injection}$	GPIO injection current per pin	–0.5	–	0.5	mA	Absolute maximum
BID44	ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	
BID45	ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	
BID46	LU	Pin current for latch-up	–140	–	140	mA	

Device Level Specifications

All specifications are valid for –40 °C ≤ TA ≤ 105 °C and TJ ≤ 125 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 2. DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID53	V_{DD}	Power Supply Input Voltage ($V_{DDA} = V_{DDD} = V_{DD}$)	1.8	–	5.5	V	With regulator enabled
SID255	V_{DDD}	Power Supply Input Voltage unregulated	1.71	1.8	1.89	V	Internally unregulated Supply
SID54	V_{CCD}	Output voltage (for core logic)	–	1.8	–	V	
SID55	C_{EFC}	External Regulator voltage bypass	1	1.3	1.6	µF	X5R ceramic or better
SID56	C_{EXC}	Power supply decoupling capacitor	–	1	–	µF	X5R ceramic or better
Active Mode, V_{DD} = 1.71 V to 5.5 V, –40 °C to +105 °C							
SID6	I_{DD1}	Execute from Flash; CPU at 6 MHz	–	2.2	2.8	mA	
SID7	I_{DD2}	Execute from Flash; CPU at 12 MHz	–	3.7	4.2	mA	
SID8	I_{DD3}	Execute from Flash; CPU at 24 MHz	–	6.7	7.2	mA	
Sleep Mode, –40 °C to +105 °C							
SID21	I_{DD16}	I^2C wakeup, WDT, and Comparators on. Regulator Off.	–	1.75	2.1	mA	V_{DD} = 1.71 to 1.89, 6 MHz
SID22	I_{DD17}	I^2C wakeup, WDT, and Comparators on.	–	1.7	2.1	mA	V_{DD} = 1.8 to 5.5, 6 MHz
SID23	I_{DD18}	I^2C wakeup, WDT, and Comparators on. Regulator Off.	–	2.35	2.8	mA	V_{DD} = 1.71 to 1.89, 12 MHz
SID24	I_{DD19}	I^2C wakeup, WDT, and Comparators on.	–	2.25	2.8	mA	V_{DD} = 1.8 to 5.5, 12 MHz

Note
1. Usage above the absolute maximum conditions listed in Table 1 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

Table 2. DC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
Deep Sleep Mode, –40 °C to + 60 °C							
SID30	I_{DD25}	I^2C wakeup and WDT on. Regulator Off.	–	1.55	20	µA	V_{DD} = 1.71 to 1.89
SID31	I_{DD26}	I^2C wakeup and WDT on.	–	1.35	15	µA	V_{DD} = 1.8 to 3.6
SID32	I_{DD27}	I^2C wakeup and WDT on.	–	1.5	15	µA	V_{DD} = 3.6 to 5.5
Deep Sleep Mode, +85 °C							
SID33	I_{DD28}	I^2C wakeup and WDT on. Regulator Off.	–	–	60	µA	V_{DD} = 1.71 to 1.89
SID34	I_{DD29}	I^2C wakeup and WDT on.	–	–	45	µA	V_{DD} = 1.8 to 3.6
SID35	I_{DD30}	I^2C wakeup and WDT on.	–	–	30	µA	V_{DD} = 3.6 to 5.5
Deep Sleep Mode, +105 °C							
SID33Q	I_{DD28Q}	I^2C wakeup and WDT on. Regulator Off.	–	–	135	µA	V_{DD} = 1.71 to 1.89
SID34Q	I_{DD29Q}	I^2C wakeup and WDT on.	–	–	180	µA	V_{DD} = 1.8 to 3.6
SID35Q	I_{DD30Q}	I^2C wakeup and WDT on.	–	–	140	µA	V_{DD} = 3.6 to 5.5
Hibernate Mode, –40 °C to + 60 °C							
SID39	I_{DD34}	Regulator Off.	–	150	3000	nA	V_{DD} = 1.71 to 1.89
SID40	I_{DD35}		–	150	1000	nA	V_{DD} = 1.8 to 3.6
SID41	I_{DD36}		–	150	1100	nA	V_{DD} = 3.6 to 5.5
Hibernate Mode, +85 °C							
SID42	I_{DD37}	Regulator Off.	–	–	4500	nA	V_{DD} = 1.71 to 1.89
SID43	I_{DD38}		–	–	3500	nA	V_{DD} = 1.8 to 3.6
SID44	I_{DD39}		–	–	3500	nA	V_{DD} = 3.6 to 5.5
Hibernate Mode, +105 °C							
SID42Q	I_{DD37Q}	Regulator Off.	–	–	19.4	µA	V_{DD} = 1.71 to 1.89
SID43Q	I_{DD38Q}		–	–	17	µA	V_{DD} = 1.8 to 3.6
SID44Q	I_{DD39Q}		–	–	16	µA	V_{DD} = 3.6 to 5.5
Stop Mode, +85 °C							
SID304	I_{DD43A}	Stop Mode current; V_{DD} = 3.6 V	–	35	85	nA	T = –40 °C to +60 °C
SID304A	I_{DD43B}	Stop Mode current; V_{DD} = 3.6 V	–	–	1450	nA	T = +85 °C
Stop Mode, +105 °C							
SID304Q	I_{DD43AQ}	Stop Mode current; V_{DD} = 3.6 V	–	–	5645	nA	
XRES current							
SID307	I_{DD_XR}	Supply current while XRES asserted	–	2	5	mA	

Table 10. Comparator AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID91	T_{RESP1}	Response time, normal mode	–	–	110	ns	50-mV overdrive
SID258	T_{RESP2}	Response time, low power mode	–	–	200	ns	50-mV overdrive
SID92	T_{RESP3}	Response time, ultra low power mode ($V_{DDD} \geq 2.2$ V for Temp < 0 °C, $V_{DDD} \geq 1.8$ V for Temp > 0 °C)	–	–	15	µs	200-mV overdrive

Temperature Sensor

Table 11. Temperature Sensor Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID93	$T_{SENSACC}$	Temperature sensor accuracy	–5	±1	+5	°C	–40 to +85 °C

SAR ADC

Table 12. SAR ADC DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID94	A_RES	Resolution	–	–	12	bits	
SID95	A_CHNIS_S	Number of channels - single ended	–	–	16		8 full speed
SID96	A-CHNKS_D	Number of channels - differential	–	–	8		Diff inputs use neighboring I/O
SID97	A-MONO	Monotonicity	–	–	–		Yes. Based on characterization
SID98	A_GAINERR	Gain error	–	–	±0.1	%	With external reference.
SID99	A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V $V_{REF.}$
SID100	A_ISAR	Current consumption	–	–	1	mA	
SID101	A_VINS	Input voltage range - single ended	V_{SS}	–	V_{DDA}	V	Based on device characterization
SID102	A_VIND	Input voltage range - differential	V_{SS}	–	V_{DDA}	V	Based on device characterization
SID103	A_INRES	Input resistance	–	–	2.2	KΩ	Based on device characterization
SID104	A_INCAP	Input capacitance	–	–	10	pF	Based on device characterization

Table 13. SAR ADC AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID106	A_PSRR	Power supply rejection ratio	70	–	–	dB	
SID107	A_CMRR	Common mode rejection ratio	66	–	–	dB	Measured at 1 V
SID108	A_SAMP_1	Sample rate with external reference bypass cap	–	–	806	ksps	

Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripheral in timer mode.

Timer/Counter/PWM

Table 15. TCPWM Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.1	ITCPWM1	Block current consumption at 3 MHz	–	–	45	µA	All modes (Timer/Counter/PWM)
SID.TCPWM.2	ITCPWM2	Block current consumption at 12 MHz	–	–	155	µA	All modes (Timer/Counter/PWM)
SID.TCPWM.2A	ITCPWM3	Block current consumption at 48 MHz	–	–	650	µA	All modes (Timer/Counter/PWM)
SID.TCPWM.3	TCPWMFREQ	Operating frequency	–	–	Fc	MHz	Fc max = Fcpu. Maximum = 24 MHz
SID.TCPWM.4	TPWMENEXT	Input Trigger Pulse Width for all Trigger Events	2/Fc	–	–	ns	Trigger Events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.
SID.TCPWM.5	TPWMEXT	Output Trigger Pulse widths	2/Fc	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) trigger outputs
SID.TCPWM.5A	TCRES	Resolution of Counter	1/Fc	–	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWMRES	PWM Resolution	1/Fc	–	–	ns	Minimum pulse width of PWM Output
SID.TCPWM.5C	QRES	Quadrature inputs resolution	1/Fc	–	–	ns	Minimum pulse width between Quadrature phase inputs.

I^2C

Table 16. Fixed I^2C DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	–	50	µA	
SID150	I_{I2C2}	Block current consumption at 400 kHz	–	–	135	µA	
SID151	I_{I2C3}	Block current consumption at 1 Mbps	–	–	310	µA	
SID152	I_{I2C4}	I^2C enabled in Deep Sleep mode	–	–	1.4	µA	

Table 17. Fixed I^2C AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID153	F_{I2C1}	Bit rate	–	–	1	Mbps	

LCD Direct Drive

Table 18. LCD Direct Drive DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID154	I_{LCDLOW}	Operating current in low power mode	–	5	–	µA	16 × 4 small segment disp. at 50 Hz
SID155	C_{LCDCAP}	LCD capacitance per segment/common driver	–	500	5000	pF	Guaranteed by Design
SID156	LCD_{OFFSET}	Long-term segment offset	–	20	–	mV	
SID157	I_{LCDOP1}	PWM Mode current. 5-V bias. 24-MHz IMO	–	0.6	–	mA	32 × 4 segments. 50 Hz, 25 °C
SID158	I_{LCDOP2}	PWM Mode current. 3.3-V bias. 24-MHz IMO.	–	0.5	–	mA	32 × 4 segments. 50 Hz, 25 °C

Table 19. LCD Direct Drive AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID159	F_{LCD}	LCD frame rate	10	50	150	Hz	

Table 20. Fixed UART DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID160	I_{UART1}	Block current consumption at 100 Kbits/sec	–	–	55	µA	
SID161	I_{UART2}	Block current consumption at 1000 Kbits/sec	–	–	312	µA	

Table 21. Fixed UART AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID162	F_{UART}	Bit rate	–	–	1	Mbps	

SPI Specifications

Table 22. Fixed SPI DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID163	I_{SPI1}	Block current consumption at 1 Mbits/sec	–	–	360	µA	
SID164	I_{SPI2}	Block current consumption at 4 Mbits/sec	–	–	560	µA	
SID165	I_{SPI3}	Block current consumption at 8 Mbits/sec	–	–	600	µA	

Table 23. Fixed SPI AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID166	F_{SPI}	SPI operating frequency (master; 6X oversampling)	–	–	8	MHz	

Table 24. Fixed SPI Master mode AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID167	T_{DMO}	MOSI valid after Sclock driving edge	–	–	15	ns	
SID168	T_{DSI}	MISO valid before Sclock capturing edge. Full clock, late MISO Sampling used	20	–	–	ns	
SID169	T_{HMO}	Previous MOSI data hold time with respect to capturing edge at Slave	0	–	–	ns	

Table 25. Fixed SPI Slave mode AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID170	T_{DMI}	MOSI valid before Sclock capturing edge	40	–	–	ns	
SID171	T_{DSO}	MISO valid after Sclock driving edge	–	–	42 + 3 × (1/FCPU)	ns	
SID171A	T_{DSO_ext}	MISO valid after Sclock driving edge in Ext. Clock mode	–	–	48	ns	
SID172	T_{HSO}	Previous MISO data hold time	0	–	–	ns	
SID172A	$T_{SSELSCK}$	SSEL Valid to first SCK Valid edge	100	–	–	ns	

Memory

Table 26. Flash DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID173	V_{PE}	Erase and program voltage	1.71	–	5.5	V	

Table 27. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID174	$T_{ROWWRITE}$	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 128 bytes
SID175	$T_{ROWERASE}$	Row erase time	–	–	13	ms	
SID176	$T_{ROWPROGRAM}$	Row program time after erase	–	–	7	ms	
SID178	$T_{BULKERASE}$	Bulk erase time (128 KB)	–	–	35	ms	
SID179	$T_{SECTORERASE}$	Sector erase time (8 KB)	–	–	15	ms	
SID180	$T_{DEVPROG}$	Total device program time	–	–	15	seconds	Guaranteed by characterization
SID181	F_{END}	Flash endurance	100 K	–	–	cycles	Guaranteed by characterization
SID182	F_{RET}	Flash retention. $T_A \le 55$ °C, 100 K P/E cycles	20	–	–	years	Guaranteed by characterization
SID182A		Flash retention. $T_A \le 85$ °C, 10 K P/E cycles	10	–	–	years	Guaranteed by characterization
SID182B	F_{RETQ}	Flash retention. $T_A \le 105$ °C, 10K P/E cycles, ≤ three years at $T_A \ge 85$ °C	10	20	–	years	Guaranteed by characterization.

Table 36. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234	$T_{STARTILO1}$	ILO startup time	–	–	2	ms	Guaranteed by characterization
SID236	$T_{ILODUTY}$	ILO duty cycle	40	50	60	%	Guaranteed by characterization
SID237	$F_{ILOTRIM1}$	32 kHz trimmed frequency	15	32	50	kHz	Max ILO frequency is 70 kHz if T_A > 85 °C

Table 37. External Clock Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID305	ExtClkFreq	External Clock input Frequency	0	–	48	MHz	Guaranteed by characterization
SID306	ExtClkDuty	Duty cycle; Measured at $V_{DD/2}$	45	–	55	%	Guaranteed by characterization

Table 38. Watch Crystal Oscillator (WCO) Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
IMO WCO-PLL calibrated mode							
SID330	IMO_{WCO1}	Frequency variation with IMO set to 3 MHz	–0.6	–	0.6	%	Does not include WCO tolerance
SID331	IMO_{WCO2}	Frequency variation with IMO set to 5 MHz	–0.4	–	0.4	%	Does not include WCO tolerance
SID332	IMO_{WCO3}	Frequency variation with IMO set to 7 MHz or 9 MHz	–0.3	–	0.3	%	Does not include WCO tolerance
SID333	IMO_{WCO4}	All other IMO frequency settings	–0.2	–	0.2	%	Does not include WCO tolerance
WCO Specifications							
SID398	F_{WCO}	Crystal frequency	–	32.768		kHz	
SID399	F_{TOL}	Frequency tolerance	–	50	250	ppm	With 20-ppm crystal.
SID400	ESR	Equivalent series resistance	–	50	–	kΩ	
SID401	PD	Drive level	–	–	1	µW	
SID402	T_{START}	Startup time	–	–	500	ms	
SID403	C_L	Crystal load capacitance	6	–	12.5	pF	
SID404	C_0	Crystal shunt capacitance	–	1.35	–	pF	
SID405	I_{WCO1}	Operating current (high power mode)	–	–	8	uA	

Table 39. Block Specs

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID257	T_{WS24}*	Number of wait states at 24 MHz	1	–	–		CPU execution from Flash
SID260	V_{REFSAR}	Trimmed internal reference to SAR	–1	–	+1	%	Percentage of Vbg (1.024 V). Guaranteed by characterization
SID261	$F_{SARINTREF}$	SAR operating speed without external reference bypass	–	–	100	ksps	12-bit resolution. Guaranteed by characterization
SID262	$T_{CLKSWITCH}$	Clock switching from clk1 to clk2 in clk1 periods	3	–	4	Periods	Guaranteed by design
* T_{WS24} is guaranteed by design							

Ordering Information

The PSoC 4100M family part numbers and features are listed in the following table.

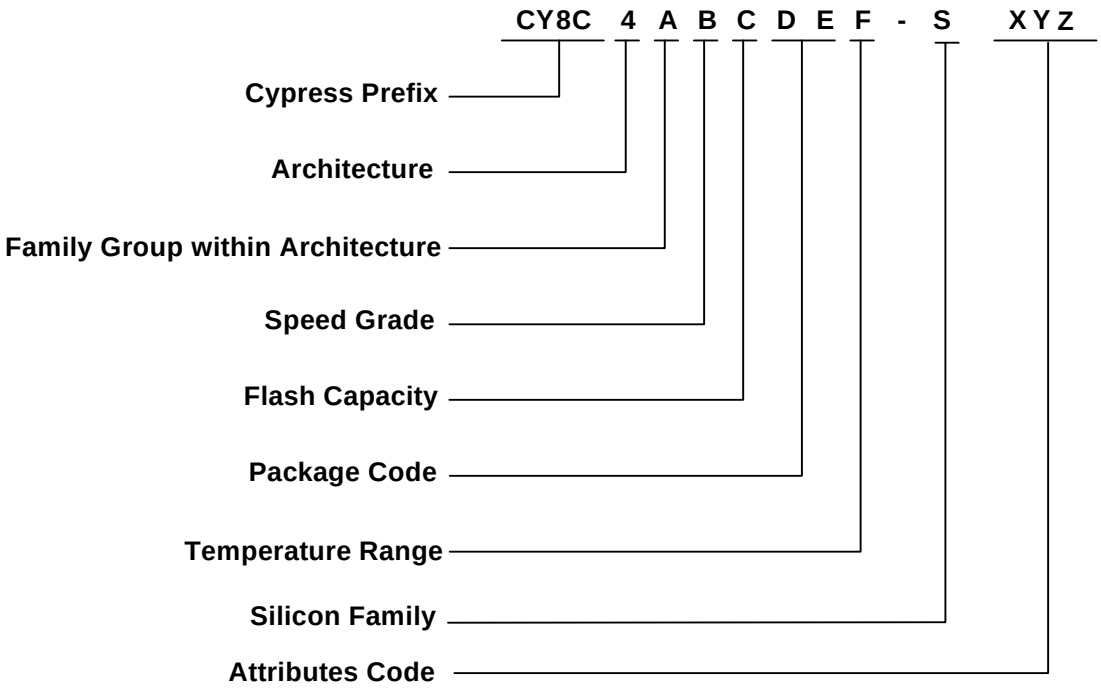
Category	MPN	Features														Package				
		Max CPU Speed (MHz)	Flash (KB)	SRAM (KB)	UDB	Opamp (CTBm)	CSD	IDAC (1X7-Bit, 1-8-Bit)	Direct LCD Drive	12-bit SAR ADC	LP Comparators	TCPWM Blocks	SCB Blocks	CAN	GPIO	44-TQFP	48-TQFP	64-TQFP (0.5-mm pitch)	64-TQFP (0.8-mm pitch)	68-QFN
4125	CY8C4125AZI-M433	24	32	4	0	2	–	–	–	806 ksps	2	8	4	–	38	–	✔	–	–	–
	CY8C4125AZI-M443	24	32	4	0	2	✔	–	✔	806 ksps	2	8	4	–	38	–	✔	–	–	–
	CY8C4125AZI-M445	24	32	4	0	2	✔	–	✔	806 ksps	2	8	4	–	51	–	–	✔	–	–
	CY8C4125LTI-M445	24	32	4	0	2	✔	–	✔	806 ksps	2	8	4	–	55	–	–	–	–	✔
	CY8C4125AXI-M445	24	32	4	0	2	✔	–	✔	806 ksps	2	8	4	–	51	–	–	–	✔	–
4126	CY8C4126AZI-M443	24	64	8	0	2	✔	–	✔	806 ksps	2	8	4	–	38	–	✔	–	–	–
	CY8C4126AXI-M443	24	64	8	0	2	✔	–	✔	806 ksps	2	8	4	–	36	✔	–	–	–	–
	CY8C4126AZI-M445	24	64	8	0	2	✔	–	✔	806 ksps	2	8	4	–	51	–	–	✔	–	–
	CY8C4126AZI-M475	24	64	8	0	4	–	✔	–	806 ksps	2	8	4	–	51	–	–	✔	–	–
	CY8C4126LTI-M445	24	64	8	0	2	✔	–	✔	806 ksps	2	8	4	–	55	–	–	–	–	✔
	CY8C4126LTI-M475	24	64	8	0	4	–	✔	–	806 ksps	2	8	4	–	55	–	–	–	–	✔
	CY8C4126AXI-M445	24	64	8	0	2	✔	–	✔	806 ksps	2	8	4	–	51	–	–	–	✔	–
4127	CY8C4127LTI-M475	24	128	16	0	4	✔	✔	–	806 ksps	2	8	4	–	55	–	–	–	–	✔
	CY8C4127AZI-M475	24	128	16	0	4	–	✔	–	806 ksps	2	8	4	–	51	–	–	✔	–	–
	CY8C4127AZI-M485	24	128	16	0	4	✔	✔	✔	806 ksps	2	8	4	–	51	–	–	✔	–	–
	CY8C4127AXI-M485	24	128	16	0	4	✔	✔	✔	806 ksps	2	8	4	–	51	–	–	–	✔	–

The nomenclature used in the preceding table is based on the following part numbering convention:

Field	Description	Values	Meaning
CY8C	Cypress Prefix		
4	Architecture	4	PSoC 4
A	Family	1	4100 Family
B	CPU Speed	4	48 MHz
C	Flash Capacity	4	16 KB
		5	32 KB
		6	64 KB
		7	128 KB
DE	Package Code	AX, AZ	TQFP
		LQ	QFN
		BU	BGA
		FD	CSP
F	Temperature Range	I	Industrial
		Q	Extended Industrial
S	Silicon Family	N/A	PSoC 4 Base Series
		L	PSoC 4 L-Series
		BL	PSoC 4 BLE
		M	PSoC 4 M-Series
XYZ	Attributes Code	000-999	Code of feature set in the specific family

Part Numbering Conventions

The part number fields are defined as follows.



Packaging

The description of the PSoC4100M package dimensions follows.

Spec ID#	Package	Description	Package Dwg #
PKG_1	68-pin QFN	68 QFN, 8 mm x 8 mm x 1.0 mm height with 0.4 mm pitch	001-09618
PKG_2	64-pin TQFP	64 TQFP, 10 mm x10 mm x 1.4 mm height with 0.5 mm pitch	51-85051
PKG_4	64-pin TQFP	64 TQFP, 14 mm x14 mm x 1.4 mm height with 0.8 mm pitch	51-85046
PKG_5	48-pin TQFP	48 TQFP, 7 mm x 7 mm x 1.4 mm height with 0.5 mm pitch	51-85135
PKG_6	44-pin TQFP	44 TQFP, 10 mm x 10 mm x 1.4 mm height with 0.8 mm pitch	51-85064

Table 40. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature		–40	25	85	°C
T_J	Operating junction temperature		–40	–	100	°C
T_{JA}	Package θ_{JA} (68-pin QFN)		–	16.8	–	°C/Watt
T_{JC}	Package θ_{JC} (68-pin QFN)		–	2.9	–	°C/Watt
T_{JA}	Package θ_{JA} (64-pin TQFP, 0.5-mm pitch)		–	56	–	°C/Watt
T_{JC}	Package θ_{JC} (64-pin TQFP, 0.5-mm pitch)		–	19.5	–	°C/Watt
T_{JA}	Package θ_{JA} (64-pin TQFP, 0.8-mm pitch)		–	66.4	–	°C/Watt
T_{JC}	Package θ_{JC} (64-pin TQFP, 0.8-mm pitch)		–	18.2	–	°C/Watt
T_{JA}	Package θ_{JA} (48-pin TQFP, 0.5-mm pitch)		–	67.3	–	°C/Watt
T_{JC}	Package θ_{JC} (48-pin TQFP, 0.5-mm pitch)		–	30.4	–	°C/Watt
T_{JA}	Package θ_{JA} (44-pin TQFP, 0.8-mm pitch)		–	57	–	°C/Watt
T_{JC}	Package θ_{JC} (44-pin TQFP, 0.8-mm pitch)		–	25.9	–	°C/Watt

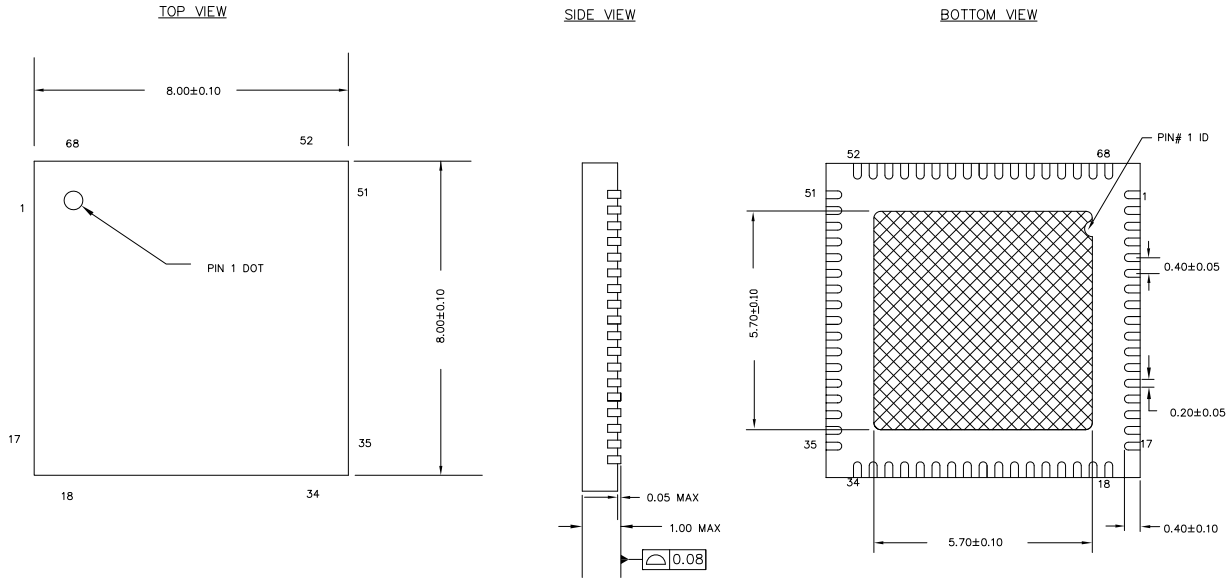
Table 41. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
All packages	260 °C	30 seconds

Table 42. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
All packages	MSL 3

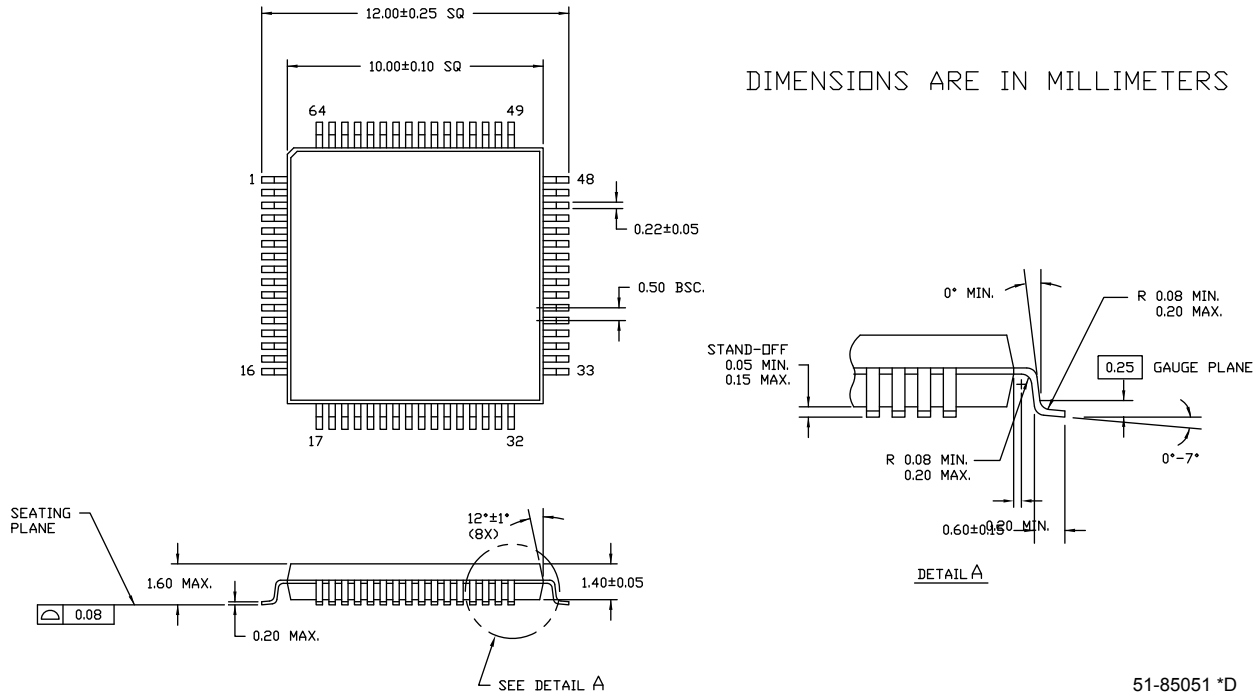
Figure 5. 68-Pin 8 × 8 × 1.0 mm QFN Package Outline



NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO–220
3. PACKAGE WEIGHT: 17 ± 2mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-09618 *E

Figure 6. 64-Pin 10 × 10 × 1.4 mm TQFP Package Outline



51-85051 *D

Figure 7. 64-Pin 14 × 14 × 1.4 mm TQFP Package Outline

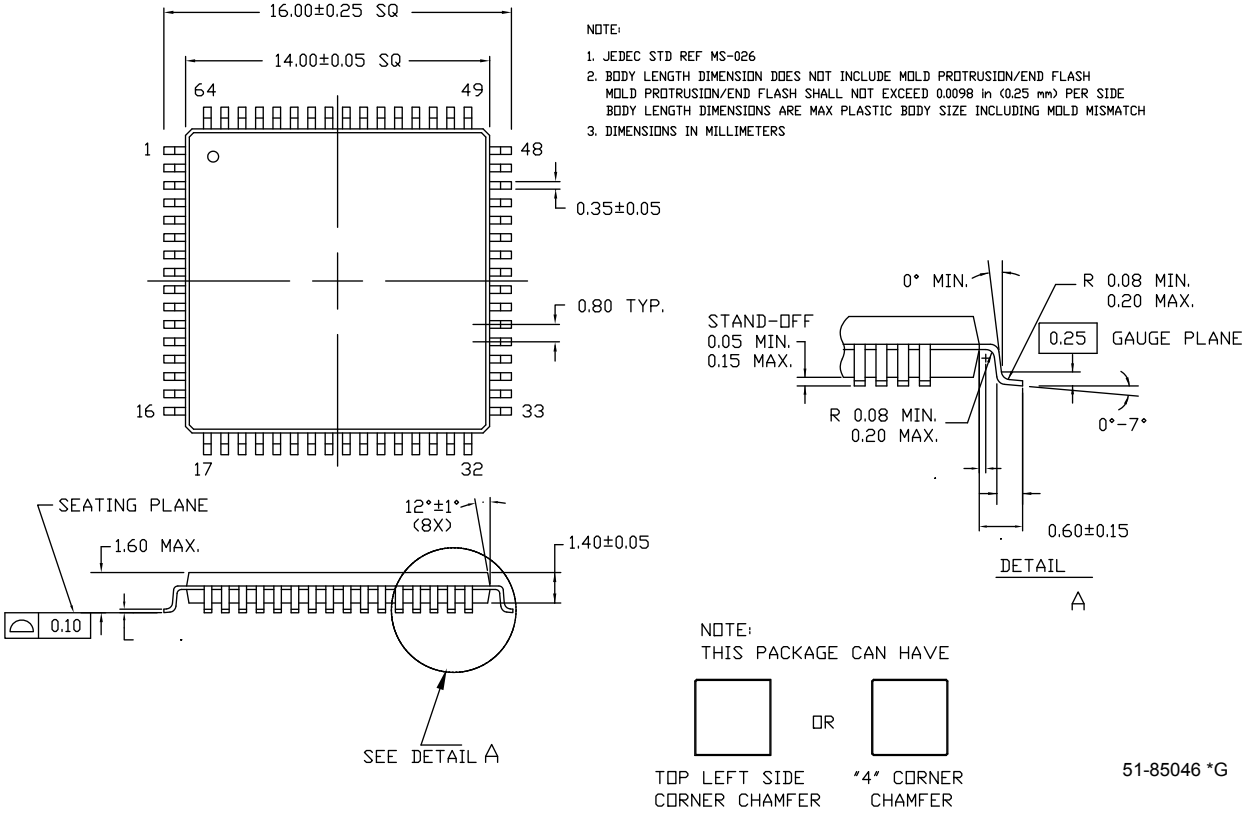
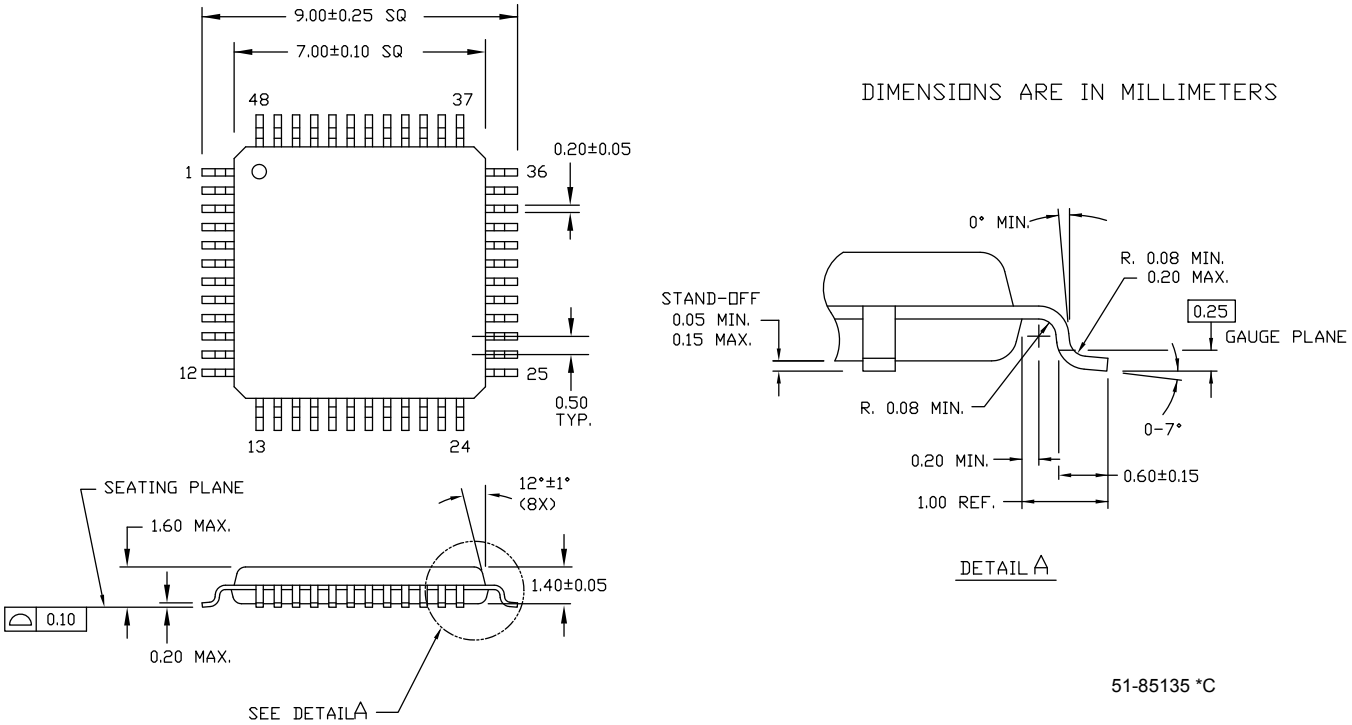


Figure 8. 48-Pin 7 × 7 × 1.4 mm TQFP Package Outline



Acronyms

Table 43. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
ARM®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge

Table 43. Acronyms Used in this Document *(continued)*

Acronym	Description
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD
PC	program counter
PCB	printed circuit board

Document Conventions

Units of Measure

Table 44. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

Revision History

Description Title: PSoC® 4: PSoC 4100M Family Datasheet Programmable System-on-Chip (PSoC®) Document Number: 001-96519				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*A	4765455	WKA	05/20/2015	Release to web.
*B	4815539	WKA	06/29/2015	Removed note regarding hardware handshaking in the UART Mode section. Changed max value of SID51A to 2 ms. Added “Guaranteed by characterization” note for SID65 and SID65A Updated Ordering Information.
*C	4941619	WKA	09/30/2015	Updated CapSense section. Updated the note at the end of the Pinout table. Removed Conditions for spec SID237.
*D	5026805	WKA	11/26/2015	Added Comparator ULP mode range restrictions and corrected typos.
*E	5408936	WKA	08/19/2016	Added extended industrial temperature range. Added specs SID290Q, SID182A, and SID299A. Updated conditions for SID290, SID223, and SID237. Added 44-pin TQFP package details. Updated Ordering Information