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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I ² C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	61
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 12x10b, 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562g7adfh-v1

Table 1.1 Outline of Specifications (2 / 5)

Classification	Module/Function	Description
Interrupt	Interrupt controller (ICU)	- Peripheral function interrupts: 101 sources - External interrupts: 9 (NMI and IRQ0 to IRQ7 pins) - Non-maskable interrupts: 3 (the NMI pin, oscillation stop detection interrupt, and voltage-monitoring interrupt) 16 levels specifiable for the order of priority
Data transfer	Data transfer controller (DTC)	- Three transfer modes: Normal transfer, repeat transfer, and block transfer - Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
I/O ports	Programmable I/O ports	I/O port pins for devices in the 112-pin LQFP/100-pin LQFP/80-pin LQFP (R5F562TxGDFF)/80-pin LQFP (except R5F562TxGDFF)/64-pin LQFP - I/O: 61/55/44/44/37 - Input only: 21/21/13/13/9 - Open-drain outputs: 2/2/2/2/2 (I²C bus interface pins) - Large-current outputs: 12/12/12/6/6(0) (MTU3 and GPT pins) The 5-V version of the 64-pin product does not have large-current outputs. - Reading out the states of pins is always possible.
Timers	Multi-function timer pulse unit 3 (MTU3)	16 bits x 8 channels - Up to 24 pulse inputs/outputs and three pulse inputs - Select from among six to eight counter-input clock signals for each channel (ICLK/1, ICLK/4, ICLK/16, ICLK/64, ICLK/256, ICLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available. 24 output compare or input capture registers - Counter clearing (clearing is synchronizable with compare match or input capture) - Simultaneous writing to multiple timer counters (TCNT) - Input to and output from all registers in synchronization with counter operation - Buffered operation - Cascade-connected operation 38 kinds of interrupt source - Automatic transfer of register data - Pulse output modes Toggled, PWM, complementary PWM, and reset synchronous PWM - Complementary PWM output mode Outputs non-overlapping waveforms for controlling 3-phase inverters Automatic specification of dead times PWM duty cycle: Selectable as any value from 0% to 100% Delay can be applied to requests for A/D conversion. Non-generation of interrupt requests at peak or trough values of counters can be selected. Double buffering - Reset-synchronous PWM mode Three PWM waveforms and corresponding inverse waveforms are output with the desired duty cycles. - Phase-counting mode - Counter functionality for dead-time compensation - Generation of triggers for A/D converters - Differential timing for initiation of A/D conversion
	Port output enable 3 (POE3)	- Control of the high-impedance state of the MTU3 and GPT's waveform output pins 5 pins for input from signal sources: POE0, POE4, POE8, POE10, POE11 - Initiation on detection of short-circuited outputs (detection of simultaneous switching of large-current pins to the active level) - Initiation by comparator-detection of analog level input to the 12-bit A/D converter - Initiation by oscillation-stoppage detection - Initiation by software - Selection of which output pins should be placed in the high-impedance state at the time of each POE input or comparator detection

Table 1.2 Functions of RX62T Group and RX62G Group Products (1 / 2)

Functions		RX62G Group		RX62T Group				
Pin number		112 Pins	100 Pins	112 Pins	100 Pins	80 Pins (R5F562T xGDFF)	80 Pins	64 Pins
Data transfer	Data transfer controller (DTC)	√						
Interrupt controller (ICU)	Input on the NMI pin	√						
	Input on the IRQ pins	√ (8)						√ (4)
Timers	Multi-function timer pulse unit 3 (MTU3)	√				√*1		
	General PWM timer (GPT)	—		√		√*1		
	General PWM timer (GPTa)	√		—				
	MTU3/GPT complementary PWM pin	12					6	
	Port output enable 3 (POE3)	√ (POE pins: 5)						√ (POE pins: 3)
	Compare match timer (CMT)	√						
	Watchdog timer (WDT)	√						
	Independent watchdog timer (IWDT)	√						
Communication function	Serial communications interface (SCI)	√						
	I ² C bus interface (RIIC)	√						
	CAN module (CAN) (as an optional function)	√						
	LIN module (LIN)	√						
	Serial peripheral interface (RSPI)	√						
12-bit A/D converter (S12ADA)		√ (4 ch. x 2 units)						
	Simultaneous sampling on three channels	√ (2 units)						
	Programmable gain amplifier	√ (3 ch. x 2 units)						
	Window comparator	√ (3 ch. x 2 units)						
10-bit A/D converter (ADA)		√ (12 ch.)				√ (4 ch.)		—
CRC calculator (CRC)		√						
I/O ports	I/O pins	61	55	61	55	44	44	37
	Input pins	21	21	21	21	13	13	9

Table 1.2 Functions of RX62T Group and RX62G Group Products (2 / 2)

Functions	RX62G Group		RX62T Group				
Pin number	112 Pins	100 Pins	112 Pins	100 Pins	80 Pins (R5F562T xGDFF)	80 Pins	64 Pins
Package	LQFP2020 (0.65-mm pitch)	LQFP1414 (0.5-mm pitch)	LQFP2020 (0.65-mm pitch)	LQFP1414 (0.5-mm pitch)	LQFP1414 (0.65-mm pitch)	LQFP1414 (0.65-mm pitch)	LQFP1010 (0.5-mm pitch) LQFP1414 (0.8-mm pitch)

O: Supported, —: Not supported

Note 1. For the MTU and GPT, the number of pins will differ with the package. See the list of pins and pin functions for details.
In addition, the CAN module is an optional function. See Table 1.3 for details.

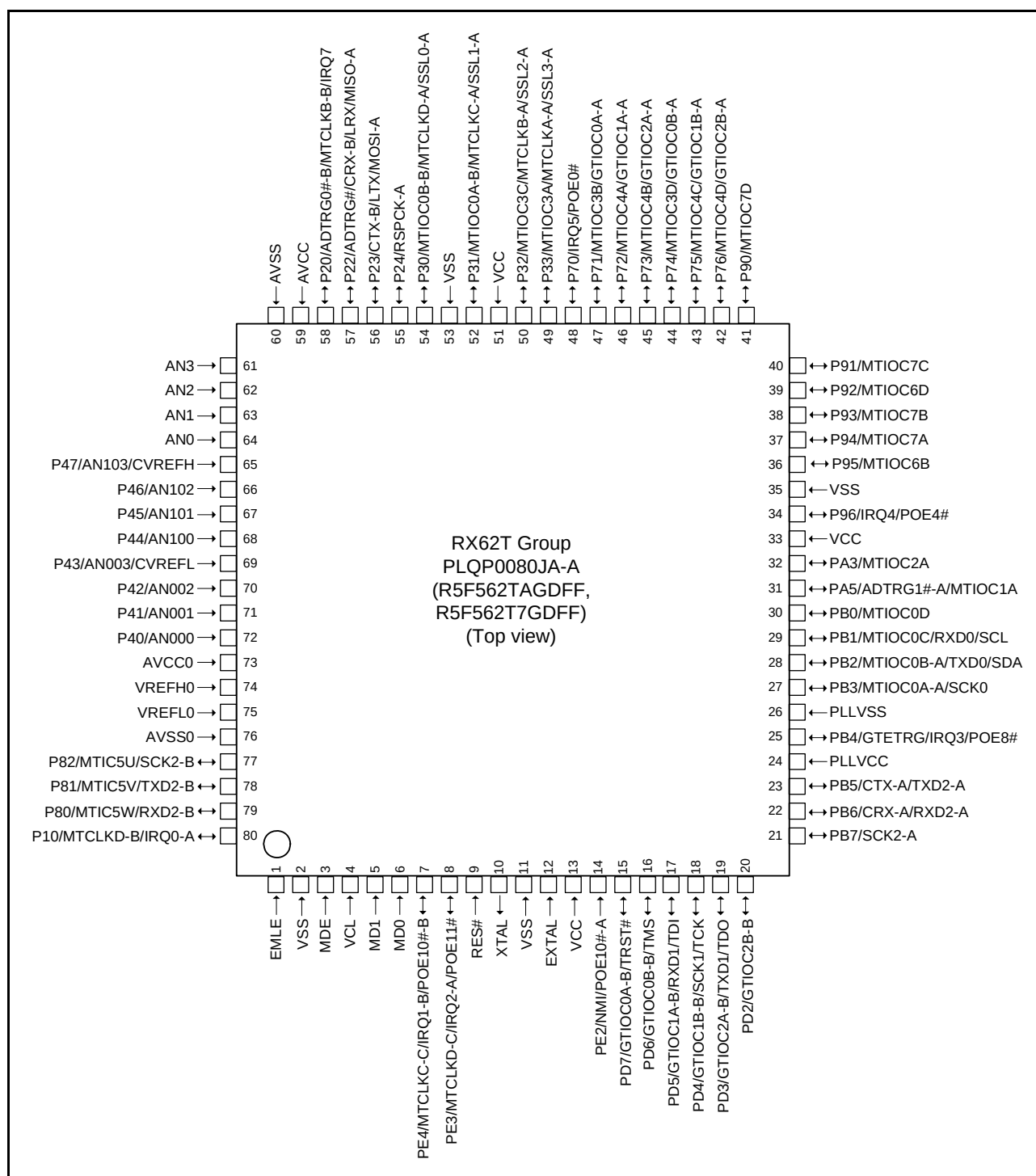


Figure 1.6 Pin Assignment of the 80-Pin LQFP (Two-Motor Control Supported Version)

Table 1.4 List of Pins and Pin Functions (112-Pin LQFP) (1 / 3)

Pin No. (112-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi- cation	Interrupt	POE	Debugging
1		PE5				IRQ0-B		
2	EMLE							
3	VSS							
4	MDE							
5	VCL							
6	MD1							
7	MD0							
8		PE4		MTCLKC-C		IRQ1-B	POE10#-B	
9		PE3		MTCLKD-C		IRQ2-A	POE11#	
10	RES#							
11	XTAL							
12	VSS							
13	EXTAL							
14	VCC							
15		PE2				NMI	POE10#-A	
16		PE1			SSL3-C			
17		PE0			CRX-C/ SSL2-C			
18		PD7		GTIOC0A-B	CTX-C/ SSL1-C			
19		PD6		GTIOC0B-B	SSL0-C			
20		PD5		GTIOC1A-B	RXD1			
21		PD4		GTIOC1B-B	SCK1			
22		PD3		GTIOC2A-B	TXD1			
23		PD2		GTIOC2B-B	MOSI-C			
24		PD1		GTIOC3A	MISO-C			
25		PD0		GTIOC3B	RSPCK-C			
26								TDI
27								TCK
28								TDO
29		PB7			SCK2-A			
30		PB6			CRX-A/ RXD2-A			
31		PB5			CTX-A/ TXD2-A			
32	PLLVC							
33		PB4		GTETRG		IRQ3	POE8#	
34	PLLVS							
35		PB3		MTIOC0A-A	SCK0			
36		PB2		MTIOC0B-A	TXD0/SDA			
37		PB1		MTIOC0C	RXD0/SCL			
38		PB0		MTIOC0D	MOSI-B			
39		PA5	ADTRG1#-A	MTIOC1A	MISO-B			
40		PA4	ADTRG0#-A	MTIOC1B	RSPCK-B			
41		PA3		MTIOC2A	SSL0-B			
42		PA2		MTIOC2B	SSL1-B			
43		PA1		MTIOC6A	SSL2-B			

Table 1.7 List of Pins and Pin Functions (80-Pin LQFP: R5F562TxGDFF) (2 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communication	Interrupt	POE	Debugging
42		P76		MTIOC4D/ GTIOC2B-A				
43		P75		MTIOC4C/ GTIOC1B-A				
44		P74		MTIOC3D/ GTIOC0B-A				
45		P73		MTIOC4B/ GTIOC2A-A				
46		P72		MTIOC4A/ GTIOC1A-A				
47		P71		MTIOC3B/ GTIOC0A-A				
48		P70				IRQ5	POE0#	
49		P33		MTIOC3A/ MTCLKA-A	SSL3-A			
50		P32		MTIOC3C/ MTCLKB-A	SSL2-A			
51	VCC							
52		P31		MTIOC0A-B/ MTCLKC-A	SSL1-A			
53	VSS							
54		P30		MTIOC0B-B/ MTCLKD-A	SSL0-A			
55		P24			RSPCK-A			
56		P23			CTX-B/ LTX/ MOSI-A			
57		P22	ADTRG#		CRX-B/ LRX/ MISO-A			
58		P20	ADTRG0#-B	MTCLKB-B		IRQ7		
59	AVCC							
60	AVSS							
61		P63	AN3					
62		P62	AN2					
63		P61	AN1					
64		P60	AN0					
65		P47	AN103/ CVREFH					
66		P46	AN102					
67		P45	AN101					
68		P44	AN100					
69		P43	AN003/ CVREFL					
70		P42	AN002					
71		P41	AN001					
72		P40	AN000					
73	AVCC0							
74	VREFH0							
75	VREFL0							

Table 1.9 Pin Functions (4 / 4)

Classifications	Pin Name	I/O	Description
I/O ports	P10, P11	I/O	2-bit input/output pins.
	P20 to P24	I/O	5-bit input/output pins. The P20/P21 pin is not included in the 64-pin version.
	P30 to P33	I/O	4-bit input/output pins.
	P40 to P47	Input	8-bit input pins.
	P50 to P55	Input	6-bit input pins. Not included in the 80-/64-pin versions.
	P60 to P65	Input	6-bit input pins. The P64/P6 pin is not included in the 80-pin version. Not included in the 64-pin version.
	P70 to P76	I/O	7-bit input/output pins.
	P80 to P82	I/O	3-bit input/output pins. Not included in the 80-/64-pin versions.
	P90 to P96	I/O	7-bit input/output pins. The P90 pin is not included in the 80-pin version. The P90/P95/P96 pin is not included in the 64-pin version.
	PA0 to PA5	I/O	6-bit input/output pins. The PA0/PA1 pin is not included in the 80-/64-pin versions.
	PB0 to PB7	I/O	8-bit input/output pins.
	PD0 to PD7	I/O	8-bit input/output pins. The PD0/PD1/PD2 pin is not included in the 80-/64-pin versions.
	PE0, PE1, PE3 to PE5	I/O	5-bit input/output pins. The PE1/PE5 pin is not included in the 80-pin version. Not included in the 64-pin version.
	PE2	Input	1-bit input pin.
	PG0 to PG5	I/O	6-bit input/output pins. Not included in the 100-/80-/64-pin versions.

Note: • Which pins are and are not incorporated depends on the package.
For details, see the list of pins and pin functions in Table 1.4 to Table 1.8.

2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen general-purpose registers (R0 to R15). R1 to R15 can be used as data registers or address registers. R0, a general-purpose register, also functions as the stack pointer (SP). The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2 Control Registers

(1) Interrupt Stack Pointer (ISP)/User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).

Set the ISP or USP to a multiple of four, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(2) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the relocatable vector table starts. Set INTB to a multiple of four.

(3) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

(4) Processor Status Word (PSW)

The processor status word (PSW) indicates results of instruction execution or the state of the CPU.

(5) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.

After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC.

(6) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.

After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

(7) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.

The FINTV register specifies a branch destination address when a fast interrupt has been generated.

(8) Floating-Point Status Word (FPSW)

The floating-point status word (FPSW) indicates the results of floating-point operations.

When an exception handling enable bit (Ej) enables the exception handling (Ej = 1), the exception cause can be identified by checking the corresponding Cj flag in the exception handling routine. If the exception handling is masked (Ej = 0), the occurrence of exception can be checked by reading the Fj flag at the end of a series of processing. Once the Fj flag has been set to 1, this value is retained until it is cleared to 0 by software (j = X, U, Z, O, or V).

3. Address Space

3.1 Address Space

This LSI has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.

Figure 3.1 shows the memory maps.

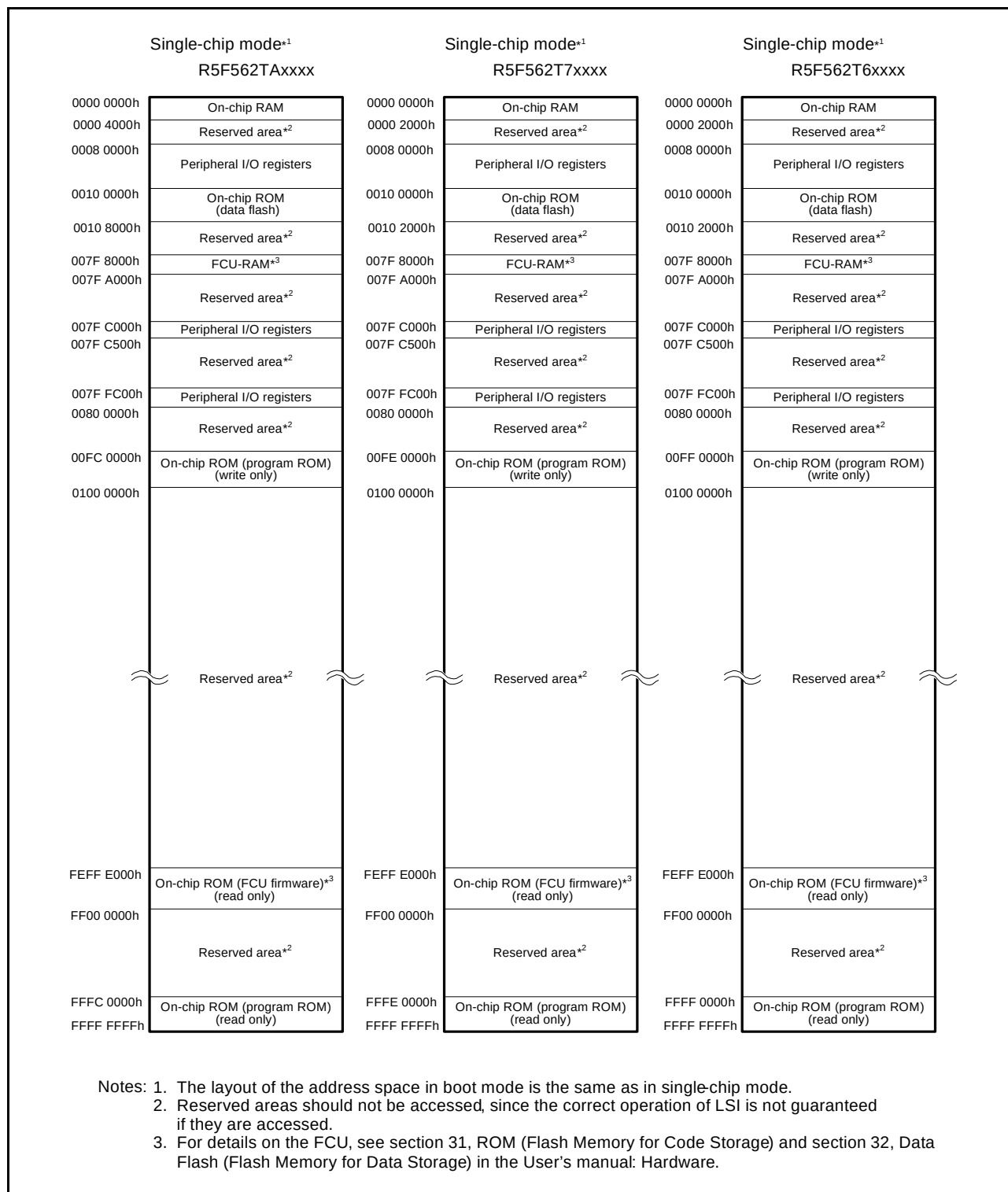


Figure 3.1 Memory Map (RX62T Group)

Table 4.1 List of I/O Registers (Address Order) (4 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 70BCh	ICU	Interrupt request register 188	IR188	8	8	2 ICLK
0008 70BDh	ICU	Interrupt request register 189	IR189	8	8	2 ICLK
0008 70BEh	ICU	Interrupt request register 190	IR190	8	8	2 ICLK
0008 70C0h	ICU	Interrupt request register 192	IR192	8	8	2 ICLK
0008 70C1h	ICU	Interrupt request register 193	IR193	8	8	2 ICLK
0008 70C2h	ICU	Interrupt request register 194	IR194	8	8	2 ICLK
0008 70C3h	ICU	Interrupt request register 195	IR195	8	8	2 ICLK
0008 70C4h	ICU	Interrupt request register 196	IR196	8	8	2 ICLK
0008 70D6h	ICU	Interrupt request register 214	IR214	8	8	2 ICLK
0008 70D7h	ICU	Interrupt request register 215	IR215	8	8	2 ICLK
0008 70D8h	ICU	Interrupt request register 216	IR216	8	8	2 ICLK
0008 70D9h	ICU	Interrupt request register 217	IR217	8	8	2 ICLK
0008 70DAh	ICU	Interrupt request register 218	IR218	8	8	2 ICLK
0008 70DBh	ICU	Interrupt request register 219	IR219	8	8	2 ICLK
0008 70DCh	ICU	Interrupt request register 220	IR220	8	8	2 ICLK
0008 70DDh	ICU	Interrupt request register 221	IR221	8	8	2 ICLK
0008 70DEh	ICU	Interrupt request register 222	IR222	8	8	2 ICLK
0008 70DFh	ICU	Interrupt request register 223	IR223	8	8	2 ICLK
0008 70E0h	ICU	Interrupt request register 224	IR224	8	8	2 ICLK
0008 70E1h	ICU	Interrupt request register 225	IR225	8	8	2 ICLK
0008 70F6h	ICU	Interrupt request register 246	IR246	8	8	2 ICLK
0008 70F7h	ICU	Interrupt request register 247	IR247	8	8	2 ICLK
0008 70F8h	ICU	Interrupt request register 248	IR248	8	8	2 ICLK
0008 70F9h	ICU	Interrupt request register 249	IR249	8	8	2 ICLK
0008 70FEh	ICU	Interrupt request register 254	IR254	8	8	2 ICLK
0008 711Bh	ICU	DTC activation enable register 027	DTCER027	8	8	2 ICLK
0008 711Ch	ICU	DTC activation enable register 028	DTCER028	8	8	2 ICLK
0008 711Dh	ICU	DTC activation enable register 029	DTCER029	8	8	2 ICLK
0008 711Eh	ICU	DTC activation enable register 030	DTCER030	8	8	2 ICLK
0008 711Fh	ICU	DTC activation enable register 031	DTCER031	8	8	2 ICLK
0008 712Dh	ICU	DTC activation enable register 045	DTCER045	8	8	2 ICLK
0008 712Eh	ICU	DTC activation enable register 046	DTCER046	8	8	2 ICLK
0008 7140h	ICU	DTC activation enable register 064	DTCER064	8	8	2 ICLK
0008 7141h	ICU	DTC activation enable register 065	DTCER065	8	8	2 ICLK
0008 7142h	ICU	DTC activation enable register 066	DTCER066	8	8	2 ICLK
0008 7143h	ICU	DTC activation enable register 067	DTCER067	8	8	2 ICLK
0008 7144h	ICU	DTC activation enable register 068	DTCER068	8	8	2 ICLK
0008 7145h	ICU	DTC activation enable register 069	DTCER069	8	8	2 ICLK
0008 7146h	ICU	DTC activation enable register 070	DTCER070	8	8	2 ICLK
0008 7147h	ICU	DTC activation enable register 071	DTCER071	8	8	2 ICLK
0008 7162h	ICU	DTC activation enable register 098	DTCER098	8	8	2 ICLK
0008 7166h	ICU	DTC activation enable register 102	DTCER102	8	8	2 ICLK
0008 7167h	ICU	DTC activation enable register 103	DTCER103	8	8	2 ICLK
0008 716Ah	ICU	DTC activation enable register 106	DTCER106	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (10 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 8250h	SCI2	Serial mode register	SMR ^{*1}	8	8	2, 3 PCLK ^{*3}
0008 8251h	SCI2	Bit rate register	BRR	8	8	2, 3 PCLK ^{*3}
0008 8252h	SCI2	Serial control register	SCR ^{*1}	8	8	2, 3 PCLK ^{*3}
0008 8253h	SCI2	Transmit data register	TDR	8	8	2, 3 PCLK ^{*3}
0008 8254h	SCI2	Serial status register	SSR ^{*1}	8	8	2, 3 PCLK ^{*3}
0008 8255h	SCI2	Receive data register	RDR	8	8	2, 3 PCLK ^{*3}
0008 8256h	SCI2	Smart card mode register	SCMR	8	8	2, 3 PCLK ^{*3}
0008 8257h	SCI2	Serial extended mode register	SEMR	8	8	2, 3 PCLK ^{*3}
0008 8250h	SMCI2	Serial mode register	SMR ^{*1}	8	8	2, 3 PCLK ^{*3}
0008 8251h	SMCI2	Bit rate register	BRR	8	8	2, 3 PCLK ^{*3}
0008 8252h	SMCI2	Serial control register	SCR ^{*1}	8	8	2, 3 PCLK ^{*3}
0008 8253h	SMCI2	Transmit data register	TDR	8	8	2, 3 PCLK ^{*3}
0008 8254h	SMCI2	Serial status register	SSR ^{*1}	8	8	2, 3 PCLK ^{*3}
0008 8255h	SMCI2	Receive data register	RDR	8	8	2, 3 PCLK ^{*3}
0008 8256h	SMCI2	Smart card mode register	SCMR	8	8	2, 3 PCLK ^{*3}
0008 8280h	CRC	CRC control register	CRCCR	8	8	2, 3 PCLK ^{*3}
0008 8281h	CRC	CRC data input register	CRCDIR	8	8	2, 3 PCLK ^{*3}
0008 8282h	CRC	CRC data output register	CRCDOR	16	16	2, 3 PCLK ^{*3}
0008 8300h	RIIC	I ² C bus control register 1	ICCR1	8	8	2, 3 PCLK ^{*3}
0008 8301h	RIIC	I ² C bus control register 2	ICCR2	8	8	2, 3 PCLK ^{*3}
0008 8302h	RIIC	I ² C bus mode register 1	ICMR1	8	8	2, 3 PCLK ^{*3}
0008 8303h	RIIC	I ² C bus mode register 2	ICMR2	8	8	2, 3 PCLK ^{*3}
0008 8304h	RIIC	I ² C bus mode register 3	ICMR3	8	8	2, 3 PCLK ^{*3}
0008 8305h	RIIC	I ² C bus function enable register	ICFER	8	8	2, 3 PCLK ^{*3}
0008 8306h	RIIC	I ² C bus status enable register	ICSER	8	8	2, 3 PCLK ^{*3}
0008 8307h	RIIC	I ² C bus interrupt enable register	ICIER	8	8	2, 3 PCLK ^{*3}
0008 8308h	RIIC	I ² C bus status register 1	ICSR1	8	8	2, 3 PCLK ^{*3}
0008 8309h	RIIC	I ² C bus status register 2	ICSR2	8	8	2, 3 PCLK ^{*3}
0008 830Ah	RIIC	Slave address register L0	SARL0	8	8	2, 3 PCLK ^{*3}
0008 830Ah	RIIC	Internal counter L for timeout	TMOCNTL	8	8	2, 3 PCLK ^{*3}
0008 830Bh	RIIC	Slave address register U0	SARU0	8	8	2, 3 PCLK ^{*3}
0008 830Bh	RIIC	Internal counter U for timeout	TMOCNTU	8	8	2, 3 PCLK ^{*3}
0008 830Bh	RIIC	Slave address register U0	SARU0	8	8	2, 3 PCLK ^{*3}
0008 830Ch	RIIC	Slave address register L1	SARL1	8	8	2, 3 PCLK ^{*3}
0008 830Dh	RIIC	Slave address register U1	SARU1	8	8	2, 3 PCLK ^{*3}
0008 830Eh	RIIC	Slave address register L2	SARL2	8	8	2, 3 PCLK ^{*3}
0008 830Fh	RIIC	Slave address register U2	SARU2	8	8	2, 3 PCLK ^{*3}
0008 8310h	RIIC	I ² C bus bit rate low-level register	ICBRL	8	8	2, 3 PCLK ^{*3}
0008 8311h	RIIC	I ² C bus bit rate high-level register	ICBRH	8	8	2, 3 PCLK ^{*3}
0008 8312h	RIIC	I ² C bus transmit data register	ICDRT	8	8	2, 3 PCLK ^{*3}
0008 8313h	RIIC	I ² C bus receive data register	ICDRR	8	8	2, 3 PCLK ^{*3}
0008 8380h	RSPI	RSPI control register	SPCR	8	8	2, 3 PCLK ^{*3}
0008 8381h	RSPI	RSPI slave select polarity register	SSLP	8	8	2, 3 PCLK ^{*3}
0008 8382h	RSPI	RSPI pin control register	SPPCR	8	8	2, 3 PCLK ^{*3}

Table 4.1 List of I/O Registers (Address Order) (16 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0009 4019h	LIN0	Data 2 buffer register	L0DB2	8	8, 16, 32	2, 3 PCLK* ³
0009 401Ah	LIN0	Data 3 buffer register	L0DB3	8	8, 16, 32	2, 3 PCLK* ³
0009 401Bh	LIN0	Data 4 buffer register	L0DB4	8	8, 16, 32	2, 3 PCLK* ³
0009 401Ch	LIN0	Data 5 buffer register	L0DB5	8	8, 16, 32	2, 3 PCLK* ³
0009 401Dh	LIN0	Data 6 buffer register	L0DB6	8	8, 16, 32	2, 3 PCLK* ³
0009 401Eh	LIN0	Data 7 buffer register	L0DB7	8	8, 16, 32	2, 3 PCLK* ³
0009 401Fh	LIN0	Data 8 buffer register	L0DB8	8	8, 16, 32	2, 3 PCLK* ³
000C 1200h	MTU3	Timer control register	TCR	8	8, 16, 32	5 ICLK
000C 1201h	MTU4	Timer control register	TCR	8	8	5 ICLK
000C 1202h	MTU3	Timer mode register 1	TMDR1	8	8, 16	5 ICLK
000C 1203h	MTU4	Timer mode register 1	TMDR1	8	8	5 ICLK
000C 1204h	MTU3	Timer I/O control register H	TIORH	8	8, 16, 32	5 ICLK
000C 1205h	MTU3	Timer I/O control register L	TIORL	8	8	5 ICLK
000C 1206h	MTU4	Timer I/O control register H	TIORH	8	8, 16	5 ICLK
000C 1207h	MTU4	Timer I/O control register L	TIORL	8	8	5 ICLK
000C 1208h	MTU3	Timer interrupt enable register	TIER	8	8, 16	5 ICLK
000C 1209h	MTU4	Timer interrupt enable register	TIER	8	8	5 ICLK
000C 120Ah	MTU	Timer output master enable register A	TOERA	8	8	5 ICLK
000C 120Dh	MTU	Timer gate control register A	TGCRA	8	8	5 ICLK
000C 120Eh	MTU	Timer output control register 1A	TOCR1A	8	8, 16	5 ICLK
000C 120Fh	MTU	Timer output control register 2A	TOCR2A	8	8	5 ICLK
000C 1210h	MTU3	Timer counter	TCNT	16	16, 32	5 ICLK
000C 1212h	MTU4	Timer counter	TCNT	16	16	5 ICLK
000C 1214h	MTU	Timer cycle data register A	TCDRA	16	16, 32	5 ICLK
000C 1216h	MTU	Timer dead time data register A	TDDRA	16	16	5 ICLK
000C 1218h	MTU3	Timer general register A	TGRA	16	16, 32	5 ICLK
000C 121Ah	MTU3	Timer general register B	TGRB	16	16	5 ICLK
000C 121Ch	MTU4	Timer general register A	TGRA	16	16, 32	5 ICLK
000C 121Eh	MTU4	Timer general register B	TGRB	16	16	5 ICLK
000C 1220h	MTU	Timer subcounter A	TCNTSA	16	16, 32	5 ICLK
000C 1222h	MTU	Timer cycle buffer register A	TCBRA	16	16	5 ICLK
000C 1224h	MTU3	Timer general register C	TGRC	16	16, 32	5 ICLK
000C 1226h	MTU3	Timer general register D	TGRD	16	16	5 ICLK
000C 1228h	MTU4	Timer general register C	TGRC	16	16, 32	5 ICLK
000C 122Ah	MTU4	Timer general register D	TGRD	16	16	5 ICLK
000C 122Ch	MTU3	Timer status register	TSR	8	8, 16	5 ICLK
000C 122Dh	MTU4	Timer status register	TSR	8	8	5 ICLK
000C 1230h	MTU	Timer interrupt skipping set register 1A	TITCR1A	8	8, 16	5 ICLK
000C 1231h	MTU	Timer interrupt skipping counter 1A	TITCNT1A	8	8	5 ICLK
000C 1232h	MTU	Timer buffer transfer set register A	TBTERA	8	8	5 ICLK
000C 1234h	MTU	Timer dead time enable register A	TDERA	8	8	5 ICLK
000C 1236h	MTU	Timer output level buffer register A	TOLBRA	8	8	5 ICLK
000C 1238h	MTU3	Timer buffer operation transfer mode register	TBTM	8	8, 16	5 ICLK
000C 1239h	MTU4	Timer buffer operation transfer mode register	TBTM	8	8	5 ICLK

Table 4.2 List of I/O Registers (Bit Order) (6 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
ICU	DTCER029	—	—	—	—	—	—	—	DTCE
ICU	DTCER030	—	—	—	—	—	—	—	DTCE
ICU	DTCER031	—	—	—	—	—	—	—	DTCE
ICU	DTCER045	—	—	—	—	—	—	—	DTCE
ICU	DTCER046	—	—	—	—	—	—	—	DTCE
ICU	DTCER064	—	—	—	—	—	—	—	DTCE
ICU	DTCER065	—	—	—	—	—	—	—	DTCE
ICU	DTCER066	—	—	—	—	—	—	—	DTCE
ICU	DTCER067	—	—	—	—	—	—	—	DTCE
ICU	DTCER068	—	—	—	—	—	—	—	DTCE
ICU	DTCER069	—	—	—	—	—	—	—	DTCE
ICU	DTCER070	—	—	—	—	—	—	—	DTCE
ICU	DTCER071	—	—	—	—	—	—	—	DTCE
ICU	DTCER098	—	—	—	—	—	—	—	DTCE
ICU	DTCER102	—	—	—	—	—	—	—	DTCE
ICU	DTCER103	—	—	—	—	—	—	—	DTCE
ICU	DTCER106	—	—	—	—	—	—	—	DTCE
ICU	DTCER114	—	—	—	—	—	—	—	DTCE
ICU	DTCER115	—	—	—	—	—	—	—	DTCE
ICU	DTCER116	—	—	—	—	—	—	—	DTCE
ICU	DTCER117	—	—	—	—	—	—	—	DTCE
ICU	DTCER121	—	—	—	—	—	—	—	DTCE
ICU	DTCER122	—	—	—	—	—	—	—	DTCE
ICU	DTCER125	—	—	—	—	—	—	—	DTCE
ICU	DTCER126	—	—	—	—	—	—	—	DTCE
ICU	DTCER129	—	—	—	—	—	—	—	DTCE
ICU	DTCER130	—	—	—	—	—	—	—	DTCE
ICU	DTCER131	—	—	—	—	—	—	—	DTCE
ICU	DTCER132	—	—	—	—	—	—	—	DTCE
ICU	DTCER134	—	—	—	—	—	—	—	DTCE
ICU	DTCER135	—	—	—	—	—	—	—	DTCE
ICU	DTCER136	—	—	—	—	—	—	—	DTCE
ICU	DTCER137	—	—	—	—	—	—	—	DTCE
ICU	DTCER138	—	—	—	—	—	—	—	DTCE
ICU	DTCER139	—	—	—	—	—	—	—	DTCE
ICU	DTCER140	—	—	—	—	—	—	—	DTCE
ICU	DTCER141	—	—	—	—	—	—	—	DTCE
ICU	DTCER142	—	—	—	—	—	—	—	DTCE
ICU	DTCER143	—	—	—	—	—	—	—	DTCE
ICU	DTCER144	—	—	—	—	—	—	—	DTCE
ICU	DTCER145	—	—	—	—	—	—	—	DTCE
ICU	DTCER149	—	—	—	—	—	—	—	DTCE
ICU	DTCER150	—	—	—	—	—	—	—	DTCE
ICU	DTCER151	—	—	—	—	—	—	—	DTCE
ICU	DTCER152	—	—	—	—	—	—	—	DTCE
ICU	DTCER153	—	—	—	—	—	—	—	DTCE
ICU	DTCER174	—	—	—	—	—	—	—	DTCE
ICU	DTCER175	—	—	—	—	—	—	—	DTCE
ICU	DTCER176	—	—	—	—	—	—	—	DTCE
ICU	DTCER177	—	—	—	—	—	—	—	DTCE
ICU	DTCER178	—	—	—	—	—	—	—	DTCE
ICU	DTCER179	—	—	—	—	—	—	—	DTCE

Table 4.2 List of I/O Registers (Bit Order) (14 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
PORT8	DR	—	—	—	—	—	B2	B1	B0
PORT9	DR	—	B6	B5	B4	B3	B2	B1	B0
PORTA	DR	—	—	B5	B4	B3	B2	B1	B0
PORTB	DR	B7	B6	B5	B4	B3	B2	B1	B0
PORTD	DR	B7	B6	B5	B4	B3	B2	B1	B0
PORTE	DR	—	—	B5	B4	B3	—	B1	B0
PORTG	DR	—	—	B5	B4	B3	B2	B1	B0
PORT1	PORT	—	—	—	—	—	—	B1	B0
PORT2	PORT	—	—	—	B4	B3	B2	B1	B0
PORT3	PORT	—	—	—	—	B3	B2	B1	B0
PORT4	PORT	B7	B6	B5	B4	B3	B2	B1	B0
PORT5	PORT	—	—	B5	B4	B3	B2	B1	B0
PORT6	PORT	—	—	B5	B4	B3	B2	B1	B0
PORT7	PORT	—	B6	B5	B4	B3	B2	B1	B0
PORT8	PORT	—	—	—	—	—	B2	B1	B0
PORT9	PORT	—	B6	B5	B4	B3	B2	B1	B0
PORTA	PORT	—	—	B5	B4	B3	B2	B1	B0
PORTB	PORT	B7	B6	B5	B4	B3	B2	B1	B0
PORTD	PORT	B7	B6	B5	B4	B3	B2	B1	B0
PORTE	PORT	—	—	B5	B4	B3	B2	B1	B0
PORTG	PORT	—	—	B5	B4	B3	B2	B1	B0
PORT1	ICR	—	—	—	—	—	—	B1	B0
PORT2	ICR	—	—	—	B4	B3	B2	B1	B0
PORT3	ICR	—	—	—	—	B3	B2	B1	B0
PORT4	ICR	B7	B6	B5	B4	B3	B2	B1	B0
PORT5	ICR	—	—	B5	B4	B3	B2	B1	B0
PORT6	ICR	—	—	B5	B4	B3	B2	B1	B0
PORT7	ICR	—	B6	B5	B4	B3	B2	B1	B0
PORT8	ICR	—	—	—	—	—	B2	B1	B0
PORT9	ICR	—	B6	B5	B4	B3	B2	B1	B0
PORTA	ICR	—	—	B5	B4	B3	B2	B1	B0
PORTB	ICR	B7	B6	B5	B4	B3	B2	B1	B0
PORTD	ICR	B7	B6	B5	B4	B3	B2	B1	B0
PORTE	ICR	—	—	B5	B4	B3	—	B1	B0
PORTG	ICR	—	—	B5	B4	B3	B2	B1	B0
IOPORT	PF8IRQ	—	—	—	—	ITS1[1:0]		ITS0[1:0]	
IOPORT	PF9IRQ	—	—	—	—	—	ITS2	—	—
IOPORT	PFAADC	—	—	—	—	—	—	ADTRG1S	ADTRG0S
IOPORT	PFCMTU	TCLKS[1:0]		—	—	—	—	MTUS1	MTUS0
IOPORT	PFDGPT	—	—	—	—	—	—	—	GPTS
IOPORT	PPFSCI	—	—	—	—	—	SCI2S	—	—
IOPORT	PFGSPI	SSL3E	SSL2E	SSL1E	SSL0E	MISOE	MOSIE	RSPCKE	—
IOPORT	PFHSPI	—	—	—	—	—	—	RSPIS[1:0]	
IOPORT	PFJCAN	CANS[1:0]		—	—	—	—	—	CANE
IOPORT	PFKLIN	—	—	—	—	—	—	—	LINE
IOPORT	PFMPOE	—	—	—	POE11E	POE10E	POE8E	POE4E	POE0E
IOPORT	PFNPOE	POE10S	—	—	—	—	—	—	—
SYSTEM	DPSBYCR	DPSBY	IOKEEP	—	—	—	—	—	—
SYSTEM	DPSWCR	—	—	—	—	WTSTS[5:0]			
SYSTEM	DPSIER	DNMIE	—	—	DLVDE	—	—	DIRQ1E	DIRQ0E

Table 4.2 List of I/O Registers (Bit Order) (16 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
POE	POECR2	—	—	—	—	—	MTU3BDZE	MTU4ACZE	MTU4BDZE
		—	—	—	—	—	MTU6BDZE	MTU7ACZE	MTU7BDZE
POE	POECR3	—	—	—	—	—	—	GPT3ABZE	GPT2ABZE
		—	—	—	—	—	—	GPT1ABZE	GPT0ABZE
POE	POECR4	—	—	IC5ADDMT67ZE	IC4ADDMT67ZE	IC3ADDMT67ZE	—	IC1ADDMT67ZE	CMADDMT67ZE
		—	—	IC5ADDMT34ZE	IC4ADDMT34ZE	IC3ADDMT34ZE	IC2ADDMT34ZE	—	CMADDMT34ZE
POE	POECR5	—	—	—	—	—	—	—	—
		—	—	IC5ADDMT0ZE	IC4ADDMT0ZE	—	IC2ADDMT0ZE	IC1ADDMT0ZE	CMADDMT0ZE
POE	POECR6	—	—	—	IC4ADDGPT23ZE	IC3ADDGPT23ZE	IC2ADDGPT23ZE	IC1ADDGPT23ZE	CMADDGPT23ZE
		—	—	IC5ADDGPT01ZE	—	IC3ADDGPT01ZE	IC2ADDGPT01ZE	IC1ADDGPT01ZE	CMADDGPT01ZE
POE	ICSR4	—	—	—	POE10F	—	—	POE10E	PIE4
		—	—	—	—	—	—	POE10M[1:0]	—
POE	ALR1	—	—	—	—	—	—	—	—
		OLSEN	—	OLSG2B	OLSG2A	OLSG1B	OLSG1A	OLSG0B	OLSG0A
POE	ICSR5	—	—	—	POE11F	—	—	POE11E	PIE5
		—	—	—	—	—	—	POE11M[1:0]	—
CAN0*3	MB.ID	IDE	RTR	—	—	—	SID[10:0]	—	—
		—	—	—	SID[10:0]	—	—	EID[17:0]	—
		—	—	—	—	EID[17:0]	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
	MB.DLC	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	DLC[3:0]	—
	MB.DATA 0 to 7	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
CAN0*3	MKR0	—	—	—	—	—	SID[10:0]	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
	MKR1	—	—	—	—	—	SID[10:0]	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
	MKR2	—	—	—	—	—	SID[10:0]	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
CAN0*3	MKR3	—	—	—	—	—	SID[10:0]	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
CAN0*3	MKR4	—	—	—	—	—	SID[10:0]	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

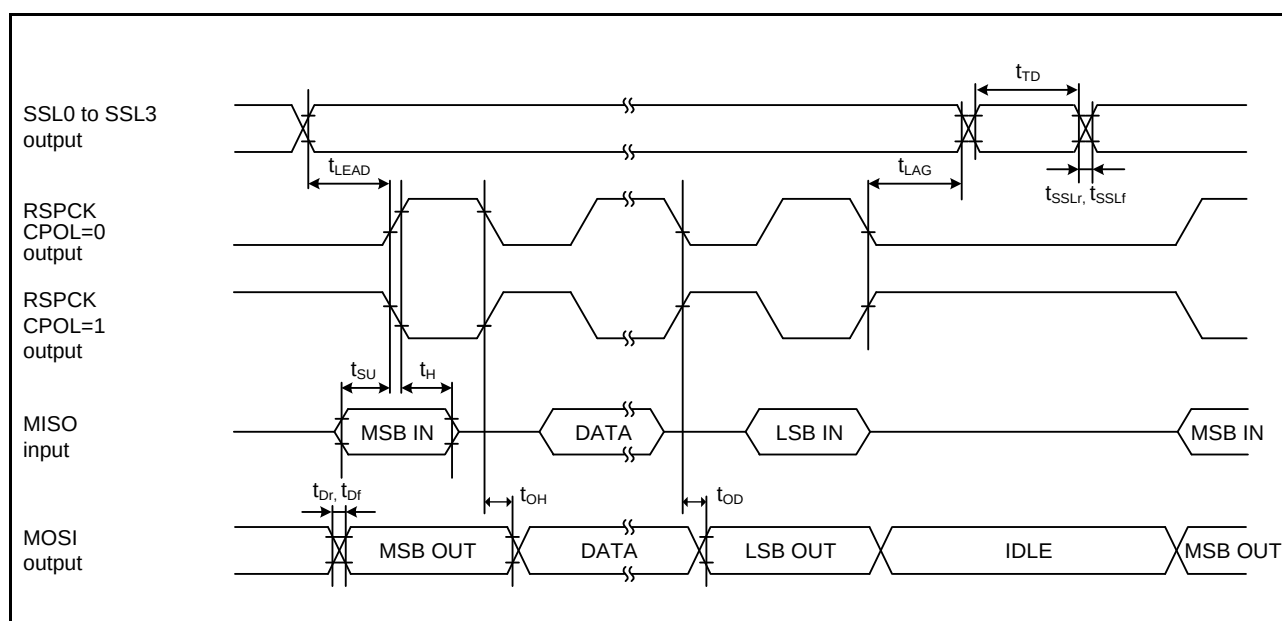
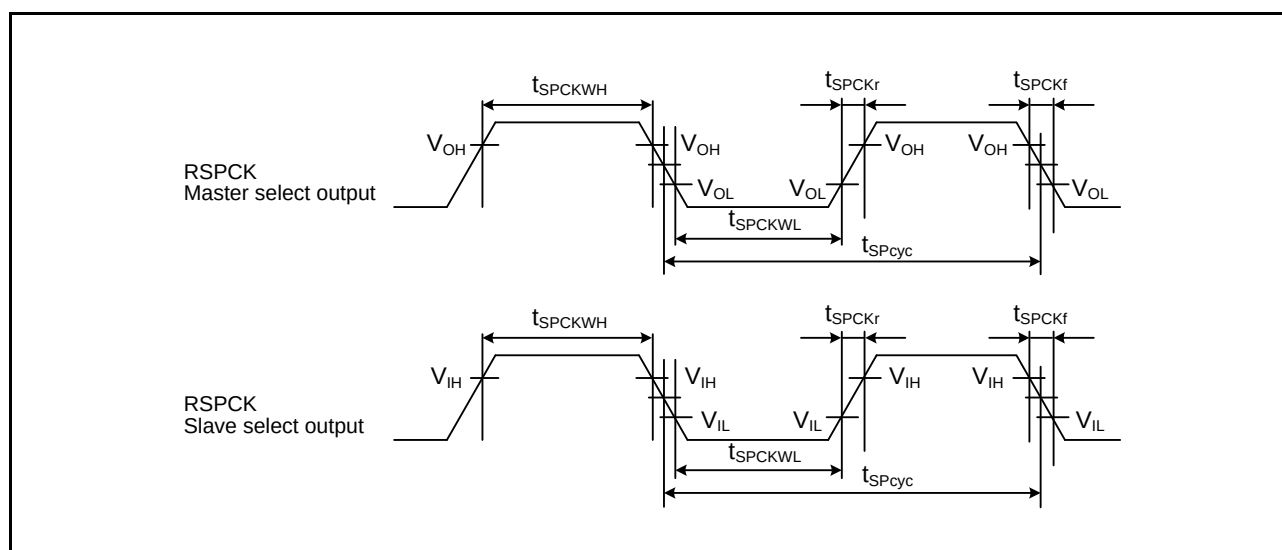
Table 5.1 Absolute Maximum Ratings

Item		Symbol	Value	Unit
Power supply voltage		VCC PLLVCC	-0.3 to +6.5	V
Input voltage (except for ports 4 to 6)		V _{IN}	-0.3 to VCC+0.3	V
Input voltage (port 4)		V _{IN}	-0.3 to AVCC0+0.3	V
Input voltage (ports 5 and 6)		V _{IN}	-0.3 to AVCC+0.3	V
Analog power supply voltage		AVCC0, AVCC* ¹	-0.3 to +6.5	V
Reference power supply voltage		VREFH0* ¹	-0.3 to AVCC0+0.3	V
		VREF* ¹	-0.3 to AVCC+0.3	
Analog input voltage (port 4)		V _{AN}	-0.3 to AVCC0+0.3	V
Analog input voltage (ports 5 and 6)		V _{AN}	-0.3 to AVCC+0.3	V
Operating temperature	D version	T _{opr}	-40 to +85	°C
	G version	T _{opr}	-40 to +105	°C
Storage temperature		T _{stg}	-55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. Do not leave the AVCC0, VREFH0, VREFL0, AVSS0, AVCC, VREF, and AVSS pins open circuit even if the A/D converter is not to be used.

- When the 12-bit converter is not in use:
Connect the AVCC0 pin to AVCC (or VCC for a 64-pin product), the VREFH0 pin to VREF (or AVCC or VCC for an 80- or 64-pin product, respectively), and the AVSS0 and VREFL0 pins to VSS.
- When the 10-bit converter is not in use:
Connect the AVCC pin to AVCC0, the VREF pin to VREFH0, and the AVSS pin to AVSS0.
- When neither the 10- nor the 12-bit converter is in use:
Connect the AVCC0, VREFH0, AVCC, and VREF pins to VCC, and the AVSS0, VREFL0, and AVSS pins to VSS.



5.4 A/D Conversion Characteristics

Table 5.15 10-Bit A/D Conversion Characteristics

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Ta = Topr

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	10	10	10	Bit	
Conversion time*1 (AD clock = 25-MHz operation)	2.0	-	-	μs	Sampling 25 states
Analog input capacitance	-	-	4	pF	
Integral nonlinearity error	-	-	±3.0	LSB	
Offset error	-	-	±3.0	LSB	
Full-scale error	-	-	±3.0	LSB	
Quantization error	-	±0.5	-	LSB	
Absolute accuracy	-	-	±4.0	LSB	
Permissible signal source impedance	-	-	1.0	kΩ	

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Ta = Topr. Ta is the same under conditions 2 and 3.

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	10	10	10	Bit	
Conversion time*1 (AD clock = 50-MHz operation)	1.0	-	-	μs	Sampling 25 states
Analog input capacitance	-	-	4	pF	
Integral nonlinearity error	-	-	±3.0	LSB	
Offset error	-	-	±3.0	LSB	
Full-scale error	-	-	±3.0	LSB	
Quantization error	-	±0.5	-	LSB	
Absolute accuracy	-	-	±4.0	LSB	
Permissible signal source impedance	-	-	1.0	kΩ	

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

5.6 Oscillation Stop Detection Timing

Table 5.20 Oscillation Stop Detection Circuit Characteristics

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t _{dr}	-	-	1.0	ms	Figure 5.23
Internal oscillation frequency when oscillation stop is detected	f _{MAIN}	0.5	-	7.0	MHz	

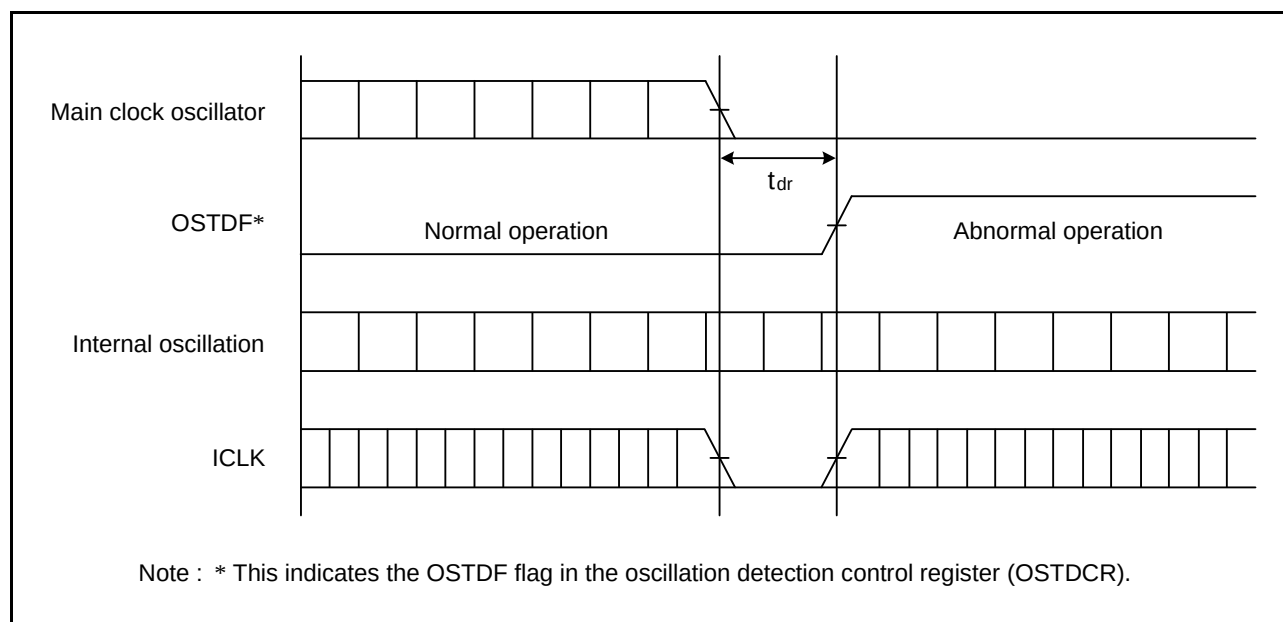


Figure 5.23 Oscillation Stop Detection Timing

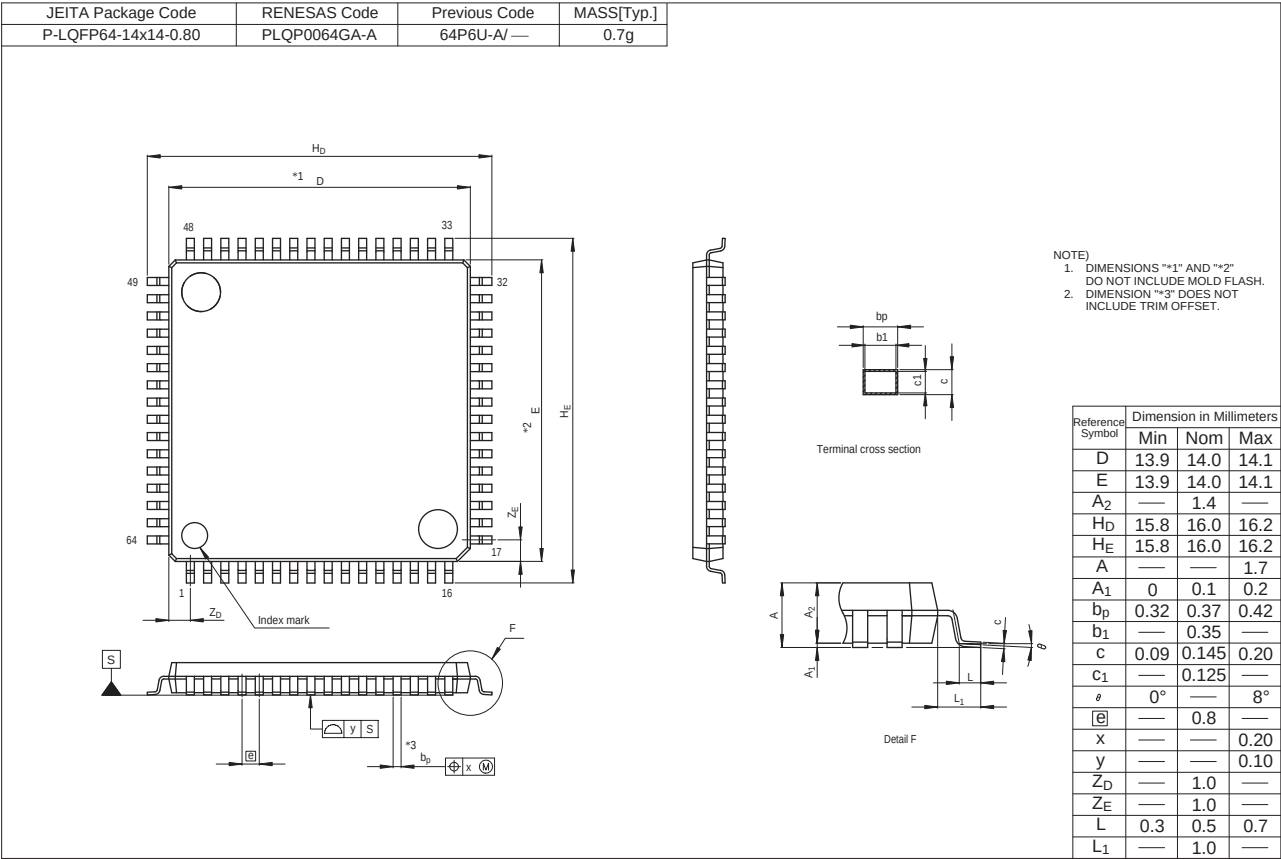


Figure E 64-Pin LQFP (PLQP0064GA-A) Package Dimensions