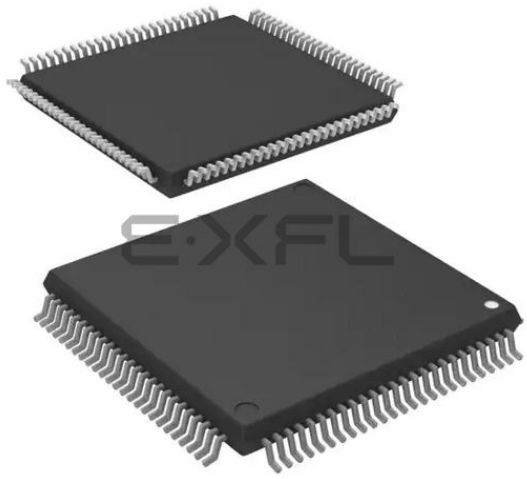
Renesas Electronics America Inc - R5F562G7ADFP#V1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 12x10b, 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562g7adfp-v1

Table 1.1 Outline of Specifications (4 / 5)

Classification	Module/Function	Description
Communications	CAN module (CAN) (as an optional function)	• 1 channel • 32 mailboxes
	Serial peripheral interface (RSPI)	• 1 unit • RSPI transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPI clock (RSPCK) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) Capable of handling serial transfer as a master or slave • Data formats Switching between MSB first and LSB first The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Buffered structure • Double buffers for both transmission and reception
	LIN module (LIN)	• 1 channel (LIN master) • Supports revisions 1.3, 2.0, and 2.1 of the LIN protocol
A/D converter	12-bit A/D converter (S12ADA)	• 12 bits (2 units x 4 channels) • 12-bit resolution • Conversion time: 1.0 μs per channel (in operation with A/D conversion clock ADCLK at 50 MHz) for AVCC = 4.0 to 5.5 V 2.0 μs per channel (in operation with A/D conversion clock ADCLK at 25 MHz) for AVCC0 = 3.0 to 3.6 V • Two basic operating modes Single mode and scan mode • Scan mode One-cycle scan mode Continuous scan mode 2-channel scan mode (Input ports of the A/D unit are divided into two groups in this mode, and the activation sources are separately selectable for each group.) • Sample-and-hold function A common sample-and-hold circuit for both units is included. Additionally, sample-and-hold circuit for each unit is included. (three channels per unit) • A/D-conversion register settings for each input pin. • Two registers for the result of conversion are provided for a single analog input pin of each unit (AN000 and AN100). • Three ways to start A/D conversion Conversion can be started by software, a conversion start trigger from a timer (MTU3 or GPT), or an external trigger signal. • Functionality for 8- or 10-bit precision output Right-shifting of the results of conversion for output by two or four bits is selectable. • Self-diagnostic function The self-diagnostic function internally generates three analog input voltages (VREFL0, VREFH0 x 1/2, VREFH0). • Amplification of input signals by a programmable gain amplifier (three channels per unit) Amplification rate: 2.0-, 2.5-, 3.077-, 3.636-, 4.0-, 4.444-, 5.0-, 5.714-, 6.667-, 10.0-, or 13.333-times amplification (a total of 11 steps) • Window comparators (three channels per unit)

Table 1.3 List of Products (2 / 2)

Group	Part No.	Order Part No.	Package	ROM Capacity	RAM Capacity	Data Flash Capacity	Power Supply Voltage	CAN	Operating Temp. Range
RX62T	R5F562T7EDFH	R5F562T7EDFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes	2.7 to 3.6 V	Not Support-ed	-40 to +85°C (D version)
	R5F562T7EDFP	R5F562T7EDFP#V3	PLQP0100KB-A						
	R5F562T7EDFF	R5F562T7EDFF#V3	PLQP0080JA-A						
	R5F562T7EDFM	R5F562T7EDFM#V3	PLQP0064KB-A						
	R5F562T7EDFK	R5F562T7EDFK#V3	PLQP0064GA-A						
	R5F562T6EDFF	R5F562T6EDFF#V3	PLQP0080JA-A	64 Kbytes	8 Kbytes				
	R5F562T6EDFM	R5F562T6EDFM#V3	PLQP0064KB-A						
	R5F562T6EDFK	R5F562T6EDFK#V3	PLQP0064GA-A						
	R5F562TAAGFH	R5F562TAAGFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes	VCC/PLLVCC 4.0 to 5.5 V AVCC/AVCC0 4.0 to 5.5 V	Support-ed	-40 to +105°C (G version) *1
	R5F562TAAGFP	R5F562TAAGFP#V3	PLQP0100KB-A						
	R5F562TAAGFF	R5F562TAAGFF#V3	PLQP0080JA-A						
	R5F562TAGGFF	R5F562TAGGFF#V3	PLQP0080JA-A						
	R5F562TAAGFM	R5F562TAAGFM#V3	PLQP0064KB-A						
	R5F562TAAGFK	R5F562TAAGFK#V3	PLQP0064GA-A						
	R5F562T7AGFH	R5F562T7AGFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes			
	R5F562T7AGFP	R5F562T7AGFP#V3	PLQP0100KB-A						
	R5F562T7AGFF	R5F562T7AGFF#V3	PLQP0080JA-A						
	R5F562T7GGFF	R5F562T7GGFF#V3	PLQP0080JA-A						
	R5F562T7AGFM	R5F562T7AGFM#V3	PLQP0064KB-A						
	R5F562T7AGFK	R5F562T7AGFK#V3	PLQP0064GA-A						
	R5F562T6AGFF	R5F562T6AGFF#V3	PLQP0080JA-A	64 Kbytes	8 Kbytes				
	R5F562T6AGFM	R5F562T6AGFM#V3	PLQP0064KB-A						
	R5F562T6AGFK	R5F562T6AGFK#V3	PLQP0064GA-A						
	R5F562TABGFH	R5F562TABGFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes	VCC/PLLVCC 2.7 to 3.6 V AVCC/AVCC0 3.0 to 3.6 V or 4.0 to 5.5 V		
	R5F562TABGFP	R5F562TABGFP#V3	PLQP0100KB-A						
	R5F562TABGFF	R5F562TABGFF#V3	PLQP0080JA-A						
	R5F562TABGFM	R5F562TABGFM#V3	PLQP0064KB-A						
	R5F562TABGFK	R5F562TABGFK#V3	PLQP0064GA-A						
	R5F562T7BGFH	R5F562T7BGFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes			
	R5F562T7BGFP	R5F562T7BGFP#V3	PLQP0100KB-A						
	R5F562T7BGFF	R5F562T7BGFF#V3	PLQP0080JA-A						
	R5F562T7BGFM	R5F562T7BGFM#V3	PLQP0064KB-A						
	R5F562T7BGFK	R5F562T7BGFK#V3	PLQP0064GA-A						
	R5F562T6BGFF	R5F562T6BGFF#V3	PLQP0080JA-A	64 Kbytes	8 Kbytes				
	R5F562T6BGFM	R5F562T6BGFM#V3	PLQP0064KB-A						
	R5F562T6BGFK	R5F562T6BGFK#V3	PLQP0064GA-A						
RX62G	R5F562GAADFH	R5F562GAADFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes	VCC/PLLVCC 4.0 to 5.5 V AVCC/AVCC0 4.0 to 5.5 V	Support-ed	-40 to +85°C (D version)
	R5F562GAADFP	R5F562GAADFP#V3	PLQP0100KB-A						
	R5F562G7ADFH	R5F562G7ADFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes			
	R5F562G7ADFP	R5F562G7ADFP#V3	PLQP0100KB-A						
	R5F562GADDFH	R5F562GADDFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes		Not Support-ed	
	R5F562GADDFP	R5F562GADDFP#V3	PLQP0100KB-A						
	R5F562G7DDFH	R5F562G7DDFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes			
	R5F562G7DDFP	R5F562G7DDFP#V3	PLQP0100KB-A						
	R5F562GAAGFH	R5F562GAAGFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes	VCC/PLLVCC 4.0 to 5.5 V AVCC/AVCC0 4.0 to 5.5 V	Support-ed	-40 to +105°C (G versio) *1
	R5F562GAAGFP	R5F562GAAGFP#V3	PLQP0100KB-A						
	R5F562G7AGFH	R5F562G7AGFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes			
	R5F562G7AGFP	R5F562G7AGFP#V3	PLQP0100KB-A						

Note 1. Please contact us if you are using a G version.

Table 1.7 List of Pins and Pin Functions (80-Pin LQFP: R5F562TxGDFF) (1 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communication	Interrupt	POE	Debugging
1	EMLE							
2	VSS							
3	MDE							
4	VCL							
5	MD1							
6	MD0							
7		PE4		MTCLKC-C		IRQ1-B	POE10#-B	
8		PE3		MTCLKD-C		IRQ2-A	POE11#	
9	RES#							
10	XTAL							
11	VSS							
12	EXTAL							
13	VCC							
14		PE2				NMI	POE10#-A	
15		PD7		GTIOC0A-B				TRST#
16		PD6		GTIOC0B-B				TMS
17		PD5		GTIOC1A-B	RXD1			TDI
18		PD4		GTIOC1B-B	SCK1			TCK
19		PD3		GTIOC2A-B	TXD1			TDO
20		PD2		GTIOC2B-B				
21		PB7			SCK2-A			
22		PB6			CRX-A/ RXD2-A			
23		PB5			CTX-A/ TXD2-A			
24	PLLVCC							
25		PB4		GTETRG		IRQ3	POE8#	
26	PLLVSS							
27		PB3		MTIOC0A-A	SCK0			
28		PB2		MTIOC0B-A	TXD0/SDA			
29		PB1		MTIOC0C	RXD0/SCL			
30		PB0		MTIOC0D				
31		PA5	ADTRG1#-A	MTIOC1A				
32		PA3		MTIOC2A				
33	VCC							
34		P96				IRQ4	POE4#	
35	VSS							
36		P95		MTIOC6B				
37		P94		MTIOC7A				
38		P93		MTIOC7B				
39		P92		MTIOC6D				
40		P91		MTIOC7C				
41		P90		MTIOC7D				

4. I/O Registers

This section gives information on the on-chip I/O register addresses and bit configurations. The information is given as shown below. Notes on writing to registers are also given at the end.

(1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to functional modules (abbreviations).
- The number of access cycles indicates the number of states based on the specified reference clock.
- Among the I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.
- A unit of access is specified for each register. Access other than in the specified unit is prohibited.

(2) I/O register bits

- Bit configurations of the registers are listed in the same order as the register addresses.
- Reserved bits are indicated by "—" in the bit name column.
- Space in the bit name field indicates that the entire register is allocated to either the counter or data.
- For the registers of 16 or 32 bits, the MSB is listed first.

(3) Notes on writing to I/O registers

When writing to an I/O register, the CPU starts executing the subsequent instruction before completing I/O register write. This may cause the subsequent instruction to be executed before the post-update I/O register value is reflected on the operation.
As described in the following examples, special care is required for the cases in which the subsequent instruction must be executed after the post-update I/O register value is actually reflected.

[Examples of cases requiring special care]

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERm of the ICU (interrupt request enable bit)*1 cleared to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

Note 1. See section 11.2.2, Interrupt Request Enable Register m (IERm) (m = 02h to 1Fh) in the User's manual: Hardware.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

Table 4.1 List of I/O Registers (Address Order) (2 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 6526h	MPU	Region invalidation operation register	MPOPI	16	16	1 ICLK
0008 6528h	MPU	Instruction-hit region register	MHITI	32	32	1 ICLK
0008 652Ch	MPU	Data-hit region register	MHITD	32	32	1 ICLK
0008 7010h	ICU	Interrupt request register 016	IR016	8	8	2 ICLK
0008 7015h	ICU	Interrupt request register 021	IR021	8	8	2 ICLK
0008 7017h	ICU	Interrupt request register 023	IR023	8	8	2 ICLK
0008 701Bh	ICU	Interrupt request register 027	IR027	8	8	2 ICLK
0008 701Ch	ICU	Interrupt request register 028	IR028	8	8	2 ICLK
0008 701Dh	ICU	Interrupt request register 029	IR029	8	8	2 ICLK
0008 701Eh	ICU	Interrupt request register 030	IR030	8	8	2 ICLK
0008 701Fh	ICU	Interrupt request register 031	IR031	8	8	2 ICLK
0008 702Ch	ICU	Interrupt request register 044	IR044	8	8	2 ICLK
0008 702Dh	ICU	Interrupt request register 045	IR045	8	8	2 ICLK
0008 702Eh	ICU	Interrupt request register 046	IR046	8	8	2 ICLK
0008 702Fh	ICU	Interrupt request register 047	IR047	8	8	2 ICLK
0008 7038h	ICU	Interrupt request register 056	IR056	8	8	2 ICLK
0008 7039h	ICU	Interrupt request register 057	IR057	8	8	2 ICLK
0008 703Ah	ICU	Interrupt request register 058	IR058	8	8	2 ICLK
0008 703Bh	ICU	Interrupt request register 059	IR059	8	8	2 ICLK
0008 703Ch	ICU	Interrupt request register 060	IR060	8	8	2 ICLK
0008 7040h	ICU	Interrupt request register 064	IR064	8	8	2 ICLK
0008 7041h	ICU	Interrupt request register 065	IR065	8	8	2 ICLK
0008 7042h	ICU	Interrupt request register 066	IR066	8	8	2 ICLK
0008 7043h	ICU	Interrupt request register 067	IR067	8	8	2 ICLK
0008 7044h	ICU	Interrupt request register 068	IR068	8	8	2 ICLK
0008 7045h	ICU	Interrupt request register 069	IR069	8	8	2 ICLK
0008 7046h	ICU	Interrupt request register 070	IR070	8	8	2 ICLK
0008 7047h	ICU	Interrupt request register 071	IR071	8	8	2 ICLK
0008 7060h	ICU	Interrupt request register 096	IR096	8	8	2 ICLK
0008 7062h	ICU	Interrupt request register 098	IR098	8	8	2 ICLK
0008 7066h	ICU	Interrupt request register 102	IR102	8	8	2 ICLK
0008 7067h	ICU	Interrupt request register 103	IR103	8	8	2 ICLK
0008 706Ah	ICU	Interrupt request register 106	IR106	8	8	2 ICLK
0008 7072h	ICU	Interrupt request register 114	IR114	8	8	2 ICLK
0008 7073h	ICU	Interrupt request register 115	IR115	8	8	2 ICLK
0008 7074h	ICU	Interrupt request register 116	IR116	8	8	2 ICLK
0008 7075h	ICU	Interrupt request register 117	IR117	8	8	2 ICLK
0008 7076h	ICU	Interrupt request register 118	IR118	8	8	2 ICLK
0008 7077h	ICU	Interrupt request register 119	IR119	8	8	2 ICLK
0008 7078h	ICU	Interrupt request register 120	IR120	8	8	2 ICLK
0008 7079h	ICU	Interrupt request register 121	IR121	8	8	2 ICLK
0008 707Ah	ICU	Interrupt request register 122	IR122	8	8	2 ICLK
0008 707Bh	ICU	Interrupt request register 123	IR123	8	8	2 ICLK
0008 707Ch	ICU	Interrupt request register 124	IR124	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (8 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 7382h	ICU	Interrupt source priority register 82	IPR82	8	8	2 ICLK
0008 7388h	ICU	Interrupt source priority register 88	IPR88	8	8	2 ICLK
0008 7389h	ICU	Interrupt source priority register 89	IPR89	8	8	2 ICLK
0008 738Ah	ICU	Interrupt source priority register 8A	IPR8A	8	8	2 ICLK
0008 738Bh	ICU	Interrupt source priority register 8B	IPR8B	8	8	2 ICLK
0008 7390h	ICU	Interrupt source priority register 90	IPR90	8	8	2 ICLK
0008 7500h	ICU	IRQ control register 0	IRQCR0	8	8	2 ICLK
0008 7501h	ICU	IRQ control register 1	IRQCR1	8	8	2 ICLK
0008 7502h	ICU	IRQ control register 2	IRQCR2	8	8	2 ICLK
0008 7503h	ICU	IRQ control register 3	IRQCR3	8	8	2 ICLK
0008 7504h	ICU	IRQ control register 4	IRQCR4	8	8	2 ICLK
0008 7505h	ICU	IRQ control register 5	IRQCR5	8	8	2 ICLK
0008 7506h	ICU	IRQ control register 6	IRQCR6	8	8	2 ICLK
0008 7507h	ICU	IRQ control register 7	IRQCR7	8	8	2 ICLK
0008 7580h	ICU	Non-maskable interrupt status register	NMISR	8	8	2 ICLK
0008 7581h	ICU	Non-maskable interrupt enable register	NMIER	8	8	2 ICLK
0008 7582h	ICU	Non-maskable interrupt clear register	NMICLR	8	8	2 ICLK
0008 7583h	ICU	NMI pin interrupt control register	NMICR	8	8	2 ICLK
0008 8000h	CMT	Compare match timer start register 0	CMSTR0	16	16	2, 3 PCLK*3
0008 8002h	CMT0	Compare match timer control register	CMCR	16	16	2, 3 PCLK*3
0008 8004h	CMT0	Compare match timer counter	CMCNT	16	16	2, 3 PCLK*3
0008 8006h	CMT0	Compare match timer constant register	CMCOR	16	16	2, 3 PCLK*3
0008 8008h	CMT1	Compare match timer control register	CMCR	16	16	2, 3 PCLK*3
0008 800Ah	CMT1	Compare match timer counter	CMCNT	16	16	2, 3 PCLK*3
0008 800Ch	CMT1	Compare match timer constant register	CMCOR	16	16	2, 3 PCLK*3
0008 8010h	CMT	Compare match timer start register 1	CMSTR1	16	16	2, 3 PCLK*3
0008 8012h	CMT2	Compare match timer control register	CMCR	16	16	2, 3 PCLK*3
0008 8014h	CMT2	Compare match timer counter	CMCNT	16	16	2, 3 PCLK*3
0008 8016h	CMT2	Compare match timer constant register	CMCOR	16	16	2, 3 PCLK*3
0008 8018h	CMT3	Compare match timer control register	CMCR	16	16	2, 3 PCLK*3
0008 801Ah	CMT3	Compare match timer counter	CMCNT	16	16	2, 3 PCLK*3
0008 801Ch	CMT3	Compare match timer constant register	CMCOR	16	16	2, 3 PCLK*3
0008 8028h	WDT	Timer control/status register	TCSR	8	8	2, 3 PCLK*3
0008 8028h	WDT	Write window A register	WINA	16	16	2, 3 PCLK*3
0008 8029h	WDT	Timer counter	TCNT	8	8	2, 3 PCLK*3
0008 802Ah	WDT	Write window B register	WINB	16	16	2, 3 PCLK*3
0008 802Bh	WDT	Reset control/status register	RSTCSR	8	8	2, 3 PCLK*3
0008 8030h	IWDT	IWDT refresh register	IWDTRR	8	8	2, 3 PCLK*3
0008 8032h	IWDT	IWDT control register	IWDTCR	16	16	2, 3 PCLK*3
0008 8034h	IWDT	IWDT status register	IWDTSR	16	16	2, 3 PCLK*3
0008 8040h	ADA	A/D data register A	ADDRA	16	16	2, 3 PCLK*3
0008 8042h	ADA	A/D data register B	ADDRB	16	16	2, 3 PCLK*3
0008 8044h	ADA	A/D data register C	ADDRC	16	16	2, 3 PCLK*3
0008 8046h	ADA	A/D data register D	ADDRD	16	16	2, 3 PCLK*3

Table 4.1 List of I/O Registers (Address Order) (11 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 8383h	RSPI	RSPI status register	SPSR	8	8	2, 3 PCLK*3
0008 8384h	RSPI	RSPI data register	SPDR	16, 32	16, 32	2, 3 PCLK*3
0008 8388h	RSPI	RSPI sequence control register	SPSCR	8	8	2, 3 PCLK*3
0008 8389h	RSPI	RSPI sequence status register	SPSSR	8	8	2, 3 PCLK*3
0008 838Ah	RSPI	RSPI bit rate register	SPBR	8	8	2, 3 PCLK*3
0008 838Bh	RSPI	RSPI data control register	SPDCR	8	8	2, 3 PCLK*3
0008 838Ch	RSPI	RSPI clock delay register	SPCKD	8	8	2, 3 PCLK*3
0008 838Dh	RSPI	RSPI slave select negation delay register	SSLND	8	8	2, 3 PCLK*3
0008 838Eh	RSPI	RSPI next-access delay register	SPND	8	8	2, 3 PCLK*3
0008 838Fh	RSPI	RSPI control register 2	SPCR2	8	8	2, 3 PCLK*3
0008 8390h	RSPI	RSPI command register 0	SPCMD0	16	16	2, 3 PCLK*3
0008 8392h	RSPI	RSPI command register 1	SPCMD1	16	16	2, 3 PCLK*3
0008 8394h	RSPI	RSPI command register 2	SPCMD2	16	16	2, 3 PCLK*3
0008 8396h	RSPI	RSPI command register 3	SPCMD3	16	16	2, 3 PCLK*3
0008 8398h	RSPI	RSPI command register 4	SPCMD4	16	16	2, 3 PCLK*3
0008 839Ah	RSPI	RSPI command register 5	SPCMD5	16	16	2, 3 PCLK*3
0008 839Ch	RSPI	RSPI command register 6	SPCMD6	16	16	2, 3 PCLK*3
0008 839Eh	RSPI	RSPI command register 7	SPCMD7	16	16	2, 3 PCLK*3
0008 9000h	S12AD0	A/D control register	ADCSR	8	8	2, 3 PCLK*3
0008 9004h	S12AD0	A/D channel select register	ADANS	16	16	2, 3 PCLK*3
0008 900Ah	S12AD0	A/D programmable gain amplifier register	ADPG	16	16	2, 3 PCLK*3
0008 900Eh	S12AD0	A/D control extended register	ADCER	16	16	2, 3 PCLK*3
0008 9010h	S12AD0	A/D start trigger select register	ADSTRGR	16	16	2, 3 PCLK*3
0008 9012h	S12AD	Comparator operating mode select register 0	ADCMPMD0	16	16	2, 3 PCLK*3
0008 9014h	S12AD	Comparator operating mode select register 1	ADCMPMD1	16	16	2, 3 PCLK*3
0008 9016h	S12AD	Comparator filter mode register 0	ADCMPNR0	16	16	2, 3 PCLK*3
0008 9018h	S12AD	Comparator filter mode register 1	ADCMPNR1	16	16	2, 3 PCLK*3
0008 901Ah	S12AD	Comparator detection flag register	ADCMPFR	8	8	2, 3 PCLK*3
0008 901Ch	S12AD	Comparator interrupt select register	ADCMPSEL	16	16	2, 3 PCLK*3
0008 901Eh	S12AD0	A/D data register Diag	ADRD	16	16	2, 3 PCLK*3
0008 9020h	S12AD0	A/D data register 0A	ADDR0A	16	16	2, 3 PCLK*3
0008 9022h	S12AD0	A/D data register 1	ADDR1	16	16	2, 3 PCLK*3
0008 9024h	S12AD0	A/D data register 2	ADDR2	16	16	2, 3 PCLK*3
0008 9026h	S12AD0	A/D data register 3	ADDR3	16	16	2, 3 PCLK*3
0008 9030h	S12AD0	A/D data register 0B	ADDR0B	16	16	2, 3 PCLK*3
0008 9060h	S12AD0	A/D sampling state register	ADSSTR	8	8	2, 3 PCLK*3
0008 9080h	S12AD1	A/D control register	ADCSR	8	8	2, 3 PCLK*3
0008 9084h	S12AD1	A/D channel select register	ADANS	16	16	2, 3 PCLK*3
0008 908Ah	S12AD1	A/D programmable gain amplifier register	ADPG	16	16	2, 3 PCLK*3
0008 908Eh	S12AD1	A/D control extended register	ADCER	16	16	2, 3 PCLK*3
0008 9090h	S12AD1	A/D start trigger select register	ADSTRGR	16	16	2, 3 PCLK*3
0008 909Eh	S12AD1	A/D data register Diag	ADRD	16	16	2, 3 PCLK*3
0008 90A0h	S12AD1	A/D data register 0A	ADDR0A	16	16	2, 3 PCLK*3
0008 90A2h	S12AD1	A/D data register 1	ADDR1	16	16	2, 3 PCLK*3

Table 4.1 List of I/O Registers (Address Order) (12 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 90A4h	S12AD1	A/D data register 2	ADDR2	16	16	2, 3 PCLK*3
0008 90A6h	S12AD1	A/D data register 3	ADDR3	16	16	2, 3 PCLK*3
0008 90B0h	S12AD1	A/D data register 0B	ADDR0B	16	16	2, 3 PCLK*3
0008 90E0h	S12AD1	A/D sampling state register	ADSSTR	8	8	2, 3 PCLK*3
0008 C001h	PORT1	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C002h	PORT2	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C003h	PORT3	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C007h	PORT7	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C008h	PORT8	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C009h	PORT9	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C00Ah	PORTA	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C00Bh	PORTB	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C00Dh	PORTD	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C00Eh	PORTE	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C010h	PORTG	Data direction register	DDR*1	8	8	2, 3 PCLK*3
0008 C021h	PORT1	Data register	DR	8	8	2, 3 PCLK*3
0008 C022h	PORT2	Data register	DR	8	8	2, 3 PCLK*3
0008 C023h	PORT3	Data register	DR	8	8	2, 3 PCLK*3
0008 C027h	PORT7	Data register	DR	8	8	2, 3 PCLK*3
0008 C028h	PORT8	Data register	DR	8	8	2, 3 PCLK*3
0008 C029h	PORT9	Data register	DR	8	8	2, 3 PCLK*3
0008 C02Ah	PORTA	Data register	DR	8	8	2, 3 PCLK*3
0008 C02Bh	PORTB	Data register	DR	8	8	2, 3 PCLK*3
0008 C02Dh	PORTD	Data register	DR	8	8	2, 3 PCLK*3
0008 C02Eh	PORTE	Data register	DR	8	8	2, 3 PCLK*3
0008 C030h	PORTG	Data register	DR*1	8	8	2, 3 PCLK*3
0008 C041h	PORT1	Data register	PORT	8	8	2, 3 PCLK*3
0008 C042h	PORT2	Data register	PORT	8	8	2, 3 PCLK*3
0008 C043h	PORT3	Data register	PORT	8	8	2, 3 PCLK*3
0008 C044h	PORT4	Data register	PORT	8	8	2, 3 PCLK*3
0008 C045h	PORT5	Data register	PORT	8	8	2, 3 PCLK*3
0008 C046h	PORT6	Data register	PORT	8	8	2, 3 PCLK*3
0008 C047h	PORT7	Data register	PORT	8	8	2, 3 PCLK*3
0008 C048h	PORT8	Data register	PORT	8	8	2, 3 PCLK*3
0008 C049h	PORT9	Data register	PORT	8	8	2, 3 PCLK*3
0008 C04Ah	PORTA	Data register	PORT	8	8	2, 3 PCLK*3
0008 C04Bh	PORTB	Data register	PORT	8	8	2, 3 PCLK*3
0008 C04Dh	PORTD	Data register	PORT	8	8	2, 3 PCLK*3
0008 C04Eh	PORTE	Data register	PORT	8	8	2, 3 PCLK*3
0008 C050h	PORTG	Port register	PORT*1	8	8	2, 3 PCLK*3
0008 C061h	PORT1	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C062h	PORT2	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C063h	PORT3	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C064h	PORT4	Input buffer control register	ICR	8	8	2, 3 PCLK*3

Table 4.2 List of I/O Registers (Bit Order) (3 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
MPU	RSPAGE7				RSPN[27:0]				
					RSPN[27:0]				
					RSPN[27:0]				
				RSPN[27:0]		—	—	—	—
MPU	REPAGE7				REPN[27:0]				
					REPN[27:0]				
					REPN[27:0]				
				REPN[27:0]			UAC[2:0]		V
MPU	MPEN	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	MPEN
MPU	MPBAC	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—		UBAC[2:0]		—
MPU	MPECLR	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	CLR
MPU	MPESTS	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	DRW	DA	IA
MPU	MPDEA				DEA[31:0]				
					DEA[31:0]				
					DEA[31:0]				
					DEA[31:0]				
MPU	MPSA				SA[31:0]				
					SA[31:0]				
					SA[31:0]				
					SA[31:0]				
MPU	MPOPS	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	S
MPU	MPOPI	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	INV
MPU	MHITI	—	—	—	—	—	—	—	—
					HITI[7:0]				
		—	—	—	—	—	—	—	—
		—	—	—	—		UHACI[2:0]		—
MPU	MHITD	—	—	—	—	—	—	—	—
					HITD[7:0]				
		—	—	—	—	—	—	—	—
		—	—	—	—		UHACD[2:0]		—
ICU	IR016	—	—	—	—	—	—	—	IR
ICU	IR021	—	—	—	—	—	—	—	IR
ICU	IR023	—	—	—	—	—	—	—	IR
ICU	IR027	—	—	—	—	—	—	—	IR
ICU	IR028	—	—	—	—	—	—	—	IR
ICU	IR029	—	—	—	—	—	—	—	IR
ICU	IR030	—	—	—	—	—	—	—	IR
ICU	IR031	—	—	—	—	—	—	—	IR

Table 4.2 List of I/O Registers (Bit Order) (4 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
ICU	IR044	—	—	—	—	—	—	—	IR
ICU	IR045	—	—	—	—	—	—	—	IR
ICU	IR046	—	—	—	—	—	—	—	IR
ICU	IR047	—	—	—	—	—	—	—	IR
ICU	IR056	—	—	—	—	—	—	—	IR
ICU	IR057	—	—	—	—	—	—	—	IR
ICU	IR058	—	—	—	—	—	—	—	IR
ICU	IR059	—	—	—	—	—	—	—	IR
ICU	IR060	—	—	—	—	—	—	—	IR
ICU	IR064	—	—	—	—	—	—	—	IR
ICU	IR065	—	—	—	—	—	—	—	IR
ICU	IR066	—	—	—	—	—	—	—	IR
ICU	IR067	—	—	—	—	—	—	—	IR
ICU	IR068	—	—	—	—	—	—	—	IR
ICU	IR069	—	—	—	—	—	—	—	IR
ICU	IR070	—	—	—	—	—	—	—	IR
ICU	IR071	—	—	—	—	—	—	—	IR
ICU	IR096	—	—	—	—	—	—	—	IR
ICU	IR098	—	—	—	—	—	—	—	IR
ICU	IR102	—	—	—	—	—	—	—	IR
ICU	IR103	—	—	—	—	—	—	—	IR
ICU	IR106	—	—	—	—	—	—	—	IR
ICU	IR114	—	—	—	—	—	—	—	IR
ICU	IR115	—	—	—	—	—	—	—	IR
ICU	IR116	—	—	—	—	—	—	—	IR
ICU	IR117	—	—	—	—	—	—	—	IR
ICU	IR118	—	—	—	—	—	—	—	IR
ICU	IR119	—	—	—	—	—	—	—	IR
ICU	IR120	—	—	—	—	—	—	—	IR
ICU	IR121	—	—	—	—	—	—	—	IR
ICU	IR122	—	—	—	—	—	—	—	IR
ICU	IR123	—	—	—	—	—	—	—	IR
ICU	IR124	—	—	—	—	—	—	—	IR
ICU	IR125	—	—	—	—	—	—	—	IR
ICU	IR126	—	—	—	—	—	—	—	IR
ICU	IR127	—	—	—	—	—	—	—	IR
ICU	IR128	—	—	—	—	—	—	—	IR
ICU	IR129	—	—	—	—	—	—	—	IR
ICU	IR130	—	—	—	—	—	—	—	IR
ICU	IR131	—	—	—	—	—	—	—	IR
ICU	IR132	—	—	—	—	—	—	—	IR
ICU	IR133	—	—	—	—	—	—	—	IR
ICU	IR134	—	—	—	—	—	—	—	IR
ICU	IR135	—	—	—	—	—	—	—	IR
ICU	IR136	—	—	—	—	—	—	—	IR
ICU	IR137	—	—	—	—	—	—	—	IR
ICU	IR138	—	—	—	—	—	—	—	IR
ICU	IR139	—	—	—	—	—	—	—	IR
ICU	IR140	—	—	—	—	—	—	—	IR
ICU	IR141	—	—	—	—	—	—	—	IR
ICU	IR142	—	—	—	—	—	—	—	IR
ICU	IR143	—	—	—	—	—	—	—	IR

Table 4.2 List of I/O Registers (Bit Order) (13 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
S12AD0	ADRD*2	DIAGST[1:0]		—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD0	ADDR0A*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD0	ADDR1*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD0	ADDR2*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD0	ADDR3*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD0	ADDR0B*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD0	ADSSTR								
S12AD1	ADCSR	ADST	ADCS[1:0]		ADIE	CKS[1:0]		TRGE	EXTRG
S12AD1	ADANS	—	—	CH[1:0]		—	PG102SEL	PG101SEL	PG100SEL
		—	—	—	—	—	PG102EN	PG101EN	PG100EN
S12AD1	ADPG	—	—	—	—	PG102GAIN[3:0]			
		PG101GAIN[3:0]				PG100GAIN[3:0]			
S12AD1	ADCER	ADRFMT	—	ADIEW	ADIE2	DIAGM	DIAGLD	DIAGVAL[1:0]	
		—	—	ACE	—	—	ADPRC[1:0]		SHBYP
S12AD1	ADSTRGR	—	—	—	ADSTRS1[4:0]				
		—	—	—	ADSTRS0[4:0]				
S12AD1	ADRD*2	DIAGST[1:0]		—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD1	ADDR0A*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD1	ADDR1*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD1	ADDR2*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD1	ADDR3*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD1	ADDR0B*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD1	ADSSTR								
PORT1	DDR	—	—	—	—	—	—	B1	B0
PORT2	DDR	—	—	—	B4	B3	B2	B1	B0
PORT3	DDR	—	—	—	—	B3	B2	B1	B0
PORT7	DDR	—	B6	B5	B4	B3	B2	B1	B0
PORT8	DDR	—	—	—	—	—	B2	B1	B0
PORT9	DDR	—	B6	B5	B4	B3	B2	B1	B0
PORTA	DDR	—	—	B5	B4	B3	B2	B1	B0
PORTB	DDR	B7	B6	B5	B4	B3	B2	B1	B0
PORTD	DDR	B7	B6	B5	B4	B3	B2	B1	B0
PORTE	DDR	—	—	B5	B4	B3	—	B1	B0
PORTG	DDR	—	—	B5	B4	B3	B2	B1	B0
PORT1	DR	—	—	—	—	—	—	B1	B0
PORT2	DR	—	—	—	B4	B3	B2	B1	B0
PORT3	DR	—	—	—	—	B3	B2	B1	B0
PORT7	DR	—	B6	B5	B4	B3	B2	B1	B0

Table 4.2 List of I/O Registers (Bit Order) (22 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
MTU7	TADCOBRB								
MTU	TSYCR	CE0A	CE0D	CE0C	CE0D	CE1A	CE1B	CE2A	CE2B
MTU	TWCRB	CCE	—	—	—	—	—	SCC	WRE
MTU	TMDR2B	—	—	—	—	—	—	—	DRS
MTU6	TGRE								
MTU7	TGRE								
MTU7	TGRF								
MTU	TSTRB	CST7	CST6	—	—	—	—	—	—
MTU	TSYRB	SYNC7	SYNC6	—	—	—	—	—	—
MTU	TRWERB	—	—	—	—	—	—	—	RWE
MTU5	TCNTU								
MTU5	TGRU								
MTU5	TCRU	—	—	—	—	—	—	TPSC[1:0]	
MTU5	TIORU	—	—	—			IOC[4:0]		
MTU5	TCNTV								
MTU5	TGRV								
MTU5	TCRV	—	—	—	—	—	—	TPSC[1:0]	
MTU5	TIORV	—	—	—			IOC[4:0]		
MTU5	TCNTW								
MTU5	TGRW								
MTU5	TCRW	—	—	—	—	—	—	TPSC[1:0]	
MTU5	TIORW	—	—	—			IOC[4:0]		
MTU5	TSR	—	—	—	—	—	CMFU5	CMFV5	CMFW5
MTU5	TIER	—	—	—	—	—	TGIE5U	TGIE5V	TGIE5W
MTU5	TSTR	—	—	—	—	—	CSTU5	CSTV5	CSTW5
MTU5	TCNTCMPCLR	—	—	—	—	—	CMPCLR5U	CMPCLR5V	CMPCLR5W
GPT	GTSTR	—	—	—	—	—	—	—	—
		—	—	—	—	CST3	CST2	CST1	CST0
GPT	GTHSCR	CPHW3[1:0]		CPHW2[1:0]		CPHW1[1:0]		CPHW0[1:0]	
		CSHW3[1:0]		CSHW2[1:0]		CSHW1[1:0]		CSHW0[1:0]	
GPT	GTHCCR	—	—	—	—	CCSW3	CCSW2	CCSW1	CCSW0
		CCHW3[1:0]		CCHW2[1:0]		CCHW1[1:0]		CCHW0[1:0]	
GPT	GTHSSR	CSHSL3[3:0]					CSHSL2[3:0]		
		CSHSL1[3:0]					CSHSL0[3:0]		
GPT	GTHPSR	CSHPL3[3:0]					CSHPL2[3:0]		
		CSHPL1[3:0]					CSHPL0[3:0]		
GPT	GTWP	—	—	—	—	—	—	—	—
		—	—	—	—	WP3	WP2	WP1	WP0
GPT	GTSYNC	—	—	SYNC3[1:0]		—	—	SYNC2[1:0]	
		—	—	SYNC1[1:0]		—	—	SYNC0[1:0]	
GPT	GTETINT	—	—	—	—	—	—	ETINF	ETIPF
		—	—	—	—	—	—	ETINEN	ETIPEN

Table 4.2 List of I/O Registers (Bit Order) (30 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
FLASH	FSTATR0	FRDY	ILGLERR	ERSERR	PRGERR	SUSRDY	—	ERSSPD	PRGSPD
FLASH	FSTATR1	FCUERR	—	—	FLOCKST	—	—	—	—
FLASH	FENTRYR	FEKEY[7:0]							
		FENTRYD	—	—	—	—	—	—	FENTRY0
FLASH	FPROTR	FPKEY[7:0]							
		—	—	—	—	—	—	—	FPROTCN
FLASH	FRESETR	FRKEY[7:0]							
		—	—	—	—	—	—	—	FRESET
FLASH	FCMDR	CMDR[7:0]							
		PCMDR[7:0]							
FLASH	FCPSR	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	ESUSPMD
FLASH	DFLBCCNT	—	—	—	—	—		BCADR[7:0]	
		BCADR[7:0]						—	BCSIZE
FLASH	FPESTAT	—	—	—	—	—	—	—	—
		PEERRST[7:0]							
FLASH	DFLBCSTAT	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	BCST
FLASH	PCKAR	—	—	—	—	—	—	—	—
		PCKA[7:0]							

Note: • In this, the I/O port related registers (0008 C001h to 0008 C116h) indicate the bit configuration of the 112-pin LQFP version. As the configuration of registers and bits differs depending on a package, see section 14, I/O Ports, for details in the User's manual: Hardware.

Note 1. This shows the bit configuration when ADDPR.DPSEL = 0 and ADDPR.DPPRC = 0 (The value has 10-bit accuracy and is padded at the LSB end).

Note 2. This shows the bit configuration when ADCER.ADRFMT = 0 (aligned to the LSB end) and ADCER.ADPRC[1:0] = 00b. For details, refer to section 28, 12-Bit A/D Converter (S12ADA) in the User's manual: Hardware.

Note 3. This function is not supported by the product without the CAN function.

Table 5.3 DC Characteristics (2)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Supply current*1	In operation	Max.*2	I_{CC}*3	-	-	70	mA	ICLK = 100 MHz PCLK = 50 MHz
		Normal*4		-	35	-		
		Increased by BGO operation*5		-	15	-		
	Sleep				22	60		
	All-module-clock-stop mode*6				14	28		
	Standby mode	Software standby mode		-	0.10	3	mA	
		Deep software standby mode		-	20	60	µA	
Analog power supply current	During 12-bit A/D conversion (when a sample-and-hold circuit is in use; per unit)		AI_{CC0}	-	3	5	mA	
	During 12-bit A/D conversion (when a sample-and-hold circuit is not in use; per unit)			-	3	5	mA	
	Programmable gain amp (per channel)			-	1	2	mA	
	Window comparator (1 channel)				0.5	1	mA	
	Window comparator (6 channels)			-	1	2	mA	
	During 12-bit A/D conversion (per unit)			-	60	90	µA	
	During 10-bit A/D conversion (per unit)		AI_{CC}	-	0.9	2	mA	
	Waiting for 10-bit A/D conversion (all units)			-	0.3	3	µA	
Reference power supply current	During 12-bit A/D conversion (per unit)		AI_{REFH0}	-	1.6	3	mA	
	Waiting for 12-bit A/D conversion (all units)			-	1.6	3	mA	
	During 10-bit A/D conversion (per unit)		AI_{REF}	-	0.1	1	mA	
	Waiting for 10-bit A/D conversion (all units)			-	0.1	3	µA	
VCC rising gradient			SV_{CC}	-	-	20	ms/V	

Note 1. Supply current values are with all output pins unloaded.
Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK: PCLK = 8:4)
ICC max. = 0.54 x f + 16 (max.)
ICC max. = 0.3 x f + 5 (normal operation)
ICC max. = 0.44 x f + 16 (sleep mode)
Note 4. Measured with clocks not supplied to the peripheral functions. This does not include the BGO operation.
Note 5. Incremented if data is written to or erased from the ROM or data flash for data storage during the program execution.
Note 6. The values are for reference.

5.3.3 Timing of On-Chip Peripheral Modules

Table 5.9 Timing of On-Chip Peripheral Modules (1)

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item			Symbol	Min.	Typ.	Max.	Unit
SCI	Input clock cycle	Asynchronous	t_{Scyc}	$4 \times t_{Pcyc}$	-	ns	Figure 5.8
		Clock synchronous		$6 \times t_{Pcyc}$	-		
	Input clock pulse width		t_{SCKW}	$0.4 \times t_{Pcyc}$	$0.6 \times t_{Scyc}$	ns	
	Input clock rise time		t_{SCKr}	-	20	ns	
	Input clock fall time		t_{SCKf}	-	20	ns	
	Output clock cycle	Asynchronous	t_{Scyc}	$16 \times t_{Pcyc}$	-	ns	
		Clock synchronous		$6 \times t_{Pcyc}$	-	ns	
	Output clock pulse width		t_{SCKW}	$0.4 \times t_{Scyc}$	$0.6 \times t_{Scyc}$	ns	
	Output clock rise time		t_{SCKr}	-	20	ns	
	Output clock fall time		t_{SCKf}	-	20	ns	
	Transmit data delay time (clock synchronous)		t_{TXD}	-	40	ns	Figure 5.9
	Receive data setup time (clock synchronous)		t_{RXS}	40	-	ns	
	Receive data hold time (clock synchronous)		t_{RXH}	40	-	ns	

Note: • t_{Pcyc}: PCLK cycle

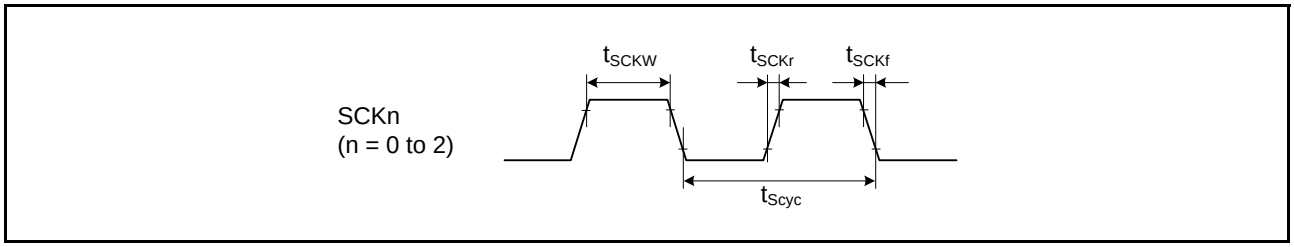

Figure 5.8 SCK Clock Input Timing

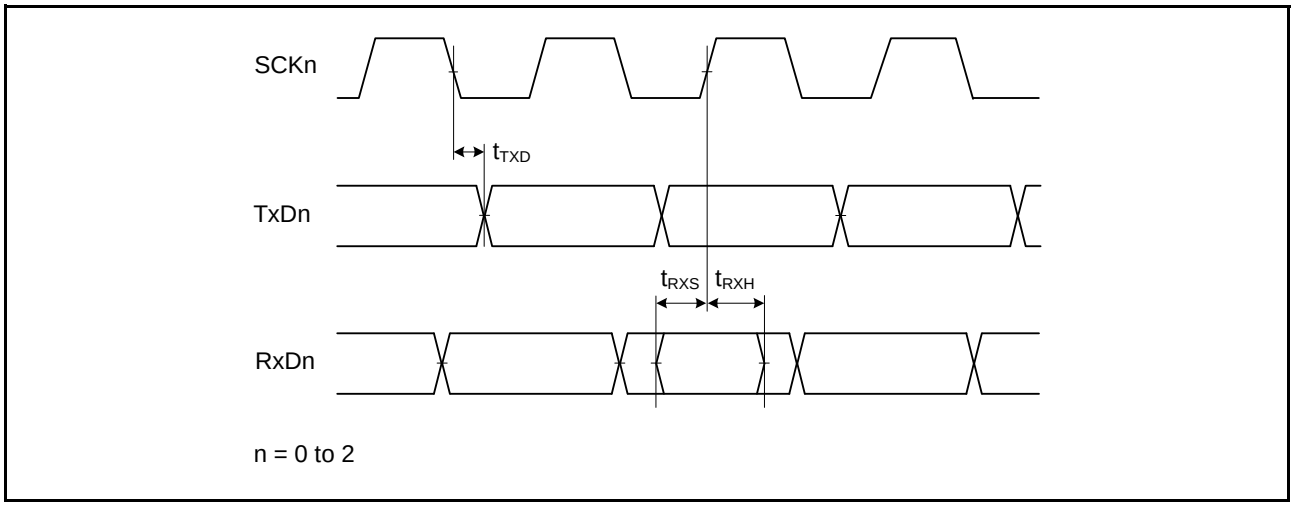

Figure 5.9 SCI Input/Output Timing: Clock Synchronous Mode

Table 5.11 Timing of On-Chip Peripheral Modules (3)

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item			Symbol	Min.	Max.	Unit	Test Conditions
RSPI	RSPCK clock cycle	Master	t_{SPcyc}	4	4096	t_{Pcyc}	Figure 5.11
		Slave		8	4096		
	RSPCK clock high pulse width	Master	t_{SPCKWH}	(t_{Spcyc} - t_{SPCKR} - t_{SPCKF}) / 2-3	-	ns	
		Slave		(t_{Spcyc} - t_{SPCKR} - t_{SPCKF}) / 2	-		
	RSPCK clock low pulse width	Master	t_{SPCKWL}	(t_{Spcyc} - t_{SPCKR} - t_{SPCKF}) / 2-3	-	ns	
		Slave		(t_{Spcyc} - t_{SPCKR} - t_{SPCKF}) / 2	-		
	RSPCK clock rise/fall time	Output	t_{SPCKR} t_{SPCKF}	-	5	ns	
		Input		-	1	µs	
	Data input setup time	Master	t_{SU}	25	-	ns	Figure 5.12 to Figure 5.15
		Slave		0	-		
	Data input hold time	Master	t_H	0	-	ns	
		Slave		20+2×t_{Pcyc}	-		
	SSL setup time	Master	t_{LEAD}	1	8	t_{SPcyc}	
		Slave		4	-	t_{Pcyc}	
	SSL hold time	Master	t_{LAG}	1	8	t_{SPcyc}	
		Slave		4	-	t_{Pcyc}	
	Data output delay time	Master	t_{OD}	-	20	ns	
		Slave		-	3×t_{Pcyc} +40		
	Data output hold time	Master	t_{OH}	0	-	ns	
		Slave		0	-		
	Successive transmission delay time	Master	t_{TD}	t_{SPcyc}+2×t_{Pcyc}	8×t_{SPcyc} +2×t_{Pcyc}	ns	
		Slave		4×t_{Pcyc}	-		
	MOSI, MISO rise/fall time	Output	t_{DR} t_{DF}	-	15	ns	Figure 5.12 to Figure 5.15
		Input		-	1	µs	
	SSL rise/fall time	Output	t_{SSLR} t_{SSLF}	-	15	ns	
		Input		-	1	µs	
	Slave access time		t_{SA}	-	4	t_{Pcyc}	Figure 5.12 to Figure 5.15
	Slave output release time		t_{REL}	-	3	t_{Pcyc}	

Note: • Note 1: t_{Pcyc}: PCLK cycle

Table 5.12 Timing of On-Chip Peripheral Modules (4)

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Max.	Unit	Test Conditions
MTU3	Input capture input pulse width (single-edge setting)	t_{TICW}	3.0	-	t_{Icyc}	Figure 5.16
	Input capture input pulse width (both-edge setting)	t_{TICW}	5.0	-	t_{Icyc}	
	Timer clock pulse width (single-edge setting)	$t_{TCKWH/L}$	3.0	-	t_{Icyc}	Figure 5.17
	Timer clock pulse width (both-edge setting)	$t_{TCKWH/L}$	5.0	-	t_{Icyc}	
	Timer clock pulse width (phase coefficient mode)	$t_{TCKWH/L}$	5.0	-	t_{Icyc}	
GPT	Input capture input pulse width (single-edge setting)	t_{GTICW}	3.0	-	t_{Icyc}	Figure 5.18
	Input capture input pulse width (both-edge setting)	t_{GTICW}	5.0	-	t_{Icyc}	

Note: • t_{Icyc}: ICLK cycle

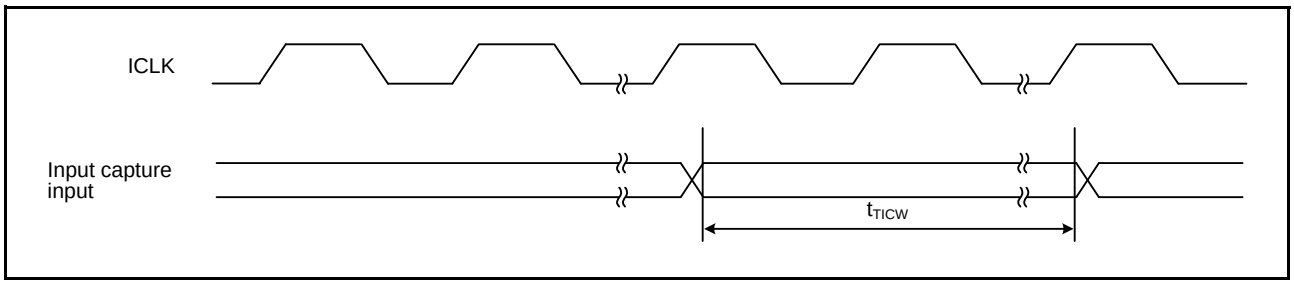

Figure 5.16 MTU3 Input/Output Timing

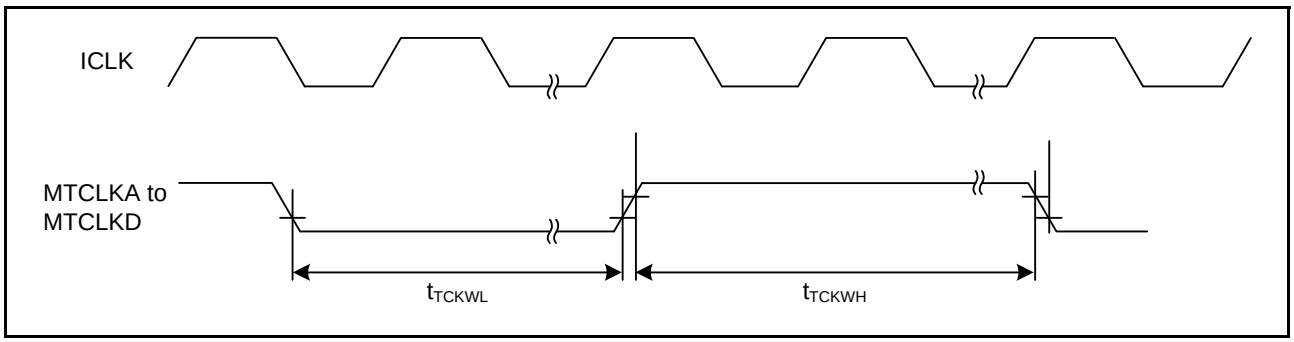

Figure 5.17 MTU3 Clock Input Timing

5.7 ROM (Flash Memory for Code Storage) Characteristics

Table 5.21 ROM (Flash Memory for Code Storage) Characteristics (1)

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Temperature range for the programming/erasure operation:
Ta = Topr. Ta is the same under conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Rewrite/erase cycle*1	N_{PEC}	1000	—	—	Times	
Data hold time	t_{DRP}	30*2	—	—	Year	Ta = +85C°

Note 1. Definition of rewrite/erase cycle:
The rewrite/erase cycle is the number of erasing for each block. When the rewrite/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 256-byte writing is performed 16 times for different addresses in 4-Kbyte block and then the entire block is erased, the rewrite/erase cycle is counted as one. However, writing to the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. The value is obtained from the reliability test.

Table 5.22 ROM (Flash Memory for Code Storage) Characteristics (2)

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Temperature range for the programming/erasure operation:
Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Programming time	256 bytes	t_{P256}	—	2	12	ms	PCLK = 50 MHz $N_{PEC} \leq 100$
	4 Kbytes	t_{P4K}	—	23	50	ms	
	16 Kbytes	t_{P16K}	—	90	200	ms	
	256 byte	t_{P256}	—	2.4	14.4	ms	PCLK = 50 MHz $N_{PEC} > 100$
	4 Kbytes	t_{P4K}	—	27.6	60	ms	
	16 Kbytes	t_{P16K}	—	108	240	ms	
Erasure time	4 Kbytes	t_{E4K}	—	25	60	ms	PCLK = 50 MHz $N_{PEC} \leq 100$
	16 Kbytes	t_{E16K}	—	100	240	ms	
	4 Kbytes	t_{E4K}	—	30	72	ms	PCLK = 50 MHz $N_{PEC} > 100$
	16 Kbytes	t_{E16K}	—	120	288	ms	
Suspend delay time during writing		t_{SPD}	—	—	120	µs	Figure 5.24 PCLK = 50 MHz
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	120	µs	
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	1.7	ms	
Suspend delay time during erasing (in erasure priority mode)		t_{SEED}	—	—	1.7	ms	

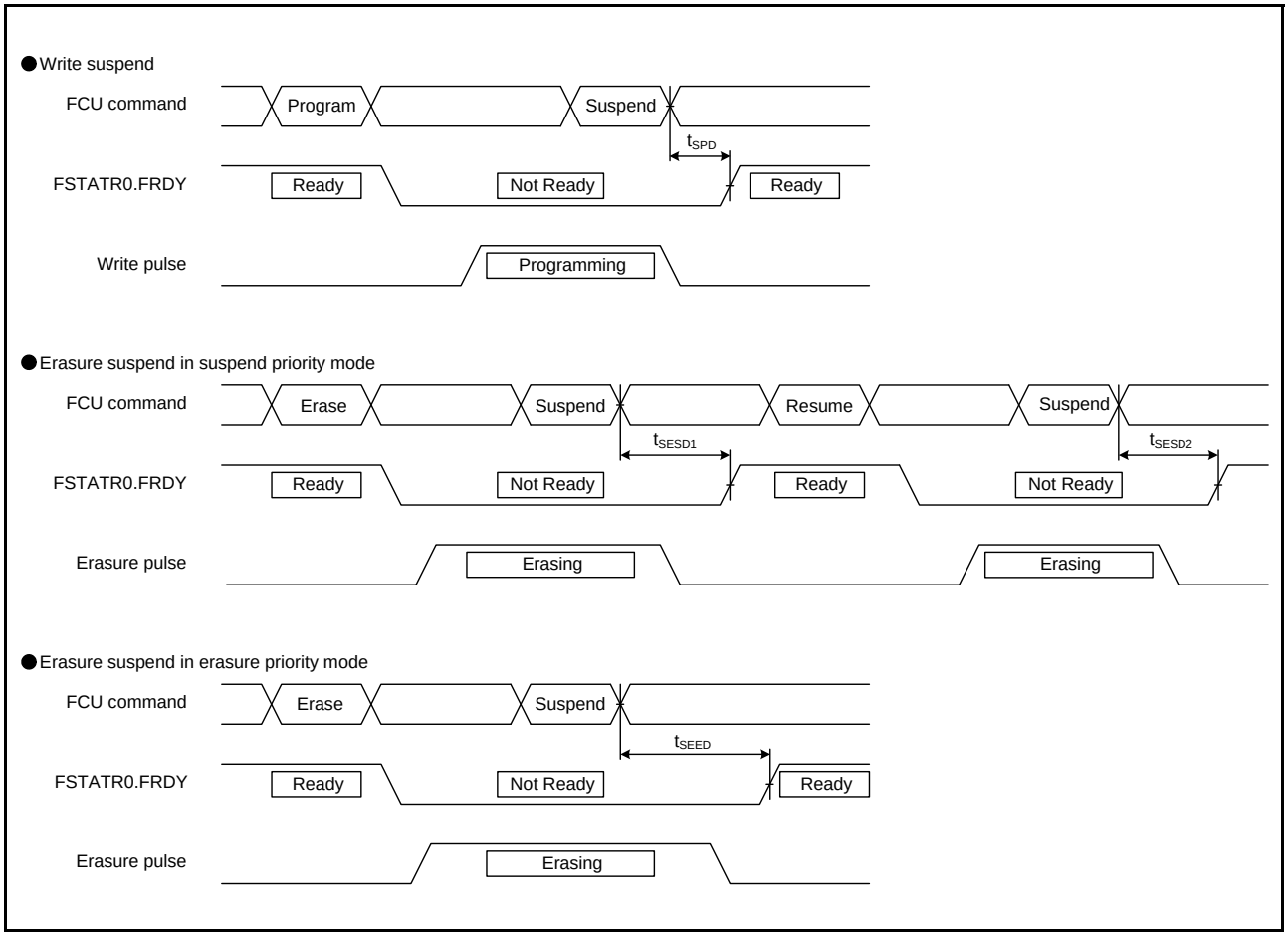

Figure 5.24 Flash Memory Write/Erase Suspend Timing

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.