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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I ² C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	61
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 12x10b, 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562g7ddfh-v1

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and Table 1.2 lists the functions of products.

Table 1.1 Outline of Specifications (1 / 5)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 100MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4-Gbyte linear • Register set of the CPU • General purpose: Sixteen 32-bit registers • Control: Nine 32-bit registers • Accumulator: One 64-bit register • Basic instructions: 73 • Floating-point instructions: 8 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement • Instructions: Little endian • Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 x 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Memory-protection unit (MPU)
	FPU	• Single precision (32-bit) floating point • Data types and floating-point exceptions in conformance with the IEEE754 standard
Memory	ROM	• ROM capacity: 256 Kbytes (max.) • Two on-board programming modes • Boot mode (The user MAT is programmable via the SCI) • User program mode • Off-board programming • A PROM programmer can be used to program the user mat.
	RAM	• RAM capacity: 16 Kbytes (max.)
	Data flash	• Data flash capacity: 32 Kbytes (max.) • Supports background operations (BGO)
MCU operating mode		• Single-chip mode
Clock	Clock generation circuit	• One circuit: Main clock oscillator • Internal oscillator: Low-speed on-chip oscillator dedicated to IWDG • Structure of a PLL frequency synthesizer and frequency divider for selectable operating frequency • Oscillation stoppage detection • Independent frequency-division and multiplication settings for the system clock (ICLK) and peripheral module clock (PCLK) • The CPU and system sections such as other bus masters, MTU3, and GPT run in synchronization with the system clock (ICLK): 8 to 100 MHz. • Peripheral modules run in synchronization with the peripheral module clock (PCLK): 8 to 50 MHz
Reset		Pin reset, power-on reset (automatic power-on reset when the power is turned on), voltage-monitoring reset, watchdog timer reset, independent watchdog timer reset, and deep software standby reset
Voltage detection circuit (LVD)		When the voltage on VCC falls below the voltage detection level (Vdet), an internal reset or internal interrupt is generated.
Low power consumption	Low power consumption facilities	• Module stop function • Four low power consumption modes • Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no.

Table 1.3 List of Products (1 / 2)

Group	Part No.	Order Part No.	Package	ROM Capacity	RAM Capacity	Data Flash Capacity	Power Supply Voltage	CAN	Operating Temp. Range		
RX62T	R5F562TAADFH	R5F562TAADFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes	VCC/PLLVC 4.0 to 5.5 V AVCC/AVCC0 4.0 to 5.5 V	Support- ed	-40 to +85°C (D version)		
	R5F562TAADFP	R5F562TAADFP#V3	PLQP0100KB-A								
	R5F562TAADFF	R5F562TAADFF#V3	PLQP0080JA-A								
	R5F562TAGDFF	R5F562TAGDFF#V3	PLQP0080JA-A								
	R5F562TAADFM	R5F562TAADFM#V3	PLQP0064KB-A								
	R5F562TAADFK	R5F562TAADFK#V3	PLQP0064GA-A								
	R5F562T7ADFH	R5F562T7ADFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes					
	R5F562T7ADFP	R5F562T7ADFP#V3	PLQP0100KB-A								
	R5F562T7ADFF	R5F562T7ADFF#V3	PLQP0080JA-A								
	R5F562T7GDFF	R5F562T7GDFF#V3	PLQP0080JA-A								
	R5F562T7ADFM	R5F562T7ADFM#V3	PLQP0064KB-A								
	R5F562T7ADFK	R5F562T7ADFK#V3	PLQP0064GA-A								
	R5F562T6ADFF	R5F562T6ADFF#V3	PLQP0080JA-A	64 Kbytes	8 Kbytes						
	R5F562T6ADFM	R5F562T6ADFM#V3	PLQP0064KB-A								
	R5F562T6ADFK	R5F562T6ADFK#V3	PLQP0064GA-A								
	R5F562TABDFH	R5F562TABDFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes	VCC/PLLVC 2.7 to 3.6 V AVCC/AVCC0 3.0 to 3.6 V or 4.0 to 5.5 V				
	R5F562TABDFP	R5F562TABDFP#V3	PLQP0100KB-A								
	R5F562TABDFF	R5F562TABDFF#V3	PLQP0080JA-A								
	R5F562TABDFM	R5F562TABDFM#V3	PLQP0064KB-A								
	R5F562TABDFK	R5F562TABDFK#V3	PLQP0064GA-A								
	R5F562T7BDFH	R5F562T7BDFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes					
	R5F562T7BDFP	R5F562T7BDFP#V3	PLQP0100KB-A								
	R5F562T7BDFF	R5F562T7BDFF#V3	PLQP0080JA-A								
	R5F562T7BDFM	R5F562T7BDFM#V3	PLQP0064KB-A								
	R5F562T7BDFK	R5F562T7BDFK#V3	PLQP0064GA-A								
	R5F562T6BDFF	R5F562T6BDFF#V3	PLQP0080JA-A	64 Kbytes	8 Kbytes						
	R5F562T6BDFM	R5F562T6BDFM#V3	PLQP0064KB-A								
	R5F562T6BDFK	R5F562T6BDFK#V3	PLQP0064GA-A								
	R5F562TADDFH	R5F562TADDFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes	4.0 to 5.5 V	Not Support- ed			
	R5F562TADDFP	R5F562TADDFP#V3	PLQP0100KB-A								
	R5F562TADDDFF	R5F562TADDDFF#V3	PLQP0080JA-A								
	R5F562TADDDFM	R5F562TADDDFM#V3	PLQP0064KB-A								
	R5F562TADDDFK	R5F562TADDDFK#V3	PLQP0064GA-A								
	R5F562T7DDFH	R5F562T7DDFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes					
	R5F562T7DDFP	R5F562T7DDFP#V3	PLQP0100KB-A								
	R5F562T7DDFF	R5F562T7DDFF#V3	PLQP0080JA-A								
	R5F562T7DDFM	R5F562T7DDFM#V3	PLQP0064KB-A								
	R5F562T7DDFK	R5F562T7DDFK#V3	PLQP0064GA-A								
	R5F562T6DDFF	R5F562T6DDFF#V3	PLQP0080JA-A	64 Kbytes	8 Kbytes						
	R5F562T6DDFM	R5F562T6DDFM#V3	PLQP0064KB-A								
	R5F562T6DDFK	R5F562T6DDFK#V3	PLQP0064GA-A								
	R5F562TAEDFH	R5F562TAEDFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes	2.7 to 3.6 V				
	R5F562TAEDFP	R5F562TAEDFP#V3	PLQP0100KB-A								
	R5F562TAEDFF	R5F562TAEDFF#V3	PLQP0080JA-A								
	R5F562TAEDFM	R5F562TAEDFM#V3	PLQP0064KB-A								
R5F562TAEDFK	R5F562TAEDFK#V3	PLQP0064GA-A									

Table 1.3 List of Products (2 / 2)

Group	Part No.	Order Part No.	Package	ROM Capacity	RAM Capacity	Data Flash Capacity	Power Supply Voltage	CAN	Operating Temp. Range
RX62T	R5F562T7EDFH	R5F562T7EDFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes	2.7 to 3.6 V	Not Supported	-40 to +85°C (D version)
	R5F562T7EDFP	R5F562T7EDFP#V3	PLQP0100KB-A						
	R5F562T7EDFF	R5F562T7EDFF#V3	PLQP0080JA-A						
	R5F562T7EDFM	R5F562T7EDFM#V3	PLQP0064KB-A						
	R5F562T7EDFK	R5F562T7EDFK#V3	PLQP0064GA-A						
	R5F562T6EDFF	R5F562T6EDFF#V3	PLQP0080JA-A	64 Kbytes	8 Kbytes				
	R5F562T6EDFM	R5F562T6EDFM#V3	PLQP0064KB-A						
	R5F562T6EDFK	R5F562T6EDFK#V3	PLQP0064GA-A						
	R5F562TAAGFH	R5F562TAAGFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes	VCC/PLL VCC 4.0 to 5.5 V AVCC/AVCC0 4.0 to 5.5 V	Support- ed	-40 to +105°C (G version) *1
	R5F562TAAGFP	R5F562TAAGFP#V3	PLQP0100KB-A						
	R5F562TAAGFF	R5F562TAAGFF#V3	PLQP0080JA-A						
	R5F562TAGGFF	R5F562TAGGFF#V3	PLQP0080JA-A						
	R5F562TAAGFM	R5F562TAAGFM#V3	PLQP0064KB-A						
	R5F562TAAGFK	R5F562TAAGFK#V3	PLQP0064GA-A						
	R5F562T7AGFH	R5F562T7AGFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes			
	R5F562T7AGFP	R5F562T7AGFP#V3	PLQP0100KB-A						
	R5F562T7AGFF	R5F562T7AGFF#V3	PLQP0080JA-A						
	R5F562T7GGFF	R5F562T7GGFF#V3	PLQP0080JA-A						
	R5F562T7AGFM	R5F562T7AGFM#V3	PLQP0064KB-A						
	R5F562T7AGFK	R5F562T7AGFK#V3	PLQP0064GA-A	64 Kbytes	8 Kbytes				
	R5F562T6AGFF	R5F562T6AGFF#V3	PLQP0080JA-A						
	R5F562T6AGFM	R5F562T6AGFM#V3	PLQP0064KB-A						
	R5F562T6AGFK	R5F562T6AGFK#V3	PLQP0064GA-A	256 Kbytes	16 Kbytes	32 Kbytes	VCC/PLL VCC 2.7 to 3.6 V AVCC/AVCC0 3.0 to 3.6 V or 4.0 to 5.5 V		
	R5F562TABGFH	R5F562TABGFH#V3	PLQP0112JA-A						
	R5F562TABGFP	R5F562TABGFP#V3	PLQP0100KB-A						
	R5F562TABGFF	R5F562TABGFF#V3	PLQP0080JA-A						
	R5F562TABGFM	R5F562TABGFM#V3	PLQP0064KB-A						
	R5F562TABGFK	R5F562TABGFK#V3	PLQP0064GA-A	128 Kbytes	8 Kbytes	8 Kbytes			
	R5F562T7BGFH	R5F562T7BGFH#V3	PLQP0112JA-A						
	R5F562T7BGFP	R5F562T7BGFP#V3	PLQP0100KB-A						
	R5F562T7BGFF	R5F562T7BGFF#V3	PLQP0080JA-A						
	R5F562T7BGFM	R5F562T7BGFM#V3	PLQP0064KB-A						
	R5F562T7BGFK	R5F562T7BGFK#V3	PLQP0064GA-A	64 Kbytes	8 Kbytes				
	R5F562T6BGFF	R5F562T6BGFF#V3	PLQP0080JA-A						
	R5F562T6BGFM	R5F562T6BGFM#V3	PLQP0064KB-A						
	R5F562T6BGFK	R5F562T6BGFK#V3	PLQP0064GA-A						
RX62G	R5F562GAADFH	R5F562GAADFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes	VCC/PLL VCC 4.0 to 5.5 V AVCC/AVCC0 4.0 to 5.5 V	Support- ed	-40 to +85°C (D version)
	R5F562GAADFP	R5F562GAADFP#V3	PLQP0100KB-A						
	R5F562G7ADFH	R5F562G7ADFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes			
	R5F562G7ADFP	R5F562G7ADFP#V3	PLQP0100KB-A						
	R5F562GADDFH	R5F562GADDFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes		Not Supported	
	R5F562GADDFP	R5F562GADDFP#V3	PLQP0100KB-A						
	R5F562G7DDFH	R5F562G7DDFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes			
	R5F562G7DDFP	R5F562G7DDFP#V3	PLQP0100KB-A						
	R5F562GAAGFH	R5F562GAAGFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes	VCC/PLL VCC 4.0 to 5.5 V AVCC/AVCC0 4.0 to 5.5 V	Support- ed	-40 to +105°C (G versio) *1
	R5F562GAAGFP	R5F562GAAGFP#V3	PLQP0100KB-A						
	R5F562G7AGFH	R5F562G7AGFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes			
	R5F562G7AGFP	R5F562G7AGFP#V3	PLQP0100KB-A						

Note 1. Please contact us if you are using a G version.

Table 1.4 List of Pins and Pin Functions (112-Pin LQFP) (1 / 3)

Pin No. (112-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi- cation	Interrupt	POE	Debugging
1		PE5				IRQ0-B		
2	EMLE							
3	VSS							
4	MDE							
5	VCL							
6	MD1							
7	MD0							
8		PE4		MTCLKC-C		IRQ1-B	POE10#-B	
9		PE3		MTCLKD-C		IRQ2-A	POE11#	
10	RES#							
11	XTAL							
12	VSS							
13	EXTAL							
14	VCC							
15		PE2				NMI	POE10#-A	
16		PE1			SSL3-C			
17		PE0			CRX-C/ SSL2-C			
18		PD7		GTIOC0A-B	CTX-C/ SSL1-C			
19		PD6		GTIOC0B-B	SSL0-C			
20		PD5		GTIOC1A-B	RXD1			
21		PD4		GTIOC1B-B	SCK1			
22		PD3		GTIOC2A-B	TXD1			
23		PD2		GTIOC2B-B	MOSI-C			
24		PD1		GTIOC3A	MISO-C			
25		PD0		GTIOC3B	RSPCK-C			
26								TDI
27								TCK
28								TDO
29		PB7			SCK2-A			
30		PB6			CRX-A/ RXD2-A			
31		PB5			CTX-A/ TXD2-A			
32	PLL VCC							
33		PB4		GTETR G		IRQ3	POE8#	
34	PLL VSS							
35		PB3		MTIOC0A-A	SCK0			
36		PB2		MTIOC0B-A	TXD0/SDA			
37		PB1		MTIOC0C	RXD0/SCL			
38		PB0		MTIOC0D	MOSI-B			
39		PA5	ADTRG1#-A	MTIOC1A	MISO-B			
40		PA4	ADTRG0#-A	MTIOC1B	RSPCK-B			
41		PA3		MTIOC2A	SSL0-B			
42		PA2		MTIOC2B	SSL1-B			
43		PA1		MTIOC6A	SSL2-B			

Table 1.5 List of Pins and Pin Functions (100-Pin LQFP) (1 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi- cation	Interrupt	POE	Debugging
1		PE5				IRQ0-B		
2	EMLE							
3	VSS							
4	MDE							
5	VCL							
6	MD1							
7	MD0							
8		PE4		MTCLKC-C		IRQ1-B	POE10#-B	
9		PE3		MTCLKD-C		IRQ2-A	POE11#	
10	RES#							
11	XTAL							
12	VSS							
13	EXTAL							
14	VCC							
15		PE2				NMI	POE10#-A	
16		PE1			SSL3-C			
17		PE0			CRX-C/ SSL2-C			
18		PD7		GTIOC0A-B	CTX-C/SSL1-C			TRST#
19		PD6		GTIOC0B-B	SSL0-C			TMS
20		PD5		GTIOC1A-B	RXD1			TDI
21		PD4		GTIOC1B-B	SCK1			TCK
22		PD3		GTIOC2A-B	TXD1			TDO
23		PD2		GTIOC2B-B	MOSI-C			TRCLK
24		PD1		GTIOC3A	MISO-C			TRDATA3
25		PD0		GTIOC3B	RSPCK-C			TRDATA2
26		PB7			SCK2-A			TRDATA1
27		PB6			CRX-A/ RXD2-A			TRDATA0
28		PB5			CTX-A/TXD2-A			TRSYNC
29	PLLVC							
30		PB4		GTETR		IRQ3	POE8#	
31	PLLVS							
32		PB3		MTIOC0A-A	SCK0			
33		PB2		MTIOC0B-A	TXD0/SDA			
34		PB1		MTIOC0C	RXD0/SCL			
35		PB0		MTIOC0D	MOSI-B			
36		PA5	ADTRG1#-A	MTIOC1A	MISO-B			
37		PA4	ADTRG0#-A	MTIOC1B	RSPCK-B			
38		PA3		MTIOC2A	SSL0-B			
39		PA2		MTIOC2B	SSL1-B			
40		PA1		MTIOC6A	SSL2-B			

Table 1.6 List of Pins and Pin Functions (80-Pin LQFP) (3 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi- cation	Interrupt	POE	Debugging
76	AVSS0							
77		P11		MTCLKC-B		IRQ1-A		
78		P10		MTCLKD-B		IRQ0-A		
79		PA5	ADTRG1#-A	MTIOC1A	MISO-B			
80		PA4	ADTRG0#-A	MTIOC1B	RSPCK-B			

Table 1.8 List of Pins and Pin Functions (64-Pin LQFP) (2 / 2)

Pin No. (64-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi- cation	Interrupt	POE	Debuggi ng
40		P33		MTIOC3A/ MTCLKA-A	SSL3-A			
41		P32		MTIOC3C/ MTCLKB-A	SSL2-A			
42	VCC							
43		P31		MTIOC0A-B/ MTCLKC-A	SSL1-A			
44	VSS							
45		P30		MTIOC0B-B/ MTCLKD-A	SSL0-A			
46		P24			RSPCK-A			
47		P23			CTX-B/ LTX/ MOSI-A			
48		P22			CRX-B/ LRX/ MISO-A			
49		P47	AN103/ CVREFH					
50		P46	AN102					
51		P45	AN101					
52		P44	AN100					
53		P43	AN003/ CVREFL					
54		P42	AN002					
55		P41	AN001					
56		P40	AN000					
57	AVCC0							
58	VREFH0							
59	VREFL0							
60	AVSS0							
61		P11		MTCLKC-B		IRQ1-A		
62		P10		MTCLKD-B		IRQ0-A		
63		PA5	ADTRG1#-A	MTIOC1A	MISO-B			
64		PA4	ADTRG0#-A	MTIOC1B	RSPCK-B			

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 0000h	SYSTEM	Mode monitor register	MDMONR	16	16	3 ICLK
0008 0002h	SYSTEM	Mode status register	MDSR	16	16	3 ICLK
0008 0006h	SYSTEM	System control register 0	SYSCR0	16	16	3 ICLK
0008 0008h	SYSTEM	System control register 1	SYSCR1	16	16	3 ICLK
0008 000Ch	SYSTEM	Standby control register	SBYCR	16	16	3 ICLK
0008 0010h	SYSTEM	Module stop control register A	MSTPCRA	32	32	3 ICLK
0008 0014h	SYSTEM	Module stop control register B	MSTPCRB	32	32	3 ICLK
0008 0018h	SYSTEM	Module stop control register C	MSTPCRC	32	32	3 ICLK
0008 0020h	SYSTEM	System clock control register	SCKCR	32	32	3 ICLK
0008 0040h	SYSTEM	Oscillation stop detection control register	OSTDCR	16	16	3 ICLK
0008 1300h	BSC	Bus error status clear register	BERCLR	8	8	2 ICLK
0008 1304h	BSC	Bus error monitoring enable register	BEREN	8	8	2 ICLK
0008 1308h	BSC	Bus error status register 1	BERSR1	8	8	2 ICLK
0008 130Ah	BSC	Bus error status register 2	BERSR2	16	16	2 ICLK
0008 2400h	DTC	DTC control register	DTCCR	8	8	2 ICLK
0008 2404h	DTC	DTC vector base register	DTCVBR	32	32	2 ICLK
0008 2408h	DTC	DTC address mode register	DTCADMOD	8	8	2 ICLK
0008 240Ch	DTC	DTC module start register	DTCST	8	8	2 ICLK
0008 240Eh	DTC	DTC status register	DTCSTS	16	16	2 ICLK
0008 6400h	MPU	Region 0 start page-number register	RSPAGE0	32	32	1 ICLK
0008 6404h	MPU	Region 0 end page-number register	REPAGE0	32	32	1 ICLK
0008 6408h	MPU	Region 1 start page-number register	RSPAGE1	32	32	1 ICLK
0008 640Ch	MPU	Region 1 end page-number register	REPAGE1	32	32	1 ICLK
0008 6410h	MPU	Region 2 start page-number register	RSPAGE2	32	32	1 ICLK
0008 6414h	MPU	Region 2 end page-number register	REPAGE2	32	32	1 ICLK
0008 6418h	MPU	Region 3 start page-number register	RSPAGE3	32	32	1 ICLK
0008 641Ch	MPU	Region 3 end page-number register	REPAGE3	32	32	1 ICLK
0008 6420h	MPU	Region 4 start page-number register	RSPAGE4	32	32	1 ICLK
0008 6424h	MPU	Region 4 end page-number register	REPAGE4	32	32	1 ICLK
0008 6428h	MPU	Region 5 start page-number register	RSPAGE5	32	32	1 ICLK
0008 642Ch	MPU	Region 5 end page-number register	REPAGE5	32	32	1 ICLK
0008 6430h	MPU	Region 6 start page-number register	RSPAGE6	32	32	1 ICLK
0008 6434h	MPU	Region 6 end page-number register	REPAGE6	32	32	1 ICLK
0008 6438h	MPU	Region 7 start page-number register	RSPAGE7	32	32	1 ICLK
0008 643Ch	MPU	Region 7 end page-number register	REPAGE7	32	32	1 ICLK
0008 6500h	MPU	Memory-protection enable register	MPEN	32	32	1 ICLK
0008 6504h	MPU	Background access control register	MPBAC	32	32	1 ICLK
0008 6508h	MPU	Memory-protection error status-clearing register	MPECLR	32	32	1 ICLK
0008 650Ch	MPU	Memory-protection error status register	MPESTS	32	32	1 ICLK
0008 6514h	MPU	Data memory-protection error address register	MPDEA	32	32	1 ICLK
0008 6520h	MPU	Region search address register	MPSA	32	32	1 ICLK
0008 6524h	MPU	Region search operation register	MPOPS	16	16	1 ICLK

Table 4.1 List of I/O Registers (Address Order) (3 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 707Dh	ICU	Interrupt request register 125	IR125	8	8	2 ICLK
0008 707Eh	ICU	Interrupt request register 126	IR126	8	8	2 ICLK
0008 707Fh	ICU	Interrupt request register 127	IR127	8	8	2 ICLK
0008 7080h	ICU	Interrupt request register 128	IR128	8	8	2 ICLK
0008 7081h	ICU	Interrupt request register 129	IR129	8	8	2 ICLK
0008 7082h	ICU	Interrupt request register 130	IR130	8	8	2 ICLK
0008 7083h	ICU	Interrupt request register 131	IR131	8	8	2 ICLK
0008 7084h	ICU	Interrupt request register 132	IR132	8	8	2 ICLK
0008 7085h	ICU	Interrupt request register 133	IR133	8	8	2 ICLK
0008 7086h	ICU	Interrupt request register 134	IR134	8	8	2 ICLK
0008 7087h	ICU	Interrupt request register 135	IR135	8	8	2 ICLK
0008 7088h	ICU	Interrupt request register 136	IR136	8	8	2 ICLK
0008 7089h	ICU	Interrupt request register 137	IR137	8	8	2 ICLK
0008 708Ah	ICU	Interrupt request register 138	IR138	8	8	2 ICLK
0008 708Bh	ICU	Interrupt request register 139	IR139	8	8	2 ICLK
0008 708Ch	ICU	Interrupt request register 140	IR140	8	8	2 ICLK
0008 708Dh	ICU	Interrupt request register 141	IR141	8	8	2 ICLK
0008 708Eh	ICU	Interrupt request register 142	IR142	8	8	2 ICLK
0008 708Fh	ICU	Interrupt request register 143	IR143	8	8	2 ICLK
0008 7090h	ICU	Interrupt request register 144	IR144	8	8	2 ICLK
0008 7091h	ICU	Interrupt request register 145	IR145	8	8	2 ICLK
0008 7092h	ICU	Interrupt request register 146	IR146	8	8	2 ICLK
0008 7095h	ICU	Interrupt request register 149	IR149	8	8	2 ICLK
0008 7096h	ICU	Interrupt request register 150	IR150	8	8	2 ICLK
0008 7097h	ICU	Interrupt request register 151	IR151	8	8	2 ICLK
0008 7098h	ICU	Interrupt request register 152	IR152	8	8	2 ICLK
0008 7099h	ICU	Interrupt request register 153	IR153	8	8	2 ICLK
0008 70AAh	ICU	Interrupt request register 170	IR170	8	8	2 ICLK
0008 70ABh	ICU	Interrupt request register 171	IR171	8	8	2 ICLK
0008 70ACh	ICU	Interrupt request register 172	IR172	8	8	2 ICLK
0008 70ADh	ICU	Interrupt request register 173	IR173	8	8	2 ICLK
0008 70AEh	ICU	Interrupt request register 174	IR174	8	8	2 ICLK
0008 70AFh	ICU	Interrupt request register 175	IR175	8	8	2 ICLK
0008 70B0h	ICU	Interrupt request register 176	IR176	8	8	2 ICLK
0008 70B1h	ICU	Interrupt request register 177	IR177	8	8	2 ICLK
0008 70B2h	ICU	Interrupt request register 178	IR178	8	8	2 ICLK
0008 70B3h	ICU	Interrupt request register 179	IR179	8	8	2 ICLK
0008 70B4h	ICU	Interrupt request register 180	IR180	8	8	2 ICLK
0008 70B5h	ICU	Interrupt request register 181	IR181	8	8	2 ICLK
0008 70B6h	ICU	Interrupt request register 182	IR182	8	8	2 ICLK
0008 70B7h	ICU	Interrupt request register 183	IR183	8	8	2 ICLK
0008 70B8h	ICU	Interrupt request register 184	IR184	8	8	2 ICLK
0008 70BAh	ICU	Interrupt request register 186	IR186	8	8	2 ICLK
0008 70BBh	ICU	Interrupt request register 187	IR187	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (5 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 7172h	ICU	DTC activation enable register 114	DTCER114	8	8	2 ICLK
0008 7173h	ICU	DTC activation enable register 115	DTCER115	8	8	2 ICLK
0008 7174h	ICU	DTC activation enable register 116	DTCER116	8	8	2 ICLK
0008 7175h	ICU	DTC activation enable register 117	DTCER117	8	8	2 ICLK
0008 7179h	ICU	DTC activation enable register 121	DTCER121	8	8	2 ICLK
0008 717Ah	ICU	DTC activation enable register 122	DTCER122	8	8	2 ICLK
0008 717Dh	ICU	DTC activation enable register 125	DTCER125	8	8	2 ICLK
0008 717Eh	ICU	DTC activation enable register 126	DTCER126	8	8	2 ICLK
0008 7181h	ICU	DTC activation enable register 129	DTCER129	8	8	2 ICLK
0008 7182h	ICU	DTC activation enable register 130	DTCER130	8	8	2 ICLK
0008 7183h	ICU	DTC activation enable register 131	DTCER131	8	8	2 ICLK
0008 7184h	ICU	DTC activation enable register 132	DTCER132	8	8	2 ICLK
0008 7186h	ICU	DTC activation enable register 134	DTCER134	8	8	2 ICLK
0008 7187h	ICU	DTC activation enable register 135	DTCER135	8	8	2 ICLK
0008 7188h	ICU	DTC activation enable register 136	DTCER136	8	8	2 ICLK
0008 7189h	ICU	DTC activation enable register 137	DTCER137	8	8	2 ICLK
0008 718Ah	ICU	DTC activation enable register 138	DTCER138	8	8	2 ICLK
0008 718Bh	ICU	DTC activation enable register 139	DTCER139	8	8	2 ICLK
0008 718Ch	ICU	DTC activation enable register 140	DTCER140	8	8	2 ICLK
0008 718Dh	ICU	DTC activation enable register 141	DTCER141	8	8	2 ICLK
0008 718Eh	ICU	DTC activation enable register 142	DTCER142	8	8	2 ICLK
0008 718Fh	ICU	DTC activation enable register 143	DTCER143	8	8	2 ICLK
0008 7190h	ICU	DTC activation enable register 144	DTCER144	8	8	2 ICLK
0008 7191h	ICU	DTC activation enable register 145	DTCER145	8	8	2 ICLK
0008 7195h	ICU	DTC activation enable register 149	DTCER149	8	8	2 ICLK
0008 7196h	ICU	DTC activation enable register 150	DTCER150	8	8	2 ICLK
0008 7197h	ICU	DTC activation enable register 151	DTCER151	8	8	2 ICLK
0008 7198h	ICU	DTC activation enable register 152	DTCER152	8	8	2 ICLK
0008 7199h	ICU	DTC activation enable register 153	DTCER153	8	8	2 ICLK
0008 71AEh	ICU	DTC activation enable register 174	DTCER174	8	8	2 ICLK
0008 71AFh	ICU	DTC activation enable register 175	DTCER175	8	8	2 ICLK
0008 71B0h	ICU	DTC activation enable register 176	DTCER176	8	8	2 ICLK
0008 71B1h	ICU	DTC activation enable register 177	DTCER177	8	8	2 ICLK
0008 71B2h	ICU	DTC activation enable register 178	DTCER178	8	8	2 ICLK
0008 71B3h	ICU	DTC activation enable register 179	DTCER179	8	8	2 ICLK
0008 71B4h	ICU	DTC activation enable register 180	DTCER180	8	8	2 ICLK
0008 71B5h	ICU	DTC activation enable register 181	DTCER181	8	8	2 ICLK
0008 71B6h	ICU	DTC activation enable register 182	DTCER182	8	8	2 ICLK
0008 71B7h	ICU	DTC activation enable register 183	DTCER183	8	8	2 ICLK
0008 71B8h	ICU	DTC activation enable register 184	DTCER184	8	8	2 ICLK
0008 71BAh	ICU	DTC activation enable register 186	DTCER186	8	8	2 ICLK
0008 71BBh	ICU	DTC activation enable register 187	DTCER187	8	8	2 ICLK
0008 71BCh	ICU	DTC activation enable register 188	DTCER188	8	8	2 ICLK
0008 71BDh	ICU	DTC activation enable register 189	DTCER189	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (7 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 7305h	ICU	Interrupt source priority register 05	IPR05	8	8	2 ICLK
0008 7306h	ICU	Interrupt source priority register 06	IPR06	8	8	2 ICLK
0008 7307h	ICU	Interrupt source priority register 07	IPR07	8	8	2 ICLK
0008 7314h	ICU	Interrupt source priority register 14	IPR14	8	8	2 ICLK
0008 7318h	ICU	Interrupt source priority register 18	IPR18	8	8	2 ICLK
0008 7320h	ICU	Interrupt source priority register 20	IPR20	8	8	2 ICLK
0008 7321h	ICU	Interrupt source priority register 21	IPR21	8	8	2 ICLK
0008 7322h	ICU	Interrupt source priority register 22	IPR22	8	8	2 ICLK
0008 7323h	ICU	Interrupt source priority register 23	IPR23	8	8	2 ICLK
0008 7324h	ICU	Interrupt source priority register 24	IPR24	8	8	2 ICLK
0008 7325h	ICU	Interrupt source priority register 25	IPR25	8	8	2 ICLK
0008 7326h	ICU	Interrupt source priority register 26	IPR26	8	8	2 ICLK
0008 7327h	ICU	Interrupt source priority register 27	IPR27	8	8	2 ICLK
0008 7340h	ICU	Interrupt source priority register 40	IPR40	8	8	2 ICLK
0008 7344h	ICU	Interrupt source priority register 44	IPR44	8	8	2 ICLK
0008 7348h	ICU	Interrupt source priority register 48	IPR48	8	8	2 ICLK
0008 7349h	ICU	Interrupt source priority register 49	IPR49	8	8	2 ICLK
0008 7351h	ICU	Interrupt source priority register 51	IPR51	8	8	2 ICLK
0008 7352h	ICU	Interrupt source priority register 52	IPR52	8	8	2 ICLK
0008 7353h	ICU	Interrupt source priority register 53	IPR53	8	8	2 ICLK
0008 7354h	ICU	Interrupt source priority register 54	IPR54	8	8	2 ICLK
0008 7355h	ICU	Interrupt source priority register 55	IPR55	8	8	2 ICLK
0008 7356h	ICU	Interrupt source priority register 56	IPR56	8	8	2 ICLK
0008 7357h	ICU	Interrupt source priority register 57	IPR57	8	8	2 ICLK
0008 7358h	ICU	Interrupt source priority register 58	IPR58	8	8	2 ICLK
0008 7359h	ICU	Interrupt source priority register 59	IPR59	8	8	2 ICLK
0008 735Ah	ICU	Interrupt source priority register 5A	IPR5A	8	8	2 ICLK
0008 735Bh	ICU	Interrupt source priority register 5B	IPR5B	8	8	2 ICLK
0008 735Ch	ICU	Interrupt source priority register 5C	IPR5C	8	8	2 ICLK
0008 735Dh	ICU	Interrupt source priority register 5D	IPR5D	8	8	2 ICLK
0008 735Eh	ICU	Interrupt source priority register 5E	IPR5E	8	8	2 ICLK
0008 735Fh	ICU	Interrupt source priority register 5F	IPR5F	8	8	2 ICLK
0008 7360h	ICU	Interrupt source priority register 60	IPR60	8	8	2 ICLK
0008 7367h	ICU	Interrupt source priority register 67	IPR67	8	8	2 ICLK
0008 7368h	ICU	Interrupt source priority register 68	IPR68	8	8	2 ICLK
0008 7369h	ICU	Interrupt source priority register 69	IPR69	8	8	2 ICLK
0008 736Ah	ICU	Interrupt source priority register 6A	IPR6A	8	8	2 ICLK
0008 736Bh	ICU	Interrupt source priority register 6B	IPR6B	8	8	2 ICLK
0008 736Ch	ICU	Interrupt source priority register 6C	IPR6C	8	8	2 ICLK
0008 736Dh	ICU	Interrupt source priority register 6D	IPR6D	8	8	2 ICLK
0008 736Eh	ICU	Interrupt source priority register 6E	IPR6E	8	8	2 ICLK
0008 736Fh	ICU	Interrupt source priority register 6F	IPR6F	8	8	2 ICLK
0008 7380h	ICU	Interrupt source priority register 80	IPR80	8	8	2 ICLK
0008 7381h	ICU	Interrupt source priority register 81	IPR81	8	8	2 ICLK

Table 4.2 List of I/O Registers (Bit Order) (18 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
CAN0*3	AFSR	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
CAN0*3	TCR	—	—	—	—	—	TSTM[1:0]		TSTE
LIN0	LWBR	—	—	—	—	—	—	—	LWBR0
LIN0	LBRP0								
LIN0	LBRP1								
LIN0	LSTC								LSTM
LIN0	L0MD	—	—	—	—	LCKS[1:0]		—	—
LIN0	L0BRK	—	—	BDT[1:0]			BLT[3:0]		
LIN0	L0SPC	—	—	IBS[1:0]		—	IBSH[2:0]		
LIN0	L0WUP		WUTL[3:0]			—	—	—	—
LIN0	L0IE	—	—	—	—	—	ERRIE	FRCIE	FTCIE
LIN0	L0EDE	—	—	—	—	FERE	FTERE	PBERE	BERE
LIN0	L0C	—	—	—	—	—	—	OM1	OM0
LIN0	L0TC	—	—	—	—	—	—	RTS	FTS
LIN0	L0MST	—	—	—	—	—	—	OMM1	OMM0
LIN0	L0ST	HTRC	D1RC	—	—	ERR	—	FRC	FTC
LIN0	L0EST	—	—	CSER	—	FER	FTER	PBER	BER
LIN0	L0RFC	—	FSM	CSM	RFT		RFDL[3:0]		
LIN0	L0IDB		IDP				ID		
LIN0	L0CBR								
LIN0	L0DB1								
LIN0	L0DB2								
LIN0	L0DB3								
LIN0	L0DB4								
LIN0	L0DB5								
LIN0	L0DB6								
LIN0	L0DB7								
LIN0	L0DB8								
MTU3	TCR		CCLR[2:0]			CKEG[1:0]		TPSC[2:0]	
MTU4	TCR		CCLR[2:0]			CKEG[1:0]		TPSC[2:0]	
MTU3	TMDR1	—	—	BFB	BFA			MD[3:0]	
MTU4	TMDR1	—	—	BFB	BFA			MD[3:0]	
MTU3	TIORH			IOB[3:0]				IOA[3:0]	
MTU3	TIORL			IOD[3:0]				IOC[3:0]	
MTU4	TIORH			IOB[3:0]				IOA[3:0]	
MTU4	TIORL			IOD[3:0]				IOC[3:0]	
MTU3	TIER	TTGE	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA
MTU4	TIER	TTGE	TTGE2	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA
MTU	TOERA	—	—	OE4D	OE4C	OE3D	OE4B	OE4A	OE3B
MTU	TGCRA	—	BDC	N	P	FB	WF	VF	UF
MTU	TOCR1A	—	PSYE	—	—	TOCL	TOCS	OLSN	OLSP
MTU	TOCR2A		BF[1:0]	OLS3N	OLS3P	OLS2N	OLS2P	OLS1N	OLS1P
MTU3	TCNT								
MTU4	TCNT								
MTU	TCDRA								
MTU	TDDRA								

Table 4.2 List of I/O Registers (Bit Order) (30 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
FLASH	FSTATR0	FRDY	ILGLERR	ERSERR	PRGERR	SUSRDY	—	ERSSPD	PRGSPD
FLASH	FSTATR1	FCUERR	—	—	FLOCKST	—	—	—	—
FLASH	FENTRYR	FEKEY[7:0]							
		FENTRYD	—	—	—	—	—	—	FENTRY0
FLASH	FPROTR	FPKEY[7:0]							
		—	—	—	—	—	—	—	FPROTCN
FLASH	FRESETR	FRKEY[7:0]							
		—	—	—	—	—	—	—	FRESET
FLASH	FCMDR	CMDR[7:0]							
		PCMDR[7:0]							
FLASH	FCPSR	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	ESUSPMD
FLASH	DFLBCCNT	BCADR[7:0]							
		BCADR[7:0]							
FLASH	FPESTAT	—	—	—	—	—	—	—	—
		PEERRST[7:0]							
FLASH	DFLBCSTAT	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	BCST
FLASH	PCKAR	—	—	—	—	—	—	—	—
		PCKA[7:0]							

Note: • In this, the I/O port related registers (0008 C001h to 0008 C116h) indicate the bit configuration of the 112-pin LQFP version. As the configuration of registers and bits differs depending on a package, see section 14, I/O Ports, for details in the User's manual: Hardware.

Note 1. This shows the bit configuration when ADDPR.DPSEL = 0 and ADDPR.DPPRC = 0 (The value has 10-bit accuracy and is padded at the LSB end).

Note 2. This shows the bit configuration when ADCER.ADRFMT = 0 (aligned to the LSB end) and ADCER.ADPRC[1:0] = 00b. For details, refer to section 28, 12-Bit A/D Converter (S12ADA) in the User's manual: Hardware.

Note 3. This function is not supported by the product without the CAN function.

5.2 DC Characteristics

Table 5.2 DC Characteristics (1) (1 / 3)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	CAN input pin IRQ input pin MTU3 input pin POE3 input pin SCI input pin A/D trigger input pin NMI input pin GPT input pin LIN input pin RES#	V _{IH}	VCC×0.8	-	VCC+0.3	V	
		V _{IL}	-0.3	-	VCC×0.2		
		ΔV _T	VCC ×0.06	-	-		
	RIIC input pin (IICBus)	V _{IH}	VCC×0.7	-	VCC+0.3		
		V _{IL}	-0.3	-	VCC×0.3		
		ΔV _T	VCC ×0.05	-	-		
	Port 4*1 (also usable as an analog port)	V _{IH}	AVCC0 ×0.8	-	AVCC0 +0.3		
		V _{IL}	- 0.3	-	AVCC0 ×0.2		
		ΔV _T	AVCC0 ×0.06	-	-		
	Ports 5 and 6*1 (also usable as analog ports)	V _{IH}	AVCC ×0.8	-	AVCC +0.3		
		V _{IL}	-0.3	-	AVCC ×0.2		
		ΔV _T	AVCC ×0.06	-	-		
	Ports 1 to 3*1 Ports 7 to B*1 Ports D, E, and G*1	V _{IH}	VCC×0.8	-	VCC+0.3		
		V _{IL}	-0.3	-	VCC×0.2		
		ΔV _T	VCC ×0.06	-	-		
Input high voltage (except Schmitt trigger input pin)	MD pin, EMLE	V _{IH}	VCC×0.9	-	VCC+0.3	V	Conditions 1 and 2
	EXTAL RSPI input pin		VCC×0.8		VCC+0.3		
	RIIC input pin (SMBus)		2.1		VCC+0.3		
Input low voltage (except Schmitt trigger input pin)	MD pin, EMLE	V _{IL}	-0.3	-	VCC×0.1	V	Conditions 1 and 2
	EXTAL RSPI input pin		-0.3	-	VCC×0.2		
	RIIC input pin (SMBus)		-0.3	-	0.8		

5.3.2 Control Signal Timing

Table 5.8 Control Signal Timing

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Ta = Topr. Ta is the same under conditions 1 to 3.

Item	Symbol	Min.	Max.	Unit	Test Conditions
RES# pulse width (except for programming or erasure of the ROM or data-flash memory or blank checking of the data-flash memory*1)	t_{RESW}^{*2}	20	-	t_{cyc}^{*4}	Figure 5.5
		1.5	-	μs	
Internal reset time*3	t_{RESW2}	35	-	μs	
NMI pulse width	t_{NMIW}	200	-	ns	Figure 5.6
IRQ pulse width	t_{IRQW}	200	-	ns	Figure 5.7

Note 1. For a reset by the signal on the RES# pin during programming or erasure of the ROM or data-flash memory or during blank checking of the data-flash memory, see section 31.12, Usage Notes in section 31, ROM (Flash Memory for Code Storage) in the User's manual: Hardware.

Note 2. Both the time and the number of cycles should satisfy the specifications.

Note 3. This is to specify the FCU reset.

Note 4. ICLK cycles.

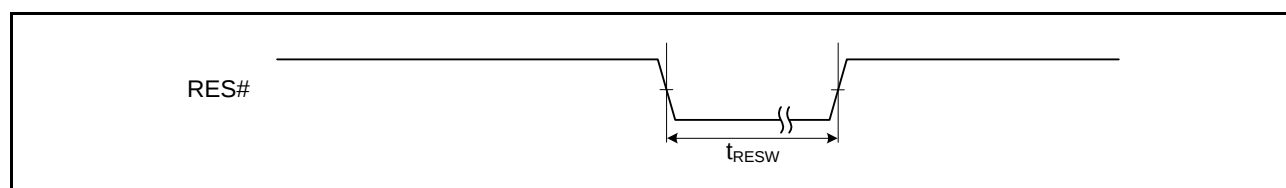


Figure 5.5 Reset Input Timing

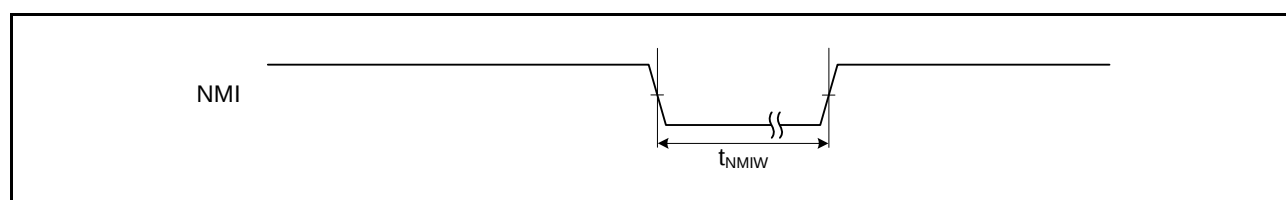


Figure 5.6 NMI Interrupt Input Timing

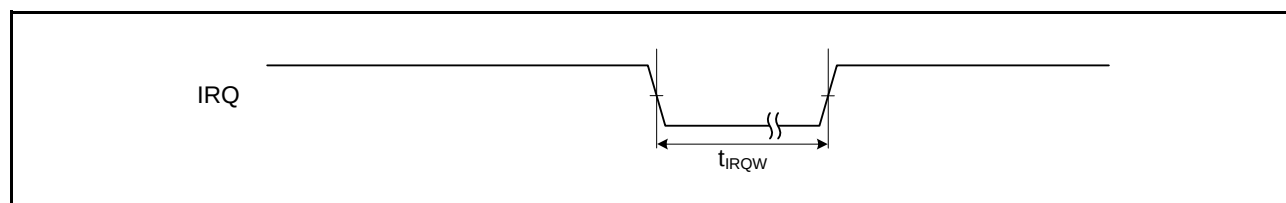


Figure 5.7 IRQ Interrupt Input Timing

Table 5.11 Timing of On-Chip Peripheral Modules (3)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item			Symbol	Min.	Max.	Unit	Test Conditions	
RSPI	RSPCK clock cycle	Master	t _{SPcyc}	4	4096	t _{Pcyc}	Figure 5.11	
		Slave		8	4096			
	RSPCK clock high pulse width	Master	t _{SPCKWH}	(t _{Sp_{cyc}} - t _{SPCKR} - t _{SPCKF}) / 2-3	-	ns		
		Slave		(t _{Sp_{cyc}} - t _{SPCKR} - t _{SPCKF}) / 2	-			
	RSPCK clock low pulse width	Master	t _{SPCKWL}	(t _{Sp_{cyc}} - t _{SPCKR} - t _{SPCKF}) / 2-3	-	ns		
		Slave		(t _{Sp_{cyc}} - t _{SPCKR} - t _{SPCKF}) / 2	-			
	RSPCK clock rise/fall time	Output	t _{SPCKR}	-	5	ns		
		Input	t _{SPCKF}	-	1	μs		
	Data input setup time	Master	t _{SU}	25	-	ns	Figure 5.12 to Figure 5.15	
		Slave		0	-			
	Data input hold time	Master	t _H	0	-	ns		
		Slave		20+2×t _{Pcyc}	-			
	SSL setup time	Master	t _{LEAD}	1	8	t _{SPcyc}		
		Slave		4	-	t _{Pcyc}		
	SSL hold time	Master	t _{LAG}	1	8	t _{SPcyc}		
		Slave		4	-	t _{Pcyc}		
	Data output delay time	Master	t _{OD}	-	20	ns		
		Slave		-	3×t _{Pcyc} +40			
	Data output hold time	Master	t _{OH}	0	-	ns		
		Slave		0	-			
	Successive transmission delay time	Master	t _{TD}	t _{SPcyc} +2×t _{Pcyc}	8×t _{SPcyc} +2×t _{Pcyc}	ns		
		Slave		4×t _{Pcyc}	-			
	MOSI, MISO rise/fall time	Output	t _{DR}	-	15	ns	Figure 5.12 to Figure 5.15	
		Input	t _{DF}	-	1	μs		
	SSL rise/fall time	Output	t _{SSLR}	-	15	ns		
		Input	t _{SSLF}	-	1	μs		
	Slave access time			t _{SA}	-	4	t _{Pcyc}	Figure 5.12 to Figure 5.15
	Slave output release time			t _{REL}	-	3	t _{Pcyc}	

Note: • Note 1: t_{PCyc} : PCLK cycle

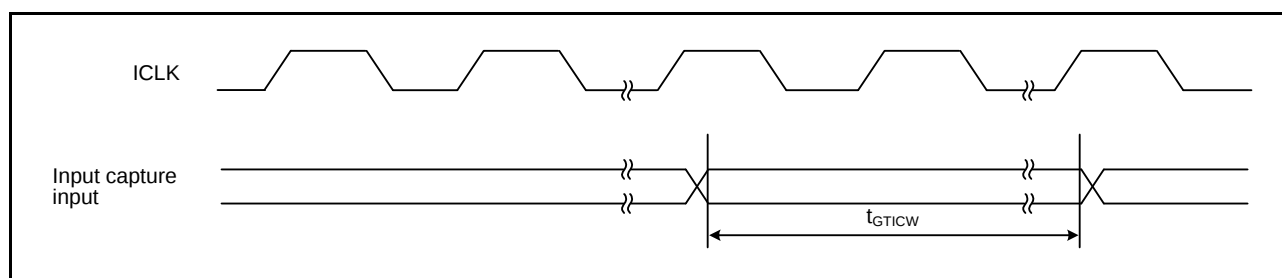


Figure 5.18 GPT Input/Output Timing

Table 5.13 Timing of On-Chip Peripheral Modules (5)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Max.	Unit	Test Conditions
POE3	POE# input pulse width	t _{POEW}	1.5	-	t _{Pcyc}	Figure 5.19

Note: • t_{Pcyc}: PCLK cycle

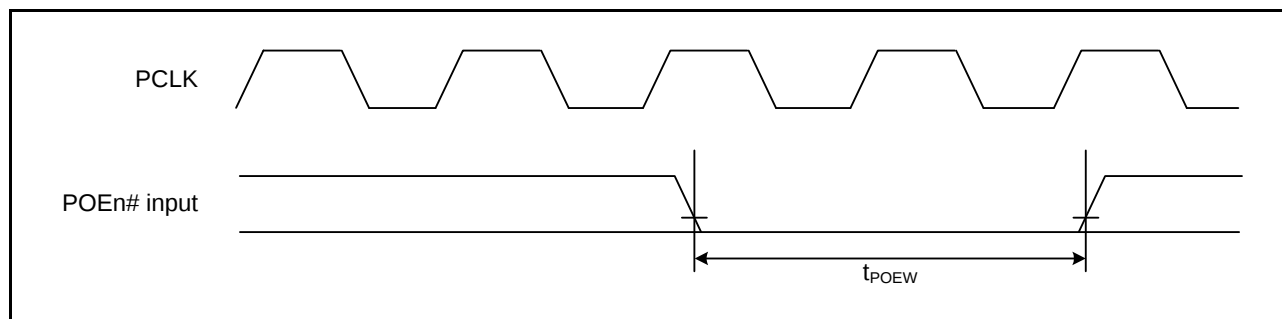


Figure 5.19 POE3# Clock Timing

5.3.4 Timing of PWM Delay Generation Circuit

Table 5.14 Timing of the PWM Delay Generation Circuit

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS = VREL0 = 0 V

AVCC = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Ta = Topr.

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Resolution	—	312.5	—	ps	ICLK = 100 MHz
DNL *1	—	±2.0	—	LSB	

Note 1. This value is correct when the difference between each code and the next is a resolution of one bit (1 LSB).

5.7 ROM (Flash Memory for Code Storage) Characteristics

Table 5.21 ROM (Flash Memory for Code Storage) Characteristics (1)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Temperature range for the programming/erasure operation:
Ta = Topr. Ta is the same under conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Rewrite/erase cycle ^{*1}	N _{PEC}	1000	—	—	Times	
Data hold time	t _{DRP}	30 ^{*2}	—	—	Year	Ta = +85C°

Note 1. Definition of rewrite/erase cycle:

The rewrite/erase cycle is the number of erasing for each block. When the rewrite/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 256-byte writing is performed 16 times for different addresses in 4-Kbyte block and then the entire block is erased, the rewrite/erase cycle is counted as one. However, writing to the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. The value is obtained from the reliability test.

Table 5.22 ROM (Flash Memory for Code Storage) Characteristics (2)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Temperature range for the programming/erasure operation:
Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Programming time	256 bytes	t _{P256}	—	2	12	ms	PCLK = 50 MHz N _{PEC} ≤ 100
	4 Kbytes	t _{P4K}	—	23	50	ms	
	16 Kbytes	t _{P16K}	—	90	200	ms	
	256 byte	t _{P256}	—	2.4	14.4	ms	PCLK = 50 MHz N _{PEC} > 100
	4 Kbytes	t _{P4K}	—	27.6	60	ms	
	16 Kbytes	t _{P16K}	—	108	240	ms	
Erasure time	4 Kbytes	t _{E4K}	—	25	60	ms	PCLK = 50 MHz N _{PEC} ≤ 100
	16 Kbytes	t _{E16K}	—	100	240	ms	
	4 Kbytes	t _{E4K}	—	30	72	ms	PCLK = 50 MHz N _{PEC} > 100
	16 Kbytes	t _{E16K}	—	120	288	ms	
Suspend delay time during writing		t _{SPD}	—	—	120	μs	Figure 5.24 PCLK = 50 MHz
First suspend delay time during erasing (in suspend priority mode)		t _{SESD1}	—	—	120	μs	
Second suspend delay time during erasing (in suspend priority mode)		t _{SESD2}	—	—	1.7	ms	
Suspend delay time during erasing (in erasure priority mode)		t _{SEED}	—	—	1.7	ms	

5.8 Data Flash (Flash Memory for Data Storage) Characteristics

Table 5.23 Data Flash (Flash Memory for Data Storage) Characteristics (1)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Temperature range for the programming/erasure operation:
Ta = Topr. Ta is the same under conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Rewrite/erase cycle ^{*1}	N _{DPEC}	30000	—	—	Times	
Data hold time	t _{DDRP}	30 ^{*2}	—	—	Year	Ta = +85C°

Note 1. Definition of rewrite/erase cycle:

The rewrite/erase cycle is the number of erasing for each block. When the rewrite/erase cycle is n times (n = 30000), erasing can be performed n times for each block. For instance, when 128-byte writing is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the rewrite/erase cycle is counted as one. However, writing to the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. The value is obtained from the reliability test.

Table 5.24 Data Flash (Flash Memory for Data Storage) Characteristics (2)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Temperature range for the programming/erasure operation:
Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Programming time	8 bytes	t _{DP8}	—	0.4	2	ms	PCLK = 50 MHz
	128 bytes	t _{DP128}	—	1	5	ms	
Erase time	2 Kbytes	t _{DE2K}	—	70	250	ms	PCLK = 50 MHz
Blank check time	8 bytes	t _{DBC8}	—	—	30	μs	PCLK = 50 MHz
	2 Kbytes	t _{DBC2K}	—	—	0.7	ms	
Suspend delay time during writing		t _{DSPD}	—	—	120	μs	Figure 5.24 PCLK = 50 MHz
First suspend delay time during erasing (in suspend priority mode)		t _{DSESD1}	—	—	120	μs	
Second suspend delay time during erasing (in suspend priority mode)		t _{DSESD2}	—	—	1.7	ms	
Suspend delay time during erasing (in erasure priority mode)		t _{DSEED}	—	—	1.7	ms	

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

- The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.