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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I ² C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	61
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 12x10b, 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562gaadf-h-v3

Table 1.2 Functions of RX62T Group and RX62G Group Products (1 / 2)

Functions		RX62G Group		RX62T Group				
Pin number		112 Pins	100 Pins	112 Pins	100 Pins	80 Pins (R5F562T xGDFF)	80 Pins	64 Pins
Data transfer	Data transfer controller (DTC)	√						
Interrupt controller (ICU)	Input on the NMI pin	√						
	Input on the IRQ pins	√ (8)						√ (4)
Timers	Multi-function timer pulse unit 3 (MTU3)	√				√*1		
	General PWM timer (GPT)	—		√		√*1		
	General PWM timer (GPTa)	√		—				
	MTU3/GPT complementary PWM pin	12					6	
	Port output enable 3 (POE3)	√ (POE pins: 5)						√ (POE pins: 3)
	Compare match timer (CMT)	√						
	Watchdog timer (WDT)	√						
	Independent watchdog timer (IWDT)	√						
Communication function	Serial communications interface (SCI)	√						
	I ² C bus interface (RIIC)	√						
	CAN module (CAN) (as an optional function)	√						
	LIN module (LIN)	√						
	Serial peripheral interface (RSPI)	√						
12-bit A/D converter (S12ADA)		√ (4 ch. x 2 units)						
	Simultaneous sampling on three channels	√ (2 units)						
	Programmable gain amplifier	√ (3 ch. x 2 units)						
	Window comparator	√ (3 ch. x 2 units)						
10-bit A/D converter (ADA)		√ (12 ch.)				√ (4 ch.)		—
CRC calculator (CRC)		√						
I/O ports	I/O pins	61	55	61	55	44	44	37
	Input pins	21	21	21	21	13	13	9

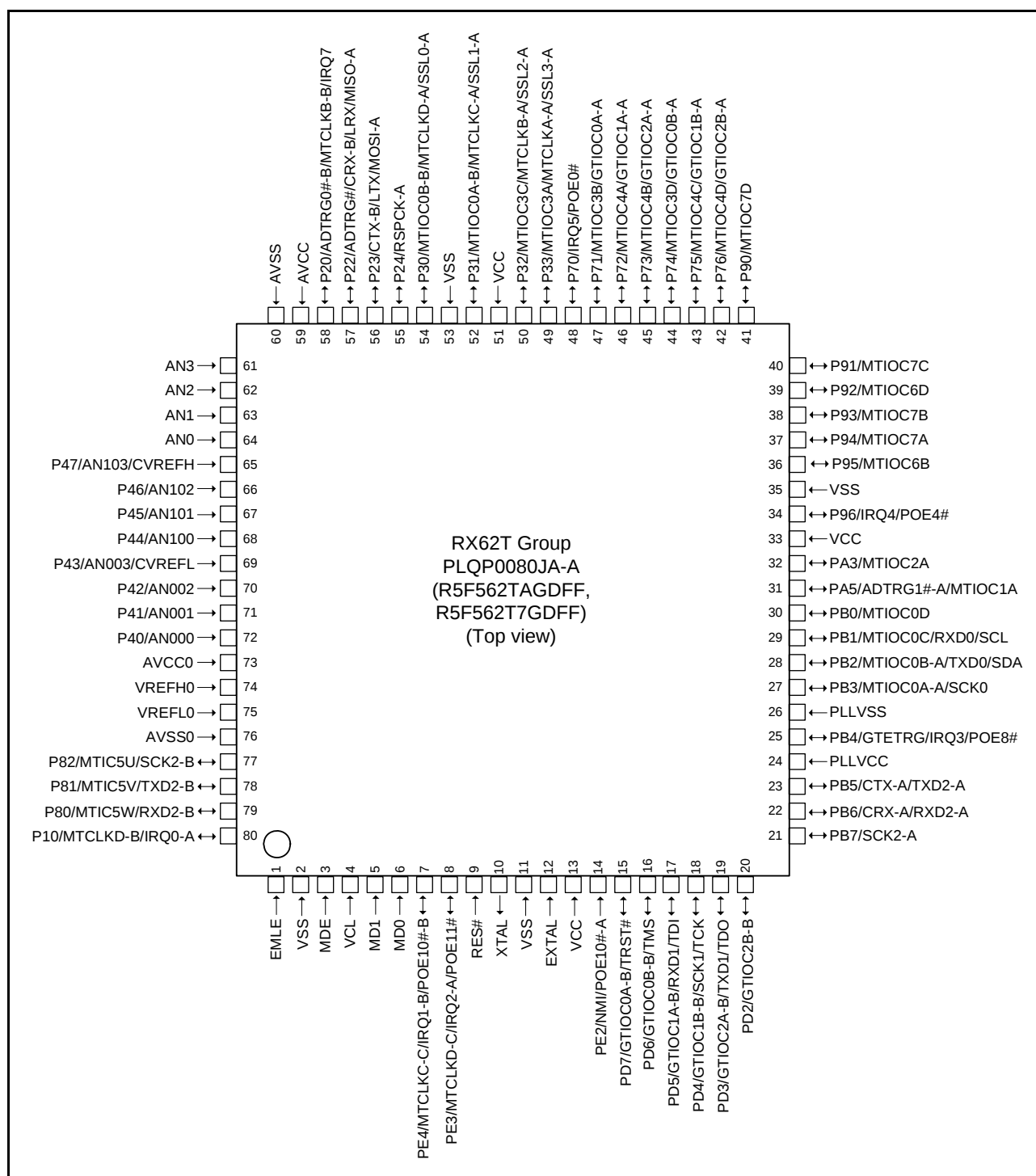


Figure 1.6 Pin Assignment of the 80-Pin LQFP (Two-Motor Control Supported Version)

Table 4.1 List of I/O Registers (Address Order) (7 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 7305h	ICU	Interrupt source priority register 05	IPR05	8	8	2 ICLK
0008 7306h	ICU	Interrupt source priority register 06	IPR06	8	8	2 ICLK
0008 7307h	ICU	Interrupt source priority register 07	IPR07	8	8	2 ICLK
0008 7314h	ICU	Interrupt source priority register 14	IPR14	8	8	2 ICLK
0008 7318h	ICU	Interrupt source priority register 18	IPR18	8	8	2 ICLK
0008 7320h	ICU	Interrupt source priority register 20	IPR20	8	8	2 ICLK
0008 7321h	ICU	Interrupt source priority register 21	IPR21	8	8	2 ICLK
0008 7322h	ICU	Interrupt source priority register 22	IPR22	8	8	2 ICLK
0008 7323h	ICU	Interrupt source priority register 23	IPR23	8	8	2 ICLK
0008 7324h	ICU	Interrupt source priority register 24	IPR24	8	8	2 ICLK
0008 7325h	ICU	Interrupt source priority register 25	IPR25	8	8	2 ICLK
0008 7326h	ICU	Interrupt source priority register 26	IPR26	8	8	2 ICLK
0008 7327h	ICU	Interrupt source priority register 27	IPR27	8	8	2 ICLK
0008 7340h	ICU	Interrupt source priority register 40	IPR40	8	8	2 ICLK
0008 7344h	ICU	Interrupt source priority register 44	IPR44	8	8	2 ICLK
0008 7348h	ICU	Interrupt source priority register 48	IPR48	8	8	2 ICLK
0008 7349h	ICU	Interrupt source priority register 49	IPR49	8	8	2 ICLK
0008 7351h	ICU	Interrupt source priority register 51	IPR51	8	8	2 ICLK
0008 7352h	ICU	Interrupt source priority register 52	IPR52	8	8	2 ICLK
0008 7353h	ICU	Interrupt source priority register 53	IPR53	8	8	2 ICLK
0008 7354h	ICU	Interrupt source priority register 54	IPR54	8	8	2 ICLK
0008 7355h	ICU	Interrupt source priority register 55	IPR55	8	8	2 ICLK
0008 7356h	ICU	Interrupt source priority register 56	IPR56	8	8	2 ICLK
0008 7357h	ICU	Interrupt source priority register 57	IPR57	8	8	2 ICLK
0008 7358h	ICU	Interrupt source priority register 58	IPR58	8	8	2 ICLK
0008 7359h	ICU	Interrupt source priority register 59	IPR59	8	8	2 ICLK
0008 735Ah	ICU	Interrupt source priority register 5A	IPR5A	8	8	2 ICLK
0008 735Bh	ICU	Interrupt source priority register 5B	IPR5B	8	8	2 ICLK
0008 735Ch	ICU	Interrupt source priority register 5C	IPR5C	8	8	2 ICLK
0008 735Dh	ICU	Interrupt source priority register 5D	IPR5D	8	8	2 ICLK
0008 735Eh	ICU	Interrupt source priority register 5E	IPR5E	8	8	2 ICLK
0008 735Fh	ICU	Interrupt source priority register 5F	IPR5F	8	8	2 ICLK
0008 7360h	ICU	Interrupt source priority register 60	IPR60	8	8	2 ICLK
0008 7367h	ICU	Interrupt source priority register 67	IPR67	8	8	2 ICLK
0008 7368h	ICU	Interrupt source priority register 68	IPR68	8	8	2 ICLK
0008 7369h	ICU	Interrupt source priority register 69	IPR69	8	8	2 ICLK
0008 736Ah	ICU	Interrupt source priority register 6A	IPR6A	8	8	2 ICLK
0008 736Bh	ICU	Interrupt source priority register 6B	IPR6B	8	8	2 ICLK
0008 736Ch	ICU	Interrupt source priority register 6C	IPR6C	8	8	2 ICLK
0008 736Dh	ICU	Interrupt source priority register 6D	IPR6D	8	8	2 ICLK
0008 736Eh	ICU	Interrupt source priority register 6E	IPR6E	8	8	2 ICLK
0008 736Fh	ICU	Interrupt source priority register 6F	IPR6F	8	8	2 ICLK
0008 7380h	ICU	Interrupt source priority register 80	IPR80	8	8	2 ICLK
0008 7381h	ICU	Interrupt source priority register 81	IPR81	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (8 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 7382h	ICU	Interrupt source priority register 82	IPR82	8	8	2 ICLK
0008 7388h	ICU	Interrupt source priority register 88	IPR88	8	8	2 ICLK
0008 7389h	ICU	Interrupt source priority register 89	IPR89	8	8	2 ICLK
0008 738Ah	ICU	Interrupt source priority register 8A	IPR8A	8	8	2 ICLK
0008 738Bh	ICU	Interrupt source priority register 8B	IPR8B	8	8	2 ICLK
0008 7390h	ICU	Interrupt source priority register 90	IPR90	8	8	2 ICLK
0008 7500h	ICU	IRQ control register 0	IRQCR0	8	8	2 ICLK
0008 7501h	ICU	IRQ control register 1	IRQCR1	8	8	2 ICLK
0008 7502h	ICU	IRQ control register 2	IRQCR2	8	8	2 ICLK
0008 7503h	ICU	IRQ control register 3	IRQCR3	8	8	2 ICLK
0008 7504h	ICU	IRQ control register 4	IRQCR4	8	8	2 ICLK
0008 7505h	ICU	IRQ control register 5	IRQCR5	8	8	2 ICLK
0008 7506h	ICU	IRQ control register 6	IRQCR6	8	8	2 ICLK
0008 7507h	ICU	IRQ control register 7	IRQCR7	8	8	2 ICLK
0008 7580h	ICU	Non-maskable interrupt status register	NMISR	8	8	2 ICLK
0008 7581h	ICU	Non-maskable interrupt enable register	NMIER	8	8	2 ICLK
0008 7582h	ICU	Non-maskable interrupt clear register	NMICLR	8	8	2 ICLK
0008 7583h	ICU	NMI pin interrupt control register	NMICR	8	8	2 ICLK
0008 8000h	CMT	Compare match timer start register 0	CMSTR0	16	16	2, 3 PCLK*3
0008 8002h	CMT0	Compare match timer control register	CMCR	16	16	2, 3 PCLK*3
0008 8004h	CMT0	Compare match timer counter	CMCNT	16	16	2, 3 PCLK*3
0008 8006h	CMT0	Compare match timer constant register	CMCOR	16	16	2, 3 PCLK*3
0008 8008h	CMT1	Compare match timer control register	CMCR	16	16	2, 3 PCLK*3
0008 800Ah	CMT1	Compare match timer counter	CMCNT	16	16	2, 3 PCLK*3
0008 800Ch	CMT1	Compare match timer constant register	CMCOR	16	16	2, 3 PCLK*3
0008 8010h	CMT	Compare match timer start register 1	CMSTR1	16	16	2, 3 PCLK*3
0008 8012h	CMT2	Compare match timer control register	CMCR	16	16	2, 3 PCLK*3
0008 8014h	CMT2	Compare match timer counter	CMCNT	16	16	2, 3 PCLK*3
0008 8016h	CMT2	Compare match timer constant register	CMCOR	16	16	2, 3 PCLK*3
0008 8018h	CMT3	Compare match timer control register	CMCR	16	16	2, 3 PCLK*3
0008 801Ah	CMT3	Compare match timer counter	CMCNT	16	16	2, 3 PCLK*3
0008 801Ch	CMT3	Compare match timer constant register	CMCOR	16	16	2, 3 PCLK*3
0008 8028h	WDT	Timer control/status register	TCSR	8	8	2, 3 PCLK*3
0008 8028h	WDT	Write window A register	WINA	16	16	2, 3 PCLK*3
0008 8029h	WDT	Timer counter	TCNT	8	8	2, 3 PCLK*3
0008 802Ah	WDT	Write window B register	WINB	16	16	2, 3 PCLK*3
0008 802Bh	WDT	Reset control/status register	RSTCSR	8	8	2, 3 PCLK*3
0008 8030h	IWDT	IWDT refresh register	IWDTRR	8	8	2, 3 PCLK*3
0008 8032h	IWDT	IWDT control register	IWDTCR	16	16	2, 3 PCLK*3
0008 8034h	IWDT	IWDT status register	IWDTSR	16	16	2, 3 PCLK*3
0008 8040h	ADA	A/D data register A	ADDRA	16	16	2, 3 PCLK*3
0008 8042h	ADA	A/D data register B	ADDRB	16	16	2, 3 PCLK*3
0008 8044h	ADA	A/D data register C	ADDRC	16	16	2, 3 PCLK*3
0008 8046h	ADA	A/D data register D	ADDRD	16	16	2, 3 PCLK*3

Table 4.1 List of I/O Registers (Address Order) (11 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 8383h	RSPI	RSPI status register	SPSR	8	8	2, 3 PCLK*3
0008 8384h	RSPI	RSPI data register	SPDR	16, 32	16, 32	2, 3 PCLK*3
0008 8388h	RSPI	RSPI sequence control register	SPSCR	8	8	2, 3 PCLK*3
0008 8389h	RSPI	RSPI sequence status register	SPSSR	8	8	2, 3 PCLK*3
0008 838Ah	RSPI	RSPI bit rate register	SPBR	8	8	2, 3 PCLK*3
0008 838Bh	RSPI	RSPI data control register	SPDCR	8	8	2, 3 PCLK*3
0008 838Ch	RSPI	RSPI clock delay register	SPCKD	8	8	2, 3 PCLK*3
0008 838Dh	RSPI	RSPI slave select negation delay register	SSLND	8	8	2, 3 PCLK*3
0008 838Eh	RSPI	RSPI next-access delay register	SPND	8	8	2, 3 PCLK*3
0008 838Fh	RSPI	RSPI control register 2	SPCR2	8	8	2, 3 PCLK*3
0008 8390h	RSPI	RSPI command register 0	SPCMD0	16	16	2, 3 PCLK*3
0008 8392h	RSPI	RSPI command register 1	SPCMD1	16	16	2, 3 PCLK*3
0008 8394h	RSPI	RSPI command register 2	SPCMD2	16	16	2, 3 PCLK*3
0008 8396h	RSPI	RSPI command register 3	SPCMD3	16	16	2, 3 PCLK*3
0008 8398h	RSPI	RSPI command register 4	SPCMD4	16	16	2, 3 PCLK*3
0008 839Ah	RSPI	RSPI command register 5	SPCMD5	16	16	2, 3 PCLK*3
0008 839Ch	RSPI	RSPI command register 6	SPCMD6	16	16	2, 3 PCLK*3
0008 839Eh	RSPI	RSPI command register 7	SPCMD7	16	16	2, 3 PCLK*3
0008 9000h	S12AD0	A/D control register	ADCSR	8	8	2, 3 PCLK*3
0008 9004h	S12AD0	A/D channel select register	ADANS	16	16	2, 3 PCLK*3
0008 900Ah	S12AD0	A/D programmable gain amplifier register	ADPG	16	16	2, 3 PCLK*3
0008 900Eh	S12AD0	A/D control extended register	ADCER	16	16	2, 3 PCLK*3
0008 9010h	S12AD0	A/D start trigger select register	ADSTRGR	16	16	2, 3 PCLK*3
0008 9012h	S12AD	Comparator operating mode select register 0	ADCMPMD0	16	16	2, 3 PCLK*3
0008 9014h	S12AD	Comparator operating mode select register 1	ADCMPMD1	16	16	2, 3 PCLK*3
0008 9016h	S12AD	Comparator filter mode register 0	ADCMFNR0	16	16	2, 3 PCLK*3
0008 9018h	S12AD	Comparator filter mode register 1	ADCMFNR1	16	16	2, 3 PCLK*3
0008 901Ah	S12AD	Comparator detection flag register	ADCMFDR	8	8	2, 3 PCLK*3
0008 901Ch	S12AD	Comparator interrupt select register	ADCMFSEL	16	16	2, 3 PCLK*3
0008 901Eh	S12AD0	A/D data register Diag	ADRD	16	16	2, 3 PCLK*3
0008 9020h	S12AD0	A/D data register 0A	ADDR0A	16	16	2, 3 PCLK*3
0008 9022h	S12AD0	A/D data register 1	ADDR1	16	16	2, 3 PCLK*3
0008 9024h	S12AD0	A/D data register 2	ADDR2	16	16	2, 3 PCLK*3
0008 9026h	S12AD0	A/D data register 3	ADDR3	16	16	2, 3 PCLK*3
0008 9030h	S12AD0	A/D data register 0B	ADDR0B	16	16	2, 3 PCLK*3
0008 9060h	S12AD0	A/D sampling state register	ADSSTR	8	8	2, 3 PCLK*3
0008 9080h	S12AD1	A/D control register	ADCSR	8	8	2, 3 PCLK*3
0008 9084h	S12AD1	A/D channel select register	ADANS	16	16	2, 3 PCLK*3
0008 908Ah	S12AD1	A/D programmable gain amplifier register	ADPG	16	16	2, 3 PCLK*3
0008 908Eh	S12AD1	A/D control extended register	ADCER	16	16	2, 3 PCLK*3
0008 9090h	S12AD1	A/D start trigger select register	ADSTRGR	16	16	2, 3 PCLK*3
0008 909Eh	S12AD1	A/D data register Diag	ADRD	16	16	2, 3 PCLK*3
0008 90A0h	S12AD1	A/D data register 0A	ADDR0A	16	16	2, 3 PCLK*3
0008 90A2h	S12AD1	A/D data register 1	ADDR1	16	16	2, 3 PCLK*3

Table 4.1 List of I/O Registers (Address Order) (12 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 90A4h	S12AD1	A/D data register 2	ADDR2	16	16	2, 3 PCLK* ³
0008 90A6h	S12AD1	A/D data register 3	ADDR3	16	16	2, 3 PCLK* ³
0008 90B0h	S12AD1	A/D data register 0B	ADDR0B	16	16	2, 3 PCLK* ³
0008 90E0h	S12AD1	A/D sampling state register	ADSSTR	8	8	2, 3 PCLK* ³
0008 C001h	PORT1	Data direction register	DDR	8	8	2, 3 PCLK* ³
0008 C002h	PORT2	Data direction register	DDR	8	8	2, 3 PCLK* ³
0008 C003h	PORT3	Data direction register	DDR	8	8	2, 3 PCLK* ³
0008 C007h	PORT7	Data direction register	DDR	8	8	2, 3 PCLK* ³
0008 C008h	PORT8	Data direction register	DDR	8	8	2, 3 PCLK* ³
0008 C009h	PORT9	Data direction register	DDR	8	8	2, 3 PCLK* ³
0008 C00Ah	PORTA	Data direction register	DDR	8	8	2, 3 PCLK* ³
0008 C00Bh	PORTB	Data direction register	DDR	8	8	2, 3 PCLK* ³
0008 C00Dh	PORTD	Data direction register	DDR	8	8	2, 3 PCLK* ³
0008 C00Eh	PORTE	Data direction register	DDR	8	8	2, 3 PCLK* ³
0008 C010h	PORTG	Data direction register	DDR* ¹	8	8	2, 3 PCLK* ³
0008 C021h	PORT1	Data register	DR	8	8	2, 3 PCLK* ³
0008 C022h	PORT2	Data register	DR	8	8	2, 3 PCLK* ³
0008 C023h	PORT3	Data register	DR	8	8	2, 3 PCLK* ³
0008 C027h	PORT7	Data register	DR	8	8	2, 3 PCLK* ³
0008 C028h	PORT8	Data register	DR	8	8	2, 3 PCLK* ³
0008 C029h	PORT9	Data register	DR	8	8	2, 3 PCLK* ³
0008 C02Ah	PORTA	Data register	DR	8	8	2, 3 PCLK* ³
0008 C02Bh	PORTB	Data register	DR	8	8	2, 3 PCLK* ³
0008 C02Dh	PORTD	Data register	DR	8	8	2, 3 PCLK* ³
0008 C02Eh	PORTE	Data register	DR	8	8	2, 3 PCLK* ³
0008 C030h	PORTG	Data register	DR* ¹	8	8	2, 3 PCLK* ³
0008 C041h	PORT1	Data register	PORT	8	8	2, 3 PCLK* ³
0008 C042h	PORT2	Data register	PORT	8	8	2, 3 PCLK* ³
0008 C043h	PORT3	Data register	PORT	8	8	2, 3 PCLK* ³
0008 C044h	PORT4	Data register	PORT	8	8	2, 3 PCLK* ³
0008 C045h	PORT5	Data register	PORT	8	8	2, 3 PCLK* ³
0008 C046h	PORT6	Data register	PORT	8	8	2, 3 PCLK* ³
0008 C047h	PORT7	Data register	PORT	8	8	2, 3 PCLK* ³
0008 C048h	PORT8	Data register	PORT	8	8	2, 3 PCLK* ³
0008 C049h	PORT9	Data register	PORT	8	8	2, 3 PCLK* ³
0008 C04Ah	PORTA	Data register	PORT	8	8	2, 3 PCLK* ³
0008 C04Bh	PORTB	Data register	PORT	8	8	2, 3 PCLK* ³
0008 C04Dh	PORTD	Data register	PORT	8	8	2, 3 PCLK* ³
0008 C04Eh	PORTE	Data register	PORT	8	8	2, 3 PCLK* ³
0008 C050h	PORTG	Port register	PORT* ¹	8	8	2, 3 PCLK* ³
0008 C061h	PORT1	Input buffer control register	ICR	8	8	2, 3 PCLK* ³
0008 C062h	PORT2	Input buffer control register	ICR	8	8	2, 3 PCLK* ³
0008 C063h	PORT3	Input buffer control register	ICR	8	8	2, 3 PCLK* ³
0008 C064h	PORT4	Input buffer control register	ICR	8	8	2, 3 PCLK* ³

Table 4.1 List of I/O Registers (Address Order) (17 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000C 123Ah	MTU	Timer interrupt skipping mode register A	TITMRA	8	8	5 ICLK
000C 123Bh	MTU	Timer interrupt skipping set register 2A	TITCR2A	8	8	5 ICLK
000C 123Ch	MTU	Timer interrupt skipping counter 2A	TITCNT2A	8	8	5 ICLK
000C 1240h	MTU4	Timer A/D converter start request control register	TADCR	16	16	5 ICLK
000C 1244h	MTU4	Timer A/D converter start request cycle set register A	TADCORA	16	16, 32	5 ICLK
000C 1246h	MTU4	Timer A/D converter start request cycle set register B	TADCORB	16	16	5 ICLK
000C 1248h	MTU4	Timer A/D converter start request cycle set buffer register A	TADCOBRA	16	16, 32	5 ICLK
000C 124Ah	MTU4	Timer A/D converter start request cycle set buffer register B	TADCOBRB	16	16	5 ICLK
000C 1260h	MTU	Timer waveform control register A	TWCRA	8	8	5 ICLK
000C 1270h	MTU3	Timer mode register 2A	TMDR2A	8	8	5 ICLK
000C 1272h	MTU3	Timer general register E	TGRE	16	16	5 ICLK
000C 1274h	MTU4	Timer general register E	TGRE	16	16	5 ICLK
000C 1276h	MTU4	Timer general register F	TGRF	16	16	5 ICLK
000C 1280h	MTU	Timer start register A	TSTRA	8	8, 16	5 ICLK
000C 1281h	MTU	Timer synchronous register A	TSYRA	8	8	5 ICLK
000C 1282h	MTU	Timer counter synchronous start register	TCSYSTR	8	8	5 ICLK
000C 1284h	MTU	Timer read/write enable register A	TRWERA	8	8	5 ICLK
000C 1300h	MTU0	Timer control register	TCR	8	8, 16, 32	5 ICLK
000C 1301h	MTU0	Timer mode register 1	TMDR1	8	8	5 ICLK
000C 1302h	MTU0	Timer I/O control register H	TIORH	8	8, 16	5 ICLK
000C 1303h	MTU0	Timer I/O control register L	TIORL	8	8	5 ICLK
000C 1304h	MTU0	Timer interrupt enable register	TIER	8	8, 16, 32	5 ICLK
000C 1305h	MTU0	Timer status register	TSR	8	8	5 ICLK
000C 1306h	MTU0	Timer counter	TCNT	16	16	5 ICLK
000C 1308h	MTU0	Timer general register A	TGRA	16	16, 32	5 ICLK
000C 130Ah	MTU0	Timer general register B	TGRB	16	16	5 ICLK
000C 130Ch	MTU0	Timer general register C	TGRC	16	16, 32	5 ICLK
000C 130Eh	MTU0	Timer general register D	TGRD	16	16	5 ICLK
000C 1320h	MTU0	Timer general register E	TGRE	16	16, 32	5 ICLK
000C 1322h	MTU0	Timer general register F	TGRF	16	16	5 ICLK
000C 1324h	MTU0	Timer interrupt enable register 2	TIER2	8	8, 16	5 ICLK
000C 1325h	MTU0	Timer status register 2	TSR2	8	8	5 ICLK
000C 1326h	MTU0	Timer buffer operation transfer mode register	TBTM	8	8	5 ICLK
000C 1380h	MTU1	Timer control register	TCR	8	8, 16	5 ICLK
000C 1381h	MTU1	Timer mode register 1	TMDR1	8	8	5 ICLK
000C 1382h	MTU1	Timer I/O control register	TIOR	8	8	5 ICLK
000C 1384h	MTU1	Timer interrupt enable register	TIER	8	8, 16, 32	5 ICLK
000C 1385h	MTU1	Timer status register	TSR	8	8	5 ICLK
000C 1386h	MTU1	Timer counter	TCNT	16	16	5 ICLK
000C 1388h	MTU1	Timer general register A	TGRA	16	16, 32	5 ICLK
000C 138Ah	MTU1	Timer general register B	TGRB	16	16	5 ICLK

Table 4.1 List of I/O Registers (Address Order) (19 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000C 1A39h	MTU7	Timer buffer operation transfer mode register	TBTM	8	8	5 ICLK
000C 1A3Ah	MTU	Timer interrupt skipping mode register B	TITMRB	8	8	5 ICLK
000C 1A3Bh	MTU	Timer interrupt skipping set register 2B	TITCR2B	8	8	5 ICLK
000C 1A3Ch	MTU	Timer interrupt skipping counter 2B	TITCNT2B	8	8	5 ICLK
000C 1A40h	MTU7	Timer A/D converter start request control register	TADCR	16	16	5 ICLK
000C 1A44h	MTU7	Timer A/D converter start request cycle set register A	TADCORA	16	16, 32	5 ICLK
000C 1A46h	MTU7	Timer A/D converter start request cycle set register B	TADCORB	16	16	5 ICLK
000C 1A48h	MTU7	Timer A/D converter start request cycle set buffer register A	TADCOBRA	16	16, 32	5 ICLK
000C 1A4Ah	MTU7	Timer A/D converter start request cycle set buffer register B	TADCOBRB	16	16	5 ICLK
000C 1A50h	MTU6	Timer synchronous clear register	TSYCR	8	8	5 ICLK
000C 1A60h	MTU	Timer waveform control register B	TWCRB	8	8	5 ICLK
000C 1A70h	MTU	Timer mode register 2B	TMDR2B	8	8	5 ICLK
000C 1A72h	MTU6	Timer general register E	TGRE	16	16	5 ICLK
000C 1A74h	MTU7	Timer general register E	TGRE	16	16	5 ICLK
000C 1A76h	MTU7	Timer general register F	TGRF	16	16	5 ICLK
000C 1A80h	MTU	Timer start register B	TSTRB	8	8, 16	5 ICLK
000C 1A81h	MTU	Timer synchronous register B	TSYRB	8	8	5 ICLK
000C 1A84h	MTU	Timer read/write enable register B	TRWERB	8	8	5 ICLK
000C 1C80h	MTU5	Timer counter U	TCNTU	16	16, 32	5 ICLK
000C 1C82h	MTU5	Timer general register U	TGRU	16	16	5 ICLK
000C 1C84h	MTU5	Timer control register U	TCRU	8	8	5 ICLK
000C 1C86h	MTU5	Timer I/O control register U	TIORU	8	8	5 ICLK
000C 1C90h	MTU5	Timer counter V	TCNTV	16	16, 32	5 ICLK
000C 1C92h	MTU5	Timer general register V	TGRV	16	16	5 ICLK
000C 1C94h	MTU5	Timer control register V	TCRV	8	8	5 ICLK
000C 1C96h	MTU5	Timer I/O control register V	TIORV	8	8	5 ICLK
000C 1CA0h	MTU5	Timer counter W	TCNTW	16	16, 32	5 ICLK
000C 1CA2h	MTU5	Timer general register W	TGRW	16	16	5 ICLK
000C 1CA4h	MTU5	Timer control register W	TCRW	8	8	5 ICLK
000C 1CA6h	MTU5	Timer I/O control register W	TIORW	8	8	5 ICLK
000C 1CB0h	MTU5	Timer status register	TSR	8	8	5 ICLK
000C 1CB2h	MTU5	Timer interrupt enable register	TIER	8	8	5 ICLK
000C 1CB4h	MTU5	Timer start register	TSTR	8	8	5 ICLK
000C 1CB6h	MTU5	Timer compare match clear register	TCNTCMPCLR	8	8	5 ICLK
000C 2000h	GPT	General PWM timer software start register	GTSTR	16	8, 16, 32	3 to 5 ICLK*4
000C 2004h	GPT	General PWM timer hardware source start control register	GTHSCR	16	8, 16, 32	3 to 5 ICLK*4
000C 2006h	GPT	General PWM timer hardware source clear control register	GTHCCR	16	8, 16, 32	3 to 5 ICLK*4
000C 2008h	GPT	General PWM timer hardware start source select register	GTHSSR	16	8, 16, 32	3 to 5 ICLK*4

Table 4.1 List of I/O Registers (Address Order) (23 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000C 222Ch	GPT2	A/D converter start request timing register B	GTADTRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 222Eh	GPT2	A/D converter start request timing buffer register B	GTADTBRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2230h	GPT2	A/D converter start request timing double-buffer register B	GTADTDBRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2234h	GPT2	General PWM timer output negate control register	GTONCR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2236h	GPT2	General PWM timer dead time control register	GTDTCR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2238h	GPT2	General PWM timer dead time value register	GTDVU	16	16, 32	3 to 5 ICLK ^{*4}
000C 223Ah	GPT2	General PWM timer dead time value register	GTDVD	16	16, 32	3 to 5 ICLK ^{*4}
000C 223Ch	GPT2	General PWM timer dead time buffer register	GTDBU	16	16, 32	3 to 5 ICLK ^{*4}
000C 223Eh	GPT2	General PWM timer dead time buffer register	GTDBD	16	16, 32	3 to 5 ICLK ^{*4}
000C 2240h	GPT2	General PWM timer output protection function status register	GTSOS	16	16, 32	3 to 5 ICLK ^{*4}
000C 2242h	GPT2	General PWM timer output protection temporary release register	GTSOTR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2280h	GPT3	General PWM timer I/O control register	GTIOR	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2282h	GPT3	General PWM timer interrupt output setting register	GTINTAD	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2284h	GPT3	General PWM timer control register	GTCR	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2286h	GPT3	General PWM timer buffer enable register	GTBER	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2288h	GPT3	General PWM timer count direction register	GTUDC	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 228Ah	GPT3	General PWM timer interrupt and A/D converter start request skipping setting register	GTITC	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 228Ch	GPT3	General PWM timer status register	GTST	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 228Eh	GPT3	General PWM timer counter	GTCNT	16	16	3 to 5 ICLK ^{*4}
000C 2290h	GPT3	General PWM timer compare capture register A	GTCCRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 2292h	GPT3	General PWM timer compare capture register B	GTCCRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2294h	GPT3	General PWM timer compare capture register C	GTCCRC	16	16, 32	3 to 5 ICLK ^{*4}
000C 2296h	GPT3	General PWM timer compare capture register D	GTCCRD	16	16, 32	3 to 5 ICLK ^{*4}
000C 2298h	GPT3	General PWM timer compare capture register E	GTCCRE	16	16, 32	3 to 5 ICLK ^{*4}
000C 229Ah	GPT3	General PWM timer compare capture register F	GTCCRF	16	16, 32	3 to 5 ICLK ^{*4}
000C 229Ch	GPT3	General PWM timer cycle setting register	GTPR	16	16, 32	3 to 5 ICLK ^{*4}
000C 229Eh	GPT3	General PWM timer cycle setting buffer register	GTPBR	16	16, 32	3 to 5 ICLK ^{*4}
000C 22A0h	GPT3	General PWM timer cycle setting double-buffer register	GTPDBR	16	16, 32	3 to 5 ICLK ^{*4}
000C 22A4h	GPT3	A/D converter start request timing register A	GTADTRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 22A6h	GPT3	A/D converter start request timing buffer register A	GTADTBRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 22A8h	GPT3	A/D converter start request timing double-buffer register A	GTADTDBRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 22ACh	GPT3	A/D converter start request timing register B	GTADTRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 22AEh	GPT3	A/D converter start request timing buffer register B	GTADTBRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 22B0h	GPT3	A/D converter start request timing double-buffer register B	GTADTDBRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 22B4h	GPT3	General PWM timer output negate control register	GTONCR	16	16, 32	3 to 5 ICLK ^{*4}

Table 4.2 List of I/O Registers (Bit Order) (11 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
SCI1	SEMR	—	—	NFEN	ABCS	—	—	—	—
SMC11	SMR	GM	BLK	PE	PM	(BCP[1:0])			CKS[1:0]
SMC11	BRR								
SMC11	SCR	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
SMC11	TDR								
SMC11	SSR	TDRE	RDRF	ORER	ERS	PER	TEND	MPB	MPBT
SMC11	RDR								
SMC11	SCMR	BCP2	—	—	—	SDIR	SINV	—	SMIF
SCI2	SMR	CM	CHR	PE	PM	STOP	MP	CKS[1:0]	
SCI2	BRR								
SCI2	SCR	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
SCI2	TDR								
SCI2	SSR	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
SCI2	RDR								
SCI2	SCMR	BCP2	—	—	—	SDIR	SINV	—	SMIF
SMC12	SMR	GM	BLK	PE	PM	(BCP[1:0])			CKS[1:0]
SMC12	BRR								
SMC12	SCR	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
SMC12	TDR								
SMC12	SSR	TDRE	RDRF	ORER	ERS	PER	TEND	MPB	MPBT
SMC12	RDR								
SMC12	SCMR	BCP2	—	—	—	SDIR	SINV	—	SMIF
CRC	CRCCR	DORCLR	—	—	—	—	LMS	GPS[1:0]	
CRC	CRCDIR								
CRC	CRCDOR								
RIIC0	ICCR1	ICE	IICRST	CLO	SOWP	SCLO	SDAO	SCLI	SDAI
RIIC0	ICCR2	BBSY	MST	TRS	—	SP	RS	ST	—
RIIC0	ICMR1	MTWP		CKS[2:0]		BCWP		BC[2:0]	
RIIC0	ICMR2	DLCS		SDDL[2:0]		TMWE	TMOH	TMOL	TMOS
RIIC0	ICMR3	SMBS	WAIT	RDRFS	ACKWP	ACKBT	ACKBR	NF[1:0]	
RIIC0	ICFER	—	SCLE	NFE	NACKE	SALE	NALE	MALE	TMOE
RIIC0	ICSER	HOAE	—	DIDE	—	GCAE	SAR2E	SAR1E	SAR0E
RIIC0	ICIER	TIE	TEIE	RIE	NAKIE	SPIE	STIE	ALIE	TMOIE
RIIC0	ICSR1	HOA	—	DID	—	GCA	AAS2	AAS1	AAS0
RIIC0	ICSR2	TDRE	TEND	RDRF	NACKF	STOP	START	AL	TMOF
RIIC0	SARL0				SVA[6:0]				SVA0
RIIC0	TMOCTL								
RIIC0	SARU0	—	—	—	—	—	SVA[1:0]		FS
RIIC0	TMOCNTU								
RIIC0	SARL1				SVA[6:0]				SVA0
RIIC0	SARU1	—	—	—	—	—	SVA[1:0]		FS
RIIC0	SARL2				SVA[6:0]				SVA0
RIIC0	SARU2	—	—	—	—	—	SVA[1:0]		FS
RIIC0	ICBRL	—	—	—			BRL[4:0]		
RIIC0	ICBRH	—	—	—			BRH[4:0]		
RIIC0	ICDRT								
RIIC0	ICDRR								
RSP10	SPCR	SPRIE	SPE	SPTIE	SPEIE	MSTR	MODFEN	TXMD	SPMS

Table 4.2 List of I/O Registers (Bit Order) (14 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
PORT8	DR	—	—	—	—	—	B2	B1	B0
PORT9	DR	—	B6	B5	B4	B3	B2	B1	B0
PORTA	DR	—	—	B5	B4	B3	B2	B1	B0
PORTB	DR	B7	B6	B5	B4	B3	B2	B1	B0
PORTD	DR	B7	B6	B5	B4	B3	B2	B1	B0
PORTE	DR	—	—	B5	B4	B3	—	B1	B0
PORTG	DR	—	—	B5	B4	B3	B2	B1	B0
PORT1	PORT	—	—	—	—	—	—	B1	B0
PORT2	PORT	—	—	—	B4	B3	B2	B1	B0
PORT3	PORT	—	—	—	—	B3	B2	B1	B0
PORT4	PORT	B7	B6	B5	B4	B3	B2	B1	B0
PORT5	PORT	—	—	B5	B4	B3	B2	B1	B0
PORT6	PORT	—	—	B5	B4	B3	B2	B1	B0
PORT7	PORT	—	B6	B5	B4	B3	B2	B1	B0
PORT8	PORT	—	—	—	—	—	B2	B1	B0
PORT9	PORT	—	B6	B5	B4	B3	B2	B1	B0
PORTA	PORT	—	—	B5	B4	B3	B2	B1	B0
PORTB	PORT	B7	B6	B5	B4	B3	B2	B1	B0
PORTD	PORT	B7	B6	B5	B4	B3	B2	B1	B0
PORTE	PORT	—	—	B5	B4	B3	B2	B1	B0
PORTG	PORT	—	—	B5	B4	B3	B2	B1	B0
PORT1	ICR	—	—	—	—	—	—	B1	B0
PORT2	ICR	—	—	—	B4	B3	B2	B1	B0
PORT3	ICR	—	—	—	—	B3	B2	B1	B0
PORT4	ICR	B7	B6	B5	B4	B3	B2	B1	B0
PORT5	ICR	—	—	B5	B4	B3	B2	B1	B0
PORT6	ICR	—	—	B5	B4	B3	B2	B1	B0
PORT7	ICR	—	B6	B5	B4	B3	B2	B1	B0
PORT8	ICR	—	—	—	—	—	B2	B1	B0
PORT9	ICR	—	B6	B5	B4	B3	B2	B1	B0
PORTA	ICR	—	—	B5	B4	B3	B2	B1	B0
PORTB	ICR	B7	B6	B5	B4	B3	B2	B1	B0
PORTD	ICR	B7	B6	B5	B4	B3	B2	B1	B0
PORTE	ICR	—	—	B5	B4	B3	—	B1	B0
PORTG	ICR	—	—	B5	B4	B3	B2	B1	B0
IOPORT	PF8IRQ	—	—	—	—	ITS1[1:0]		ITS0[1:0]	
IOPORT	PF9IRQ	—	—	—	—	—	ITS2	—	—
IOPORT	PFAADC	—	—	—	—	—	—	ADTRG1S	ADTRG0S
IOPORT	PFCMTU	TCLKS[1:0]		—	—	—	—	MTUS1	MTUS0
IOPORT	PFDGPT	—	—	—	—	—	—	—	GPTS
IOPORT	PPFSCI	—	—	—	—	—	SCI2S	—	—
IOPORT	PFGSPI	SSL3E	SSL2E	SSL1E	SSL0E	MISOE	MOSIE	RSPCKE	—
IOPORT	PFHSPI	—	—	—	—	—	—	RSPIS[1:0]	
IOPORT	PFJCAN	CANS[1:0]		—	—	—	—	—	CANE
IOPORT	PFKLIN	—	—	—	—	—	—	—	LINE
IOPORT	PFMPOE	—	—	—	POE11E	POE10E	POE8E	POE4E	POE0E
IOPORT	PFNPOE	POE10S	—	—	—	—	—	—	—
SYSTEM	DPSBYCR	DPSBY	IOKEEP	—	—	—	—	—	—
SYSTEM	DPSWCR	—	—	—	—	WTSTS[5:0]		—	—
SYSTEM	DPSIER	DNMIE	—	—	DLVDE	—	—	DIRQ1E	DIRQ0E

Table 4.2 List of I/O Registers (Bit Order) (15 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
SYSTEM	DPSIFR	DNMIF	—	—	DLVDF	—	—	DIRQ1F	DIRQ0F
SYSTEM	DPSIEGR	DNMIEG	—	—	—	—	—	DIRQ1EG	DIRQ0EG
SYSTEM	RSTSR	DPSRSTF	—	—	—	—	LVD2F	LVD1F	PORF
FLASH	FWEPROR	—	—	—	—	—	—	FLWE[1:0]	
SYSTEM	LVDKEYR	KEY[7:0]							
SYSTEM	LVDCR	LVD2E	LVD2RI	—	—	LVD1E	LVD1RI	—	—
SYSTEM	DPSBKR0								
SYSTEM	DPSBKR1								
SYSTEM	DPSBKR2								
SYSTEM	DPSBKR3								
SYSTEM	DPSBKR4								
SYSTEM	DPSBKR5								
SYSTEM	DPSBKR6								
SYSTEM	DPSBKR7								
SYSTEM	DPSBKR8								
SYSTEM	DPSBKR9								
SYSTEM	DPSBKR10								
SYSTEM	DPSBKR11								
SYSTEM	DPSBKR12								
SYSTEM	DPSBKR13								
SYSTEM	DPSBKR14								
SYSTEM	DPSBKR15								
SYSTEM	DPSBKR16								
SYSTEM	DPSBKR17								
SYSTEM	DPSBKR18								
SYSTEM	DPSBKR19								
SYSTEM	DPSBKR20								
SYSTEM	DPSBKR21								
SYSTEM	DPSBKR22								
SYSTEM	DPSBKR23								
SYSTEM	DPSBKR24								
SYSTEM	DPSBKR25								
SYSTEM	DPSBKR26								
SYSTEM	DPSBKR27								
SYSTEM	DPSBKR28								
SYSTEM	DPSBKR29								
SYSTEM	DPSBKR30								
SYSTEM	DPSBKR31								
POE	ICSR1	—	—	—	POE0F	—	—	—	PIE1
		—	—	—	—	—	—	POE0M[1:0]	
POE	OCSR1	OSF1	—	—	—	—	—	OCE1	OIE1
		—	—	—	—	—	—	—	—
POE	ICSR2	—	—	—	POE4F	—	—	—	PIE2
		—	—	—	—	—	—	POE4M[1:0]	
POE	OCSR2	OSF2	—	—	—	—	—	OCE2	OIE2
		—	—	—	—	—	—	—	—
POE	ICSR3	—	—	—	POE8F	—	—	POE8E	PIE3
		—	—	—	—	—	—	POE8M[1:0]	
POE	SPOER	—	—	—	GPT23HIZ	GPT01HIZ	MTUCH0HIZ	MTUCH67HIZ	MTUCH34HIZ
POE	POECR1	—	—	—	—	MTU0DZE	MTU0CZE	MTU0BZE	MTU0AZE

Table 4.2 List of I/O Registers (Bit Order) (21 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
MTU7	TIORL	IOD[3:0]				IOC[3:0]			
MTU6	TIER	TTEG	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA
MTU7	TIER	TTEG	TTEG2	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA
MTU	TOERB	—	—	OE7D	OE7C	OE6D	OE7B	OE7A	OE6B
MTU	TOCR1B	—	PSYE	—	—	TOCL	TOCS	OLSN	OLSP
MTU6	TCNT								
MTU7	TCNT								
MTU	TCDRB								
MTU	TDDRB								
MTU6	TGRA								
MTU6	TGRB								
MTU7	TGRA								
MTU7	TGRB								
MTU	TCNTSB								
MTU	TCBRB								
MTU6	TGRC								
MTU6	TGRD								
MTU7	TGRC								
MTU7	TGRD								
MTU6	TSR	TCFD	—	—	TCFV	TGFD	TGFC	TGFB	TGFA
MTU7	TSR	TCFD	—	—	TCFV	TGFD	TGFC	TGFB	TGFA
MTU	TITCR1B	T6AEN	T6ACOR[2:0]			T7VEN	T7VCOR[2:0]		
MTU	TITCNT1B	—	T6ACNT[2:0]			—	T7VCNT[2:0]		
MTU	TBTERB	—	—	—	—	—	—	BTE[1:0]	—
MTU	TDERB	—	—	—	—	—	—	—	TDER
MTU	TOLBRB	—	—	OLS3N	OLS3P	OLS2N	OLS2P	OLS1N	OLS1P
MTU6	TBTM	—	—	—	—	—	—	TTSB	TTSA
MTU7	TBTM	—	—	—	—	—	—	TTSB	TTSA
MTU	TITMRB	—	—	—	—	—	—	—	TITM
MTU	TITCR2B	—	—	—	—	—	TRGCR[2:0]		
MTU	TITCNT2B	—	—	—	—	—	TRG7CNT[2:0]		
MTU7	TADCR	BF[1:0]		—	—	—	—	—	—
		UT7AE	DT7AE	UT7BE	DT7BE	ITA6AE	ITA7VE	ITB6AE	ITB7VE
MTU7	TADCORA								
MTU7	TADCORB								
MTU7	TADCOBRA								

Table 4.2 List of I/O Registers (Bit Order) (30 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
FLASH	FSTATR0	FRDY	ILGLERR	ERSERR	PRGERR	SUSRDY	—	ERSSPD	PRGSPD
FLASH	FSTATR1	FCUERR	—	—	FLOCKST	—	—	—	—
FLASH	FENTRYR	FEKEY[7:0]							
		FENTRYD	—	—	—	—	—	—	FENTRY0
FLASH	FPROTR	FPKEY[7:0]							
		—	—	—	—	—	—	—	FPROTCN
FLASH	FRESETR	FRKEY[7:0]							
		—	—	—	—	—	—	—	FRESET
FLASH	FCMDR	CMDR[7:0]							
		PCMDR[7:0]							
FLASH	FCPSR	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	ESUSPMD
FLASH	DFLBCCNT	BCADR[7:0]							
		BCADR[7:0]							
FLASH	FPESTAT	—	—	—	—	—	—	—	—
		PEERRST[7:0]							
FLASH	DFLBCSTAT	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	BCST
FLASH	PCKAR	—	—	—	—	—	—	—	—
		PCKA[7:0]							

Note: • In this, the I/O port related registers (0008 C001h to 0008 C116h) indicate the bit configuration of the 112-pin LQFP version. As the configuration of registers and bits differs depending on a package, see section 14, I/O Ports, for details in the User's manual: Hardware.

Note 1. This shows the bit configuration when ADDPR.DPSEL = 0 and ADDPR.DPPRC = 0 (The value has 10-bit accuracy and is padded at the LSB end).

Note 2. This shows the bit configuration when ADCER.ADRFMT = 0 (aligned to the LSB end) and ADCER.ADPRC[1:0] = 00b. For details, refer to section 28, 12-Bit A/D Converter (S12ADA) in the User's manual: Hardware.

Note 3. This function is not supported by the product without the CAN function.

Table 5.11 Timing of On-Chip Peripheral Modules (3)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item			Symbol	Min.	Max.	Unit	Test Conditions	
RSPI	RSPCK clock cycle	Master	t _{SPcyc}	4	4096	t _{Pcyc}	Figure 5.11	
		Slave		8	4096			
	RSPCK clock high pulse width	Master	t _{SPCKWH}	(t _{Sp_{cyc}} - t _{SPCKR} - t _{SPCKF}) / 2-3	-	ns		
		Slave		(t _{Sp_{cyc}} - t _{SPCKR} - t _{SPCKF}) / 2	-			
	RSPCK clock low pulse width	Master	t _{SPCKWL}	(t _{Sp_{cyc}} - t _{SPCKR} - t _{SPCKF}) / 2-3	-	ns		
		Slave		(t _{Sp_{cyc}} - t _{SPCKR} - t _{SPCKF}) / 2	-			
	RSPCK clock rise/fall time	Output	t _{SPCKR}	-	5	ns		
		Input	t _{SPCKF}	-	1	μs		
	Data input setup time	Master	t _{SU}	25	-	ns	Figure 5.12 to Figure 5.15	
		Slave		0	-			
	Data input hold time	Master	t _H	0	-	ns		
		Slave		20+2×t _{Pcyc}	-			
	SSL setup time	Master	t _{LEAD}	1	8	t _{SPcyc}		
		Slave		4	-	t _{Pcyc}		
	SSL hold time	Master	t _{LAG}	1	8	t _{SPcyc}		
		Slave		4	-	t _{Pcyc}		
	Data output delay time	Master	t _{OD}	-	20	ns		
		Slave		-	3×t _{Pcyc} +40			
	Data output hold time	Master	t _{OH}	0	-	ns		
		Slave		0	-			
	Successive transmission delay time	Master	t _{TD}	t _{SPcyc} +2×t _{Pcyc}	8×t _{SPcyc} +2×t _{Pcyc}	ns		
		Slave		4×t _{Pcyc}	-			
	MOSI, MISO rise/fall time	Output	t _{DR}	-	15	ns	Figure 5.12 to Figure 5.15	
		Input	t _{DF}	-	1	μs		
	SSL rise/fall time	Output	t _{SSLR}	-	15	ns		
		Input	t _{SSLF}	-	1	μs		
	Slave access time			t _{SA}	-	4	t _{Pcyc}	Figure 5.12 to Figure 5.15
	Slave output release time			t _{REL}	-	3	t _{Pcyc}	

Note: • Note 1: t_{PCyc} : PCLK cycle

Table 5.17 Characteristics of the Programmable Gain Amplifier

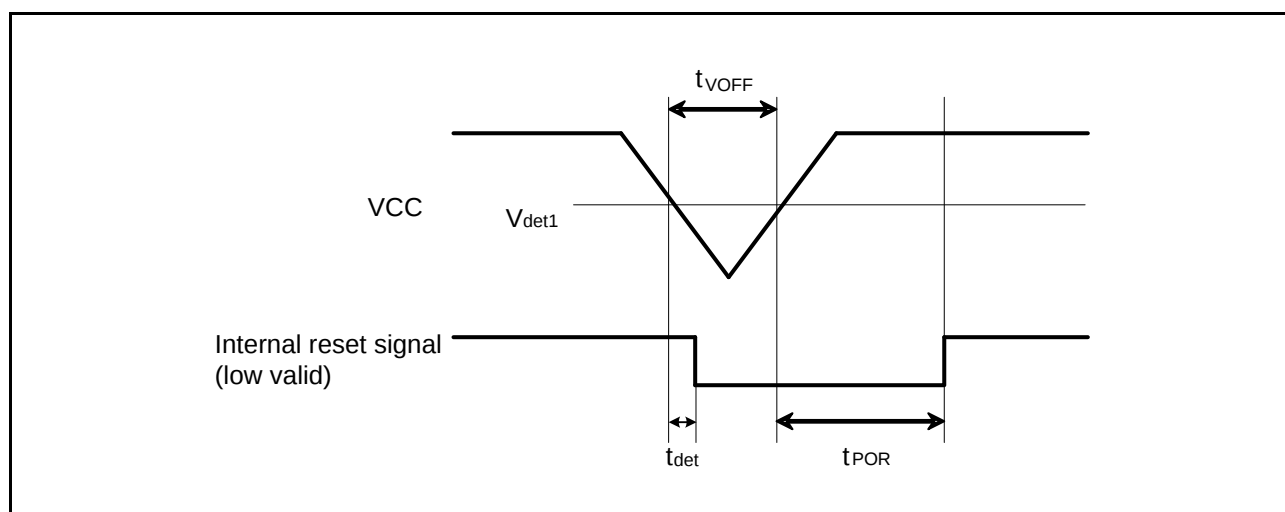
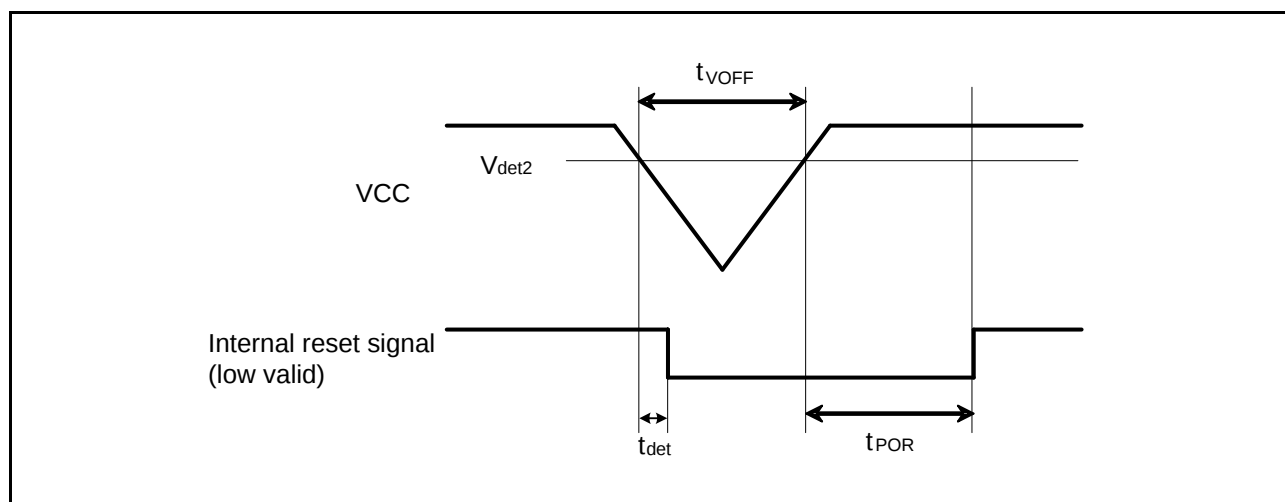
Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog input capacitance		Cin	-	-	6	pF	
Input offset voltage		Voff	-	-	8	mV	
Input voltage range (Vin)	Gain × 2.000	Vin	0.050 × AVcc	-	0.450 × AVcc	V	
	Gain × 2.500		0.047 × AVcc	-	0.360 × AVcc		
	Gain × 3.077		0.045 × AVcc	-	0.292 × AVcc		
	Gain × 3.636		0.042 × AVcc	-	0.247 × AVcc		
	Gain × 4.000		0.040 × AVcc	-	0.212 × AVcc		
	Gain × 4.444		0.036 × AVcc	-	0.191 × AVcc		
	Gain × 5.000		0.033 × AVcc	-	0.170 × AVcc		
	Gain × 5.714		0.031 × AVcc	-	0.148 × AVcc		
	Gain × 6.667		0.029 × AVcc	-	0.127 × AVcc		
	Gain × 10.000		0.025 × AVcc	-	0.08 × AVcc		
	Gain × 13.333		0.023 × AVcc	-	0.06 × AVcc		
Slew rate		SR	10	-	-	V/μs	
Gain error	Gain × 2.000	-	-	-	1	%	
	Gain × 2.500		-	-	1		
	Gain × 3.077		-	-	1		
	Gain × 3.636		-	-	1.5		
	Gain × 4.000		-	-	1.5		
	Gain × 4.444		-	-	2		
	Gain × 5.000		-	-	2		
	Gain × 5.714		-	-	2		
	Gain × 6.667		-	-	3		
	Gain × 10.000		-	-	4		
	Gain × 13.333		-	-	4		

**Figure 5.21** Voltage Detection Circuit Timing (Vdet1)**Figure 5.22** Voltage Detection Circuit Timing (Vdet2)

REVISION HISTORY	RX62T Group, RX62G Group Datasheet
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Rev.	Date	Description	
		Page	Summary
1.00	Apr 20, 2011	—	First edition issued
1.30	May 22, 2013	1	Features, Package lineup, added
		2	1. Overview
		3	Table 1.1 Outline of Specifications (1/5) Description of CPU, added
		6	Table 1.1 Outline of Specifications (2/5) Description of Programmable I/O ports, changed
		7	Table 1.1 Outline of Specifications (5/5), 64-pin packaged, added
		8	Table 1.2 Functions of RX62T Group Products, 64-pin package, and MTU3/GPT complementary PWM pins added
		9	Table 1.3 List of Products, 64-pin package part number, changed
		9	Figure 1.1 How to Read the Product Part No., 64-pin package part number, changed
		10	Figure 1.1 How to Read the Product Part No., 5-V version, two-motor control supported, added
		10	Figure 1.2 Block Diagram, changed
		14	Figure 1.6 Pin Assignment of the 80-Pin LQFP (Two-motor Control Supported), added
		15	Figure 1.7 Pin Assignment of the 64-Pin LQFP, Figure PLQP0064GA-A, added
		25 to 27	Table 1.7 List of Pins and Pin Functions (80-Pin LQFP: R5F562TxGDFF) , added
		30 to 33	Table 1.9 Pin Functions, changed
		38to 61	4. I/O Register
		47	Table 4.1 List of I/O Registers (Address Order), MPU, added
		57	Table 4.1 List of I/O Registers (Address Order) TMOCNTL, TMOCNTU register, added
		62	Table 4.1 List of I/O Registers (Address Order), GTSWP register, added
		62	5. Electrical Characteristics
		64	Table 5.1 Absolute Maximum Ratings, note changed
		66	Table 5.2 DC Characteristics (1) (2/3) Test Conditions of P90 to P95, changed
		67	Table 5.3 DC Characteristics (2), note changed
		72	Table 5.4 Permissible Output Currents, note changed
		73	Table 5.7 Control Signal Timing, notes changed
		73	Table 5.8 Timing of On-Chip Peripheral Modules (1), changed
		96	Appendix 1.Package Dimensions
		96	FigureE 64-PinLQFP (PLQP0064GA-A), added
2.00	Jan 10, 2014	1	Features, changed
		2 to 6	1. Overview
		7, 8	Table 1.1 Outline of Specifications, changed; Note 1, added
		9, 10	Table 1.2 Functions of RX62T Group and RX62G Group Products, changed
		11	Table 1.3 List of Products, changed; Note 1, added
		15	Figure 1.1 How to Read the Product Part No., changed
		27 to 29	Figure 1.6 Pin Assignment of the 80-Pin LQFP (Two-Motor Control Supported Version), added
		27 to 29	Table 1.7 List of Pins and Pin Functions (80-Pin LQFP: R5F562TxGDFF), added
		43 to 67	4. I/O Registers
		68 to 97	Table 4.1 List of I/O Registers (Address Order), changed
		68 to 97	Table 4.2 List of I/O Registers (Bit Order), changed
		—	5. Electrical Characteristics
		—	Conditions in the table, change to Ta = -40 to +105°C from Ta = -40 to +85°C.

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

- The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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