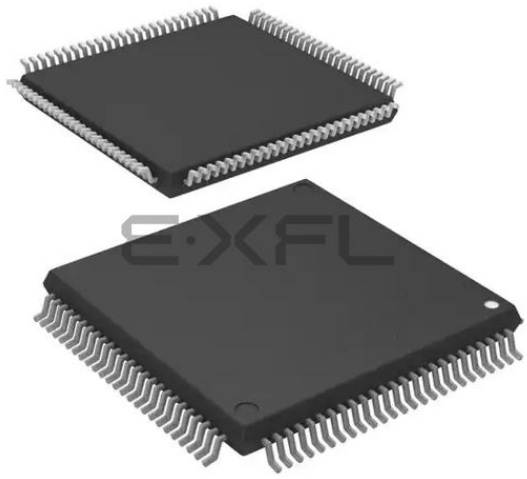
Renesas Electronics America Inc - R5F562GAADFP#V1 Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 12x10b, 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562gaadfp-v1

Table 1.2 Functions of RX62T Group and RX62G Group Products (1 / 2)

Functions		RX62G Group		RX62T Group				
Pin number		112 Pins	100 Pins	112 Pins	100 Pins	80 Pins (R5F562TxGDFF)	80 Pins	64 Pins
Data transfer	Data transfer controller (DTC)	√						
Interrupt controller (ICU)	Input on the NMI pin	√						
	Input on the IRQ pins	√ (8)						√ (4)
Timers	Multi-function timer pulse unit 3 (MTU3)	√				√*1		
	General PWM timer (GPT)	—		√		√*1		
	General PWM timer (GPTa)	√		—				
	MTU3/GPT complementary PWM pin	12					6	
	Port output enable 3 (POE3)	√ (POE pins: 5)						√ (POE pins: 3)
	Compare match timer (CMT)	√						
	Watchdog timer (WDT)	√						
	Independent watchdog timer (IWDT)	√						
Communication function	Serial communications interface (SCI)	√						
	I²C bus interface (RIIC)	√						
	CAN module (CAN) (as an optional function)	√						
	LIN module (LIN)	√						
	Serial peripheral interface (RSPI)	√						
12-bit A/D converter (S12ADA)		√ (4 ch. x 2 units)						
	Simultaneous sampling on three channels	√ (2 units)						
	Programmable gain amplifier	√ (3 ch. x 2 units)						
	Window comparator	√ (3 ch. x 2 units)						
10-bit A/D converter (ADA)		√ (12 ch.)				√ (4 ch.)		—
CRC calculator (CRC)		√						
I/O ports	I/O pins	61	55	61	55	44	44	37
	Input pins	21	21	21	21	13	13	9

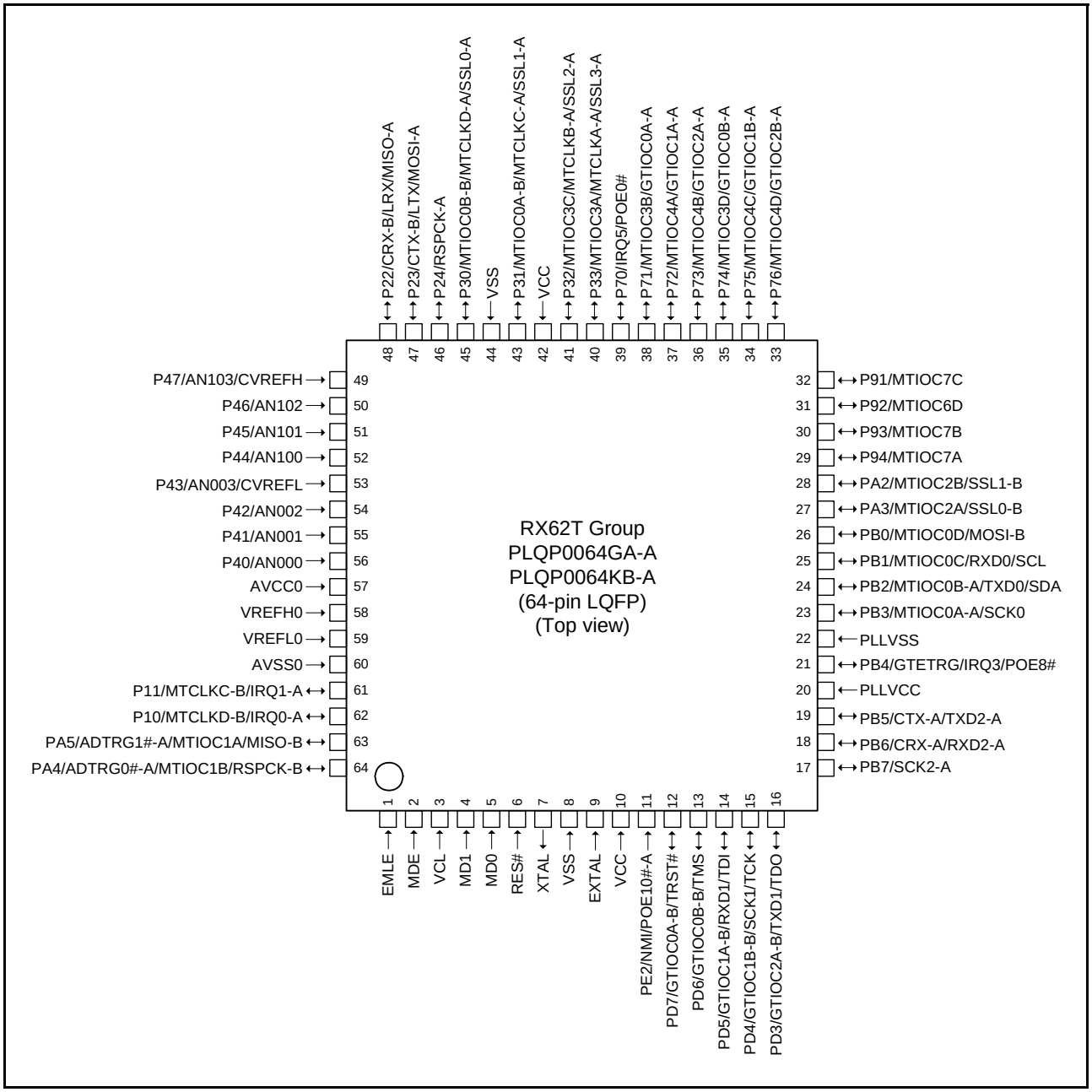


Figure 1.7 Pin Assignment of the 64-Pin LQFP

Table 1.4 List of Pins and Pin Functions (112-Pin LQFP) (1 / 3)

Pin No. (112-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi-cation	Interrupt	POE	Debugging
1		PE5				IRQ0-B		
2	EMLE							
3	VSS							
4	MDE							
5	VCL							
6	MD1							
7	MD0							
8		PE4		MTCLKC-C		IRQ1-B	POE10#-B	
9		PE3		MTCLKD-C		IRQ2-A	POE11#	
10	RES#							
11	XTAL							
12	VSS							
13	EXTAL							
14	VCC							
15		PE2				NMI	POE10#-A	
16		PE1			SSL3-C			
17		PE0			CRX-C/ SSL2-C			
18		PD7		GTIOC0A-B	CTX-C/ SSL1-C			
19		PD6		GTIOC0B-B	SSL0-C			
20		PD5		GTIOC1A-B	RXD1			
21		PD4		GTIOC1B-B	SCK1			
22		PD3		GTIOC2A-B	TXD1			
23		PD2		GTIOC2B-B	MOSI-C			
24		PD1		GTIOC3A	MISO-C			
25		PD0		GTIOC3B	RSPCK-C			
26								TDI
27								TCK
28								TDO
29		PB7			SCK2-A			
30		PB6			CRX-A/ RXD2-A			
31		PB5			CTX-A/ TXD2-A			
32	PLLVCC							
33		PB4		GTETRG		IRQ3	POE8#	
34	PLLVSS							
35		PB3		MTIOC0A-A	SCK0			
36		PB2		MTIOC0B-A	TXD0/SDA			
37		PB1		MTIOC0C	RXD0/SCL			
38		PB0		MTIOC0D	MOSI-B			
39		PA5	ADTRG1#-A	MTIOC1A	MISO-B			
40		PA4	ADTRG0#-A	MTIOC1B	RSPCK-B			
41		PA3		MTIOC2A	SSL0-B			
42		PA2		MTIOC2B	SSL1-B			
43		PA1		MTIOC6A	SSL2-B			

Table 1.4 List of Pins and Pin Functions (112-Pin LQFP) (2 / 3)

Pin No. (112-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi-cation	Interrupt	POE	Debugging
44		PA0		MTIOC6C	SSL3-B			
45	VCC							
46		P96				IRQ4	POE4#	
47	VSS							
48		P95		MTIOC6B				
49		P94		MTIOC7A				
50		P93		MTIOC7B				
51		P92		MTIOC6D				
52		P91		MTIOC7C				
53		P90		MTIOC7D				
54		PG5						TRCLK
55		PG4						TRDATA3
56		PG3						TRDATA2
57		PG2				IRQ2-B		TRDATA1
58		PG1				IRQ1-C		TRDATA0
59		PG0				IRQ0-C		TRSYNC
60		P76		MTIOC4D/ GTIOC2B-A				
61		P75		MTIOC4C/ GTIOC1B-A				
62		P74		MTIOC3D/ GTIOC0B-A				
63		P73		MTIOC4B/ GTIOC2A-A				
64		P72		MTIOC4A/ GTIOC1A-A				
65		P71		MTIOC3B/ GTIOC0A-A				
66		P70				IRQ5	POE0#	
67		P33		MTIOC3A/ MTCLKA-A	SSL3-A			
68		P32		MTIOC3C/ MTCLKB-A	SSL2-A			
69	VCC							
70		P31		MTIOC0A-B/ MTCLKC-A	SSL1-A			
71	VSS							
72		P30		MTIOC0B-B/ MTCLKD-A	SSL0-A			
73		P24			RSPCK-A			
74		P23			CTX-B/ LTX/ MOSI-A			
75		P22	ADTRG#		CRX-B/ LRX/ MISO-A			
76		P21	ADTRG1#-B	MTCLKA-B		IRQ6		
77		P20	ADTRG0#-B	MTCLKB-B		IRQ7		
78		P65	AN5					
79		P64	AN4					

Table 1.7 List of Pins and Pin Functions (80-Pin LQFP: R5F562TxGDFF) (3 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communication	Interrupt	POE	Debugging
76	AVSS0							
77		P82		MTIC5U	SCK2-B			
78		P81		MTIC5V	TXD2-B			
79		P80		MTIC5W	RXD2-B			
80		P10		MTCLKD-B		IRQ0-A		

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 0000h	SYSTEM	Mode monitor register	MDMONR	16	16	3 ICLK
0008 0002h	SYSTEM	Mode status register	MDSR	16	16	3 ICLK
0008 0006h	SYSTEM	System control register 0	SYSCR0	16	16	3 ICLK
0008 0008h	SYSTEM	System control register 1	SYSCR1	16	16	3 ICLK
0008 000Ch	SYSTEM	Standby control register	SBYCR	16	16	3 ICLK
0008 0010h	SYSTEM	Module stop control register A	MSTPCRA	32	32	3 ICLK
0008 0014h	SYSTEM	Module stop control register B	MSTPCRB	32	32	3 ICLK
0008 0018h	SYSTEM	Module stop control register C	MSTPCRC	32	32	3 ICLK
0008 0020h	SYSTEM	System clock control register	SCKCR	32	32	3 ICLK
0008 0040h	SYSTEM	Oscillation stop detection control register	OSTDCR	16	16	3 ICLK
0008 1300h	BSC	Bus error status clear register	BERCLR	8	8	2 ICLK
0008 1304h	BSC	Bus error monitoring enable register	BEREN	8	8	2 ICLK
0008 1308h	BSC	Bus error status register 1	BERSR1	8	8	2 ICLK
0008 130Ah	BSC	Bus error status register 2	BERSR2	16	16	2 ICLK
0008 2400h	DTC	DTC control register	DTCCR	8	8	2 ICLK
0008 2404h	DTC	DTC vector base register	DTCVBR	32	32	2 ICLK
0008 2408h	DTC	DTC address mode register	DTCADMOD	8	8	2 ICLK
0008 240Ch	DTC	DTC module start register	DTCST	8	8	2 ICLK
0008 240Eh	DTC	DTC status register	DTCSTS	16	16	2 ICLK
0008 6400h	MPU	Region 0 start page-number register	RSPAGE0	32	32	1 ICLK
0008 6404h	MPU	Region 0 end page-number register	REPAGE0	32	32	1 ICLK
0008 6408h	MPU	Region 1 start page-number register	RSPAGE1	32	32	1 ICLK
0008 640Ch	MPU	Region 1 end page-number register	REPAGE1	32	32	1 ICLK
0008 6410h	MPU	Region 2 start page-number register	RSPAGE2	32	32	1 ICLK
0008 6414h	MPU	Region 2 end page-number register	REPAGE2	32	32	1 ICLK
0008 6418h	MPU	Region 3 start page-number register	RSPAGE3	32	32	1 ICLK
0008 641Ch	MPU	Region 3 end page-number register	REPAGE3	32	32	1 ICLK
0008 6420h	MPU	Region 4 start page-number register	RSPAGE4	32	32	1 ICLK
0008 6424h	MPU	Region 4 end page-number register	REPAGE4	32	32	1 ICLK
0008 6428h	MPU	Region 5 start page-number register	RSPAGE5	32	32	1 ICLK
0008 642Ch	MPU	Region 5 end page-number register	REPAGE5	32	32	1 ICLK
0008 6430h	MPU	Region 6 start page-number register	RSPAGE6	32	32	1 ICLK
0008 6434h	MPU	Region 6 end page-number register	REPAGE6	32	32	1 ICLK
0008 6438h	MPU	Region 7 start page-number register	RSPAGE7	32	32	1 ICLK
0008 643Ch	MPU	Region 7 end page-number register	REPAGE7	32	32	1 ICLK
0008 6500h	MPU	Memory-protection enable register	MPEN	32	32	1 ICLK
0008 6504h	MPU	Background access control register	MPBAC	32	32	1 ICLK
0008 6508h	MPU	Memory-protection error status-clearing register	MPECLR	32	32	1 ICLK
0008 650Ch	MPU	Memory-protection error status register	MPESTS	32	32	1 ICLK
0008 6514h	MPU	Data memory-protection error address register	MPDEA	32	32	1 ICLK
0008 6520h	MPU	Region search address register	MPSA	32	32	1 ICLK
0008 6524h	MPU	Region search operation register	MPOPS	16	16	1 ICLK

Table 4.1 List of I/O Registers (Address Order) (8 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 7382h	ICU	Interrupt source priority register 82	IPR82	8	8	2 ICLK
0008 7388h	ICU	Interrupt source priority register 88	IPR88	8	8	2 ICLK
0008 7389h	ICU	Interrupt source priority register 89	IPR89	8	8	2 ICLK
0008 738Ah	ICU	Interrupt source priority register 8A	IPR8A	8	8	2 ICLK
0008 738Bh	ICU	Interrupt source priority register 8B	IPR8B	8	8	2 ICLK
0008 7390h	ICU	Interrupt source priority register 90	IPR90	8	8	2 ICLK
0008 7500h	ICU	IRQ control register 0	IRQCR0	8	8	2 ICLK
0008 7501h	ICU	IRQ control register 1	IRQCR1	8	8	2 ICLK
0008 7502h	ICU	IRQ control register 2	IRQCR2	8	8	2 ICLK
0008 7503h	ICU	IRQ control register 3	IRQCR3	8	8	2 ICLK
0008 7504h	ICU	IRQ control register 4	IRQCR4	8	8	2 ICLK
0008 7505h	ICU	IRQ control register 5	IRQCR5	8	8	2 ICLK
0008 7506h	ICU	IRQ control register 6	IRQCR6	8	8	2 ICLK
0008 7507h	ICU	IRQ control register 7	IRQCR7	8	8	2 ICLK
0008 7580h	ICU	Non-maskable interrupt status register	NMISR	8	8	2 ICLK
0008 7581h	ICU	Non-maskable interrupt enable register	NMIER	8	8	2 ICLK
0008 7582h	ICU	Non-maskable interrupt clear register	NMICLR	8	8	2 ICLK
0008 7583h	ICU	NMI pin interrupt control register	NMICR	8	8	2 ICLK
0008 8000h	CMT	Compare match timer start register 0	CMSTR0	16	16	2, 3 PCLK*3
0008 8002h	CMT0	Compare match timer control register	CMCR	16	16	2, 3 PCLK*3
0008 8004h	CMT0	Compare match timer counter	CMCNT	16	16	2, 3 PCLK*3
0008 8006h	CMT0	Compare match timer constant register	CMCOR	16	16	2, 3 PCLK*3
0008 8008h	CMT1	Compare match timer control register	CMCR	16	16	2, 3 PCLK*3
0008 800Ah	CMT1	Compare match timer counter	CMCNT	16	16	2, 3 PCLK*3
0008 800Ch	CMT1	Compare match timer constant register	CMCOR	16	16	2, 3 PCLK*3
0008 8010h	CMT	Compare match timer start register 1	CMSTR1	16	16	2, 3 PCLK*3
0008 8012h	CMT2	Compare match timer control register	CMCR	16	16	2, 3 PCLK*3
0008 8014h	CMT2	Compare match timer counter	CMCNT	16	16	2, 3 PCLK*3
0008 8016h	CMT2	Compare match timer constant register	CMCOR	16	16	2, 3 PCLK*3
0008 8018h	CMT3	Compare match timer control register	CMCR	16	16	2, 3 PCLK*3
0008 801Ah	CMT3	Compare match timer counter	CMCNT	16	16	2, 3 PCLK*3
0008 801Ch	CMT3	Compare match timer constant register	CMCOR	16	16	2, 3 PCLK*3
0008 8028h	WDT	Timer control/status register	TCSR	8	8	2, 3 PCLK*3
0008 8028h	WDT	Write window A register	WINA	16	16	2, 3 PCLK*3
0008 8029h	WDT	Timer counter	TCNT	8	8	2, 3 PCLK*3
0008 802Ah	WDT	Write window B register	WINB	16	16	2, 3 PCLK*3
0008 802Bh	WDT	Reset control/status register	RSTCSR	8	8	2, 3 PCLK*3
0008 8030h	IWDT	IWDT refresh register	IWDTRR	8	8	2, 3 PCLK*3
0008 8032h	IWDT	IWDT control register	IWDTCR	16	16	2, 3 PCLK*3
0008 8034h	IWDT	IWDT status register	IWDTSR	16	16	2, 3 PCLK*3
0008 8040h	ADA	A/D data register A	ADDRA	16	16	2, 3 PCLK*3
0008 8042h	ADA	A/D data register B	ADDRB	16	16	2, 3 PCLK*3
0008 8044h	ADA	A/D data register C	ADDRC	16	16	2, 3 PCLK*3
0008 8046h	ADA	A/D data register D	ADDRD	16	16	2, 3 PCLK*3

Table 4.1 List of I/O Registers (Address Order) (11 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 8383h	RSPI	RSPI status register	SPSR	8	8	2, 3 PCLK*3
0008 8384h	RSPI	RSPI data register	SPDR	16, 32	16, 32	2, 3 PCLK*3
0008 8388h	RSPI	RSPI sequence control register	SPSCR	8	8	2, 3 PCLK*3
0008 8389h	RSPI	RSPI sequence status register	SPSSR	8	8	2, 3 PCLK*3
0008 838Ah	RSPI	RSPI bit rate register	SPBR	8	8	2, 3 PCLK*3
0008 838Bh	RSPI	RSPI data control register	SPDCR	8	8	2, 3 PCLK*3
0008 838Ch	RSPI	RSPI clock delay register	SPCKD	8	8	2, 3 PCLK*3
0008 838Dh	RSPI	RSPI slave select negation delay register	SSLND	8	8	2, 3 PCLK*3
0008 838Eh	RSPI	RSPI next-access delay register	SPND	8	8	2, 3 PCLK*3
0008 838Fh	RSPI	RSPI control register 2	SPCR2	8	8	2, 3 PCLK*3
0008 8390h	RSPI	RSPI command register 0	SPCMD0	16	16	2, 3 PCLK*3
0008 8392h	RSPI	RSPI command register 1	SPCMD1	16	16	2, 3 PCLK*3
0008 8394h	RSPI	RSPI command register 2	SPCMD2	16	16	2, 3 PCLK*3
0008 8396h	RSPI	RSPI command register 3	SPCMD3	16	16	2, 3 PCLK*3
0008 8398h	RSPI	RSPI command register 4	SPCMD4	16	16	2, 3 PCLK*3
0008 839Ah	RSPI	RSPI command register 5	SPCMD5	16	16	2, 3 PCLK*3
0008 839Ch	RSPI	RSPI command register 6	SPCMD6	16	16	2, 3 PCLK*3
0008 839Eh	RSPI	RSPI command register 7	SPCMD7	16	16	2, 3 PCLK*3
0008 9000h	S12AD0	A/D control register	ADCSR	8	8	2, 3 PCLK*3
0008 9004h	S12AD0	A/D channel select register	ADANS	16	16	2, 3 PCLK*3
0008 900Ah	S12AD0	A/D programmable gain amplifier register	ADPG	16	16	2, 3 PCLK*3
0008 900Eh	S12AD0	A/D control extended register	ADCER	16	16	2, 3 PCLK*3
0008 9010h	S12AD0	A/D start trigger select register	ADSTRGR	16	16	2, 3 PCLK*3
0008 9012h	S12AD	Comparator operating mode select register 0	ADCMPMD0	16	16	2, 3 PCLK*3
0008 9014h	S12AD	Comparator operating mode select register 1	ADCMPMD1	16	16	2, 3 PCLK*3
0008 9016h	S12AD	Comparator filter mode register 0	ADCMPNR0	16	16	2, 3 PCLK*3
0008 9018h	S12AD	Comparator filter mode register 1	ADCMPNR1	16	16	2, 3 PCLK*3
0008 901Ah	S12AD	Comparator detection flag register	ADCMPFR	8	8	2, 3 PCLK*3
0008 901Ch	S12AD	Comparator interrupt select register	ADCMPSEL	16	16	2, 3 PCLK*3
0008 901Eh	S12AD0	A/D data register Diag	ADRD	16	16	2, 3 PCLK*3
0008 9020h	S12AD0	A/D data register 0A	ADDR0A	16	16	2, 3 PCLK*3
0008 9022h	S12AD0	A/D data register 1	ADDR1	16	16	2, 3 PCLK*3
0008 9024h	S12AD0	A/D data register 2	ADDR2	16	16	2, 3 PCLK*3
0008 9026h	S12AD0	A/D data register 3	ADDR3	16	16	2, 3 PCLK*3
0008 9030h	S12AD0	A/D data register 0B	ADDR0B	16	16	2, 3 PCLK*3
0008 9060h	S12AD0	A/D sampling state register	ADSSTR	8	8	2, 3 PCLK*3
0008 9080h	S12AD1	A/D control register	ADCSR	8	8	2, 3 PCLK*3
0008 9084h	S12AD1	A/D channel select register	ADANS	16	16	2, 3 PCLK*3
0008 908Ah	S12AD1	A/D programmable gain amplifier register	ADPG	16	16	2, 3 PCLK*3
0008 908Eh	S12AD1	A/D control extended register	ADCER	16	16	2, 3 PCLK*3
0008 9090h	S12AD1	A/D start trigger select register	ADSTRGR	16	16	2, 3 PCLK*3
0008 909Eh	S12AD1	A/D data register Diag	ADRD	16	16	2, 3 PCLK*3
0008 90A0h	S12AD1	A/D data register 0A	ADDR0A	16	16	2, 3 PCLK*3
0008 90A2h	S12AD1	A/D data register 1	ADDR1	16	16	2, 3 PCLK*3

Table 4.1 List of I/O Registers (Address Order) (19 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000C 1A39h	MTU7	Timer buffer operation transfer mode register	TBTM	8	8	5 ICLK
000C 1A3Ah	MTU	Timer interrupt skipping mode register B	TITMRB	8	8	5 ICLK
000C 1A3Bh	MTU	Timer interrupt skipping set register 2B	TITCR2B	8	8	5 ICLK
000C 1A3Ch	MTU	Timer interrupt skipping counter 2B	TITCNT2B	8	8	5 ICLK
000C 1A40h	MTU7	Timer A/D converter start request control register	TADCR	16	16	5 ICLK
000C 1A44h	MTU7	Timer A/D converter start request cycle set register A	TADCORA	16	16, 32	5 ICLK
000C 1A46h	MTU7	Timer A/D converter start request cycle set register B	TADCORB	16	16	5 ICLK
000C 1A48h	MTU7	Timer A/D converter start request cycle set buffer register A	TADCOBRA	16	16, 32	5 ICLK
000C 1A4Ah	MTU7	Timer A/D converter start request cycle set buffer register B	TADCOBRB	16	16	5 ICLK
000C 1A50h	MTU6	Timer synchronous clear register	TSYCR	8	8	5 ICLK
000C 1A60h	MTU	Timer waveform control register B	TWCRB	8	8	5 ICLK
000C 1A70h	MTU	Timer mode register 2B	TMDR2B	8	8	5 ICLK
000C 1A72h	MTU6	Timer general register E	TGRE	16	16	5 ICLK
000C 1A74h	MTU7	Timer general register E	TGRE	16	16	5 ICLK
000C 1A76h	MTU7	Timer general register F	TGRF	16	16	5 ICLK
000C 1A80h	MTU	Timer start register B	TSTRB	8	8, 16	5 ICLK
000C 1A81h	MTU	Timer synchronous register B	TSYRB	8	8	5 ICLK
000C 1A84h	MTU	Timer read/write enable register B	TRWERB	8	8	5 ICLK
000C 1C80h	MTU5	Timer counter U	TCNTU	16	16, 32	5 ICLK
000C 1C82h	MTU5	Timer general register U	TGRU	16	16	5 ICLK
000C 1C84h	MTU5	Timer control register U	TCRU	8	8	5 ICLK
000C 1C86h	MTU5	Timer I/O control register U	TIORU	8	8	5 ICLK
000C 1C90h	MTU5	Timer counter V	TCNTV	16	16, 32	5 ICLK
000C 1C92h	MTU5	Timer general register V	TGRV	16	16	5 ICLK
000C 1C94h	MTU5	Timer control register V	TCRV	8	8	5 ICLK
000C 1C96h	MTU5	Timer I/O control register V	TIORV	8	8	5 ICLK
000C 1CA0h	MTU5	Timer counter W	TCNTW	16	16, 32	5 ICLK
000C 1CA2h	MTU5	Timer general register W	TGRW	16	16	5 ICLK
000C 1CA4h	MTU5	Timer control register W	TCRW	8	8	5 ICLK
000C 1CA6h	MTU5	Timer I/O control register W	TIORW	8	8	5 ICLK
000C 1CB0h	MTU5	Timer status register	TSR	8	8	5 ICLK
000C 1CB2h	MTU5	Timer interrupt enable register	TIER	8	8	5 ICLK
000C 1CB4h	MTU5	Timer start register	TSTR	8	8	5 ICLK
000C 1CB6h	MTU5	Timer compare match clear register	TCNTCMPCLR	8	8	5 ICLK
000C 2000h	GPT	General PWM timer software start register	GTSTR	16	8, 16, 32	3 to 5 ICLK*4
000C 2004h	GPT	General PWM timer hardware source start control register	GTHSCR	16	8, 16, 32	3 to 5 ICLK*4
000C 2006h	GPT	General PWM timer hardware source clear control register	GTHCCR	16	8, 16, 32	3 to 5 ICLK*4
000C 2008h	GPT	General PWM timer hardware start source select register	GTHSSR	16	8, 16, 32	3 to 5 ICLK*4

Table 4.2 List of I/O Registers (Bit Order) (2 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
MPU	REPAGE0				REPN[27:0]				
					REPN[27:0]				
					REPN[27:0]				
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE1				RSPN[27:0]				
					RSPN[27:0]				
					RSPN[27:0]				
			RSPN[27:0]			—	—	—	—
MPU	REPAGE1				REPN[27:0]				
					REPN[27:0]				
					REPN[27:0]				
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE2				RSPN[27:0]				
					RSPN[27:0]				
					RSPN[27:0]				
			RSPN[27:0]			—	—	—	—
MPU	REPAGE2				REPN[27:0]				
					REPN[27:0]				
					REPN[27:0]				
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE3				RSPN[27:0]				
					RSPN[27:0]				
					RSPN[27:0]				
			RSPN[27:0]			—	—	—	—
MPU	REPAGE3				REPN[27:0]				
					REPN[27:0]				
					REPN[27:0]				
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE4				RSPN[27:0]				
					RSPN[27:0]				
					RSPN[27:0]				
			RSPN[27:0]			—	—	—	—
MPU	REPAGE4				REPN[27:0]				
					REPN[27:0]				
					REPN[27:0]				
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE5				RSPN[27:0]				
					RSPN[27:0]				
					RSPN[27:0]				
			RSPN[27:0]			—	—	—	—
MPU	REPAGE5				REPN[27:0]				
					REPN[27:0]				
					REPN[27:0]				
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE6				RSPN[27:0]				
					RSPN[27:0]				
					RSPN[27:0]				
			RSPN[27:0]			—	—	—	—
MPU	REPAGE6				REPN[27:0]				
					REPN[27:0]				
					REPN[27:0]				
			REPN[27:0]				UAC[2:0]		V

Table 4.2 List of I/O Registers (Bit Order) (7 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
ICU	DTCER180	—	—	—	—	—	—	—	DTCE
ICU	DTCER181	—	—	—	—	—	—	—	DTCE
ICU	DTCER182	—	—	—	—	—	—	—	DTCE
ICU	DTCER183	—	—	—	—	—	—	—	DTCE
ICU	DTCER184	—	—	—	—	—	—	—	DTCE
ICU	DTCER186	—	—	—	—	—	—	—	DTCE
ICU	DTCER187	—	—	—	—	—	—	—	DTCE
ICU	DTCER188	—	—	—	—	—	—	—	DTCE
ICU	DTCER189	—	—	—	—	—	—	—	DTCE
ICU	DTCER190	—	—	—	—	—	—	—	DTCE
ICU	DTCER192	—	—	—	—	—	—	—	DTCE
ICU	DTCER193	—	—	—	—	—	—	—	DTCE
ICU	DTCER194	—	—	—	—	—	—	—	DTCE
ICU	DTCER195	—	—	—	—	—	—	—	DTCE
ICU	DTCER196	—	—	—	—	—	—	—	DTCE
ICU	DTCER215	—	—	—	—	—	—	—	DTCE
ICU	DTCER216	—	—	—	—	—	—	—	DTCE
ICU	DTCER219	—	—	—	—	—	—	—	DTCE
ICU	DTCER220	—	—	—	—	—	—	—	DTCE
ICU	DTCER223	—	—	—	—	—	—	—	DTCE
ICU	DTCER224	—	—	—	—	—	—	—	DTCE
ICU	DTCER247	—	—	—	—	—	—	—	DTCE
ICU	DTCER248	—	—	—	—	—	—	—	DTCE
ICU	DTCER254	—	—	—	—	—	—	—	DTCE
ICU	IER02	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER03	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER05	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER07	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER08	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER0C	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER0D	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER0E	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER0F	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER10	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER11	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER12	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER13	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER15	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER16	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER17	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER18	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER1A	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER1B	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER1C	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER1E	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER1F	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	SWINTR	—	—	—	—	—	—	—	SWINT
ICU	FIR	FIEN	—	—	—	—	—	—	—
		FVCT[7:0]							
ICU	IPR00	—	—	—	—	IPR[3:0]			
ICU	IPR01	—	—	—	—	IPR[3:0]			
ICU	IPR02	—	—	—	—	IPR[3:0]			

Table 4.2 List of I/O Registers (Bit Order) (9 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
ICU	IRQCR0	—	—	—	—	IRQMD[1:0]		—	—
ICU	IRQCR1	—	—	—	—	IRQMD[1:0]		—	—
ICU	IRQCR2	—	—	—	—	IRQMD[1:0]		—	—
ICU	IRQCR3	—	—	—	—	IRQMD[1:0]		—	—
ICU	IRQCR4	—	—	—	—	IRQMD[1:0]		—	—
ICU	IRQCR5	—	—	—	—	IRQMD[1:0]		—	—
ICU	IRQCR6	—	—	—	—	IRQMD[1:0]		—	—
ICU	IRQCR7	—	—	—	—	IRQMD[1:0]		—	—
ICU	NMISR	—	—	—	—	—	OSTST	LVDST	NMIST
ICU	NMIER	—	—	—	—	—	OSTEN	LVDEN	NMIEN
ICU	NMICLR	—	—	—	—	—	OSTCLR	—	NMICLR
ICU	NMICR	—	—	—	—	NMIMD	—	—	—
CMT	CMSTR0	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	STR1	STR0
CMT0	CMCR	—	—	—	—	—	—	—	—
		—	CMIE	—	—	—	—	CKS[1:0]	
CMT0	CMCNT								
CMT0	CMCOR								
CMT1	CMCR	—	—	—	—	—	—	—	—
		—	CMIE	—	—	—	—	CKS[1:0]	
CMT1	CMCNT								
CMT1	CMCOR								
CMT	CMSTR1	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	STR3	STR2
CMT2	CMCR	—	—	—	—	—	—	—	—
		—	CMIE	—	—	—	—	CKS[1:0]	
CMT2	CMCNT								
CMT2	CMCOR								
CMT3	CMCR	—	—	—	—	—	—	—	—
		—	CMIE	—	—	—	—	CKS[1:0]	
CMT3	CMCNT								
CMT3	CMCOR								
WDT	TCSR	—	TMS	TME	—	—		CKS[2:0]	
WDT	WINA								
WDT	TCNT								
WDT	WINB								
WDT	RSTCSR	WOVF	RSTE	—	—	—	—	—	—
IWDT	IWDTCR	—	—	—	—	—	—	—	—
			CKS[3:0]			—	—	TOPS[1:0]	
IWDT	IWDTSR	—	UNDFF			CNTVAL[13:0]			
					CNTVAL[13:0]				
AD0	ADDRA*1	—	—	—	—	—	—		

Table 4.2 List of I/O Registers (Bit Order) (15 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
SYSTEM	DPSIFR	DNMIF	—	—	DLVDF	—	—	DIRQ1F	DIRQ0F
SYSTEM	DPSIEGR	DNMIEG	—	—	—	—	—	DIRQ1EG	DIRQ0EG
SYSTEM	RSTSR	DPSRSTF	—	—	—	—	LVD2F	LVD1F	PORF
FLASH	FWEPROR	—	—	—	—	—	—	FLWE[1:0]	
SYSTEM	LVDKEYR	KEY[7:0]							
SYSTEM	LVDCR	LVD2E	LVD2RI	—	—	LVD1E	LVD1RI	—	—
SYSTEM	DPSBKR0								
SYSTEM	DPSBKR1								
SYSTEM	DPSBKR2								
SYSTEM	DPSBKR3								
SYSTEM	DPSBKR4								
SYSTEM	DPSBKR5								
SYSTEM	DPSBKR6								
SYSTEM	DPSBKR7								
SYSTEM	DPSBKR8								
SYSTEM	DPSBKR9								
SYSTEM	DPSBKR10								
SYSTEM	DPSBKR11								
SYSTEM	DPSBKR12								
SYSTEM	DPSBKR13								
SYSTEM	DPSBKR14								
SYSTEM	DPSBKR15								
SYSTEM	DPSBKR16								
SYSTEM	DPSBKR17								
SYSTEM	DPSBKR18								
SYSTEM	DPSBKR19								
SYSTEM	DPSBKR20								
SYSTEM	DPSBKR21								
SYSTEM	DPSBKR22								
SYSTEM	DPSBKR23								
SYSTEM	DPSBKR24								
SYSTEM	DPSBKR25								
SYSTEM	DPSBKR26								
SYSTEM	DPSBKR27								
SYSTEM	DPSBKR28								
SYSTEM	DPSBKR29								
SYSTEM	DPSBKR30								
SYSTEM	DPSBKR31								
POE	ICSR1	—	—	—	POE0F	—	—	—	PIE1
		—	—	—	—	—	—	POE0M[1:0]	
POE	OCSR1	OSF1	—	—	—	—	—	OCE1	OIE1
		—	—	—	—	—	—	—	—
POE	ICSR2	—	—	—	POE4F	—	—	—	PIE2
		—	—	—	—	—	—	POE4M[1:0]	
POE	OCSR2	OSF2	—	—	—	—	—	OCE2	OIE2
		—	—	—	—	—	—	—	—
POE	ICSR3	—	—	—	POE8F	—	—	POE8E	PIE3
		—	—	—	—	—	—	POE8M[1:0]	
POE	SPOER	—	—	—	GPT23HIZ	GPT01HIZ	MTUCH0HIZ	MTUCH67HIZ	MTUCH34HIZ
POE	POECR1	—	—	—	—	MTU0DZE	MTU0CZE	MTU0BZE	MTU0AZE

Table 4.2 List of I/O Registers (Bit Order) (24 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
GPT0	GTCR	—	—	CCLR[1:0]		—	—	TPCS[1:0]	
		—	—	—	—	—		MD[2:0]	
GPT0	GTBER	—	ADTDB	ADTTB[1:0]		—	ADTDA	ADTTA[1:0]	
		—	CCRSWT	PR[1:0]		CCRB[1:0]		CCRA[1:0]	
GPT0	GTUDC	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	UDF	UD
GPT0	GTITC	—	ADTBL	—	ADTAL	—	IVTT[2:0]		
		IVTC[1:0]		ITLF	ITLE	ITLD	ITLC	ITLB	ITLA
GPT0	GTST	TUCF	—	—	—	DTEF		ITCNT[2:0]	
		TCFPU	TCFPO	TCFF	TCFE	TCFD	TCFC	TCFB	TCFA
GPT0	GTCNT								
GPT0	GTCCRA								
GPT0	GTCCRB								
GPT0	GTCCRC								
GPT0	GTCCRD								
GPT0	GTCCRE								
GPT0	GTCCRF								
GPT0	GTPR								
GPT0	GTPBR								
GPT0	GTPDBR								
GPT0	GTADTRA								
GPT0	GTADTBRA								
GPT0	GTADTDBRA								
GPT0	GTADTRB								
GPT0	GTADTBRB								
GPT0	GTADTDBRB								
GPT0	GTONCR	OBE	OAE	—	SWN	—	—	—	NFV
			NFS[3:0]			NVB	NVA	NEB	NEA
GPT0	GTDTCR	—	—	—	—	—	—	—	TDFER
		—	—	TDBDE	TDBUE	—	—	—	TDE
GPT0	GTDVU								
GPT0	GTDVD								

Table 4.2 List of I/O Registers (Bit Order) (28 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
GPT3	GTCCRB								
GPT3	GTCCRC								
GPT3	GTCCRD								
GPT3	GTCCRE								
GPT3	GTCCRF								
GPT3	GTPR								
GPT3	GTPBR								
GPT3	GTPDBR								
GPT3	GTADTRA								
GPT3	GTADTBRA								
GPT3	GTADTDBRA								
GPT3	GTADTRB								
GPT3	GTADTBRB								
GPT3	GTADTDBRB								
GPT3	GTONCR	OBE	OAE	—	SWN	—	—	—	NFV
				NFS[3:0]		NVB	NVA	NEB	NEA
GPT3	GTDTCR	—	—	—	—	—	—	—	TDFER
		—	—	TDBDE	TDBUE	—	—	—	TDE
GPT3	GTDVU								
GPT3	GTDVD								
GPT3	GTDBU								
GPT3	GTDBD	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	SOS[1:0]	
GPT3	GTSOS	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	SOS[1:0]	
GPT3	GTSOTR	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	SOTR
GPT0	GTDLYCR	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLYEN	DLYRST	DLLEN
GPT1	GTDLYCR	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLYEN	DLYRST	DLLEN

Table 5.3 DC Characteristics (2)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Supply current*1	In operation	Max.*2	I_{CC}*3	-	-	70	mA	ICLK = 100 MHz PCLK = 50 MHz
		Normal*4		-	35	-		
		Increased by BGO operation*5		-	15	-		
	Sleep				22	60		
	All-module-clock-stop mode*6				14	28		
	Standby mode	Software standby mode		-	0.10	3	mA	
		Deep software standby mode		-	20	60	µA	
Analog power supply current	During 12-bit A/D conversion (when a sample-and-hold circuit is in use; per unit)		AI_{CC0}	-	3	5	mA	
	During 12-bit A/D conversion (when a sample-and-hold circuit is not in use; per unit)			-	3	5	mA	
	Programmable gain amp (per channel)			-	1	2	mA	
	Window comparator (1 channel)				0.5	1	mA	
	Window comparator (6 channels)			-	1	2	mA	
	During 12-bit A/D conversion (per unit)			-	60	90	µA	
	During 10-bit A/D conversion (per unit)		AI_{CC}	-	0.9	2	mA	
	Waiting for 10-bit A/D conversion (all units)			-	0.3	3	µA	
Reference power supply current	During 12-bit A/D conversion (per unit)		AI_{REFH0}	-	1.6	3	mA	
	Waiting for 12-bit A/D conversion (all units)			-	1.6	3	mA	
	During 10-bit A/D conversion (per unit)		AI_{REF}	-	0.1	1	mA	
	Waiting for 10-bit A/D conversion (all units)			-	0.1	3	µA	
VCC rising gradient			SV_{CC}	-	-	20	ms/V	

Note 1. Supply current values are with all output pins unloaded.
Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK: PCLK = 8:4)
ICC max. = 0.54 x f + 16 (max.)
ICC max. = 0.3 x f + 5 (normal operation)
ICC max. = 0.44 x f + 16 (sleep mode)
Note 4. Measured with clocks not supplied to the peripheral functions. This does not include the BGO operation.
Note 5. Incremented if data is written to or erased from the ROM or data flash for data storage during the program execution.
Note 6. The values are for reference.

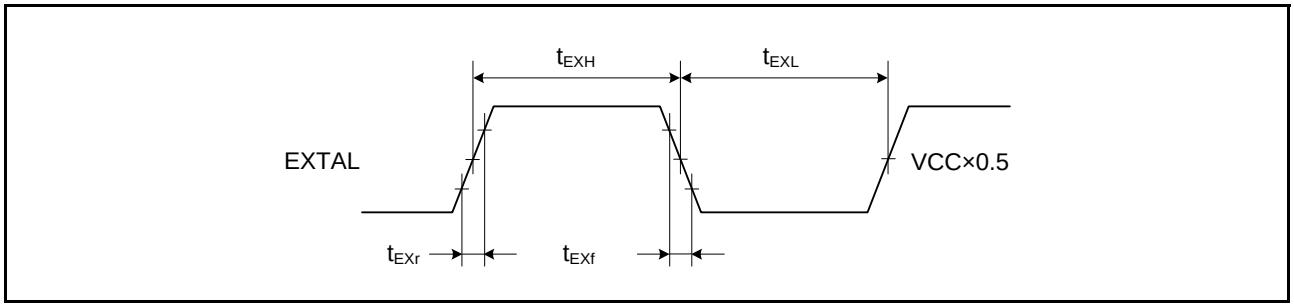


Figure 5.4 EXTAL External Input Clock Timing

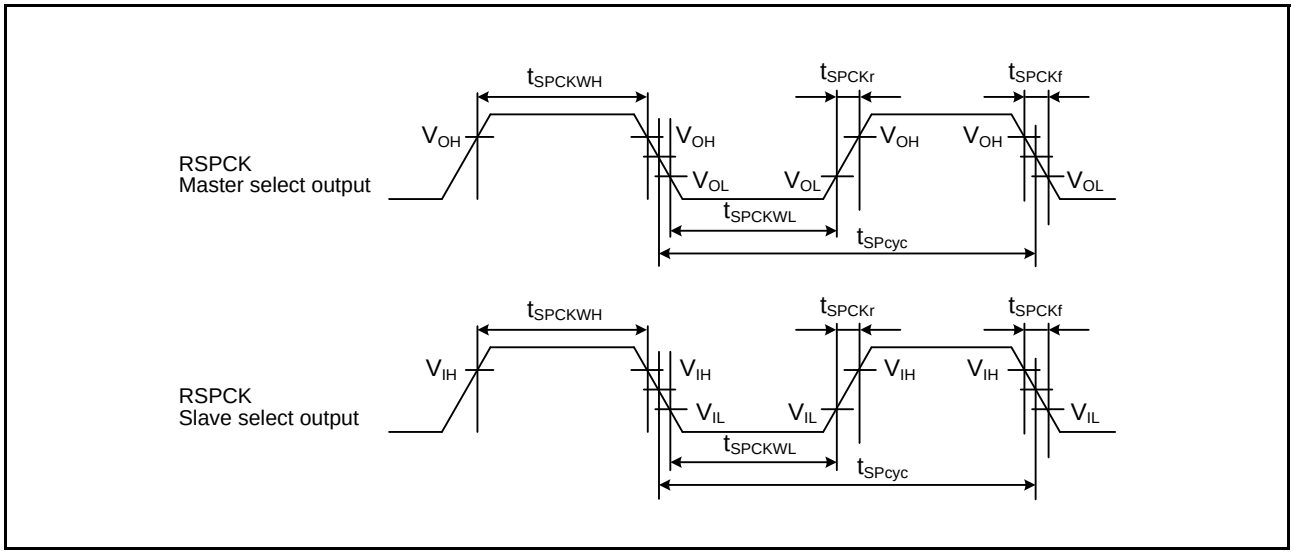


Figure 5.11 RSPI Clock Timing

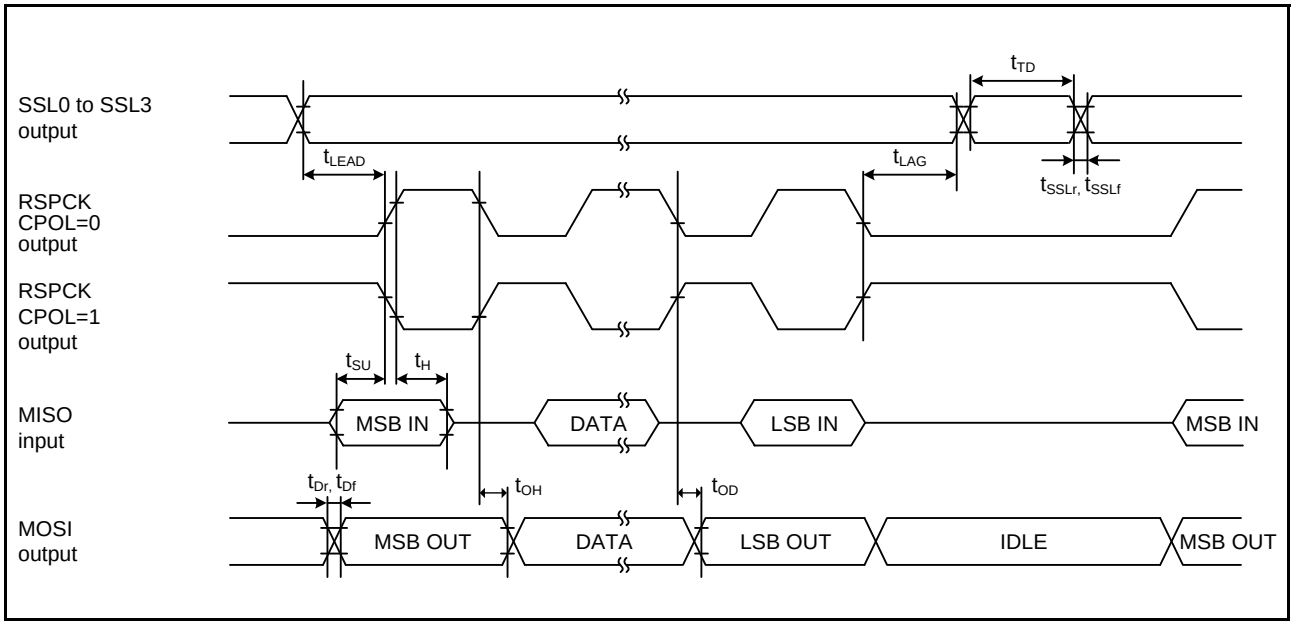
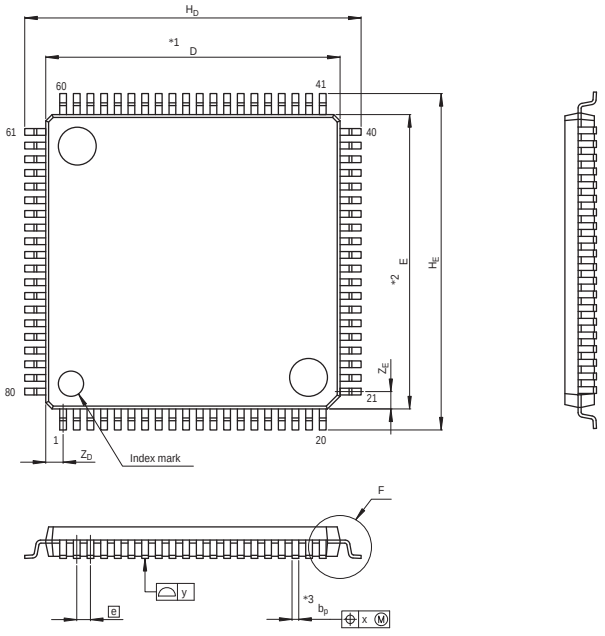
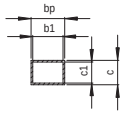


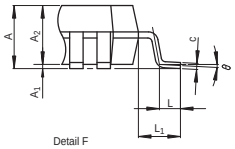
Figure 5.12 RSPI Timing (Master, CPHA = 0)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP80-14x14-0.65	PLQP0080JA-A	FP-80W / FP-80WV	0.6g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.27	0.32	0.37
b_1	—	0.30	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	0.825	—
Z_E	—	0.825	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure C 80-Pin LQFP (PLQP0080JA-A) Package Dimensions

Rev.	Date	Description	
		Page	Summary
2.00	Jan 10, 2014	98	Table 5.1 Absolute Maximum Ratings, changed
		102	Table 5.3 DC Characteristics (2): Note 3, changed
		103	Table 5.5 Permissible Power Consumption, added
		117	5.3.4 Timing of PWM Delay Generation Circuit, added
		117	Table 5.14 Timing of the PWM Delay Generation Circuit, added
		120	Table 5.17 Characteristics of the Programmable Gain Amplifier, changed
		125	Table 5.21 ROM (Flash Memory for Code Storage) Characteristics (1), changed
		125	Table 5.22 ROM (Flash Memory for Code Storage) Characteristics (2), added
		126	Table 5.23 Data Flash (Flash Memory for Data Storage) Characteristics (1), changed
		126	Table 5.24 Data Flash (Flash Memory for Data Storage) Characteristics (2), added