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Details

Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I ² C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	61
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 12x10b, 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562gaddfh-v3

1.4 Pin Assignments

Figure 1.3 to Figure 1.7 show the pins assignments. Table 1.4 to Table 1.8 show the list of pins and pin functions.

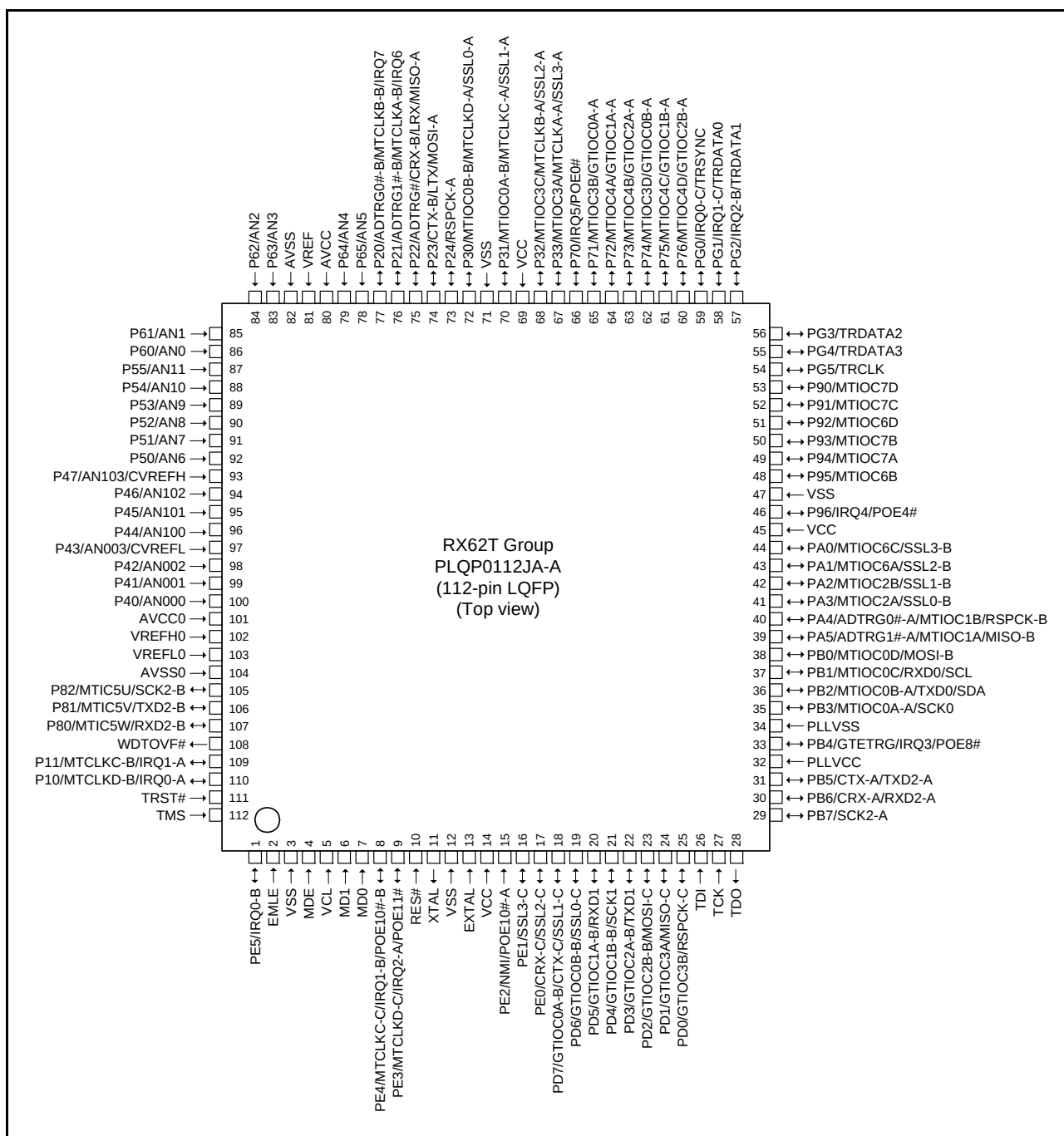


Figure 1.3 Pin Assignment of the 112-Pin LQFP

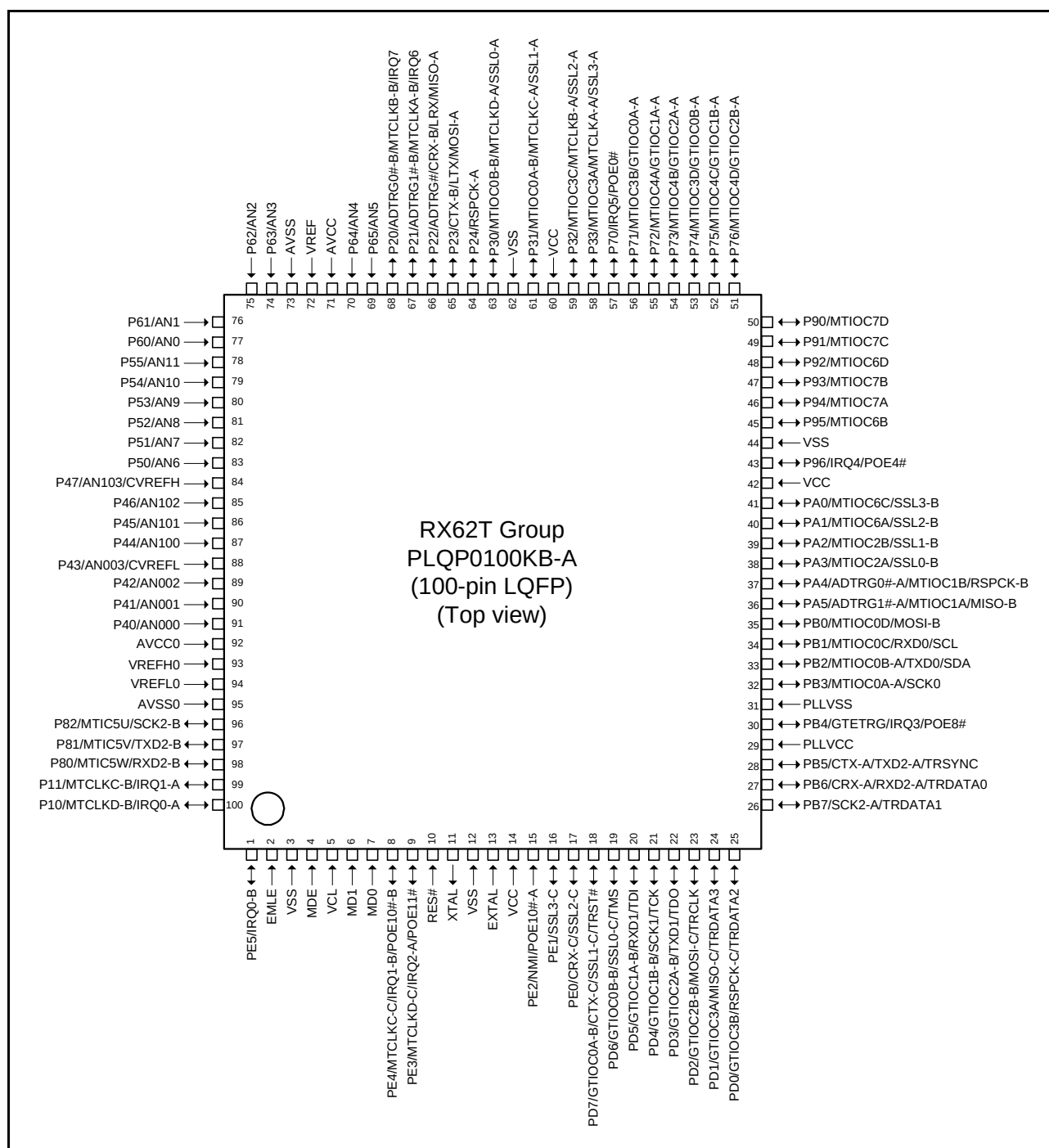


Figure 1.4 Pin Assignment of the 100-Pin LQFP

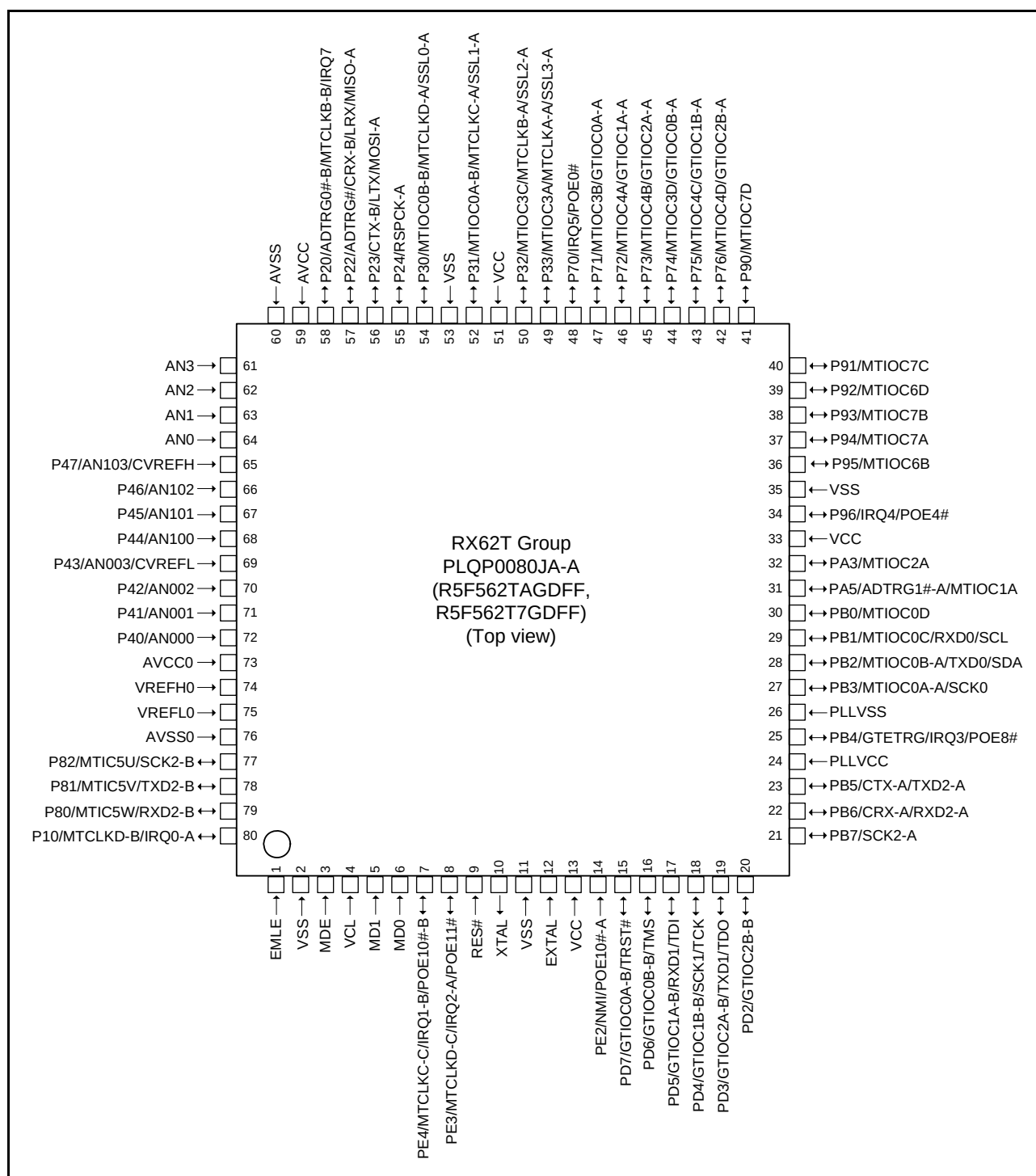


Figure 1.6 Pin Assignment of the 80-Pin LQFP (Two-Motor Control Supported Version)

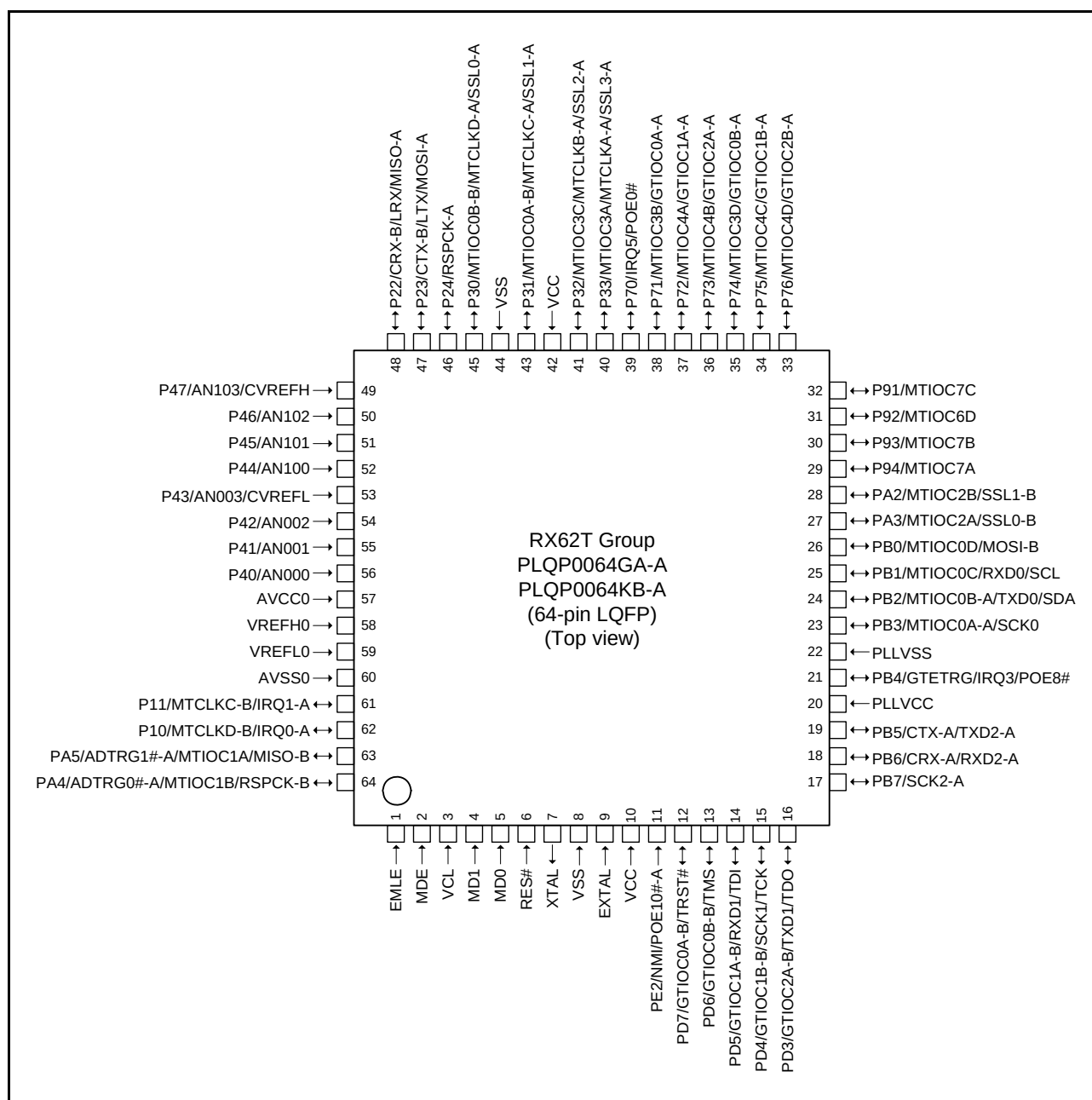


Figure 1.7 Pin Assignment of the 64-Pin LQFP

3. Address Space

3.1 Address Space

This LSI has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.

Figure 3.1 shows the memory maps.

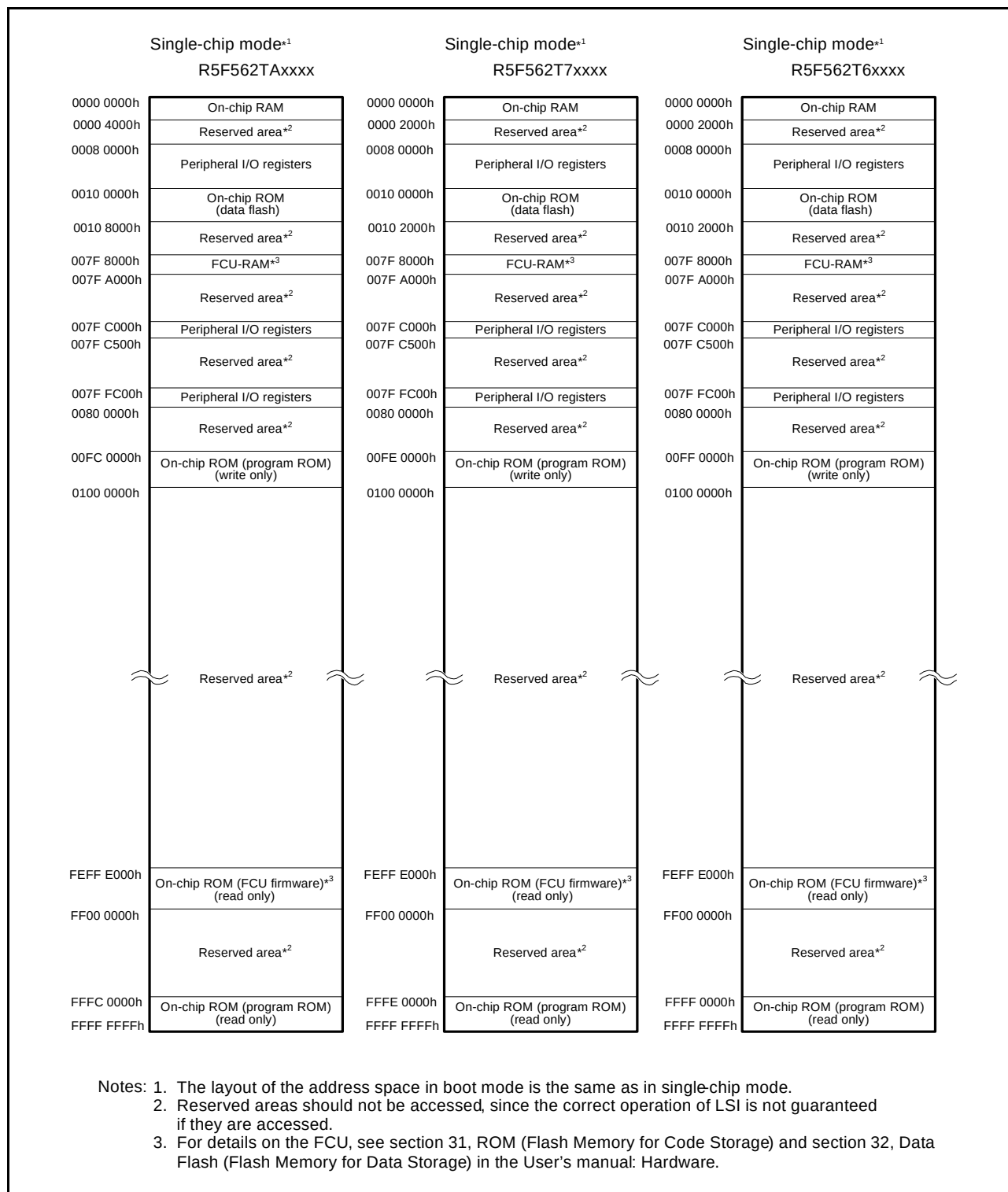


Figure 3.1 Memory Map (RX62T Group)

Table 4.1 List of I/O Registers (Address Order) (5 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 7172h	ICU	DTC activation enable register 114	DTCER114	8	8	2 ICLK
0008 7173h	ICU	DTC activation enable register 115	DTCER115	8	8	2 ICLK
0008 7174h	ICU	DTC activation enable register 116	DTCER116	8	8	2 ICLK
0008 7175h	ICU	DTC activation enable register 117	DTCER117	8	8	2 ICLK
0008 7179h	ICU	DTC activation enable register 121	DTCER121	8	8	2 ICLK
0008 717Ah	ICU	DTC activation enable register 122	DTCER122	8	8	2 ICLK
0008 717Dh	ICU	DTC activation enable register 125	DTCER125	8	8	2 ICLK
0008 717Eh	ICU	DTC activation enable register 126	DTCER126	8	8	2 ICLK
0008 7181h	ICU	DTC activation enable register 129	DTCER129	8	8	2 ICLK
0008 7182h	ICU	DTC activation enable register 130	DTCER130	8	8	2 ICLK
0008 7183h	ICU	DTC activation enable register 131	DTCER131	8	8	2 ICLK
0008 7184h	ICU	DTC activation enable register 132	DTCER132	8	8	2 ICLK
0008 7186h	ICU	DTC activation enable register 134	DTCER134	8	8	2 ICLK
0008 7187h	ICU	DTC activation enable register 135	DTCER135	8	8	2 ICLK
0008 7188h	ICU	DTC activation enable register 136	DTCER136	8	8	2 ICLK
0008 7189h	ICU	DTC activation enable register 137	DTCER137	8	8	2 ICLK
0008 718Ah	ICU	DTC activation enable register 138	DTCER138	8	8	2 ICLK
0008 718Bh	ICU	DTC activation enable register 139	DTCER139	8	8	2 ICLK
0008 718Ch	ICU	DTC activation enable register 140	DTCER140	8	8	2 ICLK
0008 718Dh	ICU	DTC activation enable register 141	DTCER141	8	8	2 ICLK
0008 718Eh	ICU	DTC activation enable register 142	DTCER142	8	8	2 ICLK
0008 718Fh	ICU	DTC activation enable register 143	DTCER143	8	8	2 ICLK
0008 7190h	ICU	DTC activation enable register 144	DTCER144	8	8	2 ICLK
0008 7191h	ICU	DTC activation enable register 145	DTCER145	8	8	2 ICLK
0008 7195h	ICU	DTC activation enable register 149	DTCER149	8	8	2 ICLK
0008 7196h	ICU	DTC activation enable register 150	DTCER150	8	8	2 ICLK
0008 7197h	ICU	DTC activation enable register 151	DTCER151	8	8	2 ICLK
0008 7198h	ICU	DTC activation enable register 152	DTCER152	8	8	2 ICLK
0008 7199h	ICU	DTC activation enable register 153	DTCER153	8	8	2 ICLK
0008 71AEh	ICU	DTC activation enable register 174	DTCER174	8	8	2 ICLK
0008 71AFh	ICU	DTC activation enable register 175	DTCER175	8	8	2 ICLK
0008 71B0h	ICU	DTC activation enable register 176	DTCER176	8	8	2 ICLK
0008 71B1h	ICU	DTC activation enable register 177	DTCER177	8	8	2 ICLK
0008 71B2h	ICU	DTC activation enable register 178	DTCER178	8	8	2 ICLK
0008 71B3h	ICU	DTC activation enable register 179	DTCER179	8	8	2 ICLK
0008 71B4h	ICU	DTC activation enable register 180	DTCER180	8	8	2 ICLK
0008 71B5h	ICU	DTC activation enable register 181	DTCER181	8	8	2 ICLK
0008 71B6h	ICU	DTC activation enable register 182	DTCER182	8	8	2 ICLK
0008 71B7h	ICU	DTC activation enable register 183	DTCER183	8	8	2 ICLK
0008 71B8h	ICU	DTC activation enable register 184	DTCER184	8	8	2 ICLK
0008 71BAh	ICU	DTC activation enable register 186	DTCER186	8	8	2 ICLK
0008 71BBh	ICU	DTC activation enable register 187	DTCER187	8	8	2 ICLK
0008 71BCh	ICU	DTC activation enable register 188	DTCER188	8	8	2 ICLK
0008 71BDh	ICU	DTC activation enable register 189	DTCER189	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (7 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 7305h	ICU	Interrupt source priority register 05	IPR05	8	8	2 ICLK
0008 7306h	ICU	Interrupt source priority register 06	IPR06	8	8	2 ICLK
0008 7307h	ICU	Interrupt source priority register 07	IPR07	8	8	2 ICLK
0008 7314h	ICU	Interrupt source priority register 14	IPR14	8	8	2 ICLK
0008 7318h	ICU	Interrupt source priority register 18	IPR18	8	8	2 ICLK
0008 7320h	ICU	Interrupt source priority register 20	IPR20	8	8	2 ICLK
0008 7321h	ICU	Interrupt source priority register 21	IPR21	8	8	2 ICLK
0008 7322h	ICU	Interrupt source priority register 22	IPR22	8	8	2 ICLK
0008 7323h	ICU	Interrupt source priority register 23	IPR23	8	8	2 ICLK
0008 7324h	ICU	Interrupt source priority register 24	IPR24	8	8	2 ICLK
0008 7325h	ICU	Interrupt source priority register 25	IPR25	8	8	2 ICLK
0008 7326h	ICU	Interrupt source priority register 26	IPR26	8	8	2 ICLK
0008 7327h	ICU	Interrupt source priority register 27	IPR27	8	8	2 ICLK
0008 7340h	ICU	Interrupt source priority register 40	IPR40	8	8	2 ICLK
0008 7344h	ICU	Interrupt source priority register 44	IPR44	8	8	2 ICLK
0008 7348h	ICU	Interrupt source priority register 48	IPR48	8	8	2 ICLK
0008 7349h	ICU	Interrupt source priority register 49	IPR49	8	8	2 ICLK
0008 7351h	ICU	Interrupt source priority register 51	IPR51	8	8	2 ICLK
0008 7352h	ICU	Interrupt source priority register 52	IPR52	8	8	2 ICLK
0008 7353h	ICU	Interrupt source priority register 53	IPR53	8	8	2 ICLK
0008 7354h	ICU	Interrupt source priority register 54	IPR54	8	8	2 ICLK
0008 7355h	ICU	Interrupt source priority register 55	IPR55	8	8	2 ICLK
0008 7356h	ICU	Interrupt source priority register 56	IPR56	8	8	2 ICLK
0008 7357h	ICU	Interrupt source priority register 57	IPR57	8	8	2 ICLK
0008 7358h	ICU	Interrupt source priority register 58	IPR58	8	8	2 ICLK
0008 7359h	ICU	Interrupt source priority register 59	IPR59	8	8	2 ICLK
0008 735Ah	ICU	Interrupt source priority register 5A	IPR5A	8	8	2 ICLK
0008 735Bh	ICU	Interrupt source priority register 5B	IPR5B	8	8	2 ICLK
0008 735Ch	ICU	Interrupt source priority register 5C	IPR5C	8	8	2 ICLK
0008 735Dh	ICU	Interrupt source priority register 5D	IPR5D	8	8	2 ICLK
0008 735Eh	ICU	Interrupt source priority register 5E	IPR5E	8	8	2 ICLK
0008 735Fh	ICU	Interrupt source priority register 5F	IPR5F	8	8	2 ICLK
0008 7360h	ICU	Interrupt source priority register 60	IPR60	8	8	2 ICLK
0008 7367h	ICU	Interrupt source priority register 67	IPR67	8	8	2 ICLK
0008 7368h	ICU	Interrupt source priority register 68	IPR68	8	8	2 ICLK
0008 7369h	ICU	Interrupt source priority register 69	IPR69	8	8	2 ICLK
0008 736Ah	ICU	Interrupt source priority register 6A	IPR6A	8	8	2 ICLK
0008 736Bh	ICU	Interrupt source priority register 6B	IPR6B	8	8	2 ICLK
0008 736Ch	ICU	Interrupt source priority register 6C	IPR6C	8	8	2 ICLK
0008 736Dh	ICU	Interrupt source priority register 6D	IPR6D	8	8	2 ICLK
0008 736Eh	ICU	Interrupt source priority register 6E	IPR6E	8	8	2 ICLK
0008 736Fh	ICU	Interrupt source priority register 6F	IPR6F	8	8	2 ICLK
0008 7380h	ICU	Interrupt source priority register 80	IPR80	8	8	2 ICLK
0008 7381h	ICU	Interrupt source priority register 81	IPR81	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (8 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 7382h	ICU	Interrupt source priority register 82	IPR82	8	8	2 ICLK
0008 7388h	ICU	Interrupt source priority register 88	IPR88	8	8	2 ICLK
0008 7389h	ICU	Interrupt source priority register 89	IPR89	8	8	2 ICLK
0008 738Ah	ICU	Interrupt source priority register 8A	IPR8A	8	8	2 ICLK
0008 738Bh	ICU	Interrupt source priority register 8B	IPR8B	8	8	2 ICLK
0008 7390h	ICU	Interrupt source priority register 90	IPR90	8	8	2 ICLK
0008 7500h	ICU	IRQ control register 0	IRQCR0	8	8	2 ICLK
0008 7501h	ICU	IRQ control register 1	IRQCR1	8	8	2 ICLK
0008 7502h	ICU	IRQ control register 2	IRQCR2	8	8	2 ICLK
0008 7503h	ICU	IRQ control register 3	IRQCR3	8	8	2 ICLK
0008 7504h	ICU	IRQ control register 4	IRQCR4	8	8	2 ICLK
0008 7505h	ICU	IRQ control register 5	IRQCR5	8	8	2 ICLK
0008 7506h	ICU	IRQ control register 6	IRQCR6	8	8	2 ICLK
0008 7507h	ICU	IRQ control register 7	IRQCR7	8	8	2 ICLK
0008 7580h	ICU	Non-maskable interrupt status register	NMISR	8	8	2 ICLK
0008 7581h	ICU	Non-maskable interrupt enable register	NMIER	8	8	2 ICLK
0008 7582h	ICU	Non-maskable interrupt clear register	NMICLR	8	8	2 ICLK
0008 7583h	ICU	NMI pin interrupt control register	NMICR	8	8	2 ICLK
0008 8000h	CMT	Compare match timer start register 0	CMSTR0	16	16	2, 3 PCLK*3
0008 8002h	CMT0	Compare match timer control register	CMCR	16	16	2, 3 PCLK*3
0008 8004h	CMT0	Compare match timer counter	CMCNT	16	16	2, 3 PCLK*3
0008 8006h	CMT0	Compare match timer constant register	CMCOR	16	16	2, 3 PCLK*3
0008 8008h	CMT1	Compare match timer control register	CMCR	16	16	2, 3 PCLK*3
0008 800Ah	CMT1	Compare match timer counter	CMCNT	16	16	2, 3 PCLK*3
0008 800Ch	CMT1	Compare match timer constant register	CMCOR	16	16	2, 3 PCLK*3
0008 8010h	CMT	Compare match timer start register 1	CMSTR1	16	16	2, 3 PCLK*3
0008 8012h	CMT2	Compare match timer control register	CMCR	16	16	2, 3 PCLK*3
0008 8014h	CMT2	Compare match timer counter	CMCNT	16	16	2, 3 PCLK*3
0008 8016h	CMT2	Compare match timer constant register	CMCOR	16	16	2, 3 PCLK*3
0008 8018h	CMT3	Compare match timer control register	CMCR	16	16	2, 3 PCLK*3
0008 801Ah	CMT3	Compare match timer counter	CMCNT	16	16	2, 3 PCLK*3
0008 801Ch	CMT3	Compare match timer constant register	CMCOR	16	16	2, 3 PCLK*3
0008 8028h	WDT	Timer control/status register	TCSR	8	8	2, 3 PCLK*3
0008 8028h	WDT	Write window A register	WINA	16	16	2, 3 PCLK*3
0008 8029h	WDT	Timer counter	TCNT	8	8	2, 3 PCLK*3
0008 802Ah	WDT	Write window B register	WINB	16	16	2, 3 PCLK*3
0008 802Bh	WDT	Reset control/status register	RSTCSR	8	8	2, 3 PCLK*3
0008 8030h	IWDT	IWDT refresh register	IWDTRR	8	8	2, 3 PCLK*3
0008 8032h	IWDT	IWDT control register	IWDTCR	16	16	2, 3 PCLK*3
0008 8034h	IWDT	IWDT status register	IWDTSR	16	16	2, 3 PCLK*3
0008 8040h	ADA	A/D data register A	ADDRA	16	16	2, 3 PCLK*3
0008 8042h	ADA	A/D data register B	ADDRB	16	16	2, 3 PCLK*3
0008 8044h	ADA	A/D data register C	ADDRC	16	16	2, 3 PCLK*3
0008 8046h	ADA	A/D data register D	ADDRD	16	16	2, 3 PCLK*3

Table 4.1 List of I/O Registers (Address Order) (11 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 8383h	RSPI	RSPI status register	SPSR	8	8	2, 3 PCLK*3
0008 8384h	RSPI	RSPI data register	SPDR	16, 32	16, 32	2, 3 PCLK*3
0008 8388h	RSPI	RSPI sequence control register	SPSCR	8	8	2, 3 PCLK*3
0008 8389h	RSPI	RSPI sequence status register	SPSSR	8	8	2, 3 PCLK*3
0008 838Ah	RSPI	RSPI bit rate register	SPBR	8	8	2, 3 PCLK*3
0008 838Bh	RSPI	RSPI data control register	SPDCR	8	8	2, 3 PCLK*3
0008 838Ch	RSPI	RSPI clock delay register	SPCKD	8	8	2, 3 PCLK*3
0008 838Dh	RSPI	RSPI slave select negation delay register	SSLND	8	8	2, 3 PCLK*3
0008 838Eh	RSPI	RSPI next-access delay register	SPND	8	8	2, 3 PCLK*3
0008 838Fh	RSPI	RSPI control register 2	SPCR2	8	8	2, 3 PCLK*3
0008 8390h	RSPI	RSPI command register 0	SPCMD0	16	16	2, 3 PCLK*3
0008 8392h	RSPI	RSPI command register 1	SPCMD1	16	16	2, 3 PCLK*3
0008 8394h	RSPI	RSPI command register 2	SPCMD2	16	16	2, 3 PCLK*3
0008 8396h	RSPI	RSPI command register 3	SPCMD3	16	16	2, 3 PCLK*3
0008 8398h	RSPI	RSPI command register 4	SPCMD4	16	16	2, 3 PCLK*3
0008 839Ah	RSPI	RSPI command register 5	SPCMD5	16	16	2, 3 PCLK*3
0008 839Ch	RSPI	RSPI command register 6	SPCMD6	16	16	2, 3 PCLK*3
0008 839Eh	RSPI	RSPI command register 7	SPCMD7	16	16	2, 3 PCLK*3
0008 9000h	S12AD0	A/D control register	ADCSR	8	8	2, 3 PCLK*3
0008 9004h	S12AD0	A/D channel select register	ADANS	16	16	2, 3 PCLK*3
0008 900Ah	S12AD0	A/D programmable gain amplifier register	ADPG	16	16	2, 3 PCLK*3
0008 900Eh	S12AD0	A/D control extended register	ADCER	16	16	2, 3 PCLK*3
0008 9010h	S12AD0	A/D start trigger select register	ADSTRGR	16	16	2, 3 PCLK*3
0008 9012h	S12AD	Comparator operating mode select register 0	ADCOMPMD0	16	16	2, 3 PCLK*3
0008 9014h	S12AD	Comparator operating mode select register 1	ADCOMPMD1	16	16	2, 3 PCLK*3
0008 9016h	S12AD	Comparator filter mode register 0	ADCOMPNR0	16	16	2, 3 PCLK*3
0008 9018h	S12AD	Comparator filter mode register 1	ADCOMPNR1	16	16	2, 3 PCLK*3
0008 901Ah	S12AD	Comparator detection flag register	ADCOMPFR	8	8	2, 3 PCLK*3
0008 901Ch	S12AD	Comparator interrupt select register	ADCOMPSEL	16	16	2, 3 PCLK*3
0008 901Eh	S12AD0	A/D data register Diag	ADRD	16	16	2, 3 PCLK*3
0008 9020h	S12AD0	A/D data register 0A	ADDR0A	16	16	2, 3 PCLK*3
0008 9022h	S12AD0	A/D data register 1	ADDR1	16	16	2, 3 PCLK*3
0008 9024h	S12AD0	A/D data register 2	ADDR2	16	16	2, 3 PCLK*3
0008 9026h	S12AD0	A/D data register 3	ADDR3	16	16	2, 3 PCLK*3
0008 9030h	S12AD0	A/D data register 0B	ADDR0B	16	16	2, 3 PCLK*3
0008 9060h	S12AD0	A/D sampling state register	ADSSTR	8	8	2, 3 PCLK*3
0008 9080h	S12AD1	A/D control register	ADCSR	8	8	2, 3 PCLK*3
0008 9084h	S12AD1	A/D channel select register	ADANS	16	16	2, 3 PCLK*3
0008 908Ah	S12AD1	A/D programmable gain amplifier register	ADPG	16	16	2, 3 PCLK*3
0008 908Eh	S12AD1	A/D control extended register	ADCER	16	16	2, 3 PCLK*3
0008 9090h	S12AD1	A/D start trigger select register	ADSTRGR	16	16	2, 3 PCLK*3
0008 909Eh	S12AD1	A/D data register Diag	ADRD	16	16	2, 3 PCLK*3
0008 90A0h	S12AD1	A/D data register 0A	ADDR0A	16	16	2, 3 PCLK*3
0008 90A2h	S12AD1	A/D data register 1	ADDR1	16	16	2, 3 PCLK*3

Table 4.1 List of I/O Registers (Address Order) (16 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0009 4019h	LIN0	Data 2 buffer register	L0DB2	8	8, 16, 32	2, 3 PCLK* ³
0009 401Ah	LIN0	Data 3 buffer register	L0DB3	8	8, 16, 32	2, 3 PCLK* ³
0009 401Bh	LIN0	Data 4 buffer register	L0DB4	8	8, 16, 32	2, 3 PCLK* ³
0009 401Ch	LIN0	Data 5 buffer register	L0DB5	8	8, 16, 32	2, 3 PCLK* ³
0009 401Dh	LIN0	Data 6 buffer register	L0DB6	8	8, 16, 32	2, 3 PCLK* ³
0009 401Eh	LIN0	Data 7 buffer register	L0DB7	8	8, 16, 32	2, 3 PCLK* ³
0009 401Fh	LIN0	Data 8 buffer register	L0DB8	8	8, 16, 32	2, 3 PCLK* ³
000C 1200h	MTU3	Timer control register	TCR	8	8, 16, 32	5 ICLK
000C 1201h	MTU4	Timer control register	TCR	8	8	5 ICLK
000C 1202h	MTU3	Timer mode register 1	TMDR1	8	8, 16	5 ICLK
000C 1203h	MTU4	Timer mode register 1	TMDR1	8	8	5 ICLK
000C 1204h	MTU3	Timer I/O control register H	TIORH	8	8, 16, 32	5 ICLK
000C 1205h	MTU3	Timer I/O control register L	TIORL	8	8	5 ICLK
000C 1206h	MTU4	Timer I/O control register H	TIORH	8	8, 16	5 ICLK
000C 1207h	MTU4	Timer I/O control register L	TIORL	8	8	5 ICLK
000C 1208h	MTU3	Timer interrupt enable register	TIER	8	8, 16	5 ICLK
000C 1209h	MTU4	Timer interrupt enable register	TIER	8	8	5 ICLK
000C 120Ah	MTU	Timer output master enable register A	TOERA	8	8	5 ICLK
000C 120Dh	MTU	Timer gate control register A	TGCRA	8	8	5 ICLK
000C 120Eh	MTU	Timer output control register 1A	TOCR1A	8	8, 16	5 ICLK
000C 120Fh	MTU	Timer output control register 2A	TOCR2A	8	8	5 ICLK
000C 1210h	MTU3	Timer counter	TCNT	16	16, 32	5 ICLK
000C 1212h	MTU4	Timer counter	TCNT	16	16	5 ICLK
000C 1214h	MTU	Timer cycle data register A	TCDRA	16	16, 32	5 ICLK
000C 1216h	MTU	Timer dead time data register A	TDDRA	16	16	5 ICLK
000C 1218h	MTU3	Timer general register A	TGRA	16	16, 32	5 ICLK
000C 121Ah	MTU3	Timer general register B	TGRB	16	16	5 ICLK
000C 121Ch	MTU4	Timer general register A	TGRA	16	16, 32	5 ICLK
000C 121Eh	MTU4	Timer general register B	TGRB	16	16	5 ICLK
000C 1220h	MTU	Timer subcounter A	TCNTSA	16	16, 32	5 ICLK
000C 1222h	MTU	Timer cycle buffer register A	TCBRA	16	16	5 ICLK
000C 1224h	MTU3	Timer general register C	TGRC	16	16, 32	5 ICLK
000C 1226h	MTU3	Timer general register D	TGRD	16	16	5 ICLK
000C 1228h	MTU4	Timer general register C	TGRC	16	16, 32	5 ICLK
000C 122Ah	MTU4	Timer general register D	TGRD	16	16	5 ICLK
000C 122Ch	MTU3	Timer status register	TSR	8	8, 16	5 ICLK
000C 122Dh	MTU4	Timer status register	TSR	8	8	5 ICLK
000C 1230h	MTU	Timer interrupt skipping set register 1A	TITCR1A	8	8, 16	5 ICLK
000C 1231h	MTU	Timer interrupt skipping counter 1A	TITCNT1A	8	8	5 ICLK
000C 1232h	MTU	Timer buffer transfer set register A	TBTERA	8	8	5 ICLK
000C 1234h	MTU	Timer dead time enable register A	TDERA	8	8	5 ICLK
000C 1236h	MTU	Timer output level buffer register A	TOLBRA	8	8	5 ICLK
000C 1238h	MTU3	Timer buffer operation transfer mode register	TBTM	8	8, 16	5 ICLK
000C 1239h	MTU4	Timer buffer operation transfer mode register	TBTM	8	8	5 ICLK

Table 4.2 List of I/O Registers (Bit Order) (2 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
MPU	REPAGE0					REPN[27:0]			
						REPN[27:0]			
						REPN[27:0]			
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE1					RSPN[27:0]			
						RSPN[27:0]			
						RSPN[27:0]			
			RSPN[27:0]			—	—	—	—
MPU	REPAGE1					REPN[27:0]			
						REPN[27:0]			
						REPN[27:0]			
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE2					RSPN[27:0]			
						RSPN[27:0]			
						RSPN[27:0]			
			RSPN[27:0]			—	—	—	—
MPU	REPAGE2					REPN[27:0]			
						REPN[27:0]			
						REPN[27:0]			
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE3					RSPN[27:0]			
						RSPN[27:0]			
						RSPN[27:0]			
			RSPN[27:0]			—	—	—	—
MPU	REPAGE3					REPN[27:0]			
						REPN[27:0]			
						REPN[27:0]			
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE4					RSPN[27:0]			
						RSPN[27:0]			
						RSPN[27:0]			
			RSPN[27:0]			—	—	—	—
MPU	REPAGE4					REPN[27:0]			
						REPN[27:0]			
						REPN[27:0]			
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE5					RSPN[27:0]			
						RSPN[27:0]			
						RSPN[27:0]			
			RSPN[27:0]			—	—	—	—
MPU	REPAGE5					REPN[27:0]			
						REPN[27:0]			
						REPN[27:0]			
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE6					RSPN[27:0]			
						RSPN[27:0]			
						RSPN[27:0]			
			RSPN[27:0]			—	—	—	—
MPU	REPAGE6					REPN[27:0]			
						REPN[27:0]			
						REPN[27:0]			
			REPN[27:0]				UAC[2:0]		V

Table 4.2 List of I/O Registers (Bit Order) (3 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
MPU	RSPAGE7					RSPN[27:0]			
						RSPN[27:0]			
						RSPN[27:0]			
				RSPN[27:0]		—	—	—	—
MPU	REPAGE7					REPN[27:0]			
						REPN[27:0]			
						REPN[27:0]			
				REPN[27:0]			UAC[2:0]		V
MPU	MPEN	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	MPEN
MPU	MPBAC	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—		UBAC[2:0]		—
MPU	MPECLR	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	CLR
MPU	MPESTS	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	DRW	DA	IA
MPU	MPDEA					DEA[31:0]			
						DEA[31:0]			
						DEA[31:0]			
						DEA[31:0]			
MPU	MPSA					SA[31:0]			
						SA[31:0]			
						SA[31:0]			
						SA[31:0]			
MPU	MPOPS	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	S
MPU	MPOPI	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	INV
MPU	MHITI	—	—	—	—	—	—	—	—
						HITI[7:0]			
		—	—	—	—	—	—	—	—
		—	—	—	—		UHACI[2:0]		—
MPU	MHITD	—	—	—	—	—	—	—	—
						HITD[7:0]			
		—	—	—	—	—	—	—	—
		—	—	—	—		UHACD[2:0]		—
ICU	IR016	—	—	—	—	—	—	—	IR
ICU	IR021	—	—	—	—	—	—	—	IR
ICU	IR023	—	—	—	—	—	—	—	IR
ICU	IR027	—	—	—	—	—	—	—	IR
ICU	IR028	—	—	—	—	—	—	—	IR
ICU	IR029	—	—	—	—	—	—	—	IR
ICU	IR030	—	—	—	—	—	—	—	IR
ICU	IR031	—	—	—	—	—	—	—	IR

Table 4.2 List of I/O Registers (Bit Order) (10 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
AD0	ADDRB ^{*1}	—	—	—	—	—	—		
AD0	ADDRC ^{*1}	—	—	—	—	—	—		
AD0	ADDRD ^{*1}	—	—	—	—	—	—		
AD0	ADDRE ^{*1}	—	—	—	—	—	—		
AD0	ADDRF ^{*1}	—	—	—	—	—	—		
AD0	ADDRG ^{*1}	—	—	—	—	—	—		
AD0	ADDRH ^{*1}	—	—	—	—	—	—		
AD0	ADCSR	—	ADIE	ADST	—		CH[3:0]		
AD0	ADCR	—	—	—	—	CKS[1:0]		MODE[1:0]	
AD0	ADSSTR								
AD0	ADDIAGR	—	—	—	—	—	—	DIAG[1:0]	
AD0	ADDRI ^{*1}	—	—	—	—	—	—		
AD0	ADDRJ ^{*1}	—	—	—	—	—	—		
AD0	ADDRK ^{*1}	—	—	—	—	—	—		
AD0	ADDRL ^{*1}	—	—	—	—	—	—		
AD0	ADSTRGR	—	—	—		ADSTRS[4:0]			
AD0	ADDP	DPSEL	—	—	—	—	—	—	DPPRC
SCI0	SMR	CM	CHR	PE	PM	STOP	MP	CKS[1:0]	
SCI0	BRR								
SCI0	SCR	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
SCI0	TDR								
SCI0	SSR	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
SCI0	RDR								
SCI0	SCMR	BCP2	—	—	—	SDIR	SINV	—	SMIF
SCI0	SEMR	—	—	NFEN	ABCS	—	—	—	—
SMCI0	SMR	GM	BLK	PE	PM	(BCP[1:0])		CKS[1:0]	
SMCI0	BRR								
SMCI0	SCR	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
SMCI0	TDR								
SMCI0	SSR	TDRE	RDRF	ORER	ERS	PER	TEND	MPB	MPBT
SMCI0	RDR								
SMCI0	SCMR	BCP2	—	—	—	SDIR	SINV	—	SMIF
SCI1	SMR	CM	CHR	PE	PM	STOP	MP	CKS[1:0]	
SCI1	BRR								
SCI1	SCR	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
SCI1	TDR								
SCI1	SSR	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
SCI1	RDR								
SCI1	SCMR	BCP2	—	—	—	SDIR	SINV	—	SMIF

Table 4.2 List of I/O Registers (Bit Order) (11 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
SCI1	SEMR	—	—	NFEN	ABCS	—	—	—	—
SMC11	SMR	GM	BLK	PE	PM	(BCP[1:0])		CKS[1:0]	
SMC11	BRR								
SMC11	SCR	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
SMC11	TDR								
SMC11	SSR	TDRE	RDRF	ORER	ERS	PER	TEND	MPB	MPBT
SMC11	RDR								
SMC11	SCMR	BCP2	—	—	—	SDIR	SINV	—	SMIF
SCI2	SMR	CM	CHR	PE	PM	STOP	MP	CKS[1:0]	
SCI2	BRR								
SCI2	SCR	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
SCI2	TDR								
SCI2	SSR	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
SCI2	RDR								
SCI2	SCMR	BCP2	—	—	—	SDIR	SINV	—	SMIF
SMC12	SMR	GM	BLK	PE	PM	(BCP[1:0])		CKS[1:0]	
SMC12	BRR								
SMC12	SCR	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
SMC12	TDR								
SMC12	SSR	TDRE	RDRF	ORER	ERS	PER	TEND	MPB	MPBT
SMC12	RDR								
SMC12	SCMR	BCP2	—	—	—	SDIR	SINV	—	SMIF
CRC	CRCCR	DORCLR	—	—	—	—	LMS	GPS[1:0]	
CRC	CRCDIR								
CRC	CRCDOR								
RIIC0	ICCR1	ICE	IICRST	CLO	SOWP	SCLO	SDAO	SCLI	SDAI
RIIC0	ICCR2	BBSY	MST	TRS	—	SP	RS	ST	—
RIIC0	ICMR1	MTWP		CKS[2:0]		BCWP		BC[2:0]	
RIIC0	ICMR2	DLCS		SDDL[2:0]		TMWE	TMOH	TMOL	TMOS
RIIC0	ICMR3	SMBS	WAIT	RDRFS	ACKWP	ACKBT	ACKBR	NF[1:0]	
RIIC0	ICFER	—	SCLE	NFE	NACKE	SALE	NALE	MALE	TMOE
RIIC0	ICSER	HOAE	—	DIDE	—	GCAE	SAR2E	SAR1E	SAR0E
RIIC0	ICIER	TIE	TEIE	RIE	NAKIE	SPIE	STIE	ALIE	TMOIE
RIIC0	ICSR1	HOA	—	DID	—	GCA	AAS2	AAS1	AAS0
RIIC0	ICSR2	TDRE	TEND	RDRF	NACKF	STOP	START	AL	TMOF
RIIC0	SARL0				SVA[6:0]				SVA0
RIIC0	TMOCNTL								
RIIC0	SARU0	—	—	—	—	—	SVA[1:0]		FS
RIIC0	TMOCNTU								
RIIC0	SARL1				SVA[6:0]				SVA0
RIIC0	SARU1	—	—	—	—	—	SVA[1:0]		FS
RIIC0	SARL2				SVA[6:0]				SVA0
RIIC0	SARU2	—	—	—	—	—	SVA[1:0]		FS
RIIC0	ICBRL	—	—	—			BRL[4:0]		
RIIC0	ICBRH	—	—	—			BRH[4:0]		
RIIC0	ICDRT								
RIIC0	ICDRR								
RSP10	SPCR	SPRIE	SPE	SPTIE	SPEIE	MSTR	MODFEN	TXMD	SPMS

Table 4.2 List of I/O Registers (Bit Order) (29 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
GPT2	GTDLYCR	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLYEN	DLYRST	DLEN
GPT3	GTDLYCR	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLYEN	DLYRST	DLEN
GPT0	GTDLYRA	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT0	GTDLYRB	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT1	GTDLYRA	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT1	GTDLYRB	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT2	GTDLYRA	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT2	GTDLYRB	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT3	GTDLYRA	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT3	GTDLYRB	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT0	GTDLYFA	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT0	GTDLYFB	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT1	GTDLYFA	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT1	GTDLYFB	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT2	GTDLYRA	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT2	GTDLYFB	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT3	GTDLYFA	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT3	GTDLYFB	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
FLASH	FMODR	—	—	—	FRDMD	—	—	—	—
FLASH	FASTAT	ROMAE	—	—	CMDLK	DFLAE	—	DFLRPE	DFLWPE
FLASH	FAEINT	ROMAEIE	—	—	CMDLKIE	DFLAEIE	—	DFLRPEIE	DFLWPEIE
FLASH	FRDYIE	—	—	—	—	—	—	—	FRDYIE
FLASH	DFLRE0	KEY[7:0]							
		DBRE07	DBRE06	DBRE05	DBRE04	DBRE03	DBRE02	DBRE01	DBRE00
FLASH	DFLRE1	KEY[7:0]							
		DBRE15	DBRE14	DBRE13	DBRE12	DBRE11	DBRE10	DBRE09	DBRE08
FLASH	DFLWE0	KEY[7:0]							
		DBWE07	DBWE06	DBWE05	DBWE04	DBWE03	DBWE02	DBWE01	DBWE00
FLASH	DFLWE1	KEY[7:0]							
		DBWE15	DBWE14	DBWE13	DBWE12	DBWE11	DBWE10	DBWE09	DBWE08
FLASH	FCURAME	KEY[7:0]							
		—	—	—	—	—	—	—	FCRME

Table 5.2 DC Characteristics (1) (2 / 3)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	All output pins (except for P71 to P76 and P90 to P95)	V_{OH}	VCC-0.5	-	-	V	$I_{OH} = -1 \text{ mA}$
	P71 to P76		VCC-0.5	-	-		$I_{OH} = -1 \text{ mA}$ 64-pin LQFP Condition 3
			VCC-1.0	-	-		$I_{OH} = -5 \text{ mA}$ 64-pin LQFP Other than condition 3
	P90 to P95		VCC-0.5	-	-		$I_{OH} = -1 \text{ mA}$ 80-pin LQFP or 64-pin LQFP
			VCC-1.0	-	-		$I_{OH} = -5 \text{ mA}$ 112-pin LQFP or 100-pin LQFP
Output low voltage	All output pins (except for P71 to P76, P90 to P95, and RIIC)	V_{OL}	-	-	0.5	V	$I_{OL} = 1.0 \text{ mA}$
	P71 to P76		-	-	0.5		$I_{OL} = 1.0 \text{ mA}$ 64-pin LQFP Other than condition 3
			-	-	1.1		$I_{OL} = 15 \text{ mA}$ Conditions 1 and 2
			-	-	1.4		$I_{OL} = 15 \text{ mA}$ Other than 64-pin LQFP Condition 3
	P90 to P95		-	-	0.5		$I_{OL} = 1.0 \text{ mA}$ 80-pin LQFP or 64-pin LQFP
			-	-	1.1		$I_{OL} = 15 \text{ mA}$ 112-pin LQFP or 100-pin LQFP Conditions 1 and 2
			-	-	1.4		$I_{OL} = 1 \text{ mA}$ 112-pin LQFP or 100-pin LQFP Condition 3
	RIIC pin		-	-	0.4		$I_{OL} = 3 \text{ mA}$
			-	-	0.6		$I_{OL} = 6 \text{ mA}$
			-	-	1.0		
Input leakage current	RES#, MD pin, EMLE	$ I_{in} $	-	-	1.0	μA	$V_{in} = 0 \text{ V}$, $V_{in} = V_{CC}$
Three-state leakage current (off state)	Ports 1 to A, PB0, PB3 to PB7, D, E, G	$ I_{TSI} $	-	-	1.0	μA	$V_{in} = 0 \text{ V}$, $V_{in} = V_{CC}$
	Ports PB1 and PB2		-	-	5.0		

5.3 AC Characteristics

Table 5.6 Operation Frequency Value

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit
Operating frequency	System clock (ICLK)	f	8	-	100	MHz
	Peripheral module clock (PCLK)		8	-	50	

5.3.1 Clock Timing

Table 5.7 Clock Timing

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC
Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item	Symbol	Min.	Max.	Unit	Test Conditions
Oscillation settling time after reset (crystal)	t _{OSC1}	10	-	ms	Figure 5.1
Oscillation settling time after leaving software standby mode (crystal)	t _{OSC2}	10	-	ms	Figure 5.2
Oscillation settling time after leaving deep software standby mode (crystal)	t _{OSC3}	10	-	ms	Figure 5.3
EXTAL external clock output delay settling time	t _{DEXT}	1	-	ms	Figure 5.1
EXTAL external clock input low pulse width	t _{EXL}	35	-	ns	Figure 5.4
EXTAL external clock input high pulse width	t _{EXH}	35	-	ns	
EXTAL external clock rising time	t _{EXr}	-	5	ns	
EXTAL external clock falling time	t _{EXf}	-	5	ns	
On-chip oscillator (IWDTCCLK) oscillation frequency	f _{IWDTCCLK}	62.5	187.5	kHz	

Table 5.18 Comparator Characteristics

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Ta = Topr. Ta is the same under conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog input capacitance	Cin	-	-	6	pF	
REFH pin offset voltage	Voff	-	-	5	mV	
REFL pin offset voltage		-	-	5	mV	
REFH input voltage range	Vin	1.7	-	AVcc – 0.3	V	
REFL input voltage range		0.3	-	AVcc – 1.7	V	
REFH reply time	tCR	-	-	1	μs	
REFL reply time	tCF	-	-	1	μs	

5.7 ROM (Flash Memory for Code Storage) Characteristics

Table 5.21 ROM (Flash Memory for Code Storage) Characteristics (1)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Temperature range for the programming/erasure operation:

Ta = Topr. Ta is the same under conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Rewrite/erase cycle ^{*1}	N _{PEC}	1000	—	—	Times	
Data hold time	t _{DRP}	30 ^{*2}	—	—	Year	Ta = +85C°

Note 1. Definition of rewrite/erase cycle:

The rewrite/erase cycle is the number of erasing for each block. When the rewrite/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 256-byte writing is performed 16 times for different addresses in 4-Kbyte block and then the entire block is erased, the rewrite/erase cycle is counted as one. However, writing to the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. The value is obtained from the reliability test.

Table 5.22 ROM (Flash Memory for Code Storage) Characteristics (2)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Temperature range for the programming/erasure operation:

Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Programming time	256 bytes	t _{P256}	—	2	12	ms	PCLK = 50 MHz N _{PEC} ≤ 100
	4 Kbytes	t _{P4K}	—	23	50	ms	
	16 Kbytes	t _{P16K}	—	90	200	ms	
	256 byte	t _{P256}	—	2.4	14.4	ms	PCLK = 50 MHz N _{PEC} > 100
	4 Kbytes	t _{P4K}	—	27.6	60	ms	
	16 Kbytes	t _{P16K}	—	108	240	ms	
Erasure time	4 Kbytes	t _{E4K}	—	25	60	ms	PCLK = 50 MHz N _{PEC} ≤ 100
	16 Kbytes	t _{E16K}	—	100	240	ms	
	4 Kbytes	t _{E4K}	—	30	72	ms	PCLK = 50 MHz N _{PEC} > 100
	16 Kbytes	t _{E16K}	—	120	288	ms	
Suspend delay time during writing		t _{SPD}	—	—	120	μs	Figure 5.24 PCLK = 50 MHz
First suspend delay time during erasing (in suspend priority mode)		t _{SESD1}	—	—	120	μs	
Second suspend delay time during erasing (in suspend priority mode)		t _{SESD2}	—	—	1.7	ms	
Suspend delay time during erasing (in erasure priority mode)		t _{SEED}	—	—	1.7	ms	

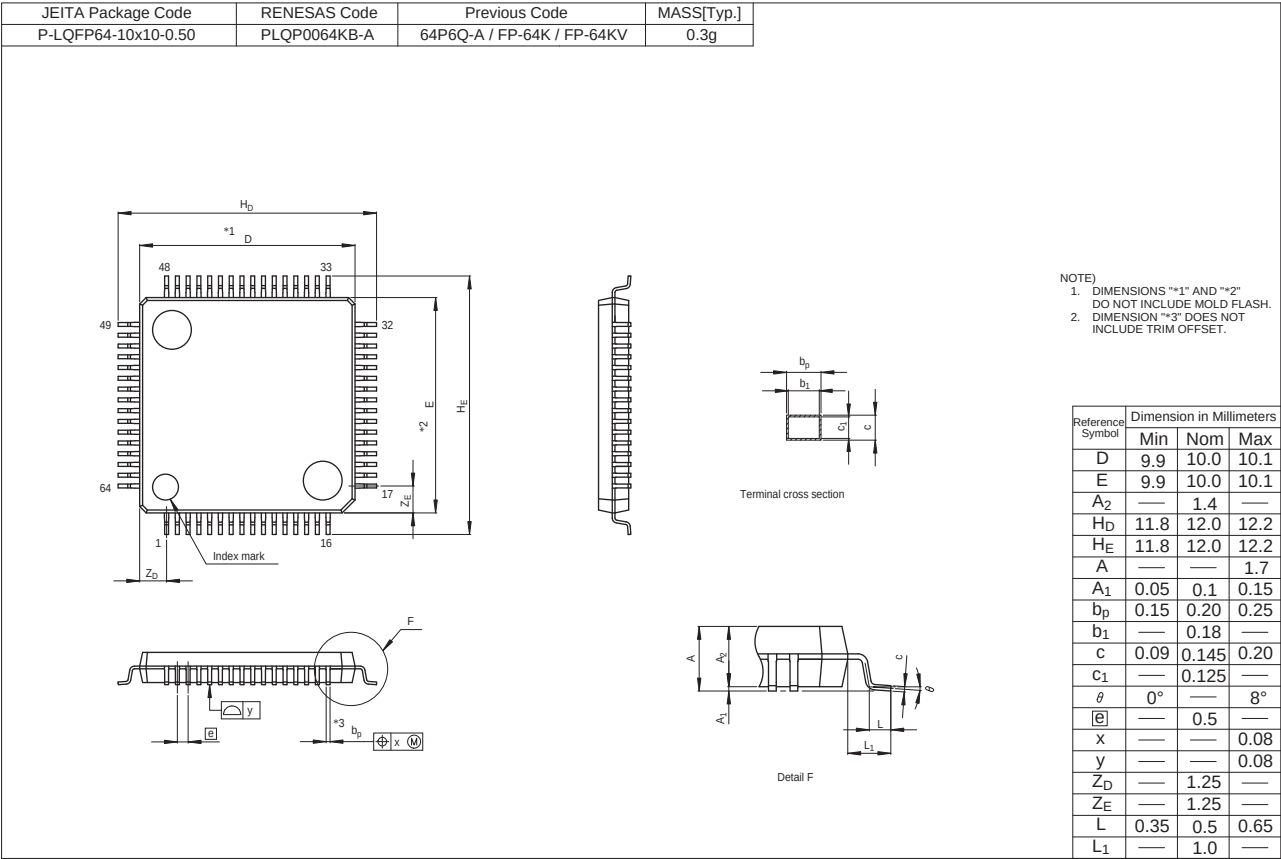


Figure D 64-Pin LQFP (PLQP0064KB-A) Package Dimensions