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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	44
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 4x10b, 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562t6adff-v3

Table 1.1 Outline of Specifications (2 / 5)

Classification	Module/Function	Description
Interrupt	Interrupt controller (ICU)	• Peripheral function interrupts: 101 sources • External interrupts: 9 (NMI and IRQ0 to IRQ7 pins) • Non-maskable interrupts: 3 (the NMI pin, oscillation stop detection interrupt, and voltage-monitoring interrupt) • 16 levels specifiable for the order of priority
Data transfer	Data transfer controller (DTC)	• Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
I/O ports	Programmable I/O ports	I/O port pins for devices in the 112-pin LQFP/100-pin LQFP/ 80-pin LQFP (R5F562TxGDFF)/80-pin LQFP (except R5F562TxGDFF)/64-pin LQFP • I/O: 61/55/44/44/37 • Input only: 21/21/13/13/9 • Open-drain outputs: 2/2/2/2/2 (I^2C bus interface pins) • Large-current outputs: 12/12/12/6/6(0) (MTU3 and GPT pins) The 5-V version of the 64-pin product does not have large-current outputs. • Reading out the states of pins is always possible.
Timers	Multi-function timer pulse unit 3 (MTU3)	• 16 bits x 8 channels • Up to 24 pulse inputs/outputs and three pulse inputs • Select from among six to eight counter-input clock signals for each channel (ICLK/1, ICLK/4, ICLK/16, ICLK/64, ICLK/256, ICLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available. • 24 output compare or input capture registers • Counter clearing (clearing is synchronizable with compare match or input capture) • Simultaneous writing to multiple timer counters (TCNT) • Input to and output from all registers in synchronization with counter operation • Buffered operation • Cascade-connected operation • 38 kinds of interrupt source • Automatic transfer of register data • Pulse output modes Toggled, PWM, complementary PWM, and reset synchronous PWM • Complementary PWM output mode Outputs non-overlapping waveforms for controlling 3-phase inverters Automatic specification of dead times PWM duty cycle: Selectable as any value from 0% to 100% Delay can be applied to requests for A/D conversion. Non-generation of interrupt requests at peak or trough values of counters can be selected. Double buffering • Reset-synchronous PWM mode Three PWM waveforms and corresponding inverse waveforms are output with the desired duty cycles. • Phase-counting mode • Counter functionality for dead-time compensation • Generation of triggers for A/D converters • Differential timing for initiation of A/D conversion
	Port output enable 3 (POE3)	• Control of the high-impedance state of the MTU3 and GPT's waveform output pins 5 pins for input from signal sources: POE0, POE4, POE8, POE10, POE11 Initiation on detection of short-circuited outputs (detection of simultaneous switching of large-current pins to the active level) Initiation by comparator-detection of analog level input to the 12-bit A/D converter Initiation by oscillation-stoppage detection Initiation by software • Selection of which output pins should be placed in the high-impedance state at the time of each POE input or comparator detection

Table 1.1 Outline of Specifications (3 / 5)

Classification	Module/Function	Description
Timers	General PWM timer (GPT/GPTa)	• 16 bits x 4 channels • Counting up or down (saw-wave), counting up and down (triangle-wave) selectable for all channels • Clock sources independently selectable for all channels • 2 input/output pins per channel • 2 output compare/input capture registers per channel • For the 2 output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally asymmetrically PWM waveforms. • Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow) • Synchronizable operation of the several counters • Modes of synchronized operation (synchronized, or displaced by desired times for phase shifting) • Generation of dead times in PWM operation • Through combination of three counters, generation of automatic three-phase PWM waveforms incorporating dead times • Starting, clearing, and stopping counters in response to external or internal triggers • Internal trigger sources: output of the internal comparator detection, software, and compare-match • The frequency-divided system clock (ICLK) can be used as a counter clock for measuring timing of the edges of signals produced by frequency-dividing the low-speed on-chip oscillator clock signal dedicated to IWDT (to detect abnormal oscillation). • PWM delay generation can control the timing with which signals on the two PWM output pins for each channel rise and fall with an accuracy of up to 1/32 times the period of the system clock (ICLK) (only for GPTa).
	Compare match timer (CMT)	• (16 bits x 2 channels) x 2 units • Select from among four internal clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Watchdog timer (WDT)	• 8 bits x 1 channel • Select from among eight counter-input clock signals (PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192, PCLK/32768, PCLK/131072) • Switchable between watchdog timer mode and interval timer mode
	Independent watchdog timer (IWDT)	• 14 bits x 1 channel • Counter-input clock: low-speed on-chip oscillator dedicated to IWDT
Communications	Serial communications interface (SCIb)	• 3 channels • Serial communications modes: Asynchronous, clock synchronous, and smart-card interface • Multiprocessor communications • On-chip baud rate generator allows selection of the desired bit rate • Choice of LSB-first or MSB-first transfer • Noise cancellation (only available in asynchronous mode)
	I^2C bus interface (RIIC)	• 1 channel • Communications formats I^2C bus format/SMBus format Master/slave selectable

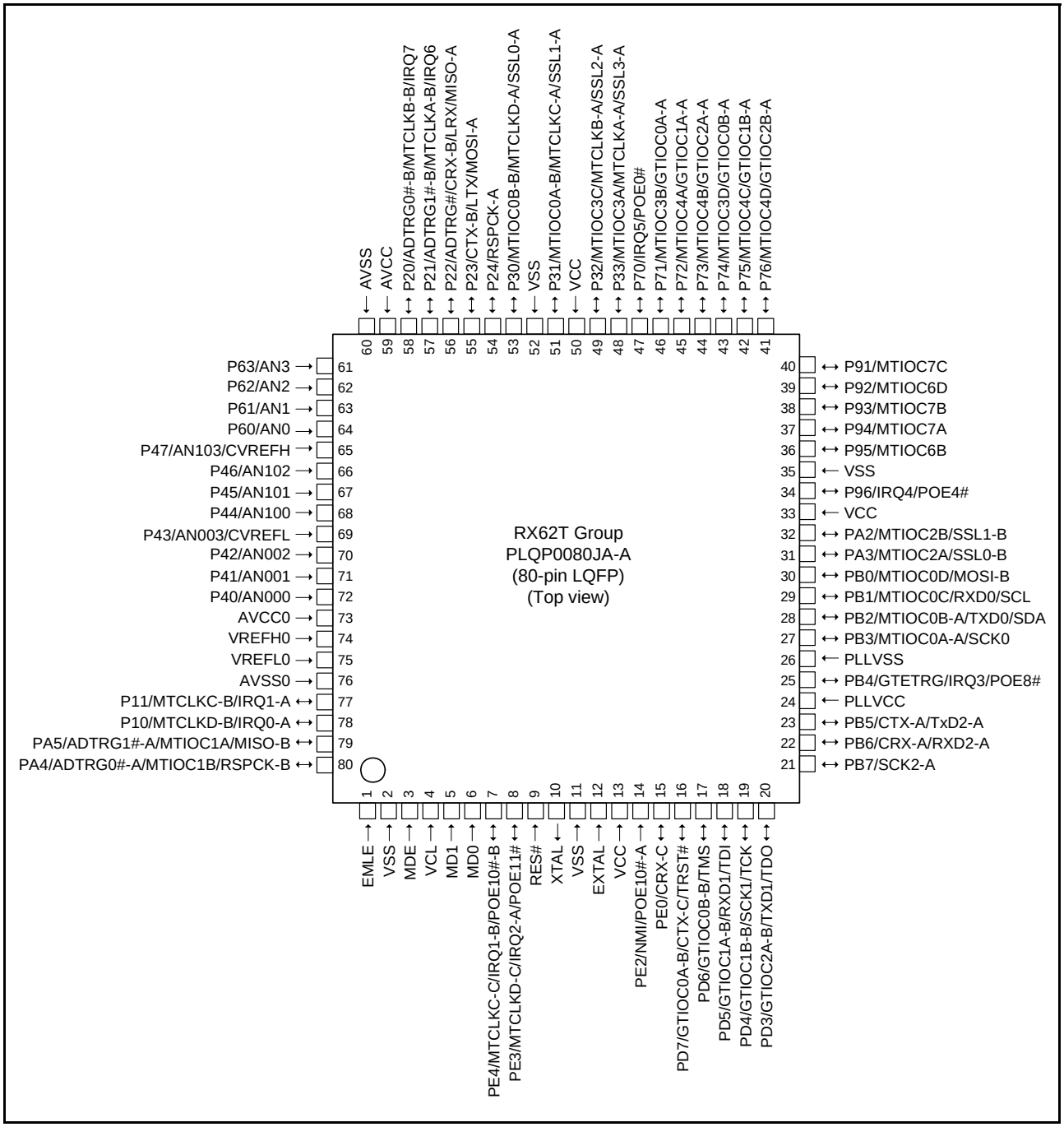


Figure 1.5 Pin Assignment of the 80-Pin LQFP

Table 1.8 List of Pins and Pin Functions (64-Pin LQFP) (1 / 2)

Pin No. (64-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi-cation	Interrupt	POE	Debugging
1	EMLE							
2	MDE							
3	VCL							
4	MD1							
5	MD0							
6	RES#							
7	XTAL							
8	VSS							
9	EXTAL							
10	VCC							
11		PE2				NMI	POE10#-A	
12		PD7		GTIOC0A-B				TRST#
13		PD6		GTIOC0B-B				TMS
14		PD5		GTIOC1A-B	RXD1			TDI
15		PD4		GTIOC1B-B	SCK1			TCK
16		PD3		GTIOC2A-B	TXD1			TDO
17		PB7			SCK2-A			
18		PB6			CRX-A/ RXD2-A			
19		PB5			CTX-A/ TXD2-A			
20	PLLVCC							
21		PB4		GTETRG		IRQ3	POE8#	
22	PLLVSS							
23		PB3		MTIOC0A-A	SCK0			
24		PB2		MTIOC0B-A	TXD0/SDA			
25		PB1		MTIOC0C	RXD0/SCL			
26		PB0		MTIOC0D	MOSI-B			
27		PA3		MTIOC2A	SSL0-B			
28		PA2		MTIOC2B	SSL1-B			
29		P94		MTIOC7A				
30		P93		MTIOC7B				
31		P92		MTIOC6D				
32		P91		MTIOC7C				
33		P76		MTIOC4D/ GTIOC2B-A				
34		P75		MTIOC4C/ GTIOC1B-A				
35		P74		MTIOC3D/ GTIOC0B-A				
36		P73		MTIOC4B/ GTIOC2A-A				
37		P72		MTIOC4A/ GTIOC1A-A				
38		P71		MTIOC3B/ GTIOC0A-A				
39		P70				IRQ5	POE0#	

Table 1.9 Pin Functions (2 / 4)

Classifications	Pin Name	I/O	Description
Multi-function timer pulse unit 3 (MTU3)	MTIOC0A-A/MTIOC0A-B MTIOC0B-A/MTIOC0B-B MTIOC0C, MTIOC0D	I/O	The MTU0.TGRA to MTU0.TGRD input capture input/output compare output/PWM output pins.
	MTIOC1A, MTIOC1B	I/O	The MTU1.TGRA and MTU1.TGRB input capture input/output compare output/PWM output pins.
	MTIOC2A, MTIOC2B	I/O	The MTU2.TGRA and MTU2.TGRB input capture input/output compare output/PWM output pins.
	MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D	I/O	The MTU3.TGRA and MTU3.TGRD input capture input/output compare output/PWM output pins. Pins MTIOC3B and MTIOC3D can be used for large-current output.
	MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D	I/O	The MTU4.TGRA and MTU4.TGRD input capture input/output compare output/PWM output pins. These pins can be used for large-current output.
	MTIC5U, MTIC5V, MTIC5W	Input	The MTU5.TGRU, MTU5.TGRV, and MTU5.TGRW input capture input/dead time compensation input pins. Not included in the 80-/64-pin versions.
	MTIOC6A, MTIOC6B MTIOC6C, MTIOC6D	I/O	The MTU6.TGRA to MTU6.TGRD input capture input/output compare output/PWM output pins. Pins MTIOC6B and MTIOC6D can be used for large-current output. The MTIOC6A/MTIOC6C pin is not included in the 80-pin version. The MTIOC6A/MTIOC6B/MTIOC6C pin is not included in the 64-pin version.
	MTIOC7A, MTIOC7B MTIOC7C, MTIOC7D	I/O	The MTU7.TGRA to MTU7.TGRD input capture input/output compare output/PWM output pins. These pins can be used for large-current output. The MTIOC7D pin is not included in the 80-/64-pin versions.
	MTCLKA-A/MTCLKA-B MTCLKB-A/MTCLKB-B MTCLKC-A/MTCLKC-B/ MTCLKC-C MTCLKD-A/MTCLKD-B/ MTCLKD-C	Input	Input pins for external clock signals. The MTCLKA-B/MTCLKB-B/MTCLKC-C/MTCLKD-C pin is not included in the 64-pin version.
General PWM timer (GPT)	GTIOC0A-A/GTIOC0A-B GTIOC0B-A/GTIOC0B-B	I/O	The GPT0.GTCCRA and GPT0.GTCCRB CCRB input capture input/output compare output/PWM output pins. Pins GTIOC0A-A and GTIOC0B-A can be used for large-current output.
	GTIOC1A-A/GTIOC1A-B GTIOC1B-A/GTIOC1B-B	I/O	The GPT1.GTCCRA and GPT1.GTCCRB input capture input/output compare output/PWM output pins. Pins GTIOC1A-A and GTIOC1B-A can be used for large-current output.
	GTIOC2A-A/GTIOC2A-B GTIOC2B-A/GTIOC2B-B	I/O	The GPT2.GTCCRA and GPT2.GTCCRB input capture input/output compare output/PWM output pins. Pins GTIOC2A-A and GTIOC2B-A can be used for large-current output. The GTIOC2B-B pin is not included in the 80-pin version.
	GTIOC3A, GTIOC3B	I/O	The GPT3.GTCCRA and GPT3.GTCCRB input capture input/output compare output/PWM output pins. Not included in the 80-/64-pin versions.
	GTETRG	Input	External trigger input pin for the GPT
Port output enable 3 (POE3)	POE0#, POE4#, POE8# POE10#-A/POE10#-B POE11#	Input	Input pins for request signals to place the MTU3 and GPT large-current pins in the high impedance state. The POE4#/POE10#-B/POE11# pin is not included in the 64-pin version.
Watchdog timer (WDT)	WDTOVF#	Output	Output pin for the counter-overflow signal in watchdog-timer mode. Not included in the 100-/80-/64-pin versions.

(a) Write to an I/O register.

(b) Read the value from the I/O register to a general register.

(c) Execute the operation using the value read.

(d) Execute the subsequent instruction.

[Instruction examples]

- Byte-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.B  #SFR_DATA, [R1]
CMP    [R1].UB, R1
;; Next process
```

- Word-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.W  #SFR_DATA, [R1]
CMP    [R1].W, R1
;; Next process
```

- Longword-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.L  #SFR_DATA, [R1]
CMP    [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

Table 4.1 List of I/O Registers (Address Order) (4 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 70BCh	ICU	Interrupt request register 188	IR188	8	8	2 ICLK
0008 70BDh	ICU	Interrupt request register 189	IR189	8	8	2 ICLK
0008 70BEh	ICU	Interrupt request register 190	IR190	8	8	2 ICLK
0008 70C0h	ICU	Interrupt request register 192	IR192	8	8	2 ICLK
0008 70C1h	ICU	Interrupt request register 193	IR193	8	8	2 ICLK
0008 70C2h	ICU	Interrupt request register 194	IR194	8	8	2 ICLK
0008 70C3h	ICU	Interrupt request register 195	IR195	8	8	2 ICLK
0008 70C4h	ICU	Interrupt request register 196	IR196	8	8	2 ICLK
0008 70D6h	ICU	Interrupt request register 214	IR214	8	8	2 ICLK
0008 70D7h	ICU	Interrupt request register 215	IR215	8	8	2 ICLK
0008 70D8h	ICU	Interrupt request register 216	IR216	8	8	2 ICLK
0008 70D9h	ICU	Interrupt request register 217	IR217	8	8	2 ICLK
0008 70DAh	ICU	Interrupt request register 218	IR218	8	8	2 ICLK
0008 70DBh	ICU	Interrupt request register 219	IR219	8	8	2 ICLK
0008 70DCh	ICU	Interrupt request register 220	IR220	8	8	2 ICLK
0008 70DDh	ICU	Interrupt request register 221	IR221	8	8	2 ICLK
0008 70DEh	ICU	Interrupt request register 222	IR222	8	8	2 ICLK
0008 70DFh	ICU	Interrupt request register 223	IR223	8	8	2 ICLK
0008 70E0h	ICU	Interrupt request register 224	IR224	8	8	2 ICLK
0008 70E1h	ICU	Interrupt request register 225	IR225	8	8	2 ICLK
0008 70F6h	ICU	Interrupt request register 246	IR246	8	8	2 ICLK
0008 70F7h	ICU	Interrupt request register 247	IR247	8	8	2 ICLK
0008 70F8h	ICU	Interrupt request register 248	IR248	8	8	2 ICLK
0008 70F9h	ICU	Interrupt request register 249	IR249	8	8	2 ICLK
0008 70FEh	ICU	Interrupt request register 254	IR254	8	8	2 ICLK
0008 711Bh	ICU	DTC activation enable register 027	DTCER027	8	8	2 ICLK
0008 711Ch	ICU	DTC activation enable register 028	DTCER028	8	8	2 ICLK
0008 711Dh	ICU	DTC activation enable register 029	DTCER029	8	8	2 ICLK
0008 711Eh	ICU	DTC activation enable register 030	DTCER030	8	8	2 ICLK
0008 711Fh	ICU	DTC activation enable register 031	DTCER031	8	8	2 ICLK
0008 712Dh	ICU	DTC activation enable register 045	DTCER045	8	8	2 ICLK
0008 712Eh	ICU	DTC activation enable register 046	DTCER046	8	8	2 ICLK
0008 7140h	ICU	DTC activation enable register 064	DTCER064	8	8	2 ICLK
0008 7141h	ICU	DTC activation enable register 065	DTCER065	8	8	2 ICLK
0008 7142h	ICU	DTC activation enable register 066	DTCER066	8	8	2 ICLK
0008 7143h	ICU	DTC activation enable register 067	DTCER067	8	8	2 ICLK
0008 7144h	ICU	DTC activation enable register 068	DTCER068	8	8	2 ICLK
0008 7145h	ICU	DTC activation enable register 069	DTCER069	8	8	2 ICLK
0008 7146h	ICU	DTC activation enable register 070	DTCER070	8	8	2 ICLK
0008 7147h	ICU	DTC activation enable register 071	DTCER071	8	8	2 ICLK
0008 7162h	ICU	DTC activation enable register 098	DTCER098	8	8	2 ICLK
0008 7166h	ICU	DTC activation enable register 102	DTCER102	8	8	2 ICLK
0008 7167h	ICU	DTC activation enable register 103	DTCER103	8	8	2 ICLK
0008 716Ah	ICU	DTC activation enable register 106	DTCER106	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (10 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 8250h	SCI2	Serial mode register	SMR*1	8	8	2, 3 PCLK*3
0008 8251h	SCI2	Bit rate register	BRR	8	8	2, 3 PCLK*3
0008 8252h	SCI2	Serial control register	SCR*1	8	8	2, 3 PCLK*3
0008 8253h	SCI2	Transmit data register	TDR	8	8	2, 3 PCLK*3
0008 8254h	SCI2	Serial status register	SSR*1	8	8	2, 3 PCLK*3
0008 8255h	SCI2	Receive data register	RDR	8	8	2, 3 PCLK*3
0008 8256h	SCI2	Smart card mode register	SCMR	8	8	2, 3 PCLK*3
0008 8257h	SCI2	Serial extended mode register	SEMR	8	8	2, 3 PCLK*3
0008 8250h	SMCI2	Serial mode register	SMR*1	8	8	2, 3 PCLK*3
0008 8251h	SMCI2	Bit rate register	BRR	8	8	2, 3 PCLK*3
0008 8252h	SMCI2	Serial control register	SCR*1	8	8	2, 3 PCLK*3
0008 8253h	SMCI2	Transmit data register	TDR	8	8	2, 3 PCLK*3
0008 8254h	SMCI2	Serial status register	SSR*1	8	8	2, 3 PCLK*3
0008 8255h	SMCI2	Receive data register	RDR	8	8	2, 3 PCLK*3
0008 8256h	SMCI2	Smart card mode register	SCMR	8	8	2, 3 PCLK*3
0008 8280h	CRC	CRC control register	CRCCR	8	8	2, 3 PCLK*3
0008 8281h	CRC	CRC data input register	CRCDIR	8	8	2, 3 PCLK*3
0008 8282h	CRC	CRC data output register	CRCDOR	16	16	2, 3 PCLK*3
0008 8300h	RIIC	I2C bus control register 1	ICCR1	8	8	2, 3 PCLK*3
0008 8301h	RIIC	I2C bus control register 2	ICCR2	8	8	2, 3 PCLK*3
0008 8302h	RIIC	I2C bus mode register 1	ICMR1	8	8	2, 3 PCLK*3
0008 8303h	RIIC	I2C bus mode register 2	ICMR2	8	8	2, 3 PCLK*3
0008 8304h	RIIC	I2C bus mode register 3	ICMR3	8	8	2, 3 PCLK*3
0008 8305h	RIIC	I2C bus function enable register	ICFER	8	8	2, 3 PCLK*3
0008 8306h	RIIC	I2C bus status enable register	ICSER	8	8	2, 3 PCLK*3
0008 8307h	RIIC	I2C bus interrupt enable register	ICIER	8	8	2, 3 PCLK*3
0008 8308h	RIIC	I2C bus status register 1	ICSR1	8	8	2, 3 PCLK*3
0008 8309h	RIIC	I2C bus status register 2	ICSR2	8	8	2, 3 PCLK*3
0008 830Ah	RIIC	Slave address register L0	SARL0	8	8	2, 3 PCLK*3
0008 830Ah	RIIC	Internal counter L for timeout	TMOCNTL	8	8	2, 3 PCLK*3
0008 830Bh	RIIC	Slave address register U0	SARU0	8	8	2, 3 PCLK*3
0008 830Bh	RIIC	Internal counter U for timeout	TMOCNTU	8	8	2, 3 PCLK*3
0008 830Bh	RIIC	Slave address register U0	SARU0	8	8	2, 3 PCLK*3
0008 830Ch	RIIC	Slave address register L1	SARL1	8	8	2, 3 PCLK*3
0008 830Dh	RIIC	Slave address register U1	SARU1	8	8	2, 3 PCLK*3
0008 830Eh	RIIC	Slave address register L2	SARL2	8	8	2, 3 PCLK*3
0008 830Fh	RIIC	Slave address register U2	SARU2	8	8	2, 3 PCLK*3
0008 8310h	RIIC	I2C bus bit rate low-level register	ICBRL	8	8	2, 3 PCLK*3
0008 8311h	RIIC	I2C bus bit rate high-level register	ICBRH	8	8	2, 3 PCLK*3
0008 8312h	RIIC	I2C bus transmit data register	ICDRT	8	8	2, 3 PCLK*3
0008 8313h	RIIC	I2C bus receive data register	ICDRR	8	8	2, 3 PCLK*3
0008 8380h	RSPI	RSPI control register	SPCR	8	8	2, 3 PCLK*3
0008 8381h	RSPI	RSPI slave select polarity register	SSLP	8	8	2, 3 PCLK*3
0008 8382h	RSPI	RSPI pin control register	SPPCR	8	8	2, 3 PCLK*3

Table 4.1 List of I/O Registers (Address Order) (11 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 8383h	RSPI	RSPI status register	SPSR	8	8	2, 3 PCLK*3
0008 8384h	RSPI	RSPI data register	SPDR	16, 32	16, 32	2, 3 PCLK*3
0008 8388h	RSPI	RSPI sequence control register	SPSCR	8	8	2, 3 PCLK*3
0008 8389h	RSPI	RSPI sequence status register	SPSSR	8	8	2, 3 PCLK*3
0008 838Ah	RSPI	RSPI bit rate register	SPBR	8	8	2, 3 PCLK*3
0008 838Bh	RSPI	RSPI data control register	SPDCR	8	8	2, 3 PCLK*3
0008 838Ch	RSPI	RSPI clock delay register	SPCKD	8	8	2, 3 PCLK*3
0008 838Dh	RSPI	RSPI slave select negation delay register	SSLND	8	8	2, 3 PCLK*3
0008 838Eh	RSPI	RSPI next-access delay register	SPND	8	8	2, 3 PCLK*3
0008 838Fh	RSPI	RSPI control register 2	SPCR2	8	8	2, 3 PCLK*3
0008 8390h	RSPI	RSPI command register 0	SPCMD0	16	16	2, 3 PCLK*3
0008 8392h	RSPI	RSPI command register 1	SPCMD1	16	16	2, 3 PCLK*3
0008 8394h	RSPI	RSPI command register 2	SPCMD2	16	16	2, 3 PCLK*3
0008 8396h	RSPI	RSPI command register 3	SPCMD3	16	16	2, 3 PCLK*3
0008 8398h	RSPI	RSPI command register 4	SPCMD4	16	16	2, 3 PCLK*3
0008 839Ah	RSPI	RSPI command register 5	SPCMD5	16	16	2, 3 PCLK*3
0008 839Ch	RSPI	RSPI command register 6	SPCMD6	16	16	2, 3 PCLK*3
0008 839Eh	RSPI	RSPI command register 7	SPCMD7	16	16	2, 3 PCLK*3
0008 9000h	S12AD0	A/D control register	ADCSR	8	8	2, 3 PCLK*3
0008 9004h	S12AD0	A/D channel select register	ADANS	16	16	2, 3 PCLK*3
0008 900Ah	S12AD0	A/D programmable gain amplifier register	ADPG	16	16	2, 3 PCLK*3
0008 900Eh	S12AD0	A/D control extended register	ADCER	16	16	2, 3 PCLK*3
0008 9010h	S12AD0	A/D start trigger select register	ADSTRGR	16	16	2, 3 PCLK*3
0008 9012h	S12AD	Comparator operating mode select register 0	ADCMPMD0	16	16	2, 3 PCLK*3
0008 9014h	S12AD	Comparator operating mode select register 1	ADCMPMD1	16	16	2, 3 PCLK*3
0008 9016h	S12AD	Comparator filter mode register 0	ADCMPNR0	16	16	2, 3 PCLK*3
0008 9018h	S12AD	Comparator filter mode register 1	ADCMPNR1	16	16	2, 3 PCLK*3
0008 901Ah	S12AD	Comparator detection flag register	ADCMPFR	8	8	2, 3 PCLK*3
0008 901Ch	S12AD	Comparator interrupt select register	ADCMPSEL	16	16	2, 3 PCLK*3
0008 901Eh	S12AD0	A/D data register Diag	ADRD	16	16	2, 3 PCLK*3
0008 9020h	S12AD0	A/D data register 0A	ADDR0A	16	16	2, 3 PCLK*3
0008 9022h	S12AD0	A/D data register 1	ADDR1	16	16	2, 3 PCLK*3
0008 9024h	S12AD0	A/D data register 2	ADDR2	16	16	2, 3 PCLK*3
0008 9026h	S12AD0	A/D data register 3	ADDR3	16	16	2, 3 PCLK*3
0008 9030h	S12AD0	A/D data register 0B	ADDR0B	16	16	2, 3 PCLK*3
0008 9060h	S12AD0	A/D sampling state register	ADSSTR	8	8	2, 3 PCLK*3
0008 9080h	S12AD1	A/D control register	ADCSR	8	8	2, 3 PCLK*3
0008 9084h	S12AD1	A/D channel select register	ADANS	16	16	2, 3 PCLK*3
0008 908Ah	S12AD1	A/D programmable gain amplifier register	ADPG	16	16	2, 3 PCLK*3
0008 908Eh	S12AD1	A/D control extended register	ADCER	16	16	2, 3 PCLK*3
0008 9090h	S12AD1	A/D start trigger select register	ADSTRGR	16	16	2, 3 PCLK*3
0008 909Eh	S12AD1	A/D data register Diag	ADRD	16	16	2, 3 PCLK*3
0008 90A0h	S12AD1	A/D data register 0A	ADDR0A	16	16	2, 3 PCLK*3
0008 90A2h	S12AD1	A/D data register 1	ADDR1	16	16	2, 3 PCLK*3

Table 4.1 List of I/O Registers (Address Order) (15 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0009 041Ch	CAN0*2	Mask register 7	MKR7	32	8, 16, 32	2, 3 PCLK*3
0009 0420h	CAN0*2	FIFO received ID compare register 0	FIDCR0	32	8, 16, 32	2, 3 PCLK*3
0009 0424h	CAN0*2	FIFO received ID compare register 1	FIDCR1	32	8, 16, 32	2, 3 PCLK*3
0009 0428h	CAN0*2	Mask invalid register	MKIVLR	32	8, 16, 32	2, 3 PCLK*3
0009 042Ch	CAN0*2	Mailbox interrupt enable register	MIER	32	8, 16, 32	2, 3 PCLK*3
0009 0820h to 0009 083Fh	CAN0*2	Message control registers 0 to 31	MCTL0 to MCTL31	8	8	2, 3 PCLK*3
0009 0840h	CAN0*2	Control register	CTLR	16	8, 16	2, 3 PCLK*3
0009 0842h	CAN0*2	Status register	STR	16	8, 16	2, 3 PCLK*3
0009 0844h	CAN0*2	Bit configuration register	BCR	32	8, 16, 32	2, 3 PCLK*3
0009 0848h	CAN0*2	Receive FIFO control register	RFCR	8	8	2, 3 PCLK*3
0009 0849h	CAN0*2	Receive FIFO pointer control register	RFPCR	8	8	2, 3 PCLK*3
0009 084Ah	CAN0*2	Transmit FIFO control register	TFCR	8	8	2, 3 PCLK*3
0009 084Bh	CAN0*2	Transmit FIFO pointer control register	TFPCR	8	8	2, 3 PCLK*3
0009 084Ch	CAN0*2	Error interrupt enable register	EIER	8	8	2, 3 PCLK*3
0009 084Dh	CAN0*2	Error interrupt factor judge register	EIFR	8	8	2, 3 PCLK*3
0009 084Eh	CAN0*2	Receive error count register	RECR	8	8	2, 3 PCLK*3
0009 084Fh	CAN0*2	Transmit error count register	TECR	8	8	2, 3 PCLK*3
0009 0850h	CAN0*2	Error code store register	ECSR	8	8	2, 3 PCLK*3
0009 0851h	CAN0*2	Channel search support register	CSSR	8	8	2, 3 PCLK*3
0009 0852h	CAN0*2	Mailbox search status register	MSSR	8	8	2, 3 PCLK*3
0009 0853h	CAN0*2	Mailbox search mode register	MSMR	8	8	2, 3 PCLK*3
0009 0854h	CAN0*2	Time stamp register	TSR	16	8, 16	2, 3 PCLK*3
0009 0856h	CAN0*2	Acceptance filter support register	AFSR	16	8, 16	2, 3 PCLK*3
0009 0858h	CAN0*2	Test control register	TCR	8	8	2, 3 PCLK*3
0009 4001h	LIN0	LIN wake-up baud rate select register	LWBR	8	8	2, 3 PCLK*3
0009 4002h	LIN0	LIN baud rate prescaler 0 register	LBRP0	8	8, 16	2, 3 PCLK*3
0009 4003h	LIN0	LIN baud rate prescaler 1 register	LBRP1	8	8, 16	2, 3 PCLK*3
0009 4004h	LIN0	LIN self-test control register	LSTC	8	8	2, 3 PCLK*3
0009 4008h	LIN0	Mode register	L0MD	8	8, 16, 32	2, 3 PCLK*3
0009 4009h	LIN0	Break field setting register	L0BRK	8	8, 16, 32	2, 3 PCLK*3
0009 400Ah	LIN0	Space setting register	L0SPC	8	8, 16, 32	2, 3 PCLK*3
0009 400Bh	LIN0	Wake-up setting register	L0WUP	8	8, 16, 32	2, 3 PCLK*3
0009 400Ch	LIN0	Interrupt enable register	L0IE	8	8, 16	2, 3 PCLK*3
0009 400Dh	LIN0	Error detection enable register	L0EDE	8	8, 16	2, 3 PCLK*3
0009 400Eh	LIN0	Control register	L0C	8	8	2, 3 PCLK*3
0009 4010h	LIN0	Transmission control register	L0TC	8	8, 16, 32	2, 3 PCLK*3
0009 4011h	LIN0	Mode status register	L0MST	8	8, 16, 32	2, 3 PCLK*3
0009 4012h	LIN0	Status register	L0ST	8	8, 16, 32	2, 3 PCLK*3
0009 4013h	LIN0	Error status register	L0EST	8	8, 16, 32	2, 3 PCLK*3
0009 4014h	LIN0	Response field set register	L0RFC	8	8, 16	2, 3 PCLK*3
0009 4015h	LIN0	Buffer register	L0IDB	8	8, 16	2, 3 PCLK*3
0009 4016h	LIN0	Check sum buffer register	L0CBR	8	8	2, 3 PCLK*3
0009 4018h	LIN0	Data 1 buffer register	L0DB1	8	8, 16, 32	2, 3 PCLK*3

Table 4.1 List of I/O Registers (Address Order) (20 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000C 200Ah	GPT	General PWM timer hardware stop/clear source select register	GTHPSR	16	8, 16, 32	3 to 5 ICLK*4
000C 200Ch	GPT	General PWM timer write-protection register	GTWP	16	8, 16, 32	3 to 5 ICLK*4
000C 200Eh	GPT	General PWM timer sync register	GTSYNC	16	8, 16, 32	3 to 5 ICLK*4
000C 2010h	GPT	General PWM timer external trigger input interrupt register	GTETINT	16	8, 16, 32	3 to 5 ICLK*4
000C 2014h	GPT	General PWM timer buffer operation disable register	GTBDR	16	8, 16, 32	3 to 5 ICLK*4
000C 2018h	GPT	General PWM timer start write protection register	GTSWP	16	16, 32	3 to 5 ICLK*4
000C 2080h	GPT	LOCO count control register	LCCR	16	8, 16, 32	3 to 5 ICLK*4
000C 2082h	GPT	LOCO count status register	LCST	16	8, 16, 32	3 to 5 ICLK*4
000C 2084h	GPT	LOCO count value register	LCNT	16	8, 16, 32	3 to 5 ICLK*4
000C 2086h	GPT	LOCO count result average register	LCNTA	16	8, 16, 32	3 to 5 ICLK*4
000C 2088h	GPT	LOCO count result register 0	LCNT00	16	8, 16, 32	3 to 5 ICLK*4
000C 208Ah	GPT	LOCO count result register 1	LCNT01	16	8, 16, 32	3 to 5 ICLK*4
000C 208Ch	GPT	LOCO count result register 2	LCNT02	16	8, 16, 32	3 to 5 ICLK*4
000C 208Eh	GPT	LOCO count result register 3	LCNT03	16	8, 16, 32	3 to 5 ICLK*4
000C 2090h	GPT	LOCO count result register 4	LCNT04	16	8, 16, 32	3 to 5 ICLK*4
000C 2092h	GPT	LOCO count result register 5	LCNT05	16	8, 16, 32	3 to 5 ICLK*4
000C 2094h	GPT	LOCO count result register 6	LCNT06	16	8, 16, 32	3 to 5 ICLK*4
000C 2096h	GPT	LOCO count result register 7	LCNT07	16	8, 16, 32	3 to 5 ICLK*4
'000C 2098h	GPT	LOCO count result register 8	LCNT08	16	8, 16, 32	3 to 5 ICLK*4
000C 209Ah	GPT	LOCO count result register 9	LCNT09	16	8, 16, 32	3 to 5 ICLK*4
000C 209Ch	GPT	LOCO count result register 10	LCNT10	16	8, 16, 32	3 to 5 ICLK*4
000C 209Eh	GPT	LOCO count result register 11	LCNT11	16	8, 16, 32	3 to 5 ICLK*4
000C 20A0h	GPT	LOCO count result register 12	LCNT12	16	8, 16, 32	3 to 5 ICLK*4
000C 20A2h	GPT	LOCO count result register 13	LCNT13	16	8, 16, 32	3 to 5 ICLK*4
000C 20A4h	GPT	LOCO count result register 14	LCNT14	16	8, 16, 32	3 to 5 ICLK*4
000C 20A6h	GPT	LOCO count result register 15	LCNT15	16	8, 16, 32	3 to 5 ICLK*4
000C 20A8h	GPT	LOCO count upper permissible deviation register	LCNTDU	16	8, 16, 32	3 to 5 ICLK*4
000C 20AAh	GPT	LOCO count lower permissible deviation register	LCNTDL	16	8, 16, 32	3 to 5 ICLK*4
000C 2100h	GPT0	General PWM timer I/O control register	GTIOR	16	8, 16, 32	3 to 5 ICLK*4
000C 2102h	GPT0	General PWM timer interrupt output setting register	GTINTAD	16	8, 16, 32	3 to 5 ICLK*4
000C 2104h	GPT0	General PWM timer control register	GTCR	16	8, 16, 32	3 to 5 ICLK*4
000C 2106h	GPT0	General PWM timer buffer enable register	GTBER	16	8, 16, 32	3 to 5 ICLK*4
000C 2108h	GPT0	General PWM timer count direction register	GTUDC	16	8, 16, 32	3 to 5 ICLK*4
000C 210Ah	GPT0	General PWM timer interrupt and A/D converter start request skipping setting register	GTITC	16	8, 16, 32	3 to 5 ICLK*4
000C 210Ch	GPT0	General PWM timer status register	GTST	16	8, 16, 32	3 to 5 ICLK*4
000C 210Eh	GPT0	General PWM timer counter	GTCNT	16	16	3 to 5 ICLK*4
000C 2110h	GPT0	General PWM timer compare capture register A	GTCCRA	16	16, 32	3 to 5 ICLK*4
000C 2112h	GPT0	General PWM timer compare capture register B	GTCCRB	16	16, 32	3 to 5 ICLK*4
000C 2114h	GPT0	General PWM timer compare capture register C	GTCCRC	16	16, 32	3 to 5 ICLK*4

Table 4.1 List of I/O Registers (Address Order) (24 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000C 22B6h	GPT3	General PWM timer dead time control register	GTDTCR	16	16, 32	3 to 5 ICLK*4
000C 22B8h	GPT3	General PWM timer dead time value register	GTDVU	16	16, 32	3 to 5 ICLK*4
000C 22BAh	GPT3	General PWM timer dead time value register	GTDVD	16	16, 32	3 to 5 ICLK*4
000C 22BCh	GPT3	General PWM timer dead time buffer register	GTDBU	16	16, 32	3 to 5 ICLK*4
000C 22BEh	GPT3	General PWM timer dead time buffer register	GTDBD	16	16, 32	3 to 5 ICLK*4
000C 22C0h	GPT3	General PWM timer output protection function status register	GTSOS	16	16, 32	3 to 5 ICLK*4
000C 22C2h	GPT3	General PWM timer output protection temporary release register	GTSOTR	16	16, 32	3 to 5 ICLK*4
000C 2300h	GPT0	PWM output delay control register	GTDLYCR	16	16, 32	3 to 5 ICLK*4
000C 2302h	GPT1	PWM output delay control register	GTDLYCR	16	16, 32	3 to 5 ICLK*4
000C 2304h	GPT2	PWM output delay control register	GTDLYCR	16	16, 32	3 to 5 ICLK*4
000C 2306h	GPT3	PWM output delay control register	GTDLYCR	16	16, 32	3 to 5 ICLK*4
000C 2318h	GPT0	GTIOCA rising output delay register	GTDLYRA	16	16, 32	3 to 5 ICLK*4
000C 231Ah	GPT0	GTIOCB rising output delay register	GTDLYRB	16	16, 32	3 to 5 ICLK*4
000C 231Ch	GPT1	GTIOCA rising output delay register	GTDLYRA	16	16, 32	3 to 5 ICLK*4
000C 231Eh	GPT1	GTIOCB rising output delay register	GTDLYRB	16	16, 32	3 to 5 ICLK*4
000C 2320h	GPT2	GTIOCA rising output delay register	GTDLYRA	16	16, 32	3 to 5 ICLK*4
000C 2322h	GPT2	GTIOCB rising output delay register	GTDLYRB	16	16, 32	3 to 5 ICLK*4
000C 2324h	GPT3	GTIOCA falling output delay register	GTDLYRA	16	16, 32	3 to 5 ICLK*4
000C 2326h	GPT3	GTIOCB falling output delay register	GTDLYRB	16	16, 32	3 to 5 ICLK*4
000C 2328h	GPT0	GTIOCA falling output delay register	GTDLYFA	16	16, 32	3 to 5 ICLK*4
000C 232Ah	GPT0	GTIOCB falling output delay register	GTDLYFB	16	16, 32	3 to 5 ICLK*4
000C 232Ch	GPT1	GTIOCA falling output delay register	GTDLYFA	16	16, 32	3 to 5 ICLK*4
000C 232Eh	GPT1	GTIOCB falling output delay register	GTDLYFB	16	16, 32	3 to 5 ICLK*4
000C 2330h	GPT2	GTIOCA falling output delay register	GTDLYFA	16	16, 32	3 to 5 ICLK*4
000C 2332h	GPT2	GTIOCB falling output delay register	GTDLYFB	16	16, 32	3 to 5 ICLK*4
000C 2334h	GPT3	GTIOCA falling output delay register	GTDLYFA	16	16, 32	3 to 5 ICLK*4
000C 2336h	GPT3	GTIOCB falling output delay register	GTDLYFB	16	16, 32	3 to 5 ICLK*4
007F C402h	FLASH	Flash mode register	FMODR	8	8	2, 3 PCLK*3
007F C410h	FLASH	Flash access status register	FASTAT	8	8	2, 3 PCLK*3
007F C411h	FLASH	Flash access error interrupt enable register	FAEINT	8	8	2, 3 PCLK*3
007F C412h	FLASH	Flash ready interrupt enable register	FRDYIE	8	8	2, 3 PCLK*3
007F C440h	FLASH	Data flash read enable register 0	DFLRE0	16	16	2, 3 PCLK*3
007F C442h	FLASH	Data flash read enable register 1	DFLRE1	16	16	2, 3 PCLK*3
007F C450h	FLASH	Data flash programming/erasure enable register 0	DFLWE0	16	16	2, 3 PCLK*3
007F C452h	FLASH	Data flash programming/erasure enable register 1	DFLWE1	16	16	2, 3 PCLK*3
007F C454h	FLASH	FCU RAM enable register	FCURAME	16	16	2, 3 PCLK*3
007F FFB0h	FLASH	Flash status register 0	FSTATR0	8	8	2, 3 PCLK*3
007F FFB1h	FLASH	Flash status register 1	FSTATR1	8	8	2, 3 PCLK*3
007F FFB2h	FLASH	Flash P/E mode entry register	FENTRYR	16	16	2, 3 PCLK*3
007F FFB4h	FLASH	Flash protect register	FPROTR	16	16	2, 3 PCLK*3
007F FFB6h	FLASH	Flash reset register	FRESETR	16	16	2, 3 PCLK*3

4.2 I/O Register Bits

Register addresses and bit names of the peripheral modules are described below.
Each line cover eight bits, and 16-bit and 32-bit registers are shown as 2 or 4 lines, respectively.

Table 4.2 List of I/O Registers (Bit Order) (1 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
SYSTEM	MDMONR	—	—	—	—	—	—	—	—
		MDE	—	—	—	—	—	MD1	MD0
SYSTEM	MDSR	—	—	—	—	—	—	—	—
		—	—	—	BOTS	—	—	—	IROM
SYSTEM	SYSCR0	KEY[7:0]							
		—	—	—	—	—	—	—	ROME
SYSTEM	SYSCR1	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	RAME
SYSTEM	SBYCR	SSBY	—	—			STS[4:0]		
		—	—	—	—	—	—	—	—
SYSTEM	MSTPCRA	ACSE	—	—	MSTPA28	—	—	—	MSTPA24
		MSTPA23	—	—	—	—	—	MSTPA17	MSTPA16
		MSTPA15	MSTPA14	—	—	—	—	MSTPA9	—
		MSTPA7	—	—	—	—	—	—	—
SYSTEM	MSTPCRB	MSTPB31	MSTPB30	MSTPB29	—	—	—	—	—
		MSTPB23	—	MSTPB21	—	—	—	MSTPB17	—
		—	—	—	—	—	—	—	—
		MSTPB7	—	—	—	—	—	—	MSTPB0
SYSTEM	MSTPCRC	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	MSTPC0
SYSTEM	SCKCR	—	—	—	—			ICK[3:0]	
		—	—	—	—	—	—	—	—
		—	—	—	—			PCK[3:0]	
		—	—	—	—	—	—	—	—
SYSTEM	OSTDCR	KEY[7:0]							
		OSTDE	OSTDF	—	—	—	—	—	—
BSC	BERCLR	—	—	—	—	—	—	—	STSCLR
BSC	BEREN	—	—	—	—	—	—	—	IGAEN
BSC	BERSR1	—		MST[2:0]		—	—	—	IA
BSC	BERSR2	ADDR[12:0]							
				ADDR[12:0]			—	—	—
DTC	DTCCR	—	—	—	RRS	—	—	—	—
DTC	DTCVBR								
DTC	DTCADMOD	—	—	—	—	—	—	—	SHORT
DTC	DTCST	—	—	—	—	—	—	—	DTCST
DTC	DTCSTS	ACT	—	—	—	—	—	—	—
					VECN[7:0]				
MPU	RSPAGE0				RSPN[27:0]				
					RSPN[27:0]				
					RSPN[27:0]				
				RSPN[27:0]		—	—	—	—

Table 4.2 List of I/O Registers (Bit Order) (8 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
ICU	IPR03	—	—	—	—	IPR[3:0]			
ICU	IPR04	—	—	—	—	IPR[3:0]			
ICU	IPR05	—	—	—	—	IPR[3:0]			
ICU	IPR06	—	—	—	—	IPR[3:0]			
ICU	IPR07	—	—	—	—	IPR[3:0]			
ICU	IPR14	—	—	—	—	IPR[3:0]			
ICU	IPR18	—	—	—	—	IPR[3:0]			
ICU	IPR20	—	—	—	—	IPR[3:0]			
ICU	IPR21	—	—	—	—	IPR[3:0]			
ICU	IPR22	—	—	—	—	IPR[3:0]			
ICU	IPR23	—	—	—	—	IPR[3:0]			
ICU	IPR24	—	—	—	—	IPR[3:0]			
ICU	IPR25	—	—	—	—	IPR[3:0]			
ICU	IPR26	—	—	—	—	IPR[3:0]			
ICU	IPR27	—	—	—	—	IPR[3:0]			
ICU	IPR40	—	—	—	—	IPR[3:0]			
ICU	IPR44	—	—	—	—	IPR[3:0]			
ICU	IPR48	—	—	—	—	IPR[3:0]			
ICU	IPR49	—	—	—	—	IPR[3:0]			
ICU	IPR51	—	—	—	—	IPR[3:0]			
ICU	IPR52	—	—	—	—	IPR[3:0]			
ICU	IPR53	—	—	—	—	IPR[3:0]			
ICU	IPR54	—	—	—	—	IPR[3:0]			
ICU	IPR55	—	—	—	—	IPR[3:0]			
ICU	IPR56	—	—	—	—	IPR[3:0]			
ICU	IPR57	—	—	—	—	IPR[3:0]			
ICU	IPR58	—	—	—	—	IPR[3:0]			
ICU	IPR59	—	—	—	—	IPR[3:0]			
ICU	IPR5A	—	—	—	—	IPR[3:0]			
ICU	IPR5B	—	—	—	—	IPR[3:0]			
ICU	IPR5C	—	—	—	—	IPR[3:0]			
ICU	IPR5D	—	—	—	—	IPR[3:0]			
ICU	IPR5E	—	—	—	—	IPR[3:0]			
ICU	IPR5F	—	—	—	—	IPR[3:0]			
ICU	IPR60	—	—	—	—	IPR[3:0]			
ICU	IPR67	—	—	—	—	IPR[3:0]			
ICU	IPR68	—	—	—	—	IPR[3:0]			
ICU	IPR69	—	—	—	—	IPR[3:0]			
ICU	IPR6A	—	—	—	—	IPR[3:0]			
ICU	IPR6B	—	—	—	—	IPR[3:0]			
ICU	IPR6C	—	—	—	—	IPR[3:0]			
ICU	IPR6D	—	—	—	—	IPR[3:0]			
ICU	IPR6E	—	—	—	—	IPR[3:0]			
ICU	IPR6F	—	—	—	—	IPR[3:0]			
ICU	IPR80	—	—	—	—	IPR[3:0]			
ICU	IPR81	—	—	—	—	IPR[3:0]			
ICU	IPR82	—	—	—	—	IPR[3:0]			
ICU	IPR88	—	—	—	—	IPR[3:0]			
ICU	IPR89	—	—	—	—	IPR[3:0]			
ICU	IPR8A	—	—	—	—	IPR[3:0]			
ICU	IPR8B	—	—	—	—	IPR[3:0]			
ICU	IPR90	—	—	—	—	IPR[3:0]			

5.2 DC Characteristics

Table 5.2 DC Characteristics (1) (1 / 3)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	CAN input pin IRQ input pin MTU3 input pin POE3 input pin SCI input pin A/D trigger input pin NMI input pin GPT input pin LIN input pin RES#	V_{IH}	VCC×0.8	-	VCC+0.3	V	
		V_{IL}	-0.3	-	VCC×0.2		
		ΔV_T	VCC ×0.06	-	-		
	RIIC input pin (IICBus)	V_{IH}	VCC×0.7	-	VCC+0.3		
		V_{IL}	-0.3	-	VCC×0.3		
		ΔV_T	VCC ×0.05	-	-		
	Port 4*1 (also usable as an analog port)	V_{IH}	AVCC0 ×0.8	-	AVCC0 +0.3		
		V_{IL}	- 0.3	-	AVCC0 ×0.2		
		ΔV_T	AVCC0 ×0.06	-	-		
	Ports 5 and 6*1 (also usable as analog ports)	V_{IH}	AVCC ×0.8	-	AVCC +0.3		
		V_{IL}	-0.3	-	AVCC ×0.2		
		ΔV_T	AVCC ×0.06	-	-		
	Ports 1 to 3*1 Ports 7 to B*1 Ports D, E, and G*1	V_{IH}	VCC×0.8	-	VCC+0.3		
		V_{IL}	-0.3	-	VCC×0.2		
		ΔV_T	VCC ×0.06	-	-		
Input high voltage (except Schmitt trigger input pin)	MD pin, EMLE	V_{IH}	VCC×0.9	-	VCC+0.3	V	
	EXTAL RSPI input pin		VCC×0.8		VCC+0.3		
	RIIC input pin (SMBus)		2.1		VCC+0.3		Conditions 1 and 2
Input low voltage (except Schmitt trigger input pin)	MD pin, EMLE	V_{IL}	-0.3	-	VCC×0.1	V	
	EXTAL RSPI input pin		-0.3	-	VCC×0.2		
	RIIC input pin (SMBus)		-0.3	-	0.8		Conditions 1 and 2

5.3.3 Timing of On-Chip Peripheral Modules

Table 5.9 Timing of On-Chip Peripheral Modules (1)

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item			Symbol	Min.	Typ.	Max.	Unit
SCI	Input clock cycle	Asynchronous	t_{Scyc}	$4 \times t_{Pcyc}$	-	ns	Figure 5.8
		Clock synchronous		$6 \times t_{Pcyc}$	-		
	Input clock pulse width		t_{SCKW}	$0.4 \times t_{Pcyc}$	$0.6 \times t_{Scyc}$	ns	
	Input clock rise time		t_{SCKr}	-	20	ns	
	Input clock fall time		t_{SCKf}	-	20	ns	
	Output clock cycle	Asynchronous	t_{Scyc}	$16 \times t_{Pcyc}$	-	ns	
		Clock synchronous		$6 \times t_{Pcyc}$	-	ns	
	Output clock pulse width		t_{SCKW}	$0.4 \times t_{Scyc}$	$0.6 \times t_{Scyc}$	ns	
	Output clock rise time		t_{SCKr}	-	20	ns	
	Output clock fall time		t_{SCKf}	-	20	ns	
	Transmit data delay time (clock synchronous)		t_{TXD}	-	40	ns	Figure 5.9
	Receive data setup time (clock synchronous)		t_{RXS}	40	-	ns	
	Receive data hold time (clock synchronous)		t_{RXH}	40	-	ns	

Note: • t_{Pcyc}: PCLK cycle

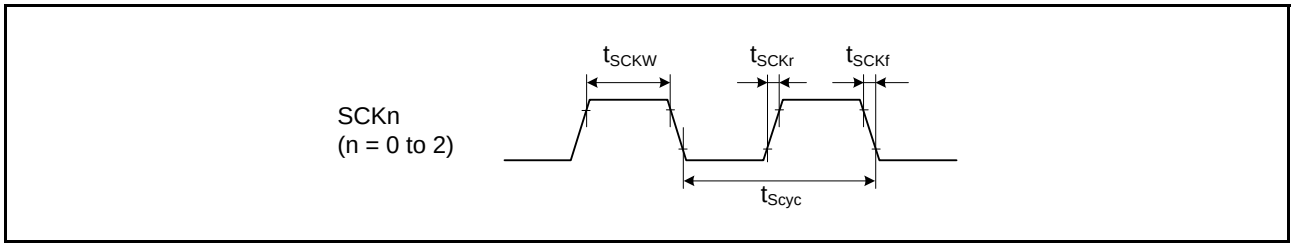


Figure 5.8 SCK Clock Input Timing

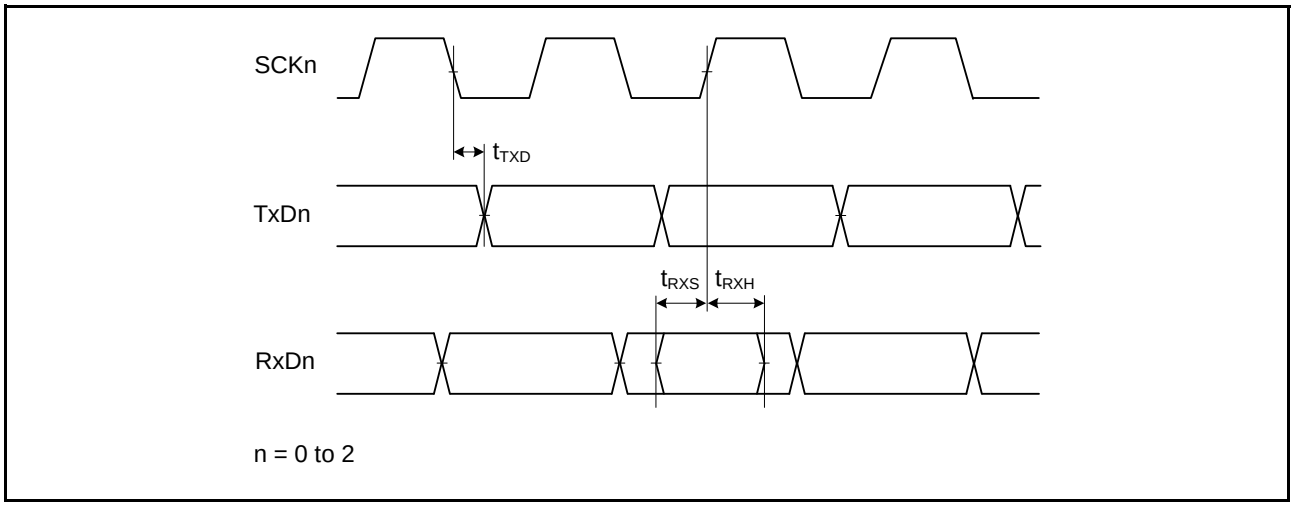


Figure 5.9 SCI Input/Output Timing: Clock Synchronous Mode

5.6 Oscillation Stop Detection Timing

Table 5.20 Oscillation Stop Detection Circuit Characteristics

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	tdr	-	-	1.0	ms	Figure 5.23
Internal oscillation frequency when oscillation stop is detected	f_{MAIN}	0.5	-	7.0	MHz	

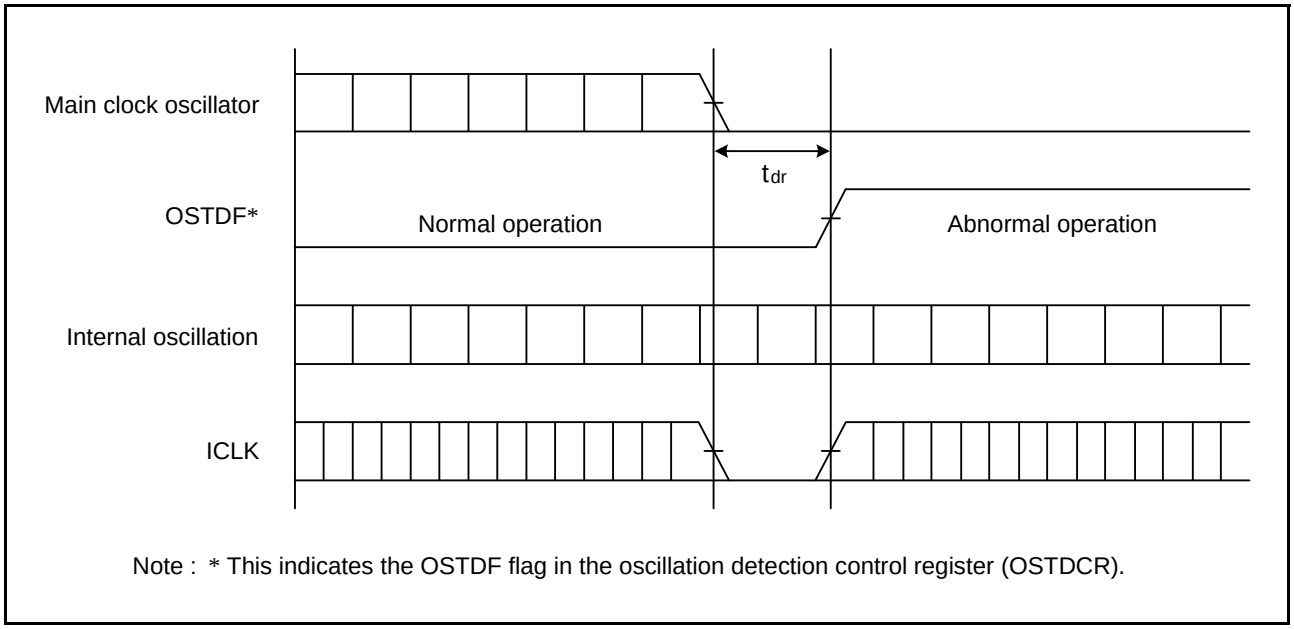
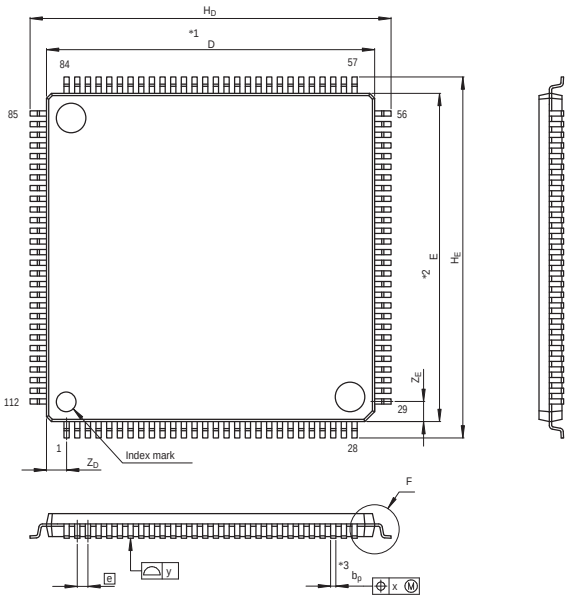
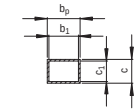


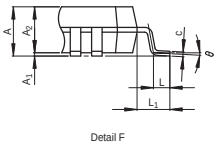
Figure 5.23 Oscillation Stop Detection Timing

Appendix 1.Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP112-20x20-0.65	PLQP0112JA-A	FP-112E / FP-112EV	1.2g





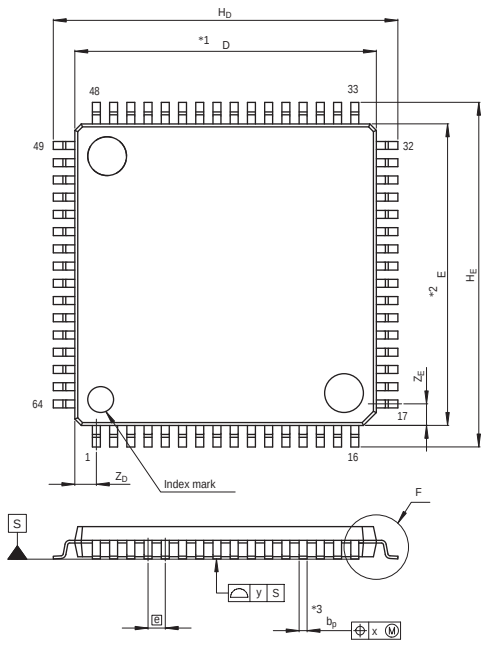


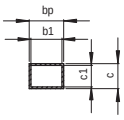
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.27	0.32	0.37
b_1	—	0.30	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	1.225	—
Z_E	—	1.225	—
L	0.35	0.5	0.65
L_1	—	1.0	—

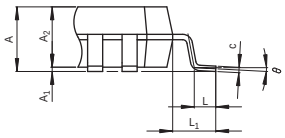
Figure A 112-Pin LQFP (PLQP0112JA-A) Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-14x14-0.80	PLQP0064GA-A	64P6U-A/ —	0.7g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.3	0.5	0.7
L_1	—	1.0	—

Figure E 64-Pin LQFP (PLQP0064GA-A) Package Dimensions

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.