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Details

Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I ² C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562t6bdfk-v3

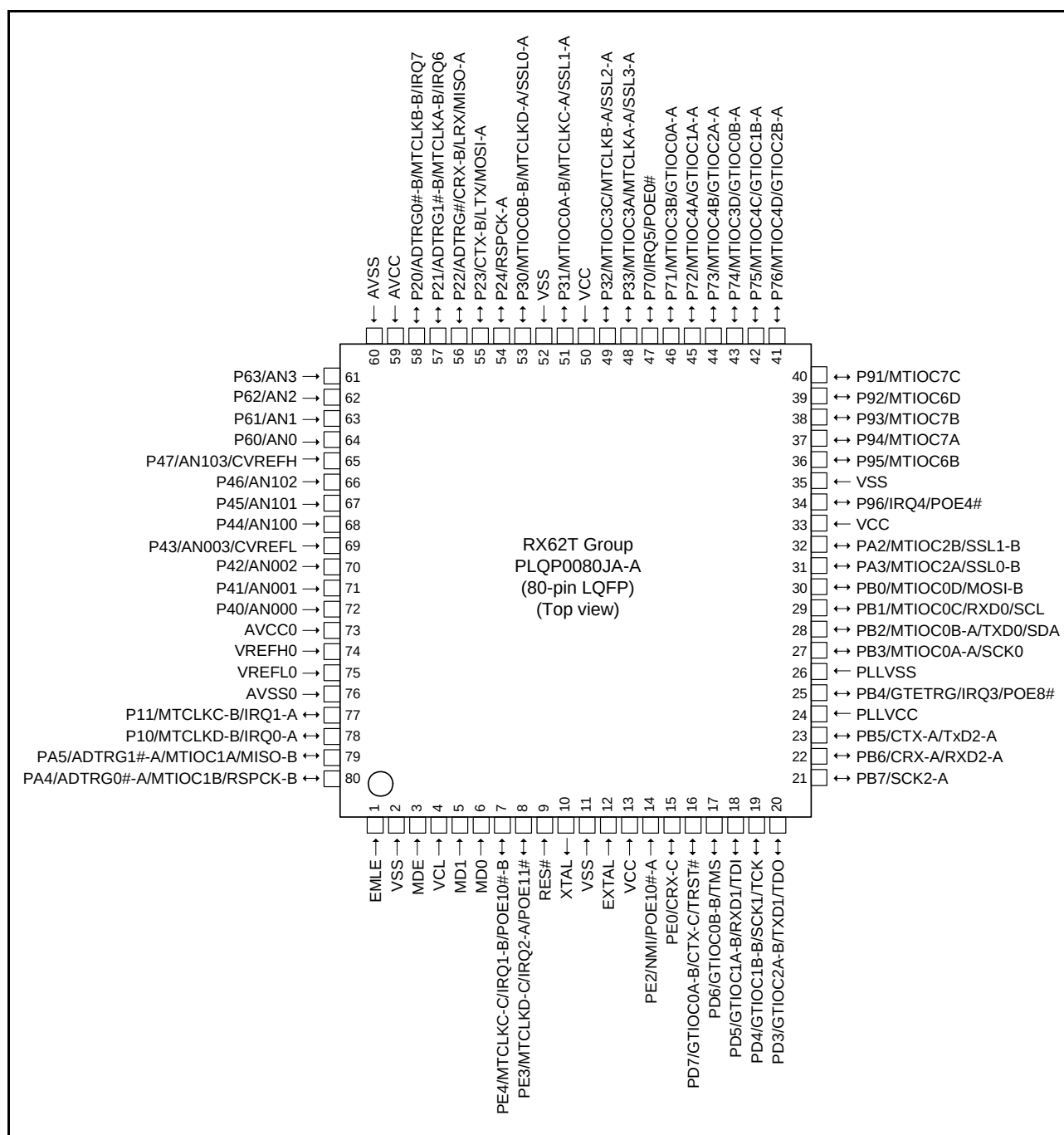


Figure 1.5 Pin Assignment of the 80-Pin LQFP

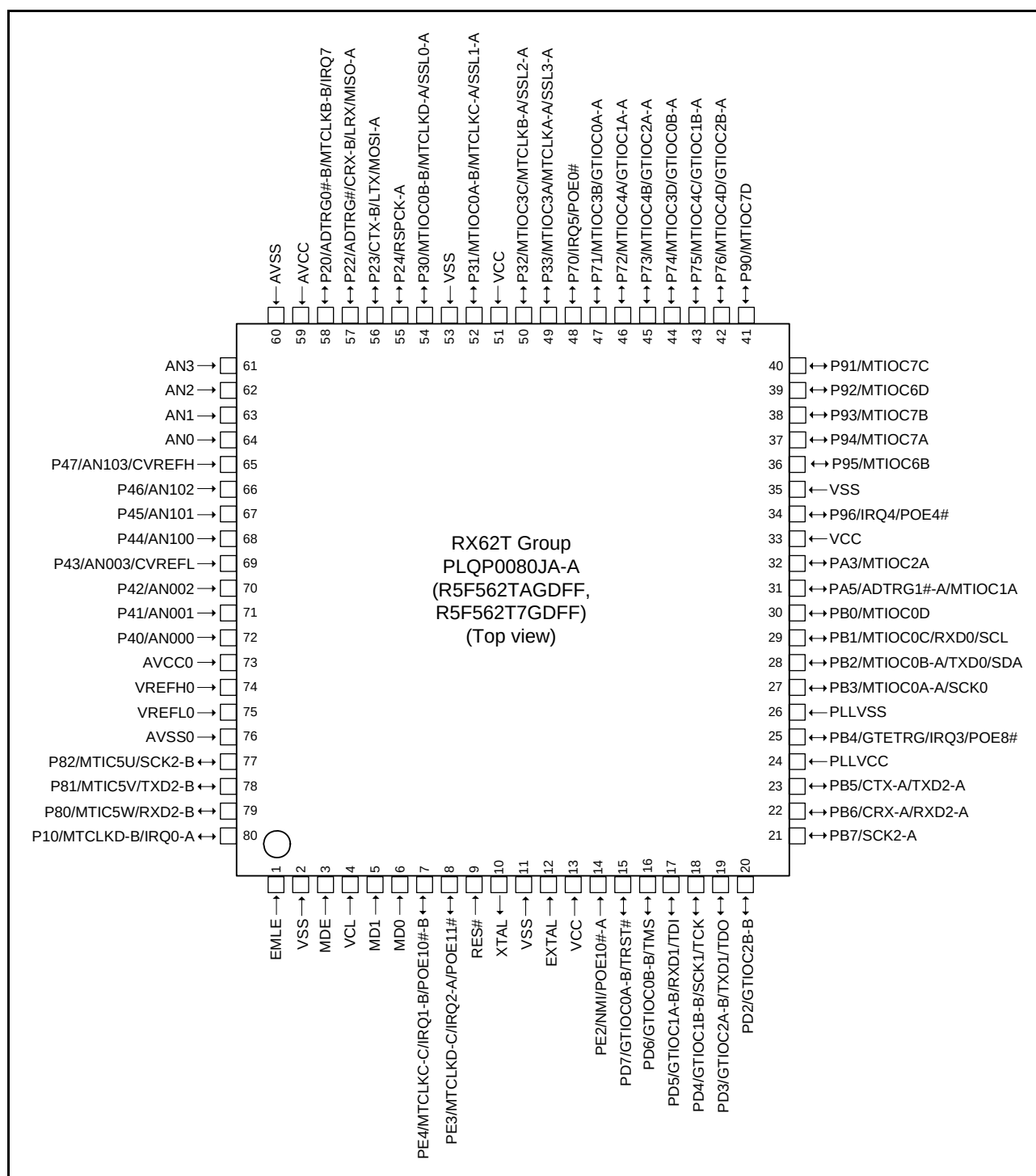


Figure 1.6 Pin Assignment of the 80-Pin LQFP (Two-Motor Control Supported Version)

Table 1.5 List of Pins and Pin Functions (100-Pin LQFP) (1 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi- cation	Interrupt	POE	Debugging
1		PE5				IRQ0-B		
2	EMLE							
3	VSS							
4	MDE							
5	VCL							
6	MD1							
7	MD0							
8		PE4		MTCLKC-C		IRQ1-B	POE10#-B	
9		PE3		MTCLKD-C		IRQ2-A	POE11#	
10	RES#							
11	XTAL							
12	VSS							
13	EXTAL							
14	VCC							
15		PE2				NMI	POE10#-A	
16		PE1			SSL3-C			
17		PE0			CRX-C/ SSL2-C			
18		PD7		GTIOC0A-B	CTX-C/SSL1-C			TRST#
19		PD6		GTIOC0B-B	SSL0-C			TMS
20		PD5		GTIOC1A-B	RXD1			TDI
21		PD4		GTIOC1B-B	SCK1			TCK
22		PD3		GTIOC2A-B	TXD1			TDO
23		PD2		GTIOC2B-B	MOSI-C			TRCLK
24		PD1		GTIOC3A	MISO-C			TRDATA3
25		PD0		GTIOC3B	RSPCK-C			TRDATA2
26		PB7			SCK2-A			TRDATA1
27		PB6			CRX-A/ RXD2-A			TRDATA0
28		PB5			CTX-A/ TXD2-A			TRSYNC
29	PLLVC							
30		PB4		GTETR		IRQ3	POE8#	
31	PLLVS							
32		PB3		MTIOC0A-A	SCK0			
33		PB2		MTIOC0B-A	TXD0/SDA			
34		PB1		MTIOC0C	RXD0/SCL			
35		PB0		MTIOC0D	MOSI-B			
36		PA5	ADTRG1#-A	MTIOC1A	MISO-B			
37		PA4	ADTRG0#-A	MTIOC1B	RSPCK-B			
38		PA3		MTIOC2A	SSL0-B			
39		PA2		MTIOC2B	SSL1-B			
40		PA1		MTIOC6A	SSL2-B			

4. I/O Registers

This section gives information on the on-chip I/O register addresses and bit configurations. The information is given as shown below. Notes on writing to registers are also given at the end.

(1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to functional modules (abbreviations).
- The number of access cycles indicates the number of states based on the specified reference clock.
- Among the I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.
- A unit of access is specified for each register. Access other than in the specified unit is prohibited.

(2) I/O register bits

- Bit configurations of the registers are listed in the same order as the register addresses.
- Reserved bits are indicated by "-" in the bit name column.
- Space in the bit name field indicates that the entire register is allocated to either the counter or data.
- For the registers of 16 or 32 bits, the MSB is listed first.

(3) Notes on writing to I/O registers

When writing to an I/O register, the CPU starts executing the subsequent instruction before completing I/O register write. This may cause the subsequent instruction to be executed before the post-update I/O register value is reflected on the operation.

As described in the following examples, special care is required for the cases in which the subsequent instruction must be executed after the post-update I/O register value is actually reflected.

[Examples of cases requiring special care]

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERm of the ICU (interrupt request enable bit)*1 cleared to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

Note 1. See section 11.2.2, Interrupt Request Enable Register m (IERm) (m = 02h to 1Fh) in the User's manual: Hardware.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

Table 4.1 List of I/O Registers (Address Order) (5 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 7172h	ICU	DTC activation enable register 114	DTCER114	8	8	2 ICLK
0008 7173h	ICU	DTC activation enable register 115	DTCER115	8	8	2 ICLK
0008 7174h	ICU	DTC activation enable register 116	DTCER116	8	8	2 ICLK
0008 7175h	ICU	DTC activation enable register 117	DTCER117	8	8	2 ICLK
0008 7179h	ICU	DTC activation enable register 121	DTCER121	8	8	2 ICLK
0008 717Ah	ICU	DTC activation enable register 122	DTCER122	8	8	2 ICLK
0008 717Dh	ICU	DTC activation enable register 125	DTCER125	8	8	2 ICLK
0008 717Eh	ICU	DTC activation enable register 126	DTCER126	8	8	2 ICLK
0008 7181h	ICU	DTC activation enable register 129	DTCER129	8	8	2 ICLK
0008 7182h	ICU	DTC activation enable register 130	DTCER130	8	8	2 ICLK
0008 7183h	ICU	DTC activation enable register 131	DTCER131	8	8	2 ICLK
0008 7184h	ICU	DTC activation enable register 132	DTCER132	8	8	2 ICLK
0008 7186h	ICU	DTC activation enable register 134	DTCER134	8	8	2 ICLK
0008 7187h	ICU	DTC activation enable register 135	DTCER135	8	8	2 ICLK
0008 7188h	ICU	DTC activation enable register 136	DTCER136	8	8	2 ICLK
0008 7189h	ICU	DTC activation enable register 137	DTCER137	8	8	2 ICLK
0008 718Ah	ICU	DTC activation enable register 138	DTCER138	8	8	2 ICLK
0008 718Bh	ICU	DTC activation enable register 139	DTCER139	8	8	2 ICLK
0008 718Ch	ICU	DTC activation enable register 140	DTCER140	8	8	2 ICLK
0008 718Dh	ICU	DTC activation enable register 141	DTCER141	8	8	2 ICLK
0008 718Eh	ICU	DTC activation enable register 142	DTCER142	8	8	2 ICLK
0008 718Fh	ICU	DTC activation enable register 143	DTCER143	8	8	2 ICLK
0008 7190h	ICU	DTC activation enable register 144	DTCER144	8	8	2 ICLK
0008 7191h	ICU	DTC activation enable register 145	DTCER145	8	8	2 ICLK
0008 7195h	ICU	DTC activation enable register 149	DTCER149	8	8	2 ICLK
0008 7196h	ICU	DTC activation enable register 150	DTCER150	8	8	2 ICLK
0008 7197h	ICU	DTC activation enable register 151	DTCER151	8	8	2 ICLK
0008 7198h	ICU	DTC activation enable register 152	DTCER152	8	8	2 ICLK
0008 7199h	ICU	DTC activation enable register 153	DTCER153	8	8	2 ICLK
0008 71AEh	ICU	DTC activation enable register 174	DTCER174	8	8	2 ICLK
0008 71AFh	ICU	DTC activation enable register 175	DTCER175	8	8	2 ICLK
0008 71B0h	ICU	DTC activation enable register 176	DTCER176	8	8	2 ICLK
0008 71B1h	ICU	DTC activation enable register 177	DTCER177	8	8	2 ICLK
0008 71B2h	ICU	DTC activation enable register 178	DTCER178	8	8	2 ICLK
0008 71B3h	ICU	DTC activation enable register 179	DTCER179	8	8	2 ICLK
0008 71B4h	ICU	DTC activation enable register 180	DTCER180	8	8	2 ICLK
0008 71B5h	ICU	DTC activation enable register 181	DTCER181	8	8	2 ICLK
0008 71B6h	ICU	DTC activation enable register 182	DTCER182	8	8	2 ICLK
0008 71B7h	ICU	DTC activation enable register 183	DTCER183	8	8	2 ICLK
0008 71B8h	ICU	DTC activation enable register 184	DTCER184	8	8	2 ICLK
0008 71BAh	ICU	DTC activation enable register 186	DTCER186	8	8	2 ICLK
0008 71BBh	ICU	DTC activation enable register 187	DTCER187	8	8	2 ICLK
0008 71BCh	ICU	DTC activation enable register 188	DTCER188	8	8	2 ICLK
0008 71BDh	ICU	DTC activation enable register 189	DTCER189	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (18 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000C 1390h	MTU1	Timer input capture control register	TICCR	8	8	5 ICLK
000C 1400h	MTU2	Timer control register	TCR	8	8, 16	5 ICLK
000C 1401h	MTU2	Timer mode register 1	TMDR1	8	8	5 ICLK
000C 1402h	MTU2	Timer I/O control register	TIOR	8	8	5 ICLK
000C 1404h	MTU2	Timer interrupt enable register	TIER	8	8, 16, 32	5 ICLK
000C 1405h	MTU2	Timer status register	TSR	8	8	5 ICLK
000C 1406h	MTU2	Timer counter	TCNT	16	16	5 ICLK
000C 1408h	MTU2	Timer general register A	TGRA	16	16, 32	5 ICLK
000C 140Ah	MTU2	Timer general register B	TGRB	16	16	5 ICLK
000C 1A00h	MTU6	Timer control register	TCR	8	8, 16, 32	5 ICLK
000C 1A01h	MTU7	Timer control register	TCR	8	8	5 ICLK
000C 1A02h	MTU6	Timer mode register 1	TMDR1	8	8, 16	5 ICLK
000C 1A03h	MTU7	Timer mode register 1	TMDR1	8	8	5 ICLK
000C 1A04h	MTU6	Timer I/O control register H	TIORH	8	8, 16, 32	5 ICLK
000C 1A05h	MTU6	Timer I/O control register L	TIORL	8	8	5 ICLK
000C 1A06h	MTU7	Timer I/O control register H	TIORH	8	8, 16	5 ICLK
000C 1A07h	MTU7	Timer I/O control register L	TIORL	8	8	5 ICLK
000C 1A08h	MTU6	Timer interrupt enable register	TIER	8	8, 16	5 ICLK
000C 1A09h	MTU7	Timer interrupt enable register	TIER	8	8	5 ICLK
000C 1A0Ah	MTU	Timer output master enable register B	TOERB	8	8	5 ICLK
000C 1A0Eh	MTU	Timer output control register 1B	TOCR1B	8	8, 16	5 ICLK
000C 1A0Fh	MTU	Timer output control register 2B	TOCR2B	8	8	5 ICLK
000C 1A10h	MTU6	Timer counter	TCNT	16	16, 32	5 ICLK
000C 1A12h	MTU7	Timer counter	TCNT	16	16	5 ICLK
000C 1A14h	MTU	Timer cycle data register B	TCDRB	16	16, 32	5 ICLK
000C 1A16h	MTU	Timer dead time data register B	TDDRB	16	16	5 ICLK
000C 1A18h	MTU6	Timer general register A	TGRA	16	16, 32	5 ICLK
000C 1A1Ah	MTU6	Timer general register B	TGRB	16	16	5 ICLK
000C 1A1Ch	MTU7	Timer general register A	TGRA	16	16, 32	5 ICLK
000C 1A1Eh	MTU7	Timer general register B	TGRB	16	16	5 ICLK
000C 1A20h	MTU	Timer subcounter B	TCNTSB	16	16, 32	5 ICLK
000C 1A22h	MTU	Timer cycle buffer register B	TCBRB	16	16	5 ICLK
000C 1A24h	MTU6	Timer general register C	TGRC	16	16, 32	5 ICLK
000C 1A26h	MTU6	Timer general register D	TGRD	16	16	5 ICLK
000C 1A28h	MTU7	Timer general register C	TGRC	16	16, 32	5 ICLK
000C 1A2Ah	MTU7	Timer general register D	TGRD	16	16	5 ICLK
000C 1A2Ch	MTU6	Timer status register	TSR	8	8, 16	5 ICLK
000C 1A2Dh	MTU7	Timer status register	TSR	8	8	5 ICLK
000C 1A30h	MTU	Timer interrupt skipping set register 1B	TITCR1B	8	8, 16	5 ICLK
000C 1A31h	MTU	Timer interrupt skipping counter 1B	TITCNT1B	8	8	5 ICLK
000C 1A32h	MTU	Timer buffer transfer set register B	TBTERB	8	8	5 ICLK
000C 1A34h	MTU	Timer dead time enable register B	TDERB	8	8	5 ICLK
000C 1A36h	MTU	Timer output level buffer register B	TOLBRB	8	8	5 ICLK
000C 1A38h	MTU6	Timer buffer operation transfer mode register	TBTM	8	8, 16	5 ICLK

Table 4.1 List of I/O Registers (Address Order) (23 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000C 222Ch	GPT2	A/D converter start request timing register B	GTADTRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 222Eh	GPT2	A/D converter start request timing buffer register B	GTADTBRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2230h	GPT2	A/D converter start request timing double-buffer register B	GTADTDBRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2234h	GPT2	General PWM timer output negate control register	GTONCR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2236h	GPT2	General PWM timer dead time control register	GTDTCR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2238h	GPT2	General PWM timer dead time value register	GTDVU	16	16, 32	3 to 5 ICLK ^{*4}
000C 223Ah	GPT2	General PWM timer dead time value register	GTDVD	16	16, 32	3 to 5 ICLK ^{*4}
000C 223Ch	GPT2	General PWM timer dead time buffer register	GTDBU	16	16, 32	3 to 5 ICLK ^{*4}
000C 223Eh	GPT2	General PWM timer dead time buffer register	GTDBD	16	16, 32	3 to 5 ICLK ^{*4}
000C 2240h	GPT2	General PWM timer output protection function status register	GTSOS	16	16, 32	3 to 5 ICLK ^{*4}
000C 2242h	GPT2	General PWM timer output protection temporary release register	GTSOTR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2280h	GPT3	General PWM timer I/O control register	GTIOR	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2282h	GPT3	General PWM timer interrupt output setting register	GTINTAD	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2284h	GPT3	General PWM timer control register	GTCR	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2286h	GPT3	General PWM timer buffer enable register	GTBER	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2288h	GPT3	General PWM timer count direction register	GTUDC	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 228Ah	GPT3	General PWM timer interrupt and A/D converter start request skipping setting register	GTITC	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 228Ch	GPT3	General PWM timer status register	GTST	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 228Eh	GPT3	General PWM timer counter	GTCNT	16	16	3 to 5 ICLK ^{*4}
000C 2290h	GPT3	General PWM timer compare capture register A	GTCCRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 2292h	GPT3	General PWM timer compare capture register B	GTCCRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2294h	GPT3	General PWM timer compare capture register C	GTCCRC	16	16, 32	3 to 5 ICLK ^{*4}
000C 2296h	GPT3	General PWM timer compare capture register D	GTCCRD	16	16, 32	3 to 5 ICLK ^{*4}
000C 2298h	GPT3	General PWM timer compare capture register E	GTCCRE	16	16, 32	3 to 5 ICLK ^{*4}
000C 229Ah	GPT3	General PWM timer compare capture register F	GTCCRF	16	16, 32	3 to 5 ICLK ^{*4}
000C 229Ch	GPT3	General PWM timer cycle setting register	GTPR	16	16, 32	3 to 5 ICLK ^{*4}
000C 229Eh	GPT3	General PWM timer cycle setting buffer register	GTPBR	16	16, 32	3 to 5 ICLK ^{*4}
000C 22A0h	GPT3	General PWM timer cycle setting double-buffer register	GTPDBR	16	16, 32	3 to 5 ICLK ^{*4}
000C 22A4h	GPT3	A/D converter start request timing register A	GTADTRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 22A6h	GPT3	A/D converter start request timing buffer register A	GTADTBRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 22A8h	GPT3	A/D converter start request timing double-buffer register A	GTADTDBRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 22ACh	GPT3	A/D converter start request timing register B	GTADTRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 22AEh	GPT3	A/D converter start request timing buffer register B	GTADTBRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 22B0h	GPT3	A/D converter start request timing double-buffer register B	GTADTDBRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 22B4h	GPT3	General PWM timer output negate control register	GTONCR	16	16, 32	3 to 5 ICLK ^{*4}

4.2 I/O Register Bits

Register addresses and bit names of the peripheral modules are described below.

Each line cover eight bits, and 16-bit and 32-bit registers are shown as 2 or 4 lines, respectively.

Table 4.2 List of I/O Registers (Bit Order) (1 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
SYSTEM	MDMONR	—	—	—	—	—	—	—	—
		MDE	—	—	—	—	—	MD1	MD0
SYSTEM	MDSR	—	—	—	—	—	—	—	—
		—	—	—	BOTS	—	—	—	IROM
SYSTEM	SYSCRO	KEY[7:0]							
		—	—	—	—	—	—	—	ROME
SYSTEM	SYSCR1	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	RAME
SYSTEM	SBYCR	SSBY	—	—	—	—	STS[4:0]	—	—
		—	—	—	—	—	—	—	—
SYSTEM	MSTPCRA	ACSE	—	—	MSTPA28	—	—	—	MSTPA24
		MSTPA23	—	—	—	—	—	MSTPA17	MSTPA16
		MSTPA15	MSTPA14	—	—	—	—	MSTPA9	—
		MSTPA7	—	—	—	—	—	—	—
SYSTEM	MSTPCRB	MSTPB31	MSTPB30	MSTPB29	—	—	—	—	—
		MSTPB23	—	MSTPB21	—	—	—	MSTPB17	—
		—	—	—	—	—	—	—	—
		MSTPB7	—	—	—	—	—	—	MSTPB0
SYSTEM	MSTPCRC	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	MSTPC0
SYSTEM	SCKCR	—	—	—	—	—	ICK[3:0]	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	PCK[3:0]	—	—
		—	—	—	—	—	—	—	—
SYSTEM	OSTDCR	KEY[7:0]							
		OSTDE	OSTDF	—	—	—	—	—	—
BSC	BERCLR	—	—	—	—	—	—	—	STSLR
BSC	BEREN	—	—	—	—	—	—	—	IGAEN
BSC	BERSR1	—	—	MST[2:0]	—	—	—	—	IA
BSC	BERSR2	ADDR[12:0]							
		ADDR[12:0]							
DTC	DTCCR	—	—	—	RRS	—	—	—	—
DTC	DTCVBR	—	—	—	—	—	—	—	—
DTC	DTCADMOD	—	—	—	—	—	—	—	SHORT
DTC	DTCST	—	—	—	—	—	—	—	DTCST
DTC	DTCSTS	ACT	—	—	—	—	—	—	—
		VECN[7:0]							
		RSPN[27:0]							
		RSPN[27:0]							
MPU	RSPAGE0	RSPN[27:0]							
		RSPN[27:0]							
		RSPN[27:0]							
		RSPN[27:0]							

Table 4.2 List of I/O Registers (Bit Order) (2 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
MPU	REPAGE0					REPN[27:0]			
						REPN[27:0]			
						REPN[27:0]			
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE1					RSPN[27:0]			
						RSPN[27:0]			
						RSPN[27:0]			
			RSPN[27:0]			—	—	—	—
MPU	REPAGE1					REPN[27:0]			
						REPN[27:0]			
						REPN[27:0]			
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE2					RSPN[27:0]			
						RSPN[27:0]			
						RSPN[27:0]			
			RSPN[27:0]			—	—	—	—
MPU	REPAGE2					REPN[27:0]			
						REPN[27:0]			
						REPN[27:0]			
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE3					RSPN[27:0]			
						RSPN[27:0]			
						RSPN[27:0]			
			RSPN[27:0]			—	—	—	—
MPU	REPAGE3					REPN[27:0]			
						REPN[27:0]			
						REPN[27:0]			
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE4					RSPN[27:0]			
						RSPN[27:0]			
						RSPN[27:0]			
			RSPN[27:0]			—	—	—	—
MPU	REPAGE4					REPN[27:0]			
						REPN[27:0]			
						REPN[27:0]			
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE5					RSPN[27:0]			
						RSPN[27:0]			
						RSPN[27:0]			
			RSPN[27:0]			—	—	—	—
MPU	REPAGE5					REPN[27:0]			
						REPN[27:0]			
						REPN[27:0]			
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE6					RSPN[27:0]			
						RSPN[27:0]			
						RSPN[27:0]			
			RSPN[27:0]			—	—	—	—
MPU	REPAGE6					REPN[27:0]			
						REPN[27:0]			
						REPN[27:0]			
			REPN[27:0]				UAC[2:0]		V

Table 4.2 List of I/O Registers (Bit Order) (4 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
ICU	IR044	—	—	—	—	—	—	—	IR
ICU	IR045	—	—	—	—	—	—	—	IR
ICU	IR046	—	—	—	—	—	—	—	IR
ICU	IR047	—	—	—	—	—	—	—	IR
ICU	IR056	—	—	—	—	—	—	—	IR
ICU	IR057	—	—	—	—	—	—	—	IR
ICU	IR058	—	—	—	—	—	—	—	IR
ICU	IR059	—	—	—	—	—	—	—	IR
ICU	IR060	—	—	—	—	—	—	—	IR
ICU	IR064	—	—	—	—	—	—	—	IR
ICU	IR065	—	—	—	—	—	—	—	IR
ICU	IR066	—	—	—	—	—	—	—	IR
ICU	IR067	—	—	—	—	—	—	—	IR
ICU	IR068	—	—	—	—	—	—	—	IR
ICU	IR069	—	—	—	—	—	—	—	IR
ICU	IR070	—	—	—	—	—	—	—	IR
ICU	IR071	—	—	—	—	—	—	—	IR
ICU	IR096	—	—	—	—	—	—	—	IR
ICU	IR098	—	—	—	—	—	—	—	IR
ICU	IR102	—	—	—	—	—	—	—	IR
ICU	IR103	—	—	—	—	—	—	—	IR
ICU	IR106	—	—	—	—	—	—	—	IR
ICU	IR114	—	—	—	—	—	—	—	IR
ICU	IR115	—	—	—	—	—	—	—	IR
ICU	IR116	—	—	—	—	—	—	—	IR
ICU	IR117	—	—	—	—	—	—	—	IR
ICU	IR118	—	—	—	—	—	—	—	IR
ICU	IR119	—	—	—	—	—	—	—	IR
ICU	IR120	—	—	—	—	—	—	—	IR
ICU	IR121	—	—	—	—	—	—	—	IR
ICU	IR122	—	—	—	—	—	—	—	IR
ICU	IR123	—	—	—	—	—	—	—	IR
ICU	IR124	—	—	—	—	—	—	—	IR
ICU	IR125	—	—	—	—	—	—	—	IR
ICU	IR126	—	—	—	—	—	—	—	IR
ICU	IR127	—	—	—	—	—	—	—	IR
ICU	IR128	—	—	—	—	—	—	—	IR
ICU	IR129	—	—	—	—	—	—	—	IR
ICU	IR130	—	—	—	—	—	—	—	IR
ICU	IR131	—	—	—	—	—	—	—	IR
ICU	IR132	—	—	—	—	—	—	—	IR
ICU	IR133	—	—	—	—	—	—	—	IR
ICU	IR134	—	—	—	—	—	—	—	IR
ICU	IR135	—	—	—	—	—	—	—	IR
ICU	IR136	—	—	—	—	—	—	—	IR
ICU	IR137	—	—	—	—	—	—	—	IR
ICU	IR138	—	—	—	—	—	—	—	IR
ICU	IR139	—	—	—	—	—	—	—	IR
ICU	IR140	—	—	—	—	—	—	—	IR
ICU	IR141	—	—	—	—	—	—	—	IR
ICU	IR142	—	—	—	—	—	—	—	IR
ICU	IR143	—	—	—	—	—	—	—	IR

Table 4.2 List of I/O Registers (Bit Order) (16 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
POE	POECR2	—	—	—	—	—	MTU3BDZE	MTU4ACZE	MTU4BDZE
		—	—	—	—	—	MTU6BDZE	MTU7ACZE	MTU7BDZE
POE	POECR3	—	—	—	—	—	—	GPT3ABZE	GPT2ABZE
		—	—	—	—	—	—	GPT1ABZE	GPT0ABZE
POE	POECR4	—	—	IC5ADDMT67 ZE	IC4ADDMT67 ZE	IC3ADDMT67 ZE	—	IC1ADDMT67 ZE	CMADDMT67 ZE
		—	—	IC5ADDMT34 ZE	IC4ADDMT34 ZE	IC3ADDMT34 ZE	IC2ADDMT34 ZE	—	CMADDMT34 ZE
POE	POECR5	—	—	—	—	—	—	—	—
		—	—	IC5ADDMT0Z E	IC4ADDMT0Z E	—	IC2ADDMT0Z E	IC1ADDMT0Z E	CMADDMT0Z E
POE	POECR6	—	—	—	IC4ADDGPT2 3ZE	IC3ADDGPT2 3ZE	IC2ADDGPT2 3ZE	IC1ADDGPT2 3ZE	CMADDGPT2 3ZE
		—	—	IC5ADDGPT0 1ZE	—	IC3ADDGPT0 1ZE	IC2ADDGPT0 1ZE	IC1ADDGPT0 1ZE	CMADDGPT0 1ZE
POE	ICSR4	—	—	—	POE10F	—	—	POE10E	PIE4
		—	—	—	—	—	—	POE10M[1:0]	
POE	ALR1	—	—	—	—	—	—	—	—
		OLSEN	—	OLSG2B	OLSG2A	OLSG1B	OLSG1A	OLSG0B	OLSG0A
POE	ICSR5	—	—	—	POE11F	—	—	POE11E	PIE5
		—	—	—	—	—	—	POE11M[1:0]	
CAN0*3	MB.ID	IDE	RTR	—	—	—	SID[10:0]		
		SID[10:0]				EID[17:0]			
		—				EID[17:0]			
		—				EID[17:0]			
	MB.DLC	—	—	—	—	—	—	—	—
		—	—	—	—	DLC[3:0]			
	MB.DATA 0 to 7								
CAN0*3	MKR0	—				TSH[7:0]			
		—				TSL[7:0]			
		—				SID[10:0]			
		—				SID[10:0]			
	MKR1	—				SID[10:0]			
		—				SID[10:0]			
		—				EID[17:0]			
		—				EID[17:0]			
CAN0*3	MKR2	—				SID[10:0]			
		—				SID[10:0]			
		—				EID[17:0]			
		—				EID[17:0]			
CAN0*3	MKR3	—				SID[10:0]			
		—				SID[10:0]			
		—				EID[17:0]			
		—				EID[17:0]			
CAN0*3	MKR4	—				SID[10:0]			
		—				SID[10:0]			
		—				EID[17:0]			
		—				EID[17:0]			

Table 4.2 List of I/O Registers (Bit Order) (17 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
CAN0*3	MKR5	—	—	—			SID[10:0]		
					SID[10:0]			EID[17:0]	
						EID[17:0]			
						EID[17:0]			
CAN0*3	MKR6	—	—	—			SID[10:0]		
					SID[10:0]			EID[17:0]	
						EID[17:0]			
						EID[17:0]			
CAN0*3	MKR7	—	—	—			SID[10:0]		
					SID[10:0]			EID[17:0]	
						EID[17:0]			
						EID[17:0]			
CAN0*3	FIDCR0	IDE	RTR	—			SID[10:0]		
					SID[10:0]			EID[17:0]	
						EID[17:0]			
						EID[17:0]			
CAN0*3	FIDCR1	IDE	RTR	—			SID[10:0]		
					SID[10:0]			EID[17:0]	
						EID[17:0]			
						EID[17:0]			
CAN0*3	MKIVLR								
CAN0*3	MIER	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
CAN0*3	MCTL.TX	TRMREQ	RECREQ	—	ONESHOT	—	TRMABT	TRMACTIVE	SENTDATA
	MCTL.RX	TRMREQ	RECREQ	—	ONESHOT	—	MSGLOST	INVALDATA	NEWDATA
CAN0*3	CTLR	—	—	RBOC	BOM[1:0]		SLPM	CANM[1:0]	
			TSPS[1:0]	TSRC	TPM	MLM	IDFM[1:0]		MBM
CAN0*3	STR	—	RECST	TRMST	BOST	EPST	SLPST	HLTST	RSTST
		EST	TABST	FMLST	NMLST	TFST	RFST	SDST	NDST
CAN0*3	BCR		TSEG1[3:0]			—	—	BRP[9:0]	
CAN0*3	RFCR	RFEST	RFWST	RFFST	RFMLF		RFUST[2:0]		RFE
CAN0*3	RFPCR	—	—	—	—	—	—	—	—
CAN0*3	TFCR	TFEST	TFFST	—	—		TFUST[2:0]		TFE
CAN0*3	TFPCR	—	—	—	—	—	—	—	—
CAN0*3	EIER	BLIE	OLIE	ORIE	BORIE	BOEIE	EPIE	EWIE	BEIE
CAN0*3	EIFR	BLIF	OLIF	ORIF	BORIF	BOEIF	EPIF	EWIF	BEIF
CAN0*3	RECR	—	—	—	—	—	—	—	—
CAN0*3	TECR	—	—	—	—	—	—	—	—
CAN0*3	ECSR	EDPM	ADEF	BE0F	BE1F	CEF	AEF	FEF	SEF
CAN0*3	CSSR	—	—	—	—	—	—	—	—
CAN0*3	MSSR	SEST	—	—			MBNST[4:0]		
CAN0*3	MSMR	—	—	—	—	—	—	MBSM[1:0]	
CAN0*3	TSR	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—

Table 4.2 List of I/O Registers (Bit Order) (23 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
GPT	GTBDR	BD33	BD32	BD31	BD30	BD23	BD22	BD21	BD20
		BD13	BD12	BD11	BD10	BD03	BD02	BD01	BD00
GPT	GTSWP	—	—	—	—	—	—	—	—
		—	—	—	—	SWP3	SWP2	SWP1	SWP0
GPT	LCCR	LPSC[1:0]		TPSC[1:0]		LCNTAT		LCTQ[2:0]	
		—	LCINTO	LCINTD	LCINTC	—	LCNTS	LCNTR	LCNTE
GPT	LCST	—	—	—	—	—	—	—	—
		—	—	—	—	—	LISO	LISD	LISC
GPT	LCNTA								
GPT	LCNT00								
GPT	LCNT01								
GPT	LCNT02								
GPT	LCNT03								
GPT	LCNT04								
GPT	LCNT05								
GPT	LCNT06								
GPT	LCNT07								
GPT	LCNT08								
GPT	LCNT09								
GPT	LCNT10								
GPT	LCNT11								
GPT	LCNT12								
GPT	LCNT13								
GPT	LCNT14								
GPT	LCNT15								
GPT	LCNTDU								
GPT	LCNTDL								
GPT0	GTIOR	OBHLD	OBDFLT	GTIOB[5:0]					
		OAHL	OADFLT	GTIOA[5:0]					
GPT0	GTINTAD	ADTRBDEN	ADTRBUEN	ADTRADEN	ADTRAUEN	EINT	—	—	—
		GTINTPR[1:0]		GTINTF	GTINTE	GTINTD	GTINTC	GTINTB	GTINTA

Table 4.2 List of I/O Registers (Bit Order) (30 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
FLASH	FSTATR0	FRDY	ILGLERR	ERSERR	PRGERR	SUSRDY	—	ERSSPD	PRGSPD
FLASH	FSTATR1	FCUERR	—	—	FLOCKST	—	—	—	—
FLASH	FENTRYR	FEKEY[7:0]							
		FENTRYD	—	—	—	—	—	—	FENTRY0
FLASH	FPROTR	FPKEY[7:0]							
		—	—	—	—	—	—	—	FPROTCN
FLASH	FRESETR	FRKEY[7:0]							
		—	—	—	—	—	—	—	FRESET
FLASH	FCMDR	CMDR[7:0]							
		PCMDR[7:0]							
FLASH	FCPSR	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	ESUSPMD
FLASH	DFLBCCNT	BCADR[7:0]							
		BCADR[7:0]							
FLASH	FPESTAT	—	—	—	—	—	—	—	—
		PEERRST[7:0]							
FLASH	DFLBCSTAT	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	BCST
FLASH	PCKAR	—	—	—	—	—	—	—	—
		PCKA[7:0]							

Note: • In this, the I/O port related registers (0008 C001h to 0008 C116h) indicate the bit configuration of the 112-pin LQFP version. As the configuration of registers and bits differs depending on a package, see section 14, I/O Ports, for details in the User's manual: Hardware.

Note 1. This shows the bit configuration when ADDPR.DPSEL = 0 and ADDPR.DPPRC = 0 (The value has 10-bit accuracy and is padded at the LSB end).

Note 2. This shows the bit configuration when ADCER.ADRFMT = 0 (aligned to the LSB end) and ADCER.ADPRC[1:0] = 00b. For details, refer to section 28, 12-Bit A/D Converter (S12ADA) in the User's manual: Hardware.

Note 3. This function is not supported by the product without the CAN function.

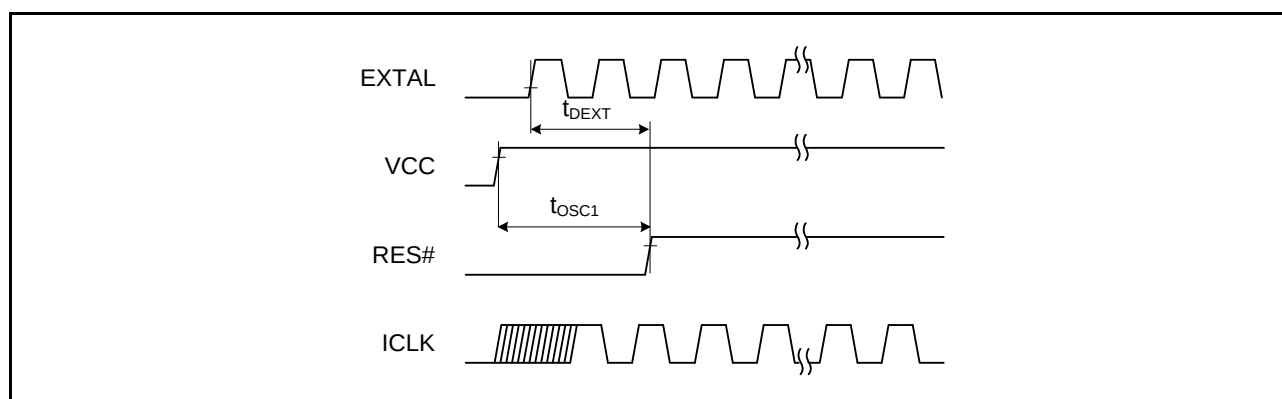


Figure 5.1 Oscillation Settling Timing

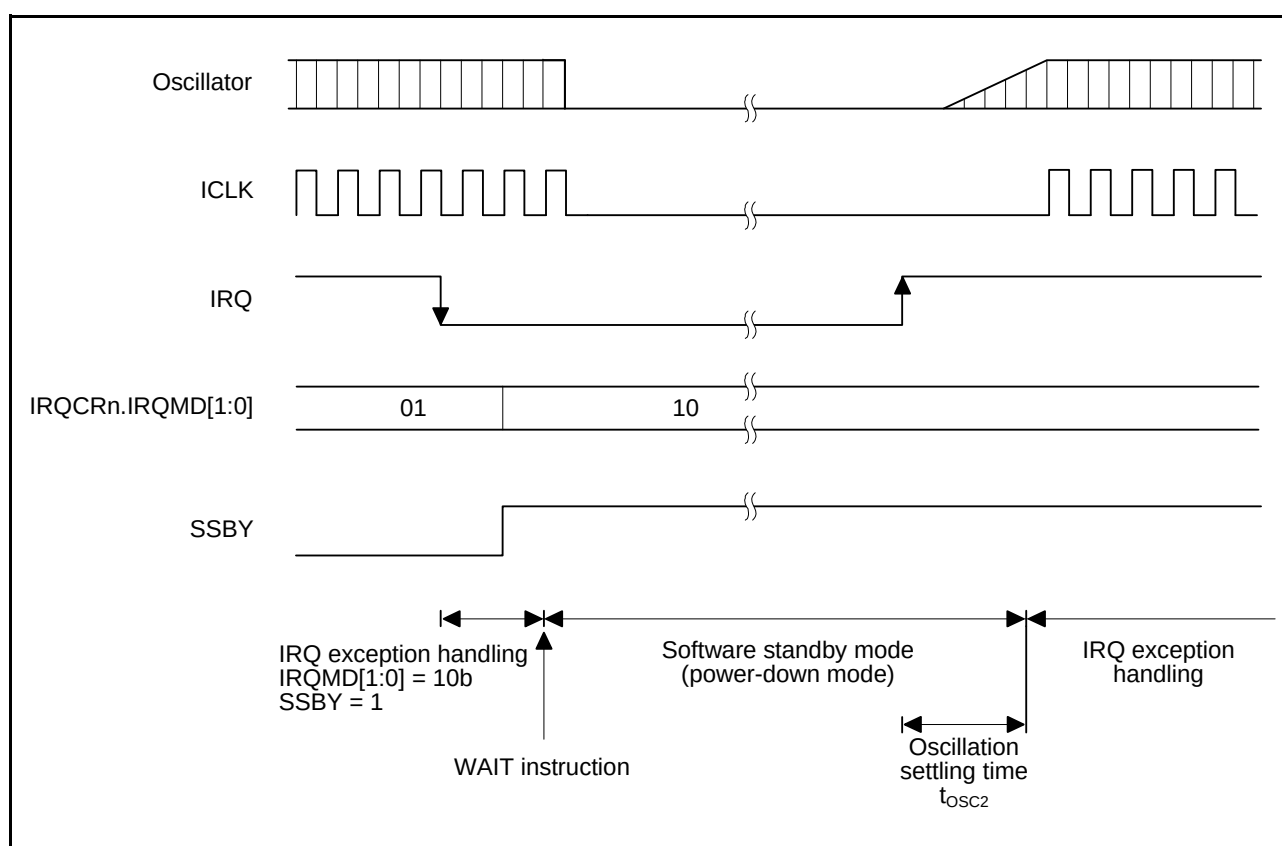


Figure 5.2 Oscillation Settling Timing after Software Standby Mode

Table 5.11 Timing of On-Chip Peripheral Modules (3)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item			Symbol	Min.	Max.	Unit	Test Conditions
RSPI	RSPCK clock cycle	Master	t_{SPCyc}	4	4096	t_{PCyc}	Figure 5.11
		Slave		8	4096		
	RSPCK clock high pulse width	Master	t_{SPCKWH}	$(t_{SPCyc} - t_{SPCKR} - t_{SPCKF}) / 2-3$	-	ns	
		Slave		$(t_{SPCyc} - t_{SPCKR} - t_{SPCKF}) / 2$	-		
	RSPCK clock low pulse width	Master	t_{SPCKWL}	$(t_{SPCyc} - t_{SPCKR} - t_{SPCKF}) / 2-3$	-	ns	
		Slave		$(t_{SPCyc} - t_{SPCKR} - t_{SPCKF}) / 2$	-		
	RSPCK clock rise/fall time	Output	t_{SPCKR}	-	5	ns	Figure 5.12 to Figure 5.15
		Input	t_{SPCKF}	-	1	μs	
	Data input setup time	Master	t_{SU}	25	-	ns	
		Slave		0	-		
	Data input hold time	Master	t_H	0	-	ns	
		Slave		$20+2 \times t_{PCyc}$	-		
	SSL setup time	Master	t_{LEAD}	1	8	t_{SPCyc}	
		Slave		4	-	t_{PCyc}	
	SSL hold time	Master	t_{LAG}	1	8	t_{SPCyc}	
		Slave		4	-	t_{PCyc}	
	Data output delay time	Master	t_{OD}	-	20	ns	
		Slave		-	$3 \times t_{PCyc} + 40$		
	Data output hold time	Master	t_{OH}	0	-	ns	
		Slave		0	-		
	Successive transmission delay time	Master	t_{TD}	$t_{SPCyc} + 2 \times t_{PCyc}$	$8 \times t_{SPCyc} + 2 \times t_{PCyc}$	ns	
		Slave		$4 \times t_{PCyc}$	-		
	MOSI, MISO rise/fall time	Output	t_{DR}	-	15	ns	Figure 5.12 to Figure 5.15
		Input	t_{DF}	-	1	μs	
	SSL rise/fall time	Output	t_{SSLR}	-	15	ns	
		Input	t_{SSLF}	-	1	μs	
	Slave access time		t_{SA}	-	4	t_{PCyc}	Figure 5.12 to Figure 5.15
	Slave output release time		t_{REL}	-	3	t_{PCyc}	

Note: • Note 1: t_{PCyc} : PCLK cycle

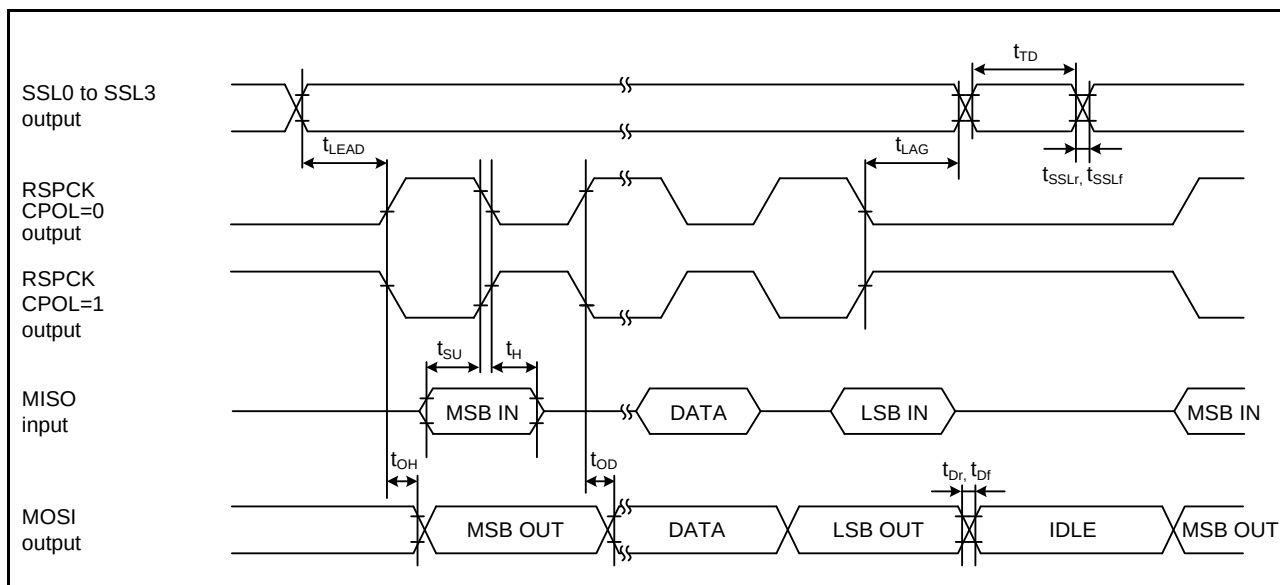


Figure 5.13 RSPI Timing (Master, CPHA = 1)

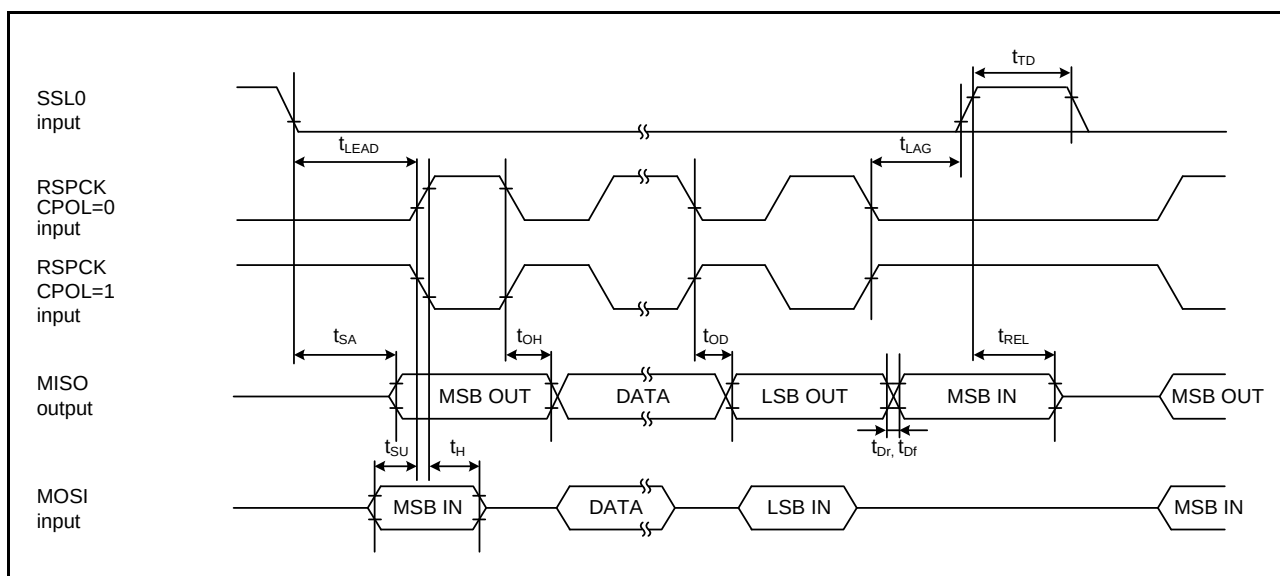


Figure 5.14 RSPI Timing (Slave, CPHA = 0)

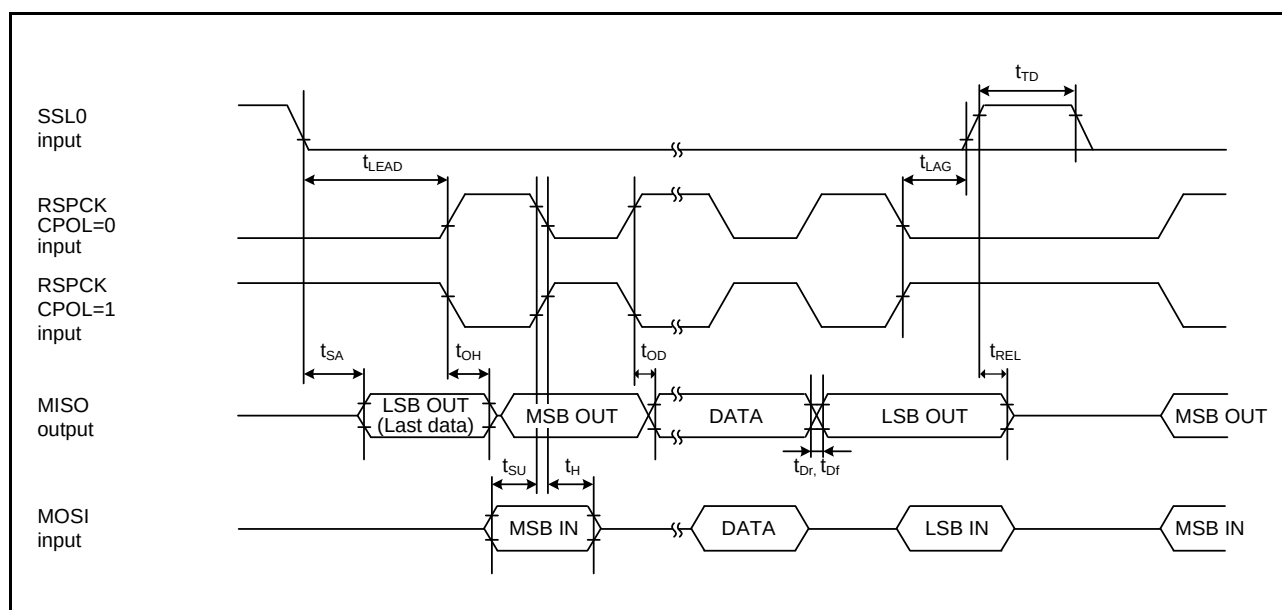
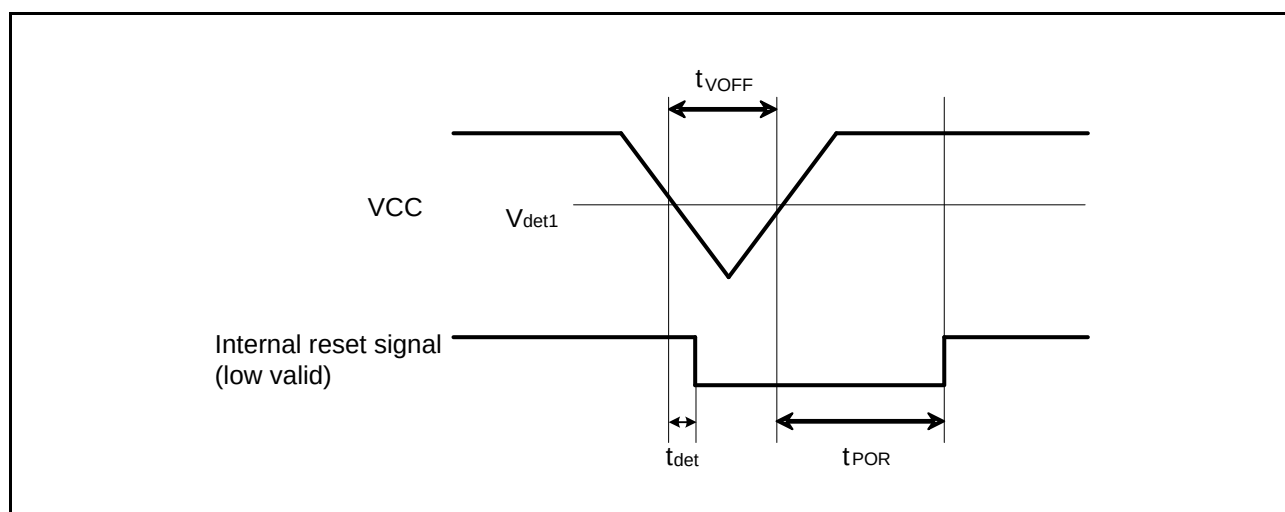
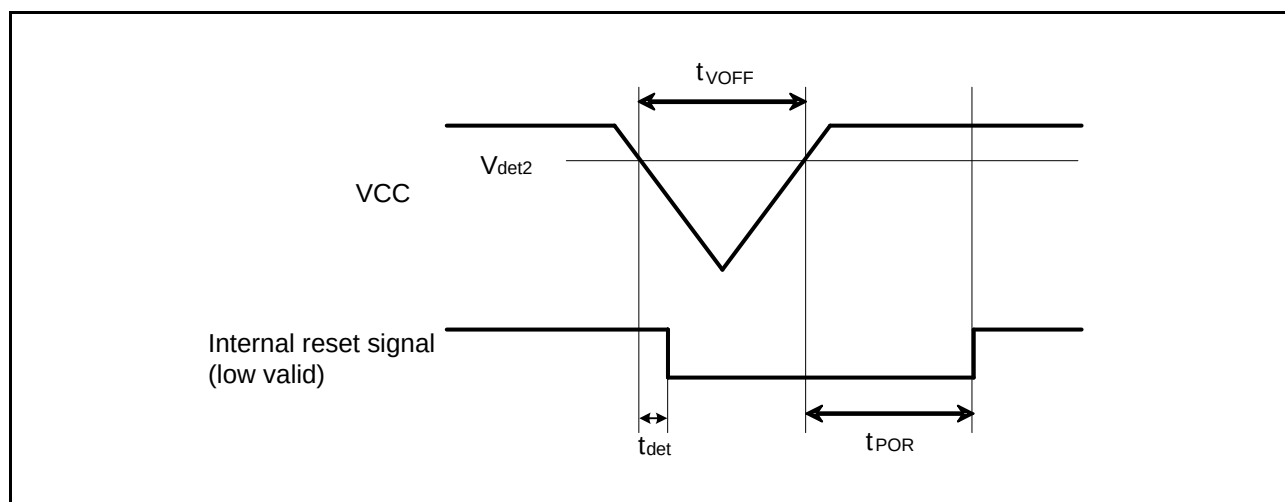


Figure 5.15 RSPI Timing (Slave, CPHA = 1)

**Figure 5.21 Voltage Detection Circuit Timing (V_{det1})****Figure 5.22 Voltage Detection Circuit Timing (V_{det2})**

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Renesas Electronics America Inc.

2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited

1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH

Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.

7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.

Unit 301, Tower A, Central Towers, 555 LanGao Rd., Putuo District, Shanghai, China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited

Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.

13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.

80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.

12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141