Renesas Electronics America Inc - R5F562T6BDFM#V1 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562t6bdfm-v1

Table 1.1 Outline of Specifications (3 / 5)

Classification	Module/Function	Description
Timers	General PWM timer (GPT/GPTa)	• 16 bits x 4 channels • Counting up or down (saw-wave), counting up and down (triangle-wave) selectable for all channels • Clock sources independently selectable for all channels • 2 input/output pins per channel • 2 output compare/input capture registers per channel • For the 2 output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally asymmetrically PWM waveforms. • Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow) • Synchronizable operation of the several counters • Modes of synchronized operation (synchronized, or displaced by desired times for phase shifting) • Generation of dead times in PWM operation • Through combination of three counters, generation of automatic three-phase PWM waveforms incorporating dead times • Starting, clearing, and stopping counters in response to external or internal triggers • Internal trigger sources: output of the internal comparator detection, software, and compare-match • The frequency-divided system clock (ICLK) can be used as a counter clock for measuring timing of the edges of signals produced by frequency-dividing the low-speed on-chip oscillator clock signal dedicated to IWDT (to detect abnormal oscillation). • PWM delay generation can control the timing with which signals on the two PWM output pins for each channel rise and fall with an accuracy of up to 1/32 times the period of the system clock (ICLK) (only for GPTa).
	Compare match timer (CMT)	• (16 bits x 2 channels) x 2 units • Select from among four internal clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Watchdog timer (WDT)	• 8 bits x 1 channel • Select from among eight counter-input clock signals (PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192, PCLK/32768, PCLK/131072) • Switchable between watchdog timer mode and interval timer mode
	Independent watchdog timer (IWDT)	• 14 bits x 1 channel • Counter-input clock: low-speed on-chip oscillator dedicated to IWDT
Communications	Serial communications interface (SCIb)	• 3 channels • Serial communications modes: Asynchronous, clock synchronous, and smart-card interface • Multiprocessor communications • On-chip baud rate generator allows selection of the desired bit rate • Choice of LSB-first or MSB-first transfer • Noise cancellation (only available in asynchronous mode)
	I^2C bus interface (RIIC)	• 1 channel • Communications formats I^2C bus format/SMBus format Master/slave selectable

Table 1.2 Functions of RX62T Group and RX62G Group Products (1 / 2)

Functions		RX62G Group		RX62T Group				
Pin number		112 Pins	100 Pins	112 Pins	100 Pins	80 Pins (R5F562TxGDFF)	80 Pins	64 Pins
Data transfer	Data transfer controller (DTC)	√						
Interrupt controller (ICU)	Input on the NMI pin	√						
	Input on the IRQ pins	√ (8)						√ (4)
Timers	Multi-function timer pulse unit 3 (MTU3)	√				√*1		
	General PWM timer (GPT)	—		√		√*1		
	General PWM timer (GPTa)	√		—				
	MTU3/GPT complementary PWM pin	12					6	
	Port output enable 3 (POE3)	√ (POE pins: 5)						√ (POE pins: 3)
	Compare match timer (CMT)	√						
	Watchdog timer (WDT)	√						
	Independent watchdog timer (IWDT)	√						
Communication function	Serial communications interface (SCI)	√						
	I²C bus interface (RIIC)	√						
	CAN module (CAN) (as an optional function)	√						
	LIN module (LIN)	√						
	Serial peripheral interface (RSPI)	√						
12-bit A/D converter (S12ADA)		√ (4 ch. x 2 units)						
	Simultaneous sampling on three channels	√ (2 units)						
	Programmable gain amplifier	√ (3 ch. x 2 units)						
	Window comparator	√ (3 ch. x 2 units)						
10-bit A/D converter (ADA)		√ (12 ch.)				√ (4 ch.)		—
CRC calculator (CRC)		√						
I/O ports	I/O pins	61	55	61	55	44	44	37
	Input pins	21	21	21	21	13	13	9

Table 1.5 List of Pins and Pin Functions (100-Pin LQFP) (2 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi-cation	Interrupt	POE	Debugging
41		PA0		MTIOC6C	SSL3-B			
42	VCC							
43		P96				IRQ4	POE4#	
44	VSS							
45		P95		MTIOC6B				
46		P94		MTIOC7A				
47		P93		MTIOC7B				
48		P92		MTIOC6D				
49		P91		MTIOC7C				
50		P90		MTIOC7D				
51		P76		MTIOC4D/ GTIOC2B-A				
52		P75		MTIOC4C/ GTIOC1B-A				
53		P74		MTIOC3D/ GTIOC0B-A				
54		P73		MTIOC4B/ GTIOC2A-A				
55		P72		MTIOC4A/ GTIOC1A-A				
56		P71		MTIOC3B/ GTIOC0A-A				
57		P70				IRQ5	POE0#	
58		P33		MTIOC3A/ MTCLKA-A	SSL3-A			
59		P32		MTIOC3C/ MTCLKB-A	SSL2-A			
60	VCC							
61		P31		MTIOC0A-B/ MTCLKC-A	SSL1-A			
62	VSS							
63		P30		MTIOC0B-B/ MTCLKD-A	SSL0-A			
64		P24			RSPCK-A			
65		P23			CTX-B/ LTX/ MOSI-A			
66		P22	ADTRG#		CRX-B/ LRX/ MISO-A			
67		P21	ADTRG1#-B	MTCLKA-B		IRQ6		
68		P20	ADTRG0#-B	MTCLKB-B		IRQ7		
69		P65	AN5					
70		P64	AN4					
71	AVCC							
72	VREF							
73	AVSS							
74		P63	AN3					
75		P62	AN2					
76		P61	AN1					

4. I/O Registers

This section gives information on the on-chip I/O register addresses and bit configurations. The information is given as shown below. Notes on writing to registers are also given at the end.

(1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to functional modules (abbreviations).
- The number of access cycles indicates the number of states based on the specified reference clock.
- Among the I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.
- A unit of access is specified for each register. Access other than in the specified unit is prohibited.

(2) I/O register bits

- Bit configurations of the registers are listed in the same order as the register addresses.
- Reserved bits are indicated by "—" in the bit name column.
- Space in the bit name field indicates that the entire register is allocated to either the counter or data.
- For the registers of 16 or 32 bits, the MSB is listed first.

(3) Notes on writing to I/O registers

When writing to an I/O register, the CPU starts executing the subsequent instruction before completing I/O register write. This may cause the subsequent instruction to be executed before the post-update I/O register value is reflected on the operation.
As described in the following examples, special care is required for the cases in which the subsequent instruction must be executed after the post-update I/O register value is actually reflected.

[Examples of cases requiring special care]

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERm of the ICU (interrupt request enable bit)*1 cleared to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

Note 1. See section 11.2.2, Interrupt Request Enable Register m (IERm) (m = 02h to 1Fh) in the User's manual: Hardware.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

Table 4.1 List of I/O Registers (Address Order) (2 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 6526h	MPU	Region invalidation operation register	MPOPI	16	16	1 ICLK
0008 6528h	MPU	Instruction-hit region register	MHITI	32	32	1 ICLK
0008 652Ch	MPU	Data-hit region register	MHITD	32	32	1 ICLK
0008 7010h	ICU	Interrupt request register 016	IR016	8	8	2 ICLK
0008 7015h	ICU	Interrupt request register 021	IR021	8	8	2 ICLK
0008 7017h	ICU	Interrupt request register 023	IR023	8	8	2 ICLK
0008 701Bh	ICU	Interrupt request register 027	IR027	8	8	2 ICLK
0008 701Ch	ICU	Interrupt request register 028	IR028	8	8	2 ICLK
0008 701Dh	ICU	Interrupt request register 029	IR029	8	8	2 ICLK
0008 701Eh	ICU	Interrupt request register 030	IR030	8	8	2 ICLK
0008 701Fh	ICU	Interrupt request register 031	IR031	8	8	2 ICLK
0008 702Ch	ICU	Interrupt request register 044	IR044	8	8	2 ICLK
0008 702Dh	ICU	Interrupt request register 045	IR045	8	8	2 ICLK
0008 702Eh	ICU	Interrupt request register 046	IR046	8	8	2 ICLK
0008 702Fh	ICU	Interrupt request register 047	IR047	8	8	2 ICLK
0008 7038h	ICU	Interrupt request register 056	IR056	8	8	2 ICLK
0008 7039h	ICU	Interrupt request register 057	IR057	8	8	2 ICLK
0008 703Ah	ICU	Interrupt request register 058	IR058	8	8	2 ICLK
0008 703Bh	ICU	Interrupt request register 059	IR059	8	8	2 ICLK
0008 703Ch	ICU	Interrupt request register 060	IR060	8	8	2 ICLK
0008 7040h	ICU	Interrupt request register 064	IR064	8	8	2 ICLK
0008 7041h	ICU	Interrupt request register 065	IR065	8	8	2 ICLK
0008 7042h	ICU	Interrupt request register 066	IR066	8	8	2 ICLK
0008 7043h	ICU	Interrupt request register 067	IR067	8	8	2 ICLK
0008 7044h	ICU	Interrupt request register 068	IR068	8	8	2 ICLK
0008 7045h	ICU	Interrupt request register 069	IR069	8	8	2 ICLK
0008 7046h	ICU	Interrupt request register 070	IR070	8	8	2 ICLK
0008 7047h	ICU	Interrupt request register 071	IR071	8	8	2 ICLK
0008 7060h	ICU	Interrupt request register 096	IR096	8	8	2 ICLK
0008 7062h	ICU	Interrupt request register 098	IR098	8	8	2 ICLK
0008 7066h	ICU	Interrupt request register 102	IR102	8	8	2 ICLK
0008 7067h	ICU	Interrupt request register 103	IR103	8	8	2 ICLK
0008 706Ah	ICU	Interrupt request register 106	IR106	8	8	2 ICLK
0008 7072h	ICU	Interrupt request register 114	IR114	8	8	2 ICLK
0008 7073h	ICU	Interrupt request register 115	IR115	8	8	2 ICLK
0008 7074h	ICU	Interrupt request register 116	IR116	8	8	2 ICLK
0008 7075h	ICU	Interrupt request register 117	IR117	8	8	2 ICLK
0008 7076h	ICU	Interrupt request register 118	IR118	8	8	2 ICLK
0008 7077h	ICU	Interrupt request register 119	IR119	8	8	2 ICLK
0008 7078h	ICU	Interrupt request register 120	IR120	8	8	2 ICLK
0008 7079h	ICU	Interrupt request register 121	IR121	8	8	2 ICLK
0008 707Ah	ICU	Interrupt request register 122	IR122	8	8	2 ICLK
0008 707Bh	ICU	Interrupt request register 123	IR123	8	8	2 ICLK
0008 707Ch	ICU	Interrupt request register 124	IR124	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (3 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 707Dh	ICU	Interrupt request register 125	IR125	8	8	2 ICLK
0008 707Eh	ICU	Interrupt request register 126	IR126	8	8	2 ICLK
0008 707Fh	ICU	Interrupt request register 127	IR127	8	8	2 ICLK
0008 7080h	ICU	Interrupt request register 128	IR128	8	8	2 ICLK
0008 7081h	ICU	Interrupt request register 129	IR129	8	8	2 ICLK
0008 7082h	ICU	Interrupt request register 130	IR130	8	8	2 ICLK
0008 7083h	ICU	Interrupt request register 131	IR131	8	8	2 ICLK
0008 7084h	ICU	Interrupt request register 132	IR132	8	8	2 ICLK
0008 7085h	ICU	Interrupt request register 133	IR133	8	8	2 ICLK
0008 7086h	ICU	Interrupt request register 134	IR134	8	8	2 ICLK
0008 7087h	ICU	Interrupt request register 135	IR135	8	8	2 ICLK
0008 7088h	ICU	Interrupt request register 136	IR136	8	8	2 ICLK
0008 7089h	ICU	Interrupt request register 137	IR137	8	8	2 ICLK
0008 708Ah	ICU	Interrupt request register 138	IR138	8	8	2 ICLK
0008 708Bh	ICU	Interrupt request register 139	IR139	8	8	2 ICLK
0008 708Ch	ICU	Interrupt request register 140	IR140	8	8	2 ICLK
0008 708Dh	ICU	Interrupt request register 141	IR141	8	8	2 ICLK
0008 708Eh	ICU	Interrupt request register 142	IR142	8	8	2 ICLK
0008 708Fh	ICU	Interrupt request register 143	IR143	8	8	2 ICLK
0008 7090h	ICU	Interrupt request register 144	IR144	8	8	2 ICLK
0008 7091h	ICU	Interrupt request register 145	IR145	8	8	2 ICLK
0008 7092h	ICU	Interrupt request register 146	IR146	8	8	2 ICLK
0008 7095h	ICU	Interrupt request register 149	IR149	8	8	2 ICLK
0008 7096h	ICU	Interrupt request register 150	IR150	8	8	2 ICLK
0008 7097h	ICU	Interrupt request register 151	IR151	8	8	2 ICLK
0008 7098h	ICU	Interrupt request register 152	IR152	8	8	2 ICLK
0008 7099h	ICU	Interrupt request register 153	IR153	8	8	2 ICLK
0008 70AAh	ICU	Interrupt request register 170	IR170	8	8	2 ICLK
0008 70ABh	ICU	Interrupt request register 171	IR171	8	8	2 ICLK
0008 70ACh	ICU	Interrupt request register 172	IR172	8	8	2 ICLK
0008 70ADh	ICU	Interrupt request register 173	IR173	8	8	2 ICLK
0008 70AEh	ICU	Interrupt request register 174	IR174	8	8	2 ICLK
0008 70AFh	ICU	Interrupt request register 175	IR175	8	8	2 ICLK
0008 70B0h	ICU	Interrupt request register 176	IR176	8	8	2 ICLK
0008 70B1h	ICU	Interrupt request register 177	IR177	8	8	2 ICLK
0008 70B2h	ICU	Interrupt request register 178	IR178	8	8	2 ICLK
0008 70B3h	ICU	Interrupt request register 179	IR179	8	8	2 ICLK
0008 70B4h	ICU	Interrupt request register 180	IR180	8	8	2 ICLK
0008 70B5h	ICU	Interrupt request register 181	IR181	8	8	2 ICLK
0008 70B6h	ICU	Interrupt request register 182	IR182	8	8	2 ICLK
0008 70B7h	ICU	Interrupt request register 183	IR183	8	8	2 ICLK
0008 70B8h	ICU	Interrupt request register 184	IR184	8	8	2 ICLK
0008 70BAh	ICU	Interrupt request register 186	IR186	8	8	2 ICLK
0008 70BBh	ICU	Interrupt request register 187	IR187	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (12 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 90A4h	S12AD1	A/D data register 2	ADDR2	16	16	2, 3 PCLK*3
0008 90A6h	S12AD1	A/D data register 3	ADDR3	16	16	2, 3 PCLK*3
0008 90B0h	S12AD1	A/D data register 0B	ADDR0B	16	16	2, 3 PCLK*3
0008 90E0h	S12AD1	A/D sampling state register	ADSSTR	8	8	2, 3 PCLK*3
0008 C001h	PORT1	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C002h	PORT2	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C003h	PORT3	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C007h	PORT7	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C008h	PORT8	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C009h	PORT9	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C00Ah	PORTA	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C00Bh	PORTB	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C00Dh	PORTD	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C00Eh	PORTE	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C010h	PORTG	Data direction register	DDR*1	8	8	2, 3 PCLK*3
0008 C021h	PORT1	Data register	DR	8	8	2, 3 PCLK*3
0008 C022h	PORT2	Data register	DR	8	8	2, 3 PCLK*3
0008 C023h	PORT3	Data register	DR	8	8	2, 3 PCLK*3
0008 C027h	PORT7	Data register	DR	8	8	2, 3 PCLK*3
0008 C028h	PORT8	Data register	DR	8	8	2, 3 PCLK*3
0008 C029h	PORT9	Data register	DR	8	8	2, 3 PCLK*3
0008 C02Ah	PORTA	Data register	DR	8	8	2, 3 PCLK*3
0008 C02Bh	PORTB	Data register	DR	8	8	2, 3 PCLK*3
0008 C02Dh	PORTD	Data register	DR	8	8	2, 3 PCLK*3
0008 C02Eh	PORTE	Data register	DR	8	8	2, 3 PCLK*3
0008 C030h	PORTG	Data register	DR*1	8	8	2, 3 PCLK*3
0008 C041h	PORT1	Data register	PORT	8	8	2, 3 PCLK*3
0008 C042h	PORT2	Data register	PORT	8	8	2, 3 PCLK*3
0008 C043h	PORT3	Data register	PORT	8	8	2, 3 PCLK*3
0008 C044h	PORT4	Data register	PORT	8	8	2, 3 PCLK*3
0008 C045h	PORT5	Data register	PORT	8	8	2, 3 PCLK*3
0008 C046h	PORT6	Data register	PORT	8	8	2, 3 PCLK*3
0008 C047h	PORT7	Data register	PORT	8	8	2, 3 PCLK*3
0008 C048h	PORT8	Data register	PORT	8	8	2, 3 PCLK*3
0008 C049h	PORT9	Data register	PORT	8	8	2, 3 PCLK*3
0008 C04Ah	PORTA	Data register	PORT	8	8	2, 3 PCLK*3
0008 C04Bh	PORTB	Data register	PORT	8	8	2, 3 PCLK*3
0008 C04Dh	PORTD	Data register	PORT	8	8	2, 3 PCLK*3
0008 C04Eh	PORTE	Data register	PORT	8	8	2, 3 PCLK*3
0008 C050h	PORTG	Port register	PORT*1	8	8	2, 3 PCLK*3
0008 C061h	PORT1	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C062h	PORT2	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C063h	PORT3	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C064h	PORT4	Input buffer control register	ICR	8	8	2, 3 PCLK*3

Table 4.1 List of I/O Registers (Address Order) (14 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 C29Ch	SYSTEM	Deep standby backup register 12	DPSBKR12	8	8	4, 5 PCLK*3
0008 C29Dh	SYSTEM	Deep standby backup register 13	DPSBKR13	8	8	4, 5 PCLK*3
0008 C29Eh	SYSTEM	Deep standby backup register 14	DPSBKR14	8	8	4, 5 PCLK*3
0008 C29Fh	SYSTEM	Deep standby backup register 15	DPSBKR15	8	8	4, 5 PCLK*3
0008 C2A0h	SYSTEM	Deep standby backup register 16	DPSBKR16	8	8	4, 5 PCLK*3
0008 C2A1h	SYSTEM	Deep standby backup register 17	DPSBKR17	8	8	4, 5 PCLK*3
0008 C2A2h	SYSTEM	Deep standby backup register 18	DPSBKR18	8	8	4, 5 PCLK*3
0008 C2A3h	SYSTEM	Deep standby backup register 19	DPSBKR19	8	8	4, 5 PCLK*3
0008 C2A4h	SYSTEM	Deep standby backup register 20	DPSBKR20	8	8	4, 5 PCLK*3
0008 C2A5h	SYSTEM	Deep standby backup register 21	DPSBKR21	8	8	4, 5 PCLK*3
0008 C2A6h	SYSTEM	Deep standby backup register 22	DPSBKR22	8	8	4, 5 PCLK*3
0008 C2A7h	SYSTEM	Deep standby backup register 23	DPSBKR23	8	8	4, 5 PCLK*3
0008 C2A8h	SYSTEM	Deep standby backup register 24	DPSBKR24	8	8	4, 5 PCLK*3
0008 C2A9h	SYSTEM	Deep standby backup register 25	DPSBKR25	8	8	4, 5 PCLK*3
0008 C2AAh	SYSTEM	Deep standby backup register 26	DPSBKR26	8	8	4, 5 PCLK*3
0008 C2ABh	SYSTEM	Deep standby backup register 27	DPSBKR27	8	8	4, 5 PCLK*3
0008 C2ACh	SYSTEM	Deep standby backup register 28	DPSBKR28	8	8	4, 5 PCLK*3
0008 C2ADh	SYSTEM	Deep standby backup register 29	DPSBKR29	8	8	4, 5 PCLK*3
0008 C2AEh	SYSTEM	Deep standby backup register 30	DPSBKR30	8	8	4, 5 PCLK*3
0008 C2AFh	SYSTEM	Deep standby backup register 31	DPSBKR31	8	8	4, 5 PCLK*3
0008 C4C0h	POE	Input level control/status register 1	ICSR1	16	8, 16	2, 3 PCLK*3
0008 C4C2h	POE	Output level control/status register 1	OCSR1	16	8, 16	2, 3 PCLK*3
0008 C4C4h	POE	Input level control/status register 2	ICSR2	16	8, 16	2, 3 PCLK*3
0008 C4C6h	POE	Output level control/status register 2	OCSR2	16	8, 16	2, 3 PCLK*3
0008 C4C8h	POE	Input level control/status register 3	ICSR3	16	8, 16	2, 3 PCLK*3
0008 C4CAh	POE	Software port output enable register	SPOER	8	8	2, 3 PCLK*3
0008 C4CBh	POE	Port output enable control register 1	POECR1	8	8	2, 3 PCLK*3
0008 C4CCh	POE	Port output enable control register 2	POECR2	16	16	2, 3 PCLK*3
0008 C4CEh	POE	Port output enable control register 3	POECR3	16	16	2, 3 PCLK*3
0008 C4D0h	POE	Port output enable control register 4	POECR4	16	16	2, 3 PCLK*3
0008 C4D2h	POE	Port output enable control register 5	POECR5	16	16	2, 3 PCLK*3
0008 C4D4h	POE	Port output enable control register 6	POECR6	16	16	2, 3 PCLK*3
0008 C4D6h	POE	Input level control/status register 4	ICSR4	16	8, 16	2, 3 PCLK*3
0008 C4D8h	POE	Input level control/status register 5	ICSR5	16	8, 16	2, 3 PCLK*3
0008 C4DAh	POE	Active level setting register 1	ALR1	16	8, 16	2, 3 PCLK*3
0009 0200h to 0009 03FFh	CAN0*2	Mailbox registers 0 to 31	MB0 to MB 31	128	8, 16, 32	2, 3 PCLK*3
0009 0400h	CAN0*2	Mask register 0	MKR0	32	8, 16, 32	2, 3 PCLK*3
0009 0404h	CAN0*2	Mask register 1	MKR1	32	8, 16, 32	2, 3 PCLK*3
0009 0408h	CAN0*2	Mask register 2	MKR2	32	8, 16, 32	2, 3 PCLK*3
0009 040Ch	CAN0*2	Mask register 3	MKR3	32	8, 16, 32	2, 3 PCLK*3
0009 0410h	CAN0*2	Mask register 4	MKR4	32	8, 16, 32	2, 3 PCLK*3
0009 0414h	CAN0*2	Mask register 5	MKR5	32	8, 16, 32	2, 3 PCLK*3
0009 0418h	CAN0*2	Mask register 6	MKR6	32	8, 16, 32	2, 3 PCLK*3

Table 4.1 List of I/O Registers (Address Order) (19 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000C 1A39h	MTU7	Timer buffer operation transfer mode register	TBTM	8	8	5 ICLK
000C 1A3Ah	MTU	Timer interrupt skipping mode register B	TITMRB	8	8	5 ICLK
000C 1A3Bh	MTU	Timer interrupt skipping set register 2B	TITCR2B	8	8	5 ICLK
000C 1A3Ch	MTU	Timer interrupt skipping counter 2B	TITCNT2B	8	8	5 ICLK
000C 1A40h	MTU7	Timer A/D converter start request control register	TADCR	16	16	5 ICLK
000C 1A44h	MTU7	Timer A/D converter start request cycle set register A	TADCORA	16	16, 32	5 ICLK
000C 1A46h	MTU7	Timer A/D converter start request cycle set register B	TADCORB	16	16	5 ICLK
000C 1A48h	MTU7	Timer A/D converter start request cycle set buffer register A	TADCOBRA	16	16, 32	5 ICLK
000C 1A4Ah	MTU7	Timer A/D converter start request cycle set buffer register B	TADCOBRB	16	16	5 ICLK
000C 1A50h	MTU6	Timer synchronous clear register	TSYCR	8	8	5 ICLK
000C 1A60h	MTU	Timer waveform control register B	TWCRB	8	8	5 ICLK
000C 1A70h	MTU	Timer mode register 2B	TMDR2B	8	8	5 ICLK
000C 1A72h	MTU6	Timer general register E	TGRE	16	16	5 ICLK
000C 1A74h	MTU7	Timer general register E	TGRE	16	16	5 ICLK
000C 1A76h	MTU7	Timer general register F	TGRF	16	16	5 ICLK
000C 1A80h	MTU	Timer start register B	TSTRB	8	8, 16	5 ICLK
000C 1A81h	MTU	Timer synchronous register B	TSYRB	8	8	5 ICLK
000C 1A84h	MTU	Timer read/write enable register B	TRWERB	8	8	5 ICLK
000C 1C80h	MTU5	Timer counter U	TCNTU	16	16, 32	5 ICLK
000C 1C82h	MTU5	Timer general register U	TGRU	16	16	5 ICLK
000C 1C84h	MTU5	Timer control register U	TCRU	8	8	5 ICLK
000C 1C86h	MTU5	Timer I/O control register U	TIORU	8	8	5 ICLK
000C 1C90h	MTU5	Timer counter V	TCNTV	16	16, 32	5 ICLK
000C 1C92h	MTU5	Timer general register V	TGRV	16	16	5 ICLK
000C 1C94h	MTU5	Timer control register V	TCRV	8	8	5 ICLK
000C 1C96h	MTU5	Timer I/O control register V	TIORV	8	8	5 ICLK
000C 1CA0h	MTU5	Timer counter W	TCNTW	16	16, 32	5 ICLK
000C 1CA2h	MTU5	Timer general register W	TGRW	16	16	5 ICLK
000C 1CA4h	MTU5	Timer control register W	TCRW	8	8	5 ICLK
000C 1CA6h	MTU5	Timer I/O control register W	TIORW	8	8	5 ICLK
000C 1CB0h	MTU5	Timer status register	TSR	8	8	5 ICLK
000C 1CB2h	MTU5	Timer interrupt enable register	TIER	8	8	5 ICLK
000C 1CB4h	MTU5	Timer start register	TSTR	8	8	5 ICLK
000C 1CB6h	MTU5	Timer compare match clear register	TCNTCMPCLR	8	8	5 ICLK
000C 2000h	GPT	General PWM timer software start register	GTSTR	16	8, 16, 32	3 to 5 ICLK*4
000C 2004h	GPT	General PWM timer hardware source start control register	GTHSCR	16	8, 16, 32	3 to 5 ICLK*4
000C 2006h	GPT	General PWM timer hardware source clear control register	GTHCCR	16	8, 16, 32	3 to 5 ICLK*4
000C 2008h	GPT	General PWM timer hardware start source select register	GTHSSR	16	8, 16, 32	3 to 5 ICLK*4

Table 4.1 List of I/O Registers (Address Order) (21 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000C 2116h	GPT0	General PWM timer compare capture register D	GTCCRD	16	16, 32	3 to 5 ICLK*4
000C 2118h	GPT0	General PWM timer compare capture register E	GTCCRE	16	16, 32	3 to 5 ICLK*4
000C 211Ah	GPT0	General PWM timer compare capture register F	GTCCRF	16	16, 32	3 to 5 ICLK*4
000C 211Ch	GPT0	General PWM timer cycle setting register	GTPR	16	16, 32	3 to 5 ICLK*4
000C 211Eh	GPT0	General PWM timer cycle setting buffer register	GTPBR	16	16, 32	3 to 5 ICLK*4
000C 2120h	GPT0	General PWM timer cycle setting double-buffer register	GTPDBR	16	16, 32	3 to 5 ICLK*4
000C 2124h	GPT0	A/D converter start request timing register A	GTADTRA	16	16, 32	3 to 5 ICLK*4
000C 2126h	GPT0	A/D converter start request timing buffer register A	GTADTBRA	16	16, 32	3 to 5 ICLK*4
000C 2128h	GPT0	A/D converter start request timing double-buffer register A	GTADTDBRA	16	16, 32	3 to 5 ICLK*4
000C 212Ch	GPT0	A/D converter start request timing register B	GTADTRB	16	16, 32	3 to 5 ICLK*4
000C 212Eh	GPT0	A/D converter start request timing buffer register B	GTADTBRB	16	16, 32	3 to 5 ICLK*4
000C 2130h	GPT0	A/D converter start request timing double-buffer register B	GTADTDBRB	16	16, 32	3 to 5 ICLK*4
000C 2134h	GPT0	General PWM timer output negate control register	GTONCR	16	16, 32	3 to 5 ICLK*4
000C 2136h	GPT0	General PWM timer dead time control register	GTDTCR	16	16, 32	3 to 5 ICLK*4
000C 2138h	GPT0	General PWM timer dead time value register	GTDVU	16	16, 32	3 to 5 ICLK*4
000C 213Ah	GPT0	General PWM timer dead time value register	GTDVD	16	16, 32	3 to 5 ICLK*4
000C 213Ch	GPT0	General PWM timer dead time buffer register	GTDBU	16	16, 32	3 to 5 ICLK*4
000C 213Eh	GPT0	General PWM timer dead time buffer register	GTDBD	16	16, 32	3 to 5 ICLK*4
000C 2140h	GPT0	General PWM timer output protection function status register	GTSOS	16	16, 32	3 to 5 ICLK*4
000C 2142h	GPT0	General PWM timer output protection function temporary release register	GTSOTR	16	16, 32	3 to 5 ICLK*4
000C 2180h	GPT1	General PWM timer I/O control register	GTIOR	16	8, 16, 32	3 to 5 ICLK*4
000C 2182h	GPT1	General PWM timer interrupt output setting register	GTINTAD	16	8, 16, 32	3 to 5 ICLK*4
000C 2184h	GPT1	General PWM timer control register	GTCR	16	8, 16, 32	3 to 5 ICLK*4
000C 2186h	GPT1	General PWM timer buffer enable register	GTBER	16	8, 16, 32	3 to 5 ICLK*4
000C 2188h	GPT1	General PWM timer count direction register	GTUDC	16	8, 16, 32	3 to 5 ICLK*4
000C 218Ah	GPT1	General PWM timer interrupt and A/D converter start request skipping setting register	GTITC	16	8, 16, 32	3 to 5 ICLK*4
000C 218Ch	GPT1	General PWM timer status register	GTST	16	8, 16, 32	3 to 5 ICLK*4
000C 218Eh	GPT1	General PWM timer counter	GTCNT	16	16	3 to 5 ICLK*4
000C 2190h	GPT1	General PWM timer compare capture register A	GTCCRA	16	16, 32	3 to 5 ICLK*4
000C 2192h	GPT1	General PWM timer compare capture register B	GTCCRB	16	16, 32	3 to 5 ICLK*4
000C 2194h	GPT1	General PWM timer compare capture register C	GTCCRC	16	16, 32	3 to 5 ICLK*4
000C 2196h	GPT1	General PWM timer compare capture register D	GTCCRD	16	16, 32	3 to 5 ICLK*4
000C 2198h	GPT1	General PWM timer compare capture register E	GTCCRE	16	16, 32	3 to 5 ICLK*4
000C 219Ah	GPT1	General PWM timer compare capture register F	GTCCRF	16	16, 32	3 to 5 ICLK*4
000C 219Ch	GPT1	General PWM timer cycle setting register	GTPR	16	16, 32	3 to 5 ICLK*4
000C 219Eh	GPT1	General PWM timer cycle setting buffer register	GTPBR	16	16, 32	3 to 5 ICLK*4

Table 4.2 List of I/O Registers (Bit Order) (3 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
MPU	RSPAGE7				RSPN[27:0]				
					RSPN[27:0]				
					RSPN[27:0]				
				RSPN[27:0]		—	—	—	—
MPU	REPAGE7				REPN[27:0]				
					REPN[27:0]				
					REPN[27:0]				
				REPN[27:0]			UAC[2:0]		V
MPU	MPEN	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	MPEN
MPU	MPBAC	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—		UBAC[2:0]		—
MPU	MPECLR	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	CLR
MPU	MPESTS	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	DRW	DA	IA
MPU	MPDEA				DEA[31:0]				
					DEA[31:0]				
					DEA[31:0]				
					DEA[31:0]				
MPU	MPSA				SA[31:0]				
					SA[31:0]				
					SA[31:0]				
					SA[31:0]				
MPU	MPOPS	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	S
MPU	MPOPI	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	INV
MPU	MHITI	—	—	—	—	—	—	—	—
					HITI[7:0]				
		—	—	—	—	—	—	—	—
		—	—	—	—		UHACI[2:0]		—
MPU	MHITD	—	—	—	—	—	—	—	—
					HITD[7:0]				
		—	—	—	—	—	—	—	—
		—	—	—	—		UHACD[2:0]		—
ICU	IR016	—	—	—	—	—	—	—	IR
ICU	IR021	—	—	—	—	—	—	—	IR
ICU	IR023	—	—	—	—	—	—	—	IR
ICU	IR027	—	—	—	—	—	—	—	IR
ICU	IR028	—	—	—	—	—	—	—	IR
ICU	IR029	—	—	—	—	—	—	—	IR
ICU	IR030	—	—	—	—	—	—	—	IR
ICU	IR031	—	—	—	—	—	—	—	IR

Table 4.2 List of I/O Registers (Bit Order) (28 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
GPT3	GTCCRB								
GPT3	GTCCRC								
GPT3	GTCCRD								
GPT3	GTCCRE								
GPT3	GTCCRF								
GPT3	GTPR								
GPT3	GTPBR								
GPT3	GTPDBR								
GPT3	GTADTRA								
GPT3	GTADTBRA								
GPT3	GTADTDBRA								
GPT3	GTADTRB								
GPT3	GTADTBRB								
GPT3	GTADTDBRB								
GPT3	GTONCR	OBE	OAE	—	SWN	—	—	—	NFV
				NFS[3:0]		NVB	NVA	NEB	NEA
GPT3	GTDTCR	—	—	—	—	—	—	—	TDFER
		—	—	TDBDE	TDBUE	—	—	—	TDE
GPT3	GTDVU								
GPT3	GTDVD								
GPT3	GTDBU								
GPT3	GTDBD	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	SOS[1:0]	
GPT3	GTSOS	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	SOS[1:0]	
GPT3	GTSOTR	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	SOTR
GPT0	GTDLYCR	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLYEN	DLYRST	DLLEN
GPT1	GTDLYCR	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLYEN	DLYRST	DLLEN

Table 4.2 List of I/O Registers (Bit Order) (29 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
GPT2	GTDLYCR	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLYEN	DLYRST	DLLEN
GPT3	GTDLYCR	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLYEN	DLYRST	DLLEN
GPT0	GTDLYRA	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT0	GTDLYRB	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT1	GTDLYRA	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT1	GTDLYRB	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT2	GTDLYRA	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT2	GTDLYRB	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT3	GTDLYRA	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT3	GTDLYRB	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT0	GTDLYFA	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT0	GTDLYFB	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT1	GTDLYFA	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT1	GTDLYFB	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT2	GTDLYRA	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT2	GTDLYFB	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT3	GTDLYFA	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT3	GTDLYFB	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
FLASH	FMODR	—	—	—	FRDMD		—	—	—
FLASH	FASTAT	ROMAE	—	—	CMDLK	DFLAE	—	DFLRPE	DFLWPE
FLASH	FAEINT	ROMAEIE	—	—	CMDLKIE	DFLAEIE	—	DFLRPEIE	DFLWPEIE
FLASH	FRDYIE	—	—	—	—	—	—	—	FRDYIE
FLASH	DFLRE0	KEY[7:0]							
		DBRE07	DBRE06	DBRE05	DBRE04	DBRE03	DBRE02	DBRE01	DBRE00
FLASH	DFLRE1	KEY[7:0]							
		DBRE15	DBRE14	DBRE13	DBRE12	DBRE11	DBRE10	DBRE09	DBRE08
FLASH	DFLWE0	KEY[7:0]							
		DBWE07	DBWE06	DBWE05	DBWE04	DBWE03	DBWE02	DBWE01	DBWE00
FLASH	DFLWE1	KEY[7:0]							
		DBWE15	DBWE14	DBWE13	DBWE12	DBWE11	DBWE10	DBWE09	DBWE08
FLASH	FCURAME	KEY[7:0]							
		—	—	—	—	—	—	—	FCRME

Table 5.2 DC Characteristics (1) (3 / 3)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input capacitance	All input pins (except for ports PB1 and PB2)	C_{in}	-	-	15	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25°C
	Ports PB1 and PB2		-	-	30		

Note 1. This includes the multiplexed input pins, except in cases where port pins PB1 and PB2 are used as RIIC input pins or port pins P22 to P24, P30, PA3 to PA5, PB0, PD0 to PD2, or PD6 are used as RSPI input pins.

5.3.3 Timing of On-Chip Peripheral Modules

Table 5.9 Timing of On-Chip Peripheral Modules (1)

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item			Symbol	Min.	Typ.	Max.	Unit
SCI	Input clock cycle	Asynchronous	t_{Scyc}	$4 \times t_{Pcyc}$	-	ns	Figure 5.8
		Clock synchronous		$6 \times t_{Pcyc}$	-		
	Input clock pulse width		t_{SCKW}	$0.4 \times t_{Pcyc}$	$0.6 \times t_{Scyc}$	ns	
	Input clock rise time		t_{SCKr}	-	20	ns	
	Input clock fall time		t_{SCKf}	-	20	ns	
	Output clock cycle	Asynchronous	t_{Scyc}	$16 \times t_{Pcyc}$	-	ns	
		Clock synchronous		$6 \times t_{Pcyc}$	-	ns	
	Output clock pulse width		t_{SCKW}	$0.4 \times t_{Scyc}$	$0.6 \times t_{Scyc}$	ns	
	Output clock rise time		t_{SCKr}	-	20	ns	
	Output clock fall time		t_{SCKf}	-	20	ns	
	Transmit data delay time (clock synchronous)		t_{TXD}	-	40	ns	Figure 5.9
	Receive data setup time (clock synchronous)		t_{RXS}	40	-	ns	
	Receive data hold time (clock synchronous)		t_{RXH}	40	-	ns	

Note: • t_{Pcyc}: PCLK cycle

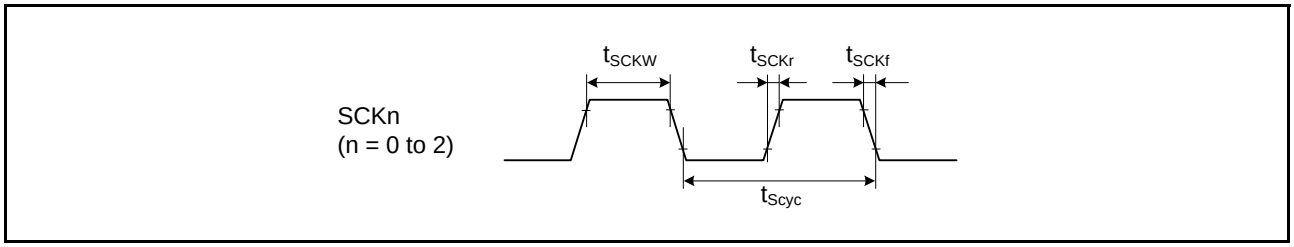

Figure 5.8 SCK Clock Input Timing

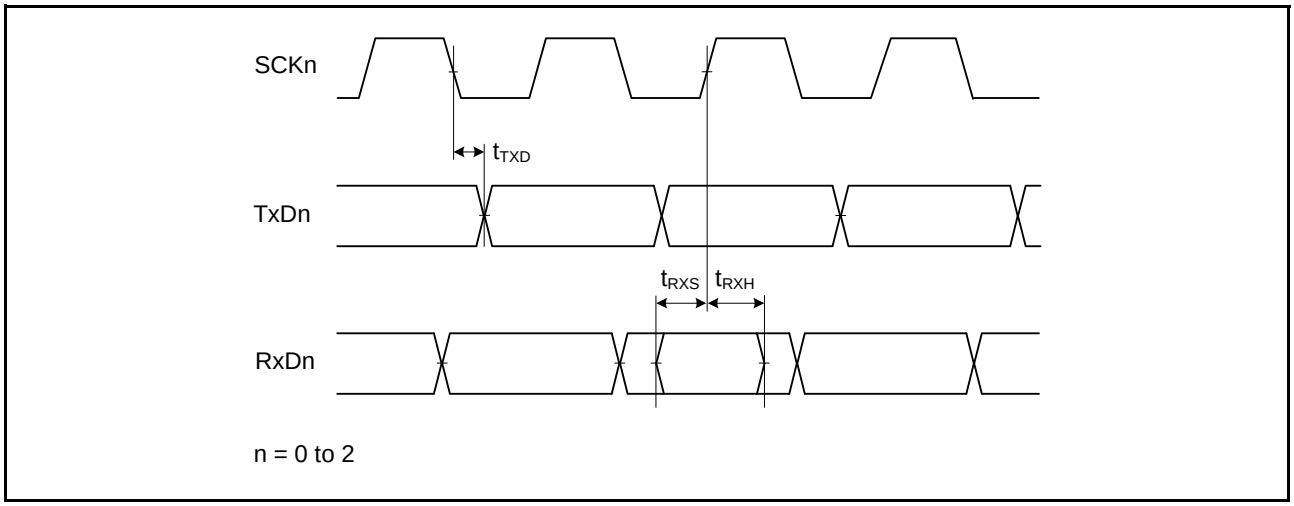

Figure 5.9 SCI Input/Output Timing: Clock Synchronous Mode

5.4 A/D Conversion Characteristics

Table 5.15 10-Bit A/D Conversion Characteristics

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC
Ta = Topr

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	10	10	10	Bit	
Conversion time*1 (AD clock = 25-MHz operation)	2.0	-	-	μs	Sampling 25 states
Analog input capacitance	-	-	4	pF	
Integral nonlinearity error	-	-	±3.0	LSB	
Offset error	-	-	±3.0	LSB	
Full-scale error	-	-	±3.0	LSB	
Quantization error	-	±0.5	-	LSB	
Absolute accuracy	-	-	±4.0	LSB	
Permissible signal source impedance	-	-	1.0	kΩ	

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 2 and 3.

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	10	10	10	Bit	
Conversion time*1 (AD clock = 50-MHz operation)	1.0	-	-	μs	Sampling 25 states
Analog input capacitance	-	-	4	pF	
Integral nonlinearity error	-	-	±3.0	LSB	
Offset error	-	-	±3.0	LSB	
Full-scale error	-	-	±3.0	LSB	
Quantization error	-	±0.5	-	LSB	
Absolute accuracy	-	-	±4.0	LSB	
Permissible signal source impedance	-	-	1.0	kΩ	

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

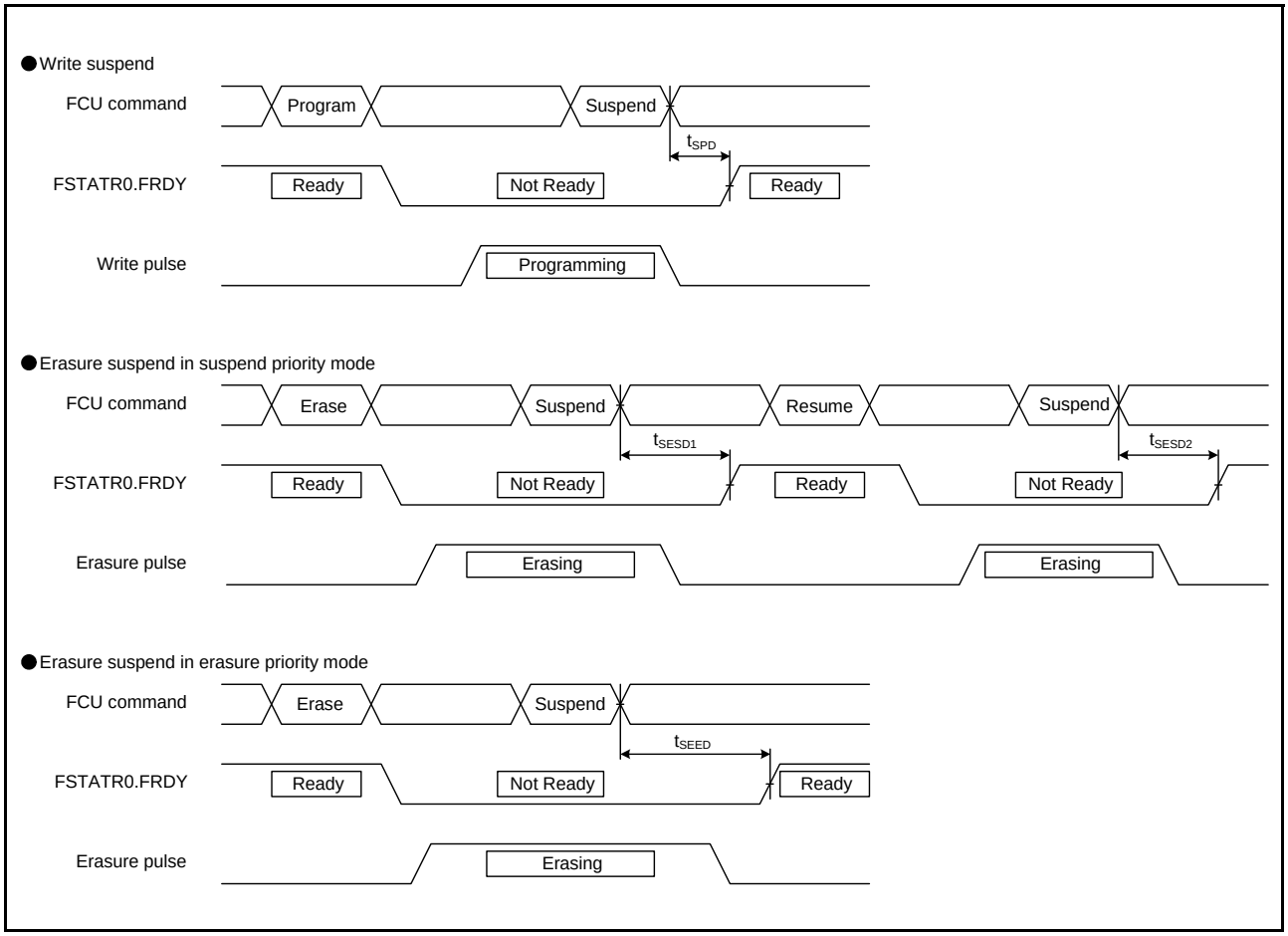

Figure 5.24 Flash Memory Write/Erase Suspend Timing

REVISION HISTORY — RX62T Group, RX62G Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Apr 20, 2011	—	First edition issued
1.30	May 22, 2013	1	Features, Package lineup, added
			1. Overview
		2	Table 1.1 Outline of Specifications (1/5) Description of CPU, added
		3	Table 1.1 Outline of Specifications (2/5) Description of Programmable I/O ports, changed
		6	Table 1.1 Outline of Specifications (5/5), 64-pin packaged, added
		7	Table 1.2 Functions of RX62T Group Products, 64-pin package, and MTU3/GPT complementary PWM pins added
		8	Table 1.3 List of Products, 64-pin package part number, changed
		9	Figure 1.1 How to Read the Product Part No., 64-pin package part number, changed
		9	Figure 1.1 How to Read the Product Part No., 5-V version, two-motor control supported, added
		10	Figure 1.2 Block Diagram, changed
		14	Figure 1.6 Pin Assignment of the 80-Pin LQFP (Two-motor Control Supported), added
		15	Figure 1.7 Pin Assignment of the 64-Pin LQFP, Figure PLQP0064GA-A, added
		25 to 27	Table 1.7 List of Pins and Pin Functions (80-Pin LQFP: R5F562TxGDFF) , added
		30 to 33	Table 1.9 Pin Functions, changed
			4. I/O Register
		38to 61	Table 4.1 List of I/O Registers (Address Order), MPU, added
		47	Table 4.1 List of I/O Registers (Address Order) TMOCNTL, TMOCNTU register, added
		57	Table 4.1 List of I/O Registers (Address Order), GTSWP register, added
			5. Electrical Characteristics
		62	Table 5.1 Absolute Maximum Ratings, note changed
		64	Table 5.2 DC Characteristics (1) (2/3) Test Conditions of P90 to P95, changed
		66	Table 5.3 DC Characteristics (2), note changed
		67	Table 5.4 Permissible Output Currents, note changed
		72	Table 5.7 Control Signal Timing, notes changed
		73	Table 5.8 Timing of On-Chip Peripheral Modules (1), changed
			Appendix 1.Package Dimensions
		96	Figure E 64-Pin LQFP (PLQP0064GA-A), added
2.00	Jan 10, 2014	1	Features, changed
			1. Overview
		2 to 6	Table 1.1 Outline of Specifications, changed; Note 1, added
		7, 8	Table 1.2 Functions of RX62T Group and RX62G Group Products, changed
		9, 10	Table 1.3 List of Products, changed; Note 1, added
		11	Figure 1.1 How to Read the Product Part No., changed
		15	Figure 1.6 Pin Assignment of the 80-Pin LQFP (Two-Motor Control Supported Version), added
		27 to 29	Table 1.7 List of Pins and Pin Functions (80-Pin LQFP: R5F562TxGDFF), added
			4. I/O Registers
		43 to 67	Table 4.1 List of I/O Registers (Address Order), changed
		68 to 97	Table 4.2 List of I/O Registers (Bit Order), changed
			5. Electrical Characteristics
		—	Conditions in the table, change to Ta = -40 to +105°C from Ta = -40 to +85°C.

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		Page	Summary
2.00	Jan 10, 2014	98	Table 5.1 Absolute Maximum Ratings, changed
		102	Table 5.3 DC Characteristics (2): Note 3, changed
		103	Table 5.5 Permissible Power Consumption, added
		117	5.3.4 Timing of PWM Delay Generation Circuit, added
		117	Table 5.14 Timing of the PWM Delay Generation Circuit, added
		120	Table 5.17 Characteristics of the Programmable Gain Amplifier, changed
		125	Table 5.21 ROM (Flash Memory for Code Storage) Characteristics (1), changed
		125	Table 5.22 ROM (Flash Memory for Code Storage) Characteristics (2), added
		126	Table 5.23 Data Flash (Flash Memory for Data Storage) Characteristics (1), changed
		126	Table 5.24 Data Flash (Flash Memory for Data Storage) Characteristics (2), added

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