Renesas Electronics America Inc - R5F562T6DDFM#V1 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562t6ddfm-v1

Table 1.1 Outline of Specifications (2 / 5)

Classification	Module/Function	Description
Interrupt	Interrupt controller (ICU)	• Peripheral function interrupts: 101 sources • External interrupts: 9 (NMI and IRQ0 to IRQ7 pins) • Non-maskable interrupts: 3 (the NMI pin, oscillation stop detection interrupt, and voltage-monitoring interrupt) • 16 levels specifiable for the order of priority
Data transfer	Data transfer controller (DTC)	• Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
I/O ports	Programmable I/O ports	I/O port pins for devices in the 112-pin LQFP/100-pin LQFP/ 80-pin LQFP (R5F562TxGDFF)/80-pin LQFP (except R5F562TxGDFF)/64-pin LQFP • I/O: 61/55/44/44/37 • Input only: 21/21/13/13/9 • Open-drain outputs: 2/2/2/2/2 (I^2C bus interface pins) • Large-current outputs: 12/12/12/6/6(0) (MTU3 and GPT pins) The 5-V version of the 64-pin product does not have large-current outputs. • Reading out the states of pins is always possible.
Timers	Multi-function timer pulse unit 3 (MTU3)	• 16 bits x 8 channels • Up to 24 pulse inputs/outputs and three pulse inputs • Select from among six to eight counter-input clock signals for each channel (ICLK/1, ICLK/4, ICLK/16, ICLK/64, ICLK/256, ICLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available. • 24 output compare or input capture registers • Counter clearing (clearing is synchronizable with compare match or input capture) • Simultaneous writing to multiple timer counters (TCNT) • Input to and output from all registers in synchronization with counter operation • Buffered operation • Cascade-connected operation • 38 kinds of interrupt source • Automatic transfer of register data • Pulse output modes Toggled, PWM, complementary PWM, and reset synchronous PWM • Complementary PWM output mode Outputs non-overlapping waveforms for controlling 3-phase inverters Automatic specification of dead times PWM duty cycle: Selectable as any value from 0% to 100% Delay can be applied to requests for A/D conversion. Non-generation of interrupt requests at peak or trough values of counters can be selected. Double buffering • Reset-synchronous PWM mode Three PWM waveforms and corresponding inverse waveforms are output with the desired duty cycles. • Phase-counting mode • Counter functionality for dead-time compensation • Generation of triggers for A/D converters • Differential timing for initiation of A/D conversion
	Port output enable 3 (POE3)	• Control of the high-impedance state of the MTU3 and GPT's waveform output pins 5 pins for input from signal sources: POE0, POE4, POE8, POE10, POE11 Initiation on detection of short-circuited outputs (detection of simultaneous switching of large-current pins to the active level) Initiation by comparator-detection of analog level input to the 12-bit A/D converter Initiation by oscillation-stoppage detection Initiation by software • Selection of which output pins should be placed in the high-impedance state at the time of each POE input or comparator detection

Table 1.1 Outline of Specifications (3 / 5)

Classification	Module/Function	Description
Timers	General PWM timer (GPT/GPTa)	• 16 bits x 4 channels • Counting up or down (saw-wave), counting up and down (triangle-wave) selectable for all channels • Clock sources independently selectable for all channels • 2 input/output pins per channel • 2 output compare/input capture registers per channel • For the 2 output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally asymmetrically PWM waveforms. • Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow) • Synchronizable operation of the several counters • Modes of synchronized operation (synchronized, or displaced by desired times for phase shifting) • Generation of dead times in PWM operation • Through combination of three counters, generation of automatic three-phase PWM waveforms incorporating dead times • Starting, clearing, and stopping counters in response to external or internal triggers • Internal trigger sources: output of the internal comparator detection, software, and compare-match • The frequency-divided system clock (ICLK) can be used as a counter clock for measuring timing of the edges of signals produced by frequency-dividing the low-speed on-chip oscillator clock signal dedicated to IWDT (to detect abnormal oscillation). • PWM delay generation can control the timing with which signals on the two PWM output pins for each channel rise and fall with an accuracy of up to 1/32 times the period of the system clock (ICLK) (only for GPTa).
	Compare match timer (CMT)	• (16 bits x 2 channels) x 2 units • Select from among four internal clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Watchdog timer (WDT)	• 8 bits x 1 channel • Select from among eight counter-input clock signals (PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192, PCLK/32768, PCLK/131072) • Switchable between watchdog timer mode and interval timer mode
	Independent watchdog timer (IWDT)	• 14 bits x 1 channel • Counter-input clock: low-speed on-chip oscillator dedicated to IWDT
Communications	Serial communications interface (SCIb)	• 3 channels • Serial communications modes: Asynchronous, clock synchronous, and smart-card interface • Multiprocessor communications • On-chip baud rate generator allows selection of the desired bit rate • Choice of LSB-first or MSB-first transfer • Noise cancellation (only available in asynchronous mode)
	I^2C bus interface (RIIC)	• 1 channel • Communications formats I^2C bus format/SMBus format Master/slave selectable

Table 1.1 Outline of Specifications (5 / 5)

Classification	Module/Function	Description
A/D converter	10-bit A/D converter (ADA)	• 10 bits (1 unit x 12 channels) • 10-bit resolution • Conversion time: 1.0 μs per channel (in operation with A/D conversion clock ADCLK at 50 MHz) for AVCC0 = 4.0 to 5.5 V 2.0 μs per channel (in operation with A/D conversion clock ADCLK at 25 MHz) for AVCC = 3.0 to 3.6 V • Two basic operating modes Single mode and scan mode • Scan mode One-cycle scan mode Continuous scan mode • Sample-and-hold function A common sample-and-hold circuit for both units is included. • A/D-conversion register settings for each input pin • Three ways to start A/D conversion Conversion can be started by software, a conversion start trigger from a timer (MTU3 or GPT), or an external trigger signal. • Functionality for 8-bit precision output Right-shifting the results of conversion for output by two bits is selectable. • Self-diagnostic function The self-diagnostic function internally generates three analog input voltages (AVSS, VREF x 1/2, VREF).
CRC calculator (CRC)		• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$. • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.
Operating frequency		ICLK: 8 to 100 MHz PCLK: 8 to 50 MHz
Power supply voltage		• 3-V version VCC = PLLVCC = 2.7 to 3.6V AVCC0 = AVCC = 3.0 to 3.6V, or 4.0 to 5.5V VREFH0 = 3.0 to AVCC0, or 4.0 to AVCC0 VREF = 3.0 to AVCC, or 4.0 to AVCC • 5-V version VCC = PLLVCC = 4.0 to 5.5V AVCC0 = AVCC = 4.0 to 5.5V VREFH0 = 4.0 to AVCC0 VREF = 4.0 to AVCC
Operating temperature		D version: -40 to +85°C, G version: -40 to +105°C*1
Packages		112-pin LQFP (PLQP0112JA-A, 20x20-0.65-mm pitch) 100-pin LQFP (PLQP0100KB-A, 14x14-0.5-mm pitch) 80-pin LQFP (PLQP0080JA-A, 14x14-0.65-mm pitch) 64-pin LQFP (PLQP0064KB-A, 10x10-0.5-mm pitch) 64-pin LQFP (PLQP0064GA-A, 14x14-0.8mm pitch)

Note 1. Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

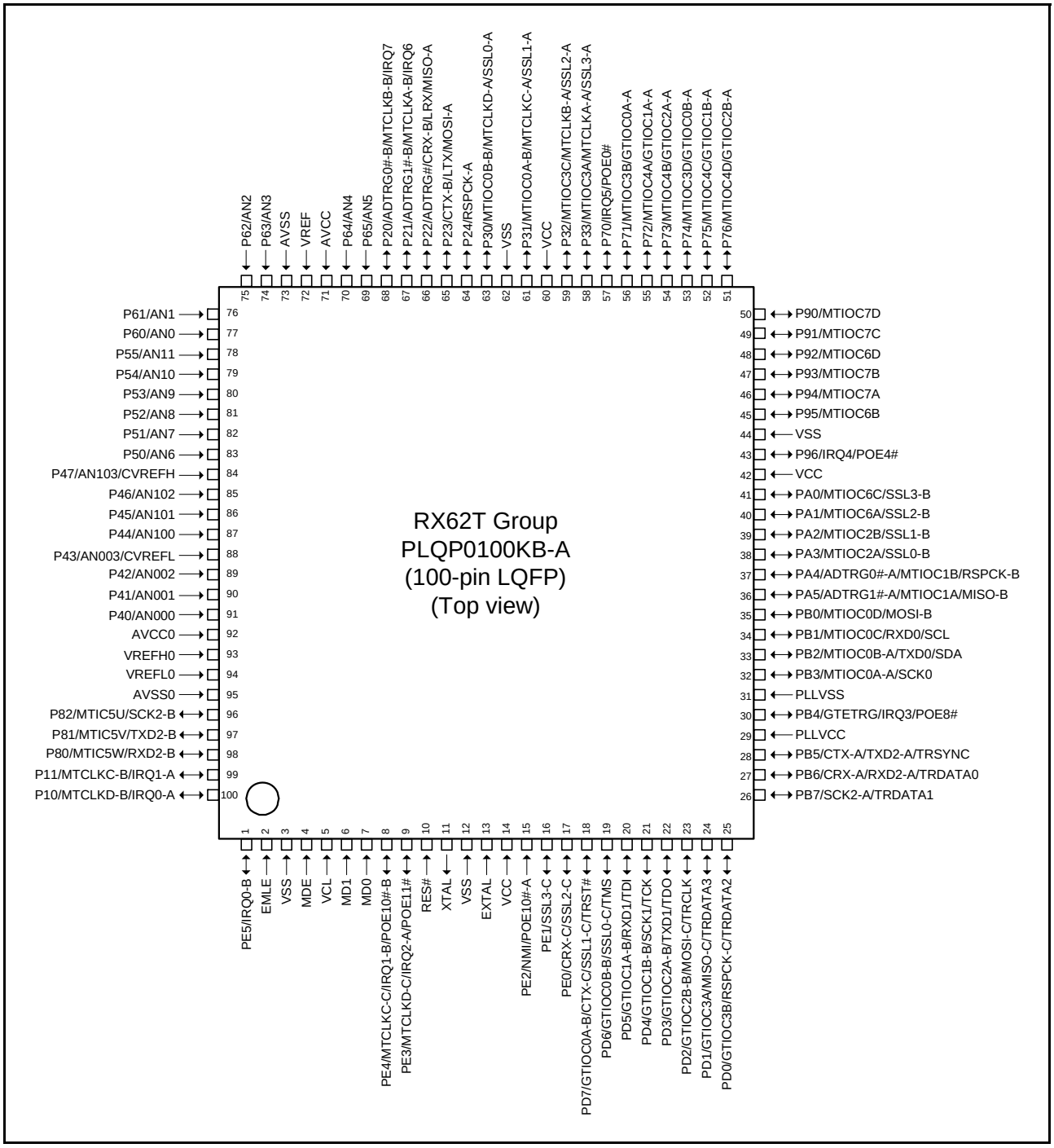

Figure 1.4 Pin Assignment of the 100-Pin LQFP

Table 1.4 List of Pins and Pin Functions (112-Pin LQFP) (3 / 3)

Pin No. (112-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi-cation	Interrupt	POE	Debugging
80	AVCC							
81	VREF							
82	AVSS							
83		P63	AN3					
84		P62	AN2					
85		P61	AN1					
86		P60	AN0					
87		P55	AN11					
88		P54	AN10					
89		P53	AN9					
90		P52	AN8					
91		P51	AN7					
92		P50	AN6					
93		P47	AN103/ CVREFH					
94		P46	AN102					
95		P45	AN101					
96		P44	AN100					
97		P43	AN003/ CVREFL					
98		P42	AN002					
99		P41	AN001					
100		P40	AN000					
101	AVCC0							
102	VREFH0							
103	VREFL0							
104	AVSS0							
105		P82		MTIC5U	SCK2-B			
106		P81		MTIC5V	TXD2-B			
107		P80		MTIC5W	RXD2-B			
108				WDTOVF#				
109		P11		MTCLKC-B		IRQ1-A		
110		P10		MTCLKD-B		IRQ0-A		
111								TRST#
112								TMS

(9) Accumulator (ACC)

The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.

Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively.

Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

Table 4.1 List of I/O Registers (Address Order) (2 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 6526h	MPU	Region invalidation operation register	MPOPI	16	16	1 ICLK
0008 6528h	MPU	Instruction-hit region register	MHITI	32	32	1 ICLK
0008 652Ch	MPU	Data-hit region register	MHITD	32	32	1 ICLK
0008 7010h	ICU	Interrupt request register 016	IR016	8	8	2 ICLK
0008 7015h	ICU	Interrupt request register 021	IR021	8	8	2 ICLK
0008 7017h	ICU	Interrupt request register 023	IR023	8	8	2 ICLK
0008 701Bh	ICU	Interrupt request register 027	IR027	8	8	2 ICLK
0008 701Ch	ICU	Interrupt request register 028	IR028	8	8	2 ICLK
0008 701Dh	ICU	Interrupt request register 029	IR029	8	8	2 ICLK
0008 701Eh	ICU	Interrupt request register 030	IR030	8	8	2 ICLK
0008 701Fh	ICU	Interrupt request register 031	IR031	8	8	2 ICLK
0008 702Ch	ICU	Interrupt request register 044	IR044	8	8	2 ICLK
0008 702Dh	ICU	Interrupt request register 045	IR045	8	8	2 ICLK
0008 702Eh	ICU	Interrupt request register 046	IR046	8	8	2 ICLK
0008 702Fh	ICU	Interrupt request register 047	IR047	8	8	2 ICLK
0008 7038h	ICU	Interrupt request register 056	IR056	8	8	2 ICLK
0008 7039h	ICU	Interrupt request register 057	IR057	8	8	2 ICLK
0008 703Ah	ICU	Interrupt request register 058	IR058	8	8	2 ICLK
0008 703Bh	ICU	Interrupt request register 059	IR059	8	8	2 ICLK
0008 703Ch	ICU	Interrupt request register 060	IR060	8	8	2 ICLK
0008 7040h	ICU	Interrupt request register 064	IR064	8	8	2 ICLK
0008 7041h	ICU	Interrupt request register 065	IR065	8	8	2 ICLK
0008 7042h	ICU	Interrupt request register 066	IR066	8	8	2 ICLK
0008 7043h	ICU	Interrupt request register 067	IR067	8	8	2 ICLK
0008 7044h	ICU	Interrupt request register 068	IR068	8	8	2 ICLK
0008 7045h	ICU	Interrupt request register 069	IR069	8	8	2 ICLK
0008 7046h	ICU	Interrupt request register 070	IR070	8	8	2 ICLK
0008 7047h	ICU	Interrupt request register 071	IR071	8	8	2 ICLK
0008 7060h	ICU	Interrupt request register 096	IR096	8	8	2 ICLK
0008 7062h	ICU	Interrupt request register 098	IR098	8	8	2 ICLK
0008 7066h	ICU	Interrupt request register 102	IR102	8	8	2 ICLK
0008 7067h	ICU	Interrupt request register 103	IR103	8	8	2 ICLK
0008 706Ah	ICU	Interrupt request register 106	IR106	8	8	2 ICLK
0008 7072h	ICU	Interrupt request register 114	IR114	8	8	2 ICLK
0008 7073h	ICU	Interrupt request register 115	IR115	8	8	2 ICLK
0008 7074h	ICU	Interrupt request register 116	IR116	8	8	2 ICLK
0008 7075h	ICU	Interrupt request register 117	IR117	8	8	2 ICLK
0008 7076h	ICU	Interrupt request register 118	IR118	8	8	2 ICLK
0008 7077h	ICU	Interrupt request register 119	IR119	8	8	2 ICLK
0008 7078h	ICU	Interrupt request register 120	IR120	8	8	2 ICLK
0008 7079h	ICU	Interrupt request register 121	IR121	8	8	2 ICLK
0008 707Ah	ICU	Interrupt request register 122	IR122	8	8	2 ICLK
0008 707Bh	ICU	Interrupt request register 123	IR123	8	8	2 ICLK
0008 707Ch	ICU	Interrupt request register 124	IR124	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (4 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 70BCh	ICU	Interrupt request register 188	IR188	8	8	2 ICLK
0008 70BDh	ICU	Interrupt request register 189	IR189	8	8	2 ICLK
0008 70BEh	ICU	Interrupt request register 190	IR190	8	8	2 ICLK
0008 70C0h	ICU	Interrupt request register 192	IR192	8	8	2 ICLK
0008 70C1h	ICU	Interrupt request register 193	IR193	8	8	2 ICLK
0008 70C2h	ICU	Interrupt request register 194	IR194	8	8	2 ICLK
0008 70C3h	ICU	Interrupt request register 195	IR195	8	8	2 ICLK
0008 70C4h	ICU	Interrupt request register 196	IR196	8	8	2 ICLK
0008 70D6h	ICU	Interrupt request register 214	IR214	8	8	2 ICLK
0008 70D7h	ICU	Interrupt request register 215	IR215	8	8	2 ICLK
0008 70D8h	ICU	Interrupt request register 216	IR216	8	8	2 ICLK
0008 70D9h	ICU	Interrupt request register 217	IR217	8	8	2 ICLK
0008 70DAh	ICU	Interrupt request register 218	IR218	8	8	2 ICLK
0008 70DBh	ICU	Interrupt request register 219	IR219	8	8	2 ICLK
0008 70DCh	ICU	Interrupt request register 220	IR220	8	8	2 ICLK
0008 70DDh	ICU	Interrupt request register 221	IR221	8	8	2 ICLK
0008 70DEh	ICU	Interrupt request register 222	IR222	8	8	2 ICLK
0008 70DFh	ICU	Interrupt request register 223	IR223	8	8	2 ICLK
0008 70E0h	ICU	Interrupt request register 224	IR224	8	8	2 ICLK
0008 70E1h	ICU	Interrupt request register 225	IR225	8	8	2 ICLK
0008 70F6h	ICU	Interrupt request register 246	IR246	8	8	2 ICLK
0008 70F7h	ICU	Interrupt request register 247	IR247	8	8	2 ICLK
0008 70F8h	ICU	Interrupt request register 248	IR248	8	8	2 ICLK
0008 70F9h	ICU	Interrupt request register 249	IR249	8	8	2 ICLK
0008 70FEh	ICU	Interrupt request register 254	IR254	8	8	2 ICLK
0008 711Bh	ICU	DTC activation enable register 027	DTCER027	8	8	2 ICLK
0008 711Ch	ICU	DTC activation enable register 028	DTCER028	8	8	2 ICLK
0008 711Dh	ICU	DTC activation enable register 029	DTCER029	8	8	2 ICLK
0008 711Eh	ICU	DTC activation enable register 030	DTCER030	8	8	2 ICLK
0008 711Fh	ICU	DTC activation enable register 031	DTCER031	8	8	2 ICLK
0008 712Dh	ICU	DTC activation enable register 045	DTCER045	8	8	2 ICLK
0008 712Eh	ICU	DTC activation enable register 046	DTCER046	8	8	2 ICLK
0008 7140h	ICU	DTC activation enable register 064	DTCER064	8	8	2 ICLK
0008 7141h	ICU	DTC activation enable register 065	DTCER065	8	8	2 ICLK
0008 7142h	ICU	DTC activation enable register 066	DTCER066	8	8	2 ICLK
0008 7143h	ICU	DTC activation enable register 067	DTCER067	8	8	2 ICLK
0008 7144h	ICU	DTC activation enable register 068	DTCER068	8	8	2 ICLK
0008 7145h	ICU	DTC activation enable register 069	DTCER069	8	8	2 ICLK
0008 7146h	ICU	DTC activation enable register 070	DTCER070	8	8	2 ICLK
0008 7147h	ICU	DTC activation enable register 071	DTCER071	8	8	2 ICLK
0008 7162h	ICU	DTC activation enable register 098	DTCER098	8	8	2 ICLK
0008 7166h	ICU	DTC activation enable register 102	DTCER102	8	8	2 ICLK
0008 7167h	ICU	DTC activation enable register 103	DTCER103	8	8	2 ICLK
0008 716Ah	ICU	DTC activation enable register 106	DTCER106	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (9 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 8048h	ADA	A/D data register E	ADDRE	16	16	2, 3 PCLK*3
0008 804Ah	ADA	A/D data register F	ADDRF	16	16	2, 3 PCLK*3
0008 804Ch	ADA	A/D data register G	ADDRG	16	16	2, 3 PCLK*3
0008 804Eh	ADA	A/D data register H	ADDRH	16	16	2, 3 PCLK*3
0008 8050h	ADA	A/D control/status register	ADCSR	8	8	2, 3 PCLK*3
0008 8051h	ADA	A/D control register	ADCR	8	8	2, 3 PCLK*3
0008 805Bh	ADA	A/D sampling state register	ADSSTR	8	8	2, 3 PCLK*3
0008 805Dh	ADA	A/D self-diagnostic register	ADDIAGR	8	8	2, 3 PCLK*3
0008 8060h	ADA	A/D data register I	ADDRI	16	16	2, 3 PCLK*3
0008 8062h	ADA	A/D data register J	ADDRJ	16	16	2, 3 PCLK*3
0008 8064h	ADA	A/D data register K	ADDRK	16	16	2, 3 PCLK*3
0008 8066h	ADA	A/D data register L	ADDRL	16	16	2, 3 PCLK*3
0008 8070h	ADA	A/D start trigger select register	ADSTRGR	8	8	2, 3 PCLK*3
0008 8072h	ADA	A/D data placement register	ADDPR	8	8	2, 3 PCLK*3
0008 8240h	SCI0	Serial mode register	SMR*1	8	8	2, 3 PCLK*3
0008 8241h	SCI0	Bit rate register	BRR	8	8	2, 3 PCLK*3
0008 8242h	SCI0	Serial control register	SCR*1	8	8	2, 3 PCLK*3
0008 8243h	SCI0	Transmit data register	TDR	8	8	2, 3 PCLK*3
0008 8244h	SCI0	Serial status register	SSR*1	8	8	2, 3 PCLK*3
0008 8245h	SCI0	Receive data register	RDR	8	8	2, 3 PCLK*3
0008 8246h	SCI0	Smart card mode register	SCMR	8	8	2, 3 PCLK*3
0008 8247h	SCI0	Serial extended mode register	SEMR	8	8	2, 3 PCLK*3
0008 8240h	SMCI0	Serial mode register	SMR	8	8	2, 3 PCLK*3
0008 8241h	SMCI0	Bit rate register	BRR	8	8	2, 3 PCLK*3
0008 8242h	SMCI0	Serial control register	SCR	8	8	2, 3 PCLK*3
0008 8243h	SMCI0	Transmit data register	TDR	8	8	2, 3 PCLK*3
0008 8244h	SMCI0	Serial status register	SSR	8	8	2, 3 PCLK*3
0008 8245h	SMCI0	Receive data register	RDR	8	8	2, 3 PCLK*3
0008 8246h	SMCI0	Smart card mode register	SCMR	8	8	2, 3 PCLK*3
0008 8248h	SCI1	Serial mode register	SMR*1	8	8	2, 3 PCLK*3
0008 8249h	SCI1	Bit rate register	BRR	8	8	2, 3 PCLK*3
0008 824Ah	SCI1	Serial control register	SCR*1	8	8	2, 3 PCLK*3
0008 824Bh	SCI1	Transmit data register	TDR	8	8	2, 3 PCLK*3
0008 824Ch	SCI1	Serial status register	SSR*1	8	8	2, 3 PCLK*3
0008 824Dh	SCI1	Receive data register	RDR	8	8	2, 3 PCLK*3
0008 824Eh	SCI1	Smart card mode register	SCMR	8	8	2, 3 PCLK*3
0008 824Fh	SCI1	Serial extended mode register	SEMR	8	8	2, 3 PCLK*3
0008 8248h	SMCI1	Serial mode register	SMR	8	8	2, 3 PCLK*3
0008 8249h	SMCI1	Bit rate register	BRR	8	8	2, 3 PCLK*3
0008 824Ah	SMCI1	Serial control register	SCR	8	8	2, 3 PCLK*3
0008 824Bh	SMCI1	Transmit data register	TDR	8	8	2, 3 PCLK*3
0008 824Ch	SMCI1	Serial status register	SSR	8	8	2, 3 PCLK*3
0008 824Dh	SMCI1	Receive data register	RDR	8	8	2, 3 PCLK*3
0008 824Eh	SMCI1	Smart card mode register	SCMR	8	8	2, 3 PCLK*3

Table 4.2 List of I/O Registers (Bit Order) (5 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
ICU	IR144	—	—	—	—	—	—	—	IR
ICU	IR145	—	—	—	—	—	—	—	IR
ICU	IR146	—	—	—	—	—	—	—	IR
ICU	IR149	—	—	—	—	—	—	—	IR
ICU	IR150	—	—	—	—	—	—	—	IR
ICU	IR151	—	—	—	—	—	—	—	IR
ICU	IR152	—	—	—	—	—	—	—	IR
ICU	IR153	—	—	—	—	—	—	—	IR
ICU	IR170	—	—	—	—	—	—	—	IR
ICU	IR171	—	—	—	—	—	—	—	IR
ICU	IR172	—	—	—	—	—	—	—	IR
ICU	IR173	—	—	—	—	—	—	—	IR
ICU	IR174	—	—	—	—	—	—	—	IR
ICU	IR175	—	—	—	—	—	—	—	IR
ICU	IR176	—	—	—	—	—	—	—	IR
ICU	IR177	—	—	—	—	—	—	—	IR
ICU	IR178	—	—	—	—	—	—	—	IR
ICU	IR179	—	—	—	—	—	—	—	IR
ICU	IR180	—	—	—	—	—	—	—	IR
ICU	IR181	—	—	—	—	—	—	—	IR
ICU	IR182	—	—	—	—	—	—	—	IR
ICU	IR183	—	—	—	—	—	—	—	IR
ICU	IR184	—	—	—	—	—	—	—	IR
ICU	IR186	—	—	—	—	—	—	—	IR
ICU	IR187	—	—	—	—	—	—	—	IR
ICU	IR188	—	—	—	—	—	—	—	IR
ICU	IR189	—	—	—	—	—	—	—	IR
ICU	IR190	—	—	—	—	—	—	—	IR
ICU	IR192	—	—	—	—	—	—	—	IR
ICU	IR193	—	—	—	—	—	—	—	IR
ICU	IR194	—	—	—	—	—	—	—	IR
ICU	IR195	—	—	—	—	—	—	—	IR
ICU	IR196	—	—	—	—	—	—	—	IR
ICU	IR214	—	—	—	—	—	—	—	IR
ICU	IR215	—	—	—	—	—	—	—	IR
ICU	IR216	—	—	—	—	—	—	—	IR
ICU	IR217	—	—	—	—	—	—	—	IR
ICU	IR218	—	—	—	—	—	—	—	IR
ICU	IR219	—	—	—	—	—	—	—	IR
ICU	IR220	—	—	—	—	—	—	—	IR
ICU	IR221	—	—	—	—	—	—	—	IR
ICU	IR222	—	—	—	—	—	—	—	IR
ICU	IR223	—	—	—	—	—	—	—	IR
ICU	IR224	—	—	—	—	—	—	—	IR
ICU	IR225	—	—	—	—	—	—	—	IR
ICU	IR246	—	—	—	—	—	—	—	IR
ICU	IR247	—	—	—	—	—	—	—	IR
ICU	IR248	—	—	—	—	—	—	—	IR
ICU	IR249	—	—	—	—	—	—	—	IR
ICU	IR254	—	—	—	—	—	—	—	IR
ICU	DTCER027	—	—	—	—	—	—	—	DTCE
ICU	DTCER028	—	—	—	—	—	—	—	DTCE

Table 4.2 List of I/O Registers (Bit Order) (6 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
ICU	DTCER029	—	—	—	—	—	—	—	DTCE
ICU	DTCER030	—	—	—	—	—	—	—	DTCE
ICU	DTCER031	—	—	—	—	—	—	—	DTCE
ICU	DTCER045	—	—	—	—	—	—	—	DTCE
ICU	DTCER046	—	—	—	—	—	—	—	DTCE
ICU	DTCER064	—	—	—	—	—	—	—	DTCE
ICU	DTCER065	—	—	—	—	—	—	—	DTCE
ICU	DTCER066	—	—	—	—	—	—	—	DTCE
ICU	DTCER067	—	—	—	—	—	—	—	DTCE
ICU	DTCER068	—	—	—	—	—	—	—	DTCE
ICU	DTCER069	—	—	—	—	—	—	—	DTCE
ICU	DTCER070	—	—	—	—	—	—	—	DTCE
ICU	DTCER071	—	—	—	—	—	—	—	DTCE
ICU	DTCER098	—	—	—	—	—	—	—	DTCE
ICU	DTCER102	—	—	—	—	—	—	—	DTCE
ICU	DTCER103	—	—	—	—	—	—	—	DTCE
ICU	DTCER106	—	—	—	—	—	—	—	DTCE
ICU	DTCER114	—	—	—	—	—	—	—	DTCE
ICU	DTCER115	—	—	—	—	—	—	—	DTCE
ICU	DTCER116	—	—	—	—	—	—	—	DTCE
ICU	DTCER117	—	—	—	—	—	—	—	DTCE
ICU	DTCER121	—	—	—	—	—	—	—	DTCE
ICU	DTCER122	—	—	—	—	—	—	—	DTCE
ICU	DTCER125	—	—	—	—	—	—	—	DTCE
ICU	DTCER126	—	—	—	—	—	—	—	DTCE
ICU	DTCER129	—	—	—	—	—	—	—	DTCE
ICU	DTCER130	—	—	—	—	—	—	—	DTCE
ICU	DTCER131	—	—	—	—	—	—	—	DTCE
ICU	DTCER132	—	—	—	—	—	—	—	DTCE
ICU	DTCER134	—	—	—	—	—	—	—	DTCE
ICU	DTCER135	—	—	—	—	—	—	—	DTCE
ICU	DTCER136	—	—	—	—	—	—	—	DTCE
ICU	DTCER137	—	—	—	—	—	—	—	DTCE
ICU	DTCER138	—	—	—	—	—	—	—	DTCE
ICU	DTCER139	—	—	—	—	—	—	—	DTCE
ICU	DTCER140	—	—	—	—	—	—	—	DTCE
ICU	DTCER141	—	—	—	—	—	—	—	DTCE
ICU	DTCER142	—	—	—	—	—	—	—	DTCE
ICU	DTCER143	—	—	—	—	—	—	—	DTCE
ICU	DTCER144	—	—	—	—	—	—	—	DTCE
ICU	DTCER145	—	—	—	—	—	—	—	DTCE
ICU	DTCER149	—	—	—	—	—	—	—	DTCE
ICU	DTCER150	—	—	—	—	—	—	—	DTCE
ICU	DTCER151	—	—	—	—	—	—	—	DTCE
ICU	DTCER152	—	—	—	—	—	—	—	DTCE
ICU	DTCER153	—	—	—	—	—	—	—	DTCE
ICU	DTCER174	—	—	—	—	—	—	—	DTCE
ICU	DTCER175	—	—	—	—	—	—	—	DTCE
ICU	DTCER176	—	—	—	—	—	—	—	DTCE
ICU	DTCER177	—	—	—	—	—	—	—	DTCE
ICU	DTCER178	—	—	—	—	—	—	—	DTCE
ICU	DTCER179	—	—	—	—	—	—	—	DTCE

Table 4.2 List of I/O Registers (Bit Order) (13 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
S12AD0	ADRD*2	DIAGST[1:0]		—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD0	ADDR0A*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD0	ADDR1*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD0	ADDR2*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD0	ADDR3*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD0	ADDR0B*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD0	ADSSTR								
S12AD1	ADCSR	ADST	ADCS[1:0]		ADIE	CKS[1:0]		TRGE	EXTRG
S12AD1	ADANS	—	—	CH[1:0]		—	PG102SEL	PG101SEL	PG100SEL
		—	—	—	—	—	PG102EN	PG101EN	PG100EN
S12AD1	ADPG	—	—	—	—	PG102GAIN[3:0]			
		PG101GAIN[3:0]				PG100GAIN[3:0]			
S12AD1	ADCER	ADRFMT	—	ADIEW	ADIE2	DIAGM	DIAGLD	DIAGVAL[1:0]	
		—	—	ACE	—	—	ADPRC[1:0]		SHBYP
S12AD1	ADSTRGR	—	—	—	ADSTRS1[4:0]				
		—	—	—	ADSTRS0[4:0]				
S12AD1	ADRD*2	DIAGST[1:0]		—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD1	ADDR0A*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD1	ADDR1*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD1	ADDR2*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD1	ADDR3*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD1	ADDR0B*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD1	ADSSTR								
PORT1	DDR	—	—	—	—	—	—	B1	B0
PORT2	DDR	—	—	—	B4	B3	B2	B1	B0
PORT3	DDR	—	—	—	—	B3	B2	B1	B0
PORT7	DDR	—	B6	B5	B4	B3	B2	B1	B0
PORT8	DDR	—	—	—	—	—	B2	B1	B0
PORT9	DDR	—	B6	B5	B4	B3	B2	B1	B0
PORTA	DDR	—	—	B5	B4	B3	B2	B1	B0
PORTB	DDR	B7	B6	B5	B4	B3	B2	B1	B0
PORTD	DDR	B7	B6	B5	B4	B3	B2	B1	B0
PORTE	DDR	—	—	B5	B4	B3	—	B1	B0
PORTG	DDR	—	—	B5	B4	B3	B2	B1	B0
PORT1	DR	—	—	—	—	—	—	B1	B0
PORT2	DR	—	—	—	B4	B3	B2	B1	B0
PORT3	DR	—	—	—	—	B3	B2	B1	B0
PORT7	DR	—	B6	B5	B4	B3	B2	B1	B0

Table 4.2 List of I/O Registers (Bit Order) (18 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
CAN0*3	AFSR	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
CAN0*3	TCR	—	—	—	—	—	TSTM[1:0]		TSTE
LIN0	LWBR	—	—	—	—	—	—	—	LWBR0
LIN0	LBRP0								
LIN0	LBRP1								
LIN0	LSTC								LSTM
LIN0	L0MD	—	—	—	—	LCKS[1:0]		—	—
LIN0	L0BRK	—	—	BDT[1:0]			BLT[3:0]		
LIN0	L0SPC	—	—	IBS[1:0]		—		IBSH[2:0]	
LIN0	L0WUP		WUTL[3:0]			—	—	—	—
LIN0	L0IE	—	—	—	—	—	ERRIE	FRCIE	FTCIE
LIN0	L0EDE	—	—	—	—	FERE	FTERE	PBERE	BERE
LIN0	L0C	—	—	—	—	—	—	OM1	OM0
LIN0	L0TC	—	—	—	—	—	—	RTS	FTS
LIN0	L0MST	—	—	—	—	—	—	OMM1	OMM0
LIN0	L0ST	HTRC	D1RC	—	—	ERR	—	FRC	FTC
LIN0	L0EST	—	—	CSER	—	FER	FTER	PBER	BER
LIN0	L0RFC	—	FSM	CSM	RFT		RFDL[3:0]		
LIN0	L0IDB	IDP				ID			
LIN0	L0CBR								
LIN0	L0DB1								
LIN0	L0DB2								
LIN0	L0DB3								
LIN0	L0DB4								
LIN0	L0DB5								
LIN0	L0DB6								
LIN0	L0DB7								
LIN0	L0DB8								
MTU3	TCR		CCLR[2:0]			CKEG[1:0]		TPSC[2:0]	
MTU4	TCR		CCLR[2:0]			CKEG[1:0]		TPSC[2:0]	
MTU3	TMDR1	—	—	BFB	BFA			MD[3:0]	
MTU4	TMDR1	—	—	BFB	BFA			MD[3:0]	
MTU3	TIORH		IOB[3:0]					IOA[3:0]	
MTU3	TIORL		IOD[3:0]					IOC[3:0]	
MTU4	TIORH		IOB[3:0]					IOA[3:0]	
MTU4	TIORL		IOD[3:0]					IOC[3:0]	
MTU3	TIER	TTGE	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA
MTU4	TIER	TTGE	TTGE2	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA
MTU	TOERA	—	—	OE4D	OE4C	OE3D	OE4B	OE4A	OE3B
MTU	TGCRA	—	BDC	N	P	FB	WF	VF	UF
MTU	TOCR1A	—	PSYE	—	—	TOCL	TOCS	OLSN	OLSP
MTU	TOCR2A	BF[1:0]		OLS3N	OLS3P	OLS2N	OLS2P	OLS1N	OLS1P
MTU3	TCNT								
MTU4	TCNT								
MTU	TCDRA								
MTU	TDDRA								

Table 4.2 List of I/O Registers (Bit Order) (20 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
MTU0	TMDR1	—	BFE	BFB	BFA			MD[3:0]	
MTU0	TIORH		IOB[3:0]					IOA[3:0]	
MTU0	TIORL		IOD[3:0]					IOC[3:0]	
MTU0	TIER	TTEG	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA
MTU0	TSR	—	—	—	TCFV	TGFD	TGFC	TGFB	TGFA
MTU0	TCNT								
MTU0	TGRA								
MTU0	TGRB								
MTU0	TGRC								
MTU0	TGRD								
MTU0	TGRE								
MTU0	TGRF								
MTU0	TIER2	TTGE2	—	—	—	—	—	TGIEF	TGIEE
MTU0	TSR2	—	—	—	—	—	—	TGFF	TGFE
MTU0	TBTM	—	—	—	—	—	TTSE	TTSB	TTSA
MTU1	TCR	—	CCLR[1:0]		CKEG[1:0]			TPSC[2:0]	
MTU1	TMDR1	—	—	—	—			MD[3:0]	
MTU1	TIOR		IOB[3:0]					IOA[3:0]	
MTU1	TIER	TTEG	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA
MTU1	TSR	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA
MTU1	TCNT								
MTU1	TGRA								
MTU1	TGRB								
MTU1	TICCR	—	—	—	—	I2BE	I2AE	I1BE	I1AE
MTU2	TCR	—	CCLR[1:0]		CKEG[1:0]			TPSC[2:0]	
MTU2	TMDR1	—	—	—	—			MD[3:0]	
MTU2	TIOR		IOB[3:0]					IOA[3:0]	
MTU2	TIER	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA
MTU2	TSR	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA
MTU2	TCNT								
MTU2	TGRA								
MTU2	TGRB								
MTU6	TCR		CCLR[20]		CKEG[1:0]			TPSC[2:0]	
MTU7	TCR		CCLR[20]		CKEG[1:0]			TPSC[2:0]	
MTU6	TMDR1	—	—	BFB	BFA			MD[3:0]	
MTU7	TMDR1	—	—	BFB	BFA			MD[3:0]	
MTU6	TIORH		IOB[3:0]					IOA[3:0]	
MTU6	TIORL		IOD[3:0]					IOC[3:0]	
MTU7	TIORH		IOB[3:0]					IOA[3:0]	

Table 4.2 List of I/O Registers (Bit Order) (22 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
MTU7	TADCOBRB								
MTU	TSYCR	CE0A	CE0D	CE0C	CE0D	CE1A	CE1B	CE2A	CE2B
MTU	TWCRB	CCE	—	—	—	—	—	SCC	WRE
MTU	TMDR2B	—	—	—	—	—	—	—	DRS
MTU6	TGRE								
MTU7	TGRE								
MTU7	TGRF								
MTU	TSTRB	CST7	CST6	—	—	—	—	—	—
MTU	TSYRB	SYNC7	SYNC6	—	—	—	—	—	—
MTU	TRWERB	—	—	—	—	—	—	—	RWE
MTU5	TCNTU								
MTU5	TGRU								
MTU5	TCRU	—	—	—	—	—	—	TPSC[1:0]	
MTU5	TIORU	—	—	—			IOC[4:0]		
MTU5	TCNTV								
MTU5	TGRV								
MTU5	TCRV	—	—	—	—	—	—	TPSC[1:0]	
MTU5	TIORV	—	—	—			IOC[4:0]		
MTU5	TCNTW								
MTU5	TGRW								
MTU5	TCRW	—	—	—	—	—	—	TPSC[1:0]	
MTU5	TIORW	—	—	—			IOC[4:0]		
MTU5	TSR	—	—	—	—	—	CMFU5	CMFV5	CMFW5
MTU5	TIER	—	—	—	—	—	TGIE5U	TGIE5V	TGIE5W
MTU5	TSTR	—	—	—	—	—	CSTU5	CSTV5	CSTW5
MTU5	TCNTCMPCLR	—	—	—	—	—	CMPCLR5U	CMPCLR5V	CMPCLR5W
GPT	GTSTR	—	—	—	—	—	—	—	—
		—	—	—	—	CST3	CST2	CST1	CST0
GPT	GTHSCR	CPHW3[1:0]		CPHW2[1:0]		CPHW1[1:0]		CPHW0[1:0]	
		CSHW3[1:0]		CSHW2[1:0]		CSHW1[1:0]		CSHW0[1:0]	
GPT	GTHCCR	—	—	—	—	CCSW3	CCSW2	CCSW1	CCSW0
		CCHW3[1:0]		CCHW2[1:0]		CCHW1[1:0]		CCHW0[1:0]	
GPT	GTHSSR	CSHSL3[3:0]					CSHSL2[3:0]		
		CSHSL1[3:0]					CSHSL0[3:0]		
GPT	GTHPSR	CSHPL3[3:0]					CSHPL2[3:0]		
		CSHPL1[3:0]					CSHPL0[3:0]		
GPT	GTWP	—	—	—	—	—	—	—	—
		—	—	—	—	WP3	WP2	WP1	WP0
GPT	GTSYNC	—	—	SYNC3[1:0]		—	—	SYNC2[1:0]	
		—	—	SYNC1[1:0]		—	—	SYNC0[1:0]	
GPT	GTETINT	—	—	—	—	—	—	ETINF	ETIPF
		—	—	—	—	—	—	ETINEN	ETIPEN

Table 4.2 List of I/O Registers (Bit Order) (29 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
GPT2	GTDLYCR	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLYEN	DLYRST	DLLEN
GPT3	GTDLYCR	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLYEN	DLYRST	DLLEN
GPT0	GTDLYRA	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT0	GTDLYRB	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT1	GTDLYRA	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT1	GTDLYRB	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT2	GTDLYRA	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT2	GTDLYRB	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT3	GTDLYRA	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT3	GTDLYRB	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT0	GTDLYFA	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT0	GTDLYFB	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT1	GTDLYFA	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT1	GTDLYFB	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT2	GTDLYRA	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT2	GTDLYFB	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT3	GTDLYFA	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT3	GTDLYFB	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
FLASH	FMODR	—	—	—	FRDMD		—	—	—
FLASH	FASTAT	ROMAE	—	—	CMDLK	DFLAE	—	DFLRPE	DFLWPE
FLASH	FAEINT	ROMAEIE	—	—	CMDLKIE	DFLAEIE	—	DFLRPEIE	DFLWPEIE
FLASH	FRDYIE	—	—	—	—	—	—	—	FRDYIE
FLASH	DFLRE0				KEY[7:0]				
		DBRE07	DBRE06	DBRE05	DBRE04	DBRE03	DBRE02	DBRE01	DBRE00
FLASH	DFLRE1				KEY[7:0]				
		DBRE15	DBRE14	DBRE13	DBRE12	DBRE11	DBRE10	DBRE09	DBRE08
FLASH	DFLWE0				KEY[7:0]				
		DBWE07	DBWE06	DBWE05	DBWE04	DBWE03	DBWE02	DBWE01	DBWE00
FLASH	DFLWE1				KEY[7:0]				
		DBWE15	DBWE14	DBWE13	DBWE12	DBWE11	DBWE10	DBWE09	DBWE08
FLASH	FCURAME				KEY[7:0]				
		—	—	—	—	—	—	—	FCRME

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Item		Symbol	Value	Unit
Power supply voltage		VCC PLLVCC	-0.3 to +6.5	V
Input voltage (except for ports 4 to 6)		V_{IN}	-0.3 to VCC+0.3	V
Input voltage (port 4)		V_{IN}	-0.3 to AVCC0+0.3	V
Input voltage (ports 5 and 6)		V_{IN}	-0.3 to AVCC+0.3	V
Analog power supply voltage		AVCC0, AVCC*1	-0.3 to +6.5	V
Reference power supply voltage		VREFH0*1	-0.3 to AVCC0+0.3	V
		VREF*1	-0.3 to AVCC+0.3	
Analog input voltage (port 4)		V_{AN}	-0.3 to AVCC0+0.3	V
Analog input voltage (ports 5 and 6)		V_{AN}	-0.3 to AVCC+0.3	V
Operating temperature	D version	T_{opr}	-40 to +85	°C
	G version	T_{opr}	-40 to +105	°C
Storage temperature		T_{stg}	-55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. Do not leave the AVCC0, VREFH0, VREFL0, AVSS0, AVCC, VREF, and AVSS pins open circuit even if the A/D converter is not to be used.
- When the 12-bit converter is not in use:
  Connect the AVCC0 pin to AVCC (or VCC for a 64-pin product), the VREFH0 pin to VREF (or AVCC or VCC for an 80- or 64-pin product, respectively), and the AVSS0 and VREFL0 pins to VSS.
- When the 10-bit converter is not in use:
  Connect the AVCC pin to AVCC0, the VREF pin to VREFH0, and the AVSS pin to AVSS0.
- When neither the 10- nor the 12-bit converter is in use:
  Connect the AVCC0, VREFH0, AVCC, and VREF pins to VCC, and the AVSS0, VREFL0, and AVSS pins to VSS.

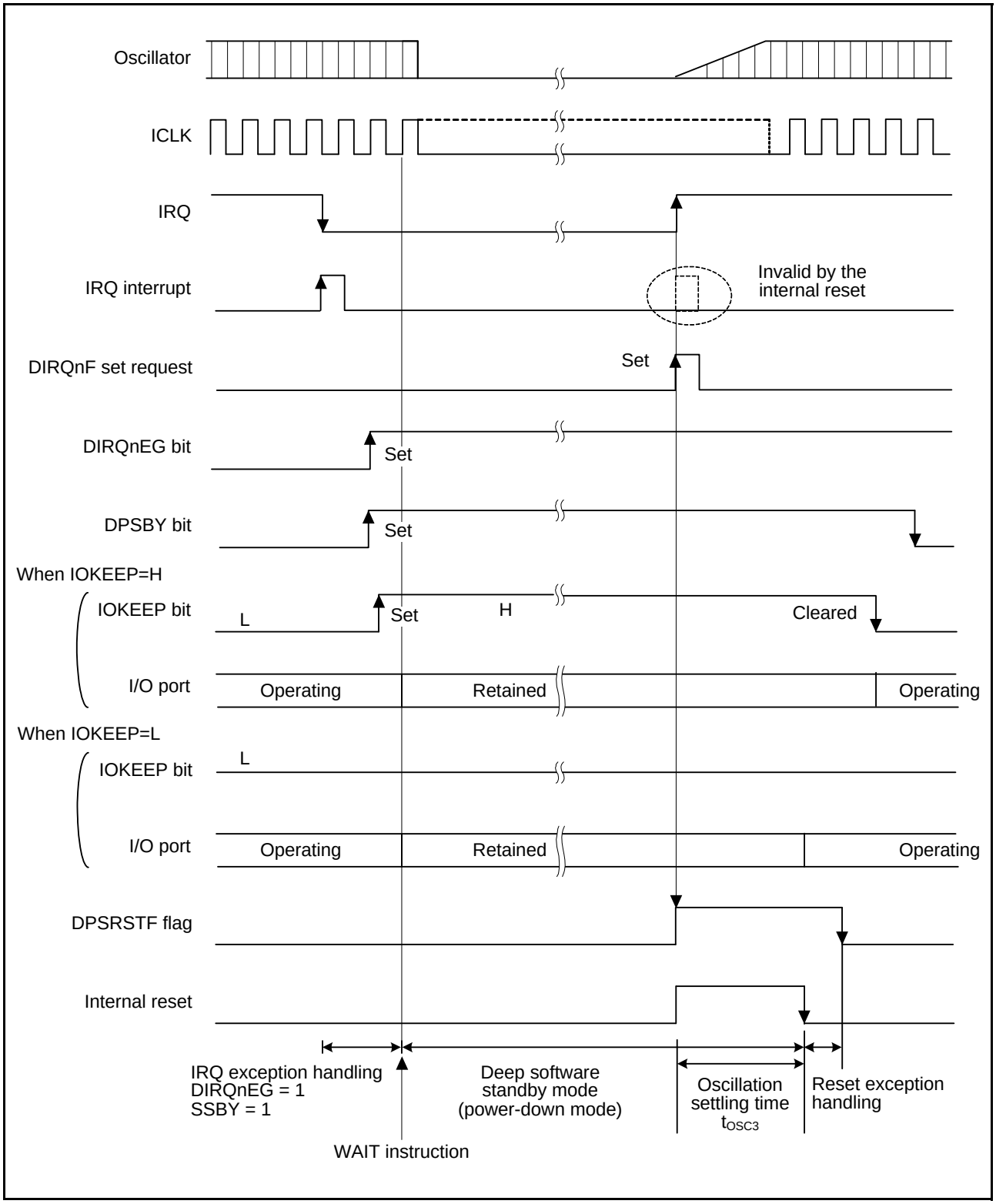

Figure 5.3 Oscillation Settling Timing after Deep Software Standby Mode

Table 5.16 12-Bit A/D Conversion Characteristics

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC
Ta = Topr, ICLK = 8 to 100 MHz, PCLK = 8 to 50 MHz

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		12	12	12	Bit	
Conversion time*1 (AD clock = 25-MHz operation)		2.0	-	-	µs	Sampling 20 states
Analog input capacitance		-	-	6	pF	
Integral nonlinearity error		-	-	±4.0	LSB	
Offset error		-	-	±7.5	LSB	
Full-scale error		-	-	±7.5	LSB	
Quantization error		-	±0.5	-	LSB	
Absolute accuracy	When a sample-and-hold circuit is in use	-	-	±8.0	LSB	AVin = 0.25 to AV_{REFH} - 0.25
	When a sample-and-hold circuit is not in use	-	-	±8.0	LSB	AVin = AV_{REFL} to AV_{REFH}
Permissible signal source impedance		-	-	3.0	kΩ	

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 2 and 3. ICLK = 8 to 100 MHz, PCLK = 8 to 50 MHz.

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		12	12	12	Bit	
Conversion time*1 (AD clock = 25-MHz operation)		1.0	-	-	µs	Sampling 20 states
Analog input capacitance		-	-	6	pF	
Integral nonlinearity error		-	-	±4.0	LSB	
Offset error		-	-	±7.5	LSB	
Full-scale error		-	-	±7.5	LSB	
Quantization error		-	±0.5	-	LSB	
Absolute accuracy	When a sample-and-hold circuit is in use	-	-	±8.0	LSB	AVin = 0.25 to AV_{REFH} - 0.25
	When a sample-and-hold circuit is not in use	-	-	±8.0	LSB	AVin = AV_{REFL} to AV_{REFH}
Permissible signal source impedance		-	-	3.0	kΩ	

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 5.17 Characteristics of the Programmable Gain Amplifier

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog input capacitance		Cin	-	-	6	pF	
Input offset voltage		Voff	-	-	8	mV	
Input voltage range (Vin)	Gain × 2.000	Vin	0.050 x AVcc	-	0.450 x AVcc	V	
	Gain × 2.500		0.047 x AVcc	-	0.360 x AVcc		
	Gain × 3.077		0.045 x AVcc	-	0.292 x AVcc		
	Gain × 3.636		0.042 x AVcc	-	0.247 x AVcc		
	Gain × 4.000		0.040 x AVcc	-	0.212 x AVcc		
	Gain × 4.444		0.036 x AVcc	-	0.191 x AVcc		
	Gain × 5.000		0.033 x AVcc	-	0.170 x AVcc		
	Gain × 5.714		0.031 x AVcc	-	0.148 x AVcc		
	Gain × 6.667		0.029 x AVcc	-	0.127 x AVcc		
	Gain × 10.000		0.025 x AVcc	-	0.08 x AVcc		
	Gain × 13.333		0.023 x AVcc	-	0.06 x AVcc		
Slew rate		SR	10	-	-	V/µs	
Gain error	Gain × 2.000	-	-	-	1	%	
	Gain × 2.500		-	-	1		
	Gain × 3.077		-	-	1		
	Gain × 3.636		-	-	1.5		
	Gain × 4.000		-	-	1.5		
	Gain × 4.444		-	-	2		
	Gain × 5.000		-	-	2		
	Gain × 5.714		-	-	2		
	Gain × 6.667		-	-	3		
	Gain × 10.000		-	-	4		
	Gain × 13.333		-	-	4		