Renesas Electronics America Inc - R5F562T6DDFM#V3 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562t6ddfm-v3

Table 1.1 Outline of Specifications (3 / 5)

Classification	Module/Function	Description
Timers	General PWM timer (GPT/GPTa)	• 16 bits x 4 channels • Counting up or down (saw-wave), counting up and down (triangle-wave) selectable for all channels • Clock sources independently selectable for all channels • 2 input/output pins per channel • 2 output compare/input capture registers per channel • For the 2 output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally asymmetrically PWM waveforms. • Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow) • Synchronizable operation of the several counters • Modes of synchronized operation (synchronized, or displaced by desired times for phase shifting) • Generation of dead times in PWM operation • Through combination of three counters, generation of automatic three-phase PWM waveforms incorporating dead times • Starting, clearing, and stopping counters in response to external or internal triggers • Internal trigger sources: output of the internal comparator detection, software, and compare-match • The frequency-divided system clock (ICLK) can be used as a counter clock for measuring timing of the edges of signals produced by frequency-dividing the low-speed on-chip oscillator clock signal dedicated to IWDT (to detect abnormal oscillation). • PWM delay generation can control the timing with which signals on the two PWM output pins for each channel rise and fall with an accuracy of up to 1/32 times the period of the system clock (ICLK) (only for GPTa).
	Compare match timer (CMT)	• (16 bits x 2 channels) x 2 units • Select from among four internal clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Watchdog timer (WDT)	• 8 bits x 1 channel • Select from among eight counter-input clock signals (PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192, PCLK/32768, PCLK/131072) • Switchable between watchdog timer mode and interval timer mode
	Independent watchdog timer (IWDT)	• 14 bits x 1 channel • Counter-input clock: low-speed on-chip oscillator dedicated to IWDT
Communications	Serial communications interface (SCIb)	• 3 channels • Serial communications modes: Asynchronous, clock synchronous, and smart-card interface • Multiprocessor communications • On-chip baud rate generator allows selection of the desired bit rate • Choice of LSB-first or MSB-first transfer • Noise cancellation (only available in asynchronous mode)
	I^2C bus interface (RIIC)	• 1 channel • Communications formats I^2C bus format/SMBus format Master/slave selectable

Table 1.1 Outline of Specifications (5 / 5)

Classification	Module/Function	Description
A/D converter	10-bit A/D converter (ADA)	• 10 bits (1 unit x 12 channels) • 10-bit resolution • Conversion time: 1.0 μs per channel (in operation with A/D conversion clock ADCLK at 50 MHz) for AVCC0 = 4.0 to 5.5 V 2.0 μs per channel (in operation with A/D conversion clock ADCLK at 25 MHz) for AVCC = 3.0 to 3.6 V • Two basic operating modes Single mode and scan mode • Scan mode One-cycle scan mode Continuous scan mode • Sample-and-hold function A common sample-and-hold circuit for both units is included. • A/D-conversion register settings for each input pin • Three ways to start A/D conversion Conversion can be started by software, a conversion start trigger from a timer (MTU3 or GPT), or an external trigger signal. • Functionality for 8-bit precision output Right-shifting the results of conversion for output by two bits is selectable. • Self-diagnostic function The self-diagnostic function internally generates three analog input voltages (AVSS, VREF x 1/2, VREF).
CRC calculator (CRC)		• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$. • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.
Operating frequency		ICLK: 8 to 100 MHz PCLK: 8 to 50 MHz
Power supply voltage		• 3-V version VCC = PLLVCC = 2.7 to 3.6V AVCC0 = AVCC = 3.0 to 3.6V, or 4.0 to 5.5V VREFH0 = 3.0 to AVCC0, or 4.0 to AVCC0 VREF = 3.0 to AVCC, or 4.0 to AVCC • 5-V version VCC = PLLVCC = 4.0 to 5.5V AVCC0 = AVCC = 4.0 to 5.5V VREFH0 = 4.0 to AVCC0 VREF = 4.0 to AVCC
Operating temperature		D version: -40 to +85°C, G version: -40 to +105°C*1
Packages		112-pin LQFP (PLQP0112JA-A, 20x20-0.65-mm pitch) 100-pin LQFP (PLQP0100KB-A, 14x14-0.5-mm pitch) 80-pin LQFP (PLQP0080JA-A, 14x14-0.65-mm pitch) 64-pin LQFP (PLQP0064KB-A, 10x10-0.5-mm pitch) 64-pin LQFP (PLQP0064GA-A, 14x14-0.8mm pitch)

Note 1. Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

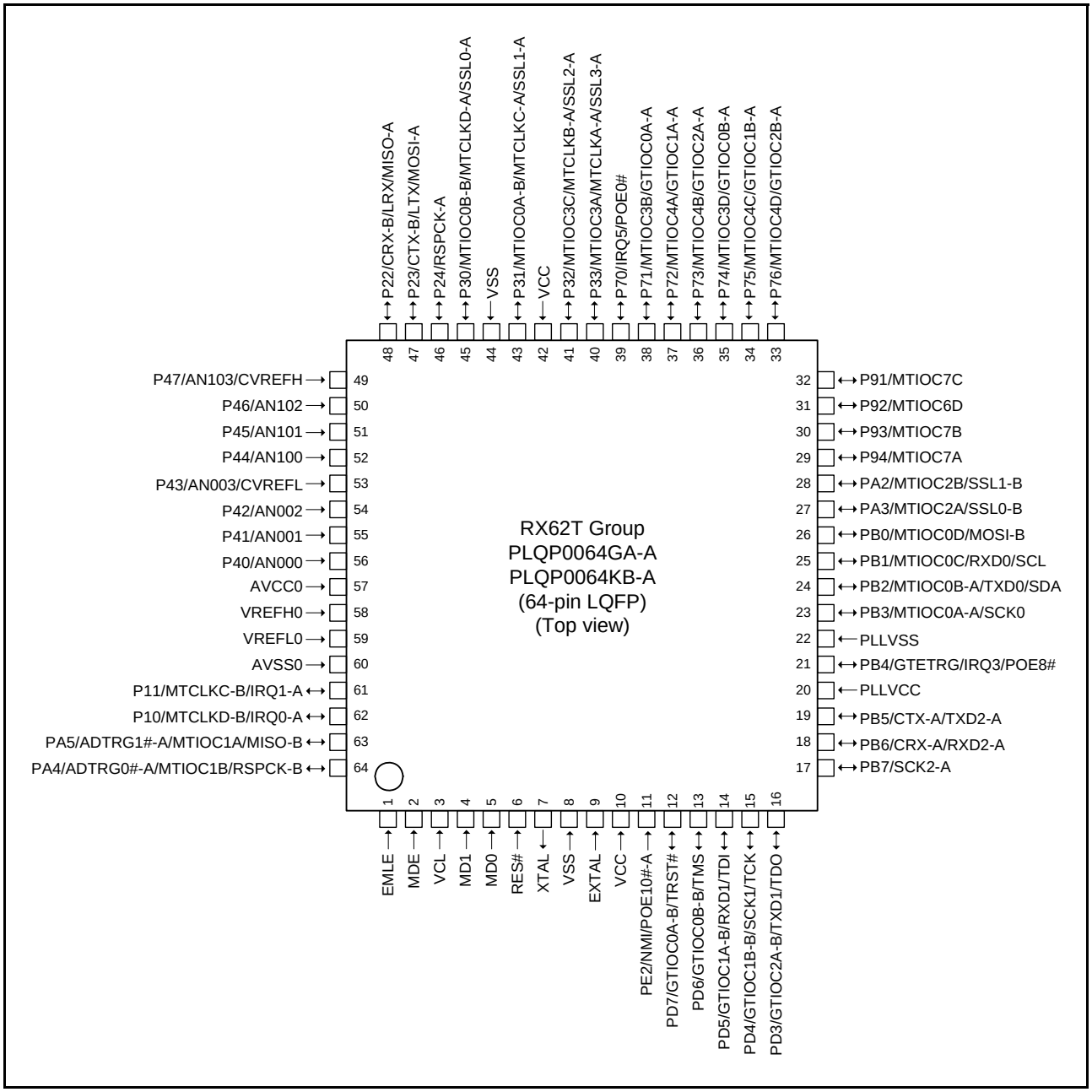

Figure 1.7 Pin Assignment of the 64-Pin LQFP

Table 1.5 List of Pins and Pin Functions (100-Pin LQFP) (1 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi-cation	Interrupt	POE	Debugging
1		PE5				IRQ0-B		
2	EMLE							
3	VSS							
4	MDE							
5	VCL							
6	MD1							
7	MD0							
8		PE4		MTCLKC-C		IRQ1-B	POE10#-B	
9		PE3		MTCLKD-C		IRQ2-A	POE11#	
10	RES#							
11	XTAL							
12	VSS							
13	EXTAL							
14	VCC							
15		PE2				NMI	POE10#-A	
16		PE1			SSL3-C			
17		PE0			CRX-C/ SSL2-C			
18		PD7		GTIOC0A-B	CTX-C/ SSL1-C			TRST#
19		PD6		GTIOC0B-B	SSL0-C			TMS
20		PD5		GTIOC1A-B	RXD1			TDI
21		PD4		GTIOC1B-B	SCK1			TCK
22		PD3		GTIOC2A-B	TXD1			TDO
23		PD2		GTIOC2B-B	MOSI-C			TRCLK
24		PD1		GTIOC3A	MISO-C			TRDATA3
25		PD0		GTIOC3B	RSPCK-C			TRDATA2
26		PB7			SCK2-A			TRDATA1
27		PB6			CRX-A/ RXD2-A			TRDATA0
28		PB5			CTX-A/ TXD2-A			TRSYNC
29	PLLVCC							
30		PB4		GTETRG		IRQ3	POE8#	
31	PLLVSS							
32		PB3		MTIOC0A-A	SCK0			
33		PB2		MTIOC0B-A	TXD0/SDA			
34		PB1		MTIOC0C	RXD0/SCL			
35		PB0		MTIOC0D	MOSI-B			
36		PA5	ADTRG1#-A	MTIOC1A	MISO-B			
37		PA4	ADTRG0#-A	MTIOC1B	RSPCK-B			
38		PA3		MTIOC2A	SSL0-B			
39		PA2		MTIOC2B	SSL1-B			
40		PA1		MTIOC6A	SSL2-B			

Table 1.5 List of Pins and Pin Functions (100-Pin LQFP) (2 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi-cation	Interrupt	POE	Debugging
41		PA0		MTIOC6C	SSL3-B			
42	VCC							
43		P96				IRQ4	POE4#	
44	VSS							
45		P95		MTIOC6B				
46		P94		MTIOC7A				
47		P93		MTIOC7B				
48		P92		MTIOC6D				
49		P91		MTIOC7C				
50		P90		MTIOC7D				
51		P76		MTIOC4D/ GTIOC2B-A				
52		P75		MTIOC4C/ GTIOC1B-A				
53		P74		MTIOC3D/ GTIOC0B-A				
54		P73		MTIOC4B/ GTIOC2A-A				
55		P72		MTIOC4A/ GTIOC1A-A				
56		P71		MTIOC3B/ GTIOC0A-A				
57		P70				IRQ5	POE0#	
58		P33		MTIOC3A/ MTCLKA-A	SSL3-A			
59		P32		MTIOC3C/ MTCLKB-A	SSL2-A			
60	VCC							
61		P31		MTIOC0A-B/ MTCLKC-A	SSL1-A			
62	VSS							
63		P30		MTIOC0B-B/ MTCLKD-A	SSL0-A			
64		P24			RSPCK-A			
65		P23			CTX-B/ LTX/ MOSI-A			
66		P22	ADTRG#		CRX-B/ LRX/ MISO-A			
67		P21	ADTRG1#-B	MTCLKA-B		IRQ6		
68		P20	ADTRG0#-B	MTCLKB-B		IRQ7		
69		P65	AN5					
70		P64	AN4					
71	AVCC							
72	VREF							
73	AVSS							
74		P63	AN3					
75		P62	AN2					
76		P61	AN1					

Table 1.7 List of Pins and Pin Functions (80-Pin LQFP: R5F562TxGDFF) (2 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communication	Interrupt	POE	Debugging
42		P76		MTIOC4D/ GTIOC2B-A				
43		P75		MTIOC4C/ GTIOC1B-A				
44		P74		MTIOC3D/ GTIOC0B-A				
45		P73		MTIOC4B/ GTIOC2A-A				
46		P72		MTIOC4A/ GTIOC1A-A				
47		P71		MTIOC3B/ GTIOC0A-A				
48		P70				IRQ5	POE0#	
49		P33		MTIOC3A/ MTCLKA-A	SSL3-A			
50		P32		MTIOC3C/ MTCLKB-A	SSL2-A			
51	VCC							
52		P31		MTIOC0A-B/ MTCLKC-A	SSL1-A			
53	VSS							
54		P30		MTIOC0B-B/ MTCLKD-A	SSL0-A			
55		P24			RSPCK-A			
56		P23			CTX-B/ LTX/ MOSI-A			
57		P22	ADTRG#		CRX-B/ LRX/ MISO-A			
58		P20	ADTRG0#-B	MTCLKB-B		IRQ7		
59	AVCC							
60	AVSS							
61		P63	AN3					
62		P62	AN2					
63		P61	AN1					
64		P60	AN0					
65		P47	AN103/ CVREFH					
66		P46	AN102					
67		P45	AN101					
68		P44	AN100					
69		P43	AN003/ CVREFL					
70		P42	AN002					
71		P41	AN001					
72		P40	AN000					
73	AVCC0							
74	VREFH0							
75	VREFL0							

Table 1.7 List of Pins and Pin Functions (80-Pin LQFP: R5F562TxGDFF) (3 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communication	Interrupt	POE	Debugging
76	AVSS0							
77		P82		MTIC5U	SCK2-B			
78		P81		MTIC5V	TXD2-B			
79		P80		MTIC5W	RXD2-B			
80		P10		MTCLKD-B		IRQ0-A		

Table 1.9 Pin Functions (3 / 4)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCIb)	TXD0, TXD1, TXD2-A/TXD2-B	Output	Output pins for data transmission. The TXD2-B pin is not included in the 80-/64-pin versions.
	RXD0, RXD1, RXD2-A/ RXD2-B	Input	Input pins for data reception. The RXD2-B pin is not included in the 80-/64-pin versions.
	SCK0, SCK1, SCK2-A/ SCK2-B	I/O	Input/output pins for clock signals. The SCK2-B pin is not included in the 80-/64-pin versions.
I^2C bus interface (RIIC)	SCL	I/O	Input/output pin for I^2C bus interface clocks. Bus can be directly driven by the NMOS open drain output.
	SDA	I/O	Input/output pin for I^2C bus interface data. Bus can be directly driven by the NMOS open drain output.
CAN module (CAN) (as an optional function)	CRX-A/CRX-B/CRX-C	Input	Input pin for the CAN. The CRX-C pin is not included in the 64-pin version.
	CTX-A/CTX-B/CTX-C	Output	Output pin for the CAN. The CTX-C pin is not included in the 64-pin version.
LIN module (LIN)	LRX	Input	Input pin for the LIN.
	LTX	Output	Output pin for the LIN.
Serial peripheral interface (RSPI)	RSPCK-A/RSPCK-B/ RSPCK-C	I/O	Clock input/output pin for the RSPI. The RSPCK-C pin is not included in the 80-/64-pin versions.
	MOSI-A/MOSI-B/MOSI-C	I/O	Inputs or outputs data output from the master for the RSPI. The MOSI-C pin is not included in the 80-/64-pin versions.
	MISO-A/MISO-B/MISO-C	I/O	Inputs or outputs data output from the slave for the RSPI. The MISO-C pin is not included in the 80-/64-pin versions.
	SSL0-A/SSL0-B/SSL0-C	I/O	Select the slave for the RSPI. The SSL0-C/SSL1-C/SSL2-C/ SSL3-C pin is not included in the 80-/64-pin versions.
	SSL1-A/SSL1-B/SSL1-C SSL2-A/SSL2-B/SSL2-C SSL3-A/SSL3-B/SSL3-C	Output	
A/D converter	AN000 to AN003 AN100 to AN103	Input	Input pins for the analog signals to be processed by the 12-bit A/D converter.
	AN0 to AN11	Input	Input pins for the analog signals to be processed by the 10-bit A/D converter. The AN4 to AN11 pins are not included in the 80-pin version. Not included in the 64-pin version.
	ADTRG0#-A/ADTRG0#-B ADTRG1#-A/ADTRG1#-B ADTRG#	Input	Input pins for the external trigger signals that start the A/D conversion. The ADTRG0#-B/ADTRG1#-B/ADTRG# pin is not included in the 64-pin version.
	CVREFH	Input	Input pin for the high-level reference voltage to the comparator
	CVREFL	Input	Input pin for the low-level reference voltage to the comparator
Analog power supply	AVCC0	Input	Analog power supply pin for the 12-bit A/D converter. When the A/D converter is not in use, connect this pin to the system power supply.
	AVSS0	Input	Ground pin for the 12-bit A/D converter. Connect this pin to the system power supply (0 V).
	VREFH0	Input	Reference power supply pin for the 12-bit A/D converter. When the 12-bit A/D converter is not in use, connect this pin to the system power supply.
	VREFL0	Input	Ground pin of the reference power supply pin for the 12-bit A/D converter. When the 12-bit A/D converter is not in use, connect this pin to the system power supply (0 V).
	AVCC	Input	Analog power supply pin for the 10-bit A/D converter. When the A/D converter is not in use, connect this pin to the system power supply. Not included in the 64-pin version.
	AVSS	Input	Ground pin for the 10-bit A/D converter. Connect this pin to the system power supply (0 V). Not included in the 64-pin version.
	VREF	Input	Reference power supply pin for the 10-bit A/D converter. When the 10-bit A/D converter is not in use, connect this pin to the system power supply. Not included in the 80-/64-pin versions.

(9) Accumulator (ACC)

The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.

Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively.

Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

(4) Number of Access Cycles to I/O Registers

The number of access cycles to I/O registers is obtained by following equation.*

Number of access cycles to I/O registers = Number of bus cycles for internal main bus 1 +
Number of divided cycles for clock synchronization +
Number of bus cycles for internal peripheral buses 1, 2, 4, and 6

The number of bus cycles for internal peripheral buses 1, 2, 4, and 6 differs according to the register to be accessed. For the number of access cycles to each I/O register, see Table 4.1, List of I/O Registers.

When peripheral functions connected to internal peripheral bus 6 are accessed, the number of divided cycles for clock synchronization is added.

Although the number of divided cycles for clock synchronization differs depending on the number of frequency ratio between ICLK and PCLK or bus access timing, the sum of the number of bus cycles for internal main bus 1 and the number of divided cycles for clock synchronization will be one PCLK at a maximum. Therefore, one PCLK is added to the number of access cycles shown in Table 4.1.

Note: • This applies to the number of cycles when the access from the CPU does not conflict with the instruction fetching to the external memory or bus access from the different bus master (DTC).

Table 4.1 List of I/O Registers (Address Order) (4 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 70BCh	ICU	Interrupt request register 188	IR188	8	8	2 ICLK
0008 70BDh	ICU	Interrupt request register 189	IR189	8	8	2 ICLK
0008 70BEh	ICU	Interrupt request register 190	IR190	8	8	2 ICLK
0008 70C0h	ICU	Interrupt request register 192	IR192	8	8	2 ICLK
0008 70C1h	ICU	Interrupt request register 193	IR193	8	8	2 ICLK
0008 70C2h	ICU	Interrupt request register 194	IR194	8	8	2 ICLK
0008 70C3h	ICU	Interrupt request register 195	IR195	8	8	2 ICLK
0008 70C4h	ICU	Interrupt request register 196	IR196	8	8	2 ICLK
0008 70D6h	ICU	Interrupt request register 214	IR214	8	8	2 ICLK
0008 70D7h	ICU	Interrupt request register 215	IR215	8	8	2 ICLK
0008 70D8h	ICU	Interrupt request register 216	IR216	8	8	2 ICLK
0008 70D9h	ICU	Interrupt request register 217	IR217	8	8	2 ICLK
0008 70DAh	ICU	Interrupt request register 218	IR218	8	8	2 ICLK
0008 70DBh	ICU	Interrupt request register 219	IR219	8	8	2 ICLK
0008 70DCh	ICU	Interrupt request register 220	IR220	8	8	2 ICLK
0008 70DDh	ICU	Interrupt request register 221	IR221	8	8	2 ICLK
0008 70DEh	ICU	Interrupt request register 222	IR222	8	8	2 ICLK
0008 70DFh	ICU	Interrupt request register 223	IR223	8	8	2 ICLK
0008 70E0h	ICU	Interrupt request register 224	IR224	8	8	2 ICLK
0008 70E1h	ICU	Interrupt request register 225	IR225	8	8	2 ICLK
0008 70F6h	ICU	Interrupt request register 246	IR246	8	8	2 ICLK
0008 70F7h	ICU	Interrupt request register 247	IR247	8	8	2 ICLK
0008 70F8h	ICU	Interrupt request register 248	IR248	8	8	2 ICLK
0008 70F9h	ICU	Interrupt request register 249	IR249	8	8	2 ICLK
0008 70FEh	ICU	Interrupt request register 254	IR254	8	8	2 ICLK
0008 711Bh	ICU	DTC activation enable register 027	DTCER027	8	8	2 ICLK
0008 711Ch	ICU	DTC activation enable register 028	DTCER028	8	8	2 ICLK
0008 711Dh	ICU	DTC activation enable register 029	DTCER029	8	8	2 ICLK
0008 711Eh	ICU	DTC activation enable register 030	DTCER030	8	8	2 ICLK
0008 711Fh	ICU	DTC activation enable register 031	DTCER031	8	8	2 ICLK
0008 712Dh	ICU	DTC activation enable register 045	DTCER045	8	8	2 ICLK
0008 712Eh	ICU	DTC activation enable register 046	DTCER046	8	8	2 ICLK
0008 7140h	ICU	DTC activation enable register 064	DTCER064	8	8	2 ICLK
0008 7141h	ICU	DTC activation enable register 065	DTCER065	8	8	2 ICLK
0008 7142h	ICU	DTC activation enable register 066	DTCER066	8	8	2 ICLK
0008 7143h	ICU	DTC activation enable register 067	DTCER067	8	8	2 ICLK
0008 7144h	ICU	DTC activation enable register 068	DTCER068	8	8	2 ICLK
0008 7145h	ICU	DTC activation enable register 069	DTCER069	8	8	2 ICLK
0008 7146h	ICU	DTC activation enable register 070	DTCER070	8	8	2 ICLK
0008 7147h	ICU	DTC activation enable register 071	DTCER071	8	8	2 ICLK
0008 7162h	ICU	DTC activation enable register 098	DTCER098	8	8	2 ICLK
0008 7166h	ICU	DTC activation enable register 102	DTCER102	8	8	2 ICLK
0008 7167h	ICU	DTC activation enable register 103	DTCER103	8	8	2 ICLK
0008 716Ah	ICU	DTC activation enable register 106	DTCER106	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (14 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 C29Ch	SYSTEM	Deep standby backup register 12	DPSBKR12	8	8	4, 5 PCLK*3
0008 C29Dh	SYSTEM	Deep standby backup register 13	DPSBKR13	8	8	4, 5 PCLK*3
0008 C29Eh	SYSTEM	Deep standby backup register 14	DPSBKR14	8	8	4, 5 PCLK*3
0008 C29Fh	SYSTEM	Deep standby backup register 15	DPSBKR15	8	8	4, 5 PCLK*3
0008 C2A0h	SYSTEM	Deep standby backup register 16	DPSBKR16	8	8	4, 5 PCLK*3
0008 C2A1h	SYSTEM	Deep standby backup register 17	DPSBKR17	8	8	4, 5 PCLK*3
0008 C2A2h	SYSTEM	Deep standby backup register 18	DPSBKR18	8	8	4, 5 PCLK*3
0008 C2A3h	SYSTEM	Deep standby backup register 19	DPSBKR19	8	8	4, 5 PCLK*3
0008 C2A4h	SYSTEM	Deep standby backup register 20	DPSBKR20	8	8	4, 5 PCLK*3
0008 C2A5h	SYSTEM	Deep standby backup register 21	DPSBKR21	8	8	4, 5 PCLK*3
0008 C2A6h	SYSTEM	Deep standby backup register 22	DPSBKR22	8	8	4, 5 PCLK*3
0008 C2A7h	SYSTEM	Deep standby backup register 23	DPSBKR23	8	8	4, 5 PCLK*3
0008 C2A8h	SYSTEM	Deep standby backup register 24	DPSBKR24	8	8	4, 5 PCLK*3
0008 C2A9h	SYSTEM	Deep standby backup register 25	DPSBKR25	8	8	4, 5 PCLK*3
0008 C2AAh	SYSTEM	Deep standby backup register 26	DPSBKR26	8	8	4, 5 PCLK*3
0008 C2ABh	SYSTEM	Deep standby backup register 27	DPSBKR27	8	8	4, 5 PCLK*3
0008 C2ACh	SYSTEM	Deep standby backup register 28	DPSBKR28	8	8	4, 5 PCLK*3
0008 C2ADh	SYSTEM	Deep standby backup register 29	DPSBKR29	8	8	4, 5 PCLK*3
0008 C2AEh	SYSTEM	Deep standby backup register 30	DPSBKR30	8	8	4, 5 PCLK*3
0008 C2AFh	SYSTEM	Deep standby backup register 31	DPSBKR31	8	8	4, 5 PCLK*3
0008 C4C0h	POE	Input level control/status register 1	ICSR1	16	8, 16	2, 3 PCLK*3
0008 C4C2h	POE	Output level control/status register 1	OCSR1	16	8, 16	2, 3 PCLK*3
0008 C4C4h	POE	Input level control/status register 2	ICSR2	16	8, 16	2, 3 PCLK*3
0008 C4C6h	POE	Output level control/status register 2	OCSR2	16	8, 16	2, 3 PCLK*3
0008 C4C8h	POE	Input level control/status register 3	ICSR3	16	8, 16	2, 3 PCLK*3
0008 C4CAh	POE	Software port output enable register	SPOER	8	8	2, 3 PCLK*3
0008 C4CBh	POE	Port output enable control register 1	POECR1	8	8	2, 3 PCLK*3
0008 C4CCh	POE	Port output enable control register 2	POECR2	16	16	2, 3 PCLK*3
0008 C4CEh	POE	Port output enable control register 3	POECR3	16	16	2, 3 PCLK*3
0008 C4D0h	POE	Port output enable control register 4	POECR4	16	16	2, 3 PCLK*3
0008 C4D2h	POE	Port output enable control register 5	POECR5	16	16	2, 3 PCLK*3
0008 C4D4h	POE	Port output enable control register 6	POECR6	16	16	2, 3 PCLK*3
0008 C4D6h	POE	Input level control/status register 4	ICSR4	16	8, 16	2, 3 PCLK*3
0008 C4D8h	POE	Input level control/status register 5	ICSR5	16	8, 16	2, 3 PCLK*3
0008 C4DAh	POE	Active level setting register 1	ALR1	16	8, 16	2, 3 PCLK*3
0009 0200h to 0009 03FFh	CAN0*2	Mailbox registers 0 to 31	MB0 to MB 31	128	8, 16, 32	2, 3 PCLK*3
0009 0400h	CAN0*2	Mask register 0	MKR0	32	8, 16, 32	2, 3 PCLK*3
0009 0404h	CAN0*2	Mask register 1	MKR1	32	8, 16, 32	2, 3 PCLK*3
0009 0408h	CAN0*2	Mask register 2	MKR2	32	8, 16, 32	2, 3 PCLK*3
0009 040Ch	CAN0*2	Mask register 3	MKR3	32	8, 16, 32	2, 3 PCLK*3
0009 0410h	CAN0*2	Mask register 4	MKR4	32	8, 16, 32	2, 3 PCLK*3
0009 0414h	CAN0*2	Mask register 5	MKR5	32	8, 16, 32	2, 3 PCLK*3
0009 0418h	CAN0*2	Mask register 6	MKR6	32	8, 16, 32	2, 3 PCLK*3

Table 4.1 List of I/O Registers (Address Order) (15 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0009 041Ch	CAN0*2	Mask register 7	MKR7	32	8, 16, 32	2, 3 PCLK*3
0009 0420h	CAN0*2	FIFO received ID compare register 0	FIDCR0	32	8, 16, 32	2, 3 PCLK*3
0009 0424h	CAN0*2	FIFO received ID compare register 1	FIDCR1	32	8, 16, 32	2, 3 PCLK*3
0009 0428h	CAN0*2	Mask invalid register	MKIVLR	32	8, 16, 32	2, 3 PCLK*3
0009 042Ch	CAN0*2	Mailbox interrupt enable register	MIER	32	8, 16, 32	2, 3 PCLK*3
0009 0820h to 0009 083Fh	CAN0*2	Message control registers 0 to 31	MCTL0 to MCTL31	8	8	2, 3 PCLK*3
0009 0840h	CAN0*2	Control register	CTLR	16	8, 16	2, 3 PCLK*3
0009 0842h	CAN0*2	Status register	STR	16	8, 16	2, 3 PCLK*3
0009 0844h	CAN0*2	Bit configuration register	BCR	32	8, 16, 32	2, 3 PCLK*3
0009 0848h	CAN0*2	Receive FIFO control register	RFCR	8	8	2, 3 PCLK*3
0009 0849h	CAN0*2	Receive FIFO pointer control register	RFPCR	8	8	2, 3 PCLK*3
0009 084Ah	CAN0*2	Transmit FIFO control register	TFCR	8	8	2, 3 PCLK*3
0009 084Bh	CAN0*2	Transmit FIFO pointer control register	TFPCR	8	8	2, 3 PCLK*3
0009 084Ch	CAN0*2	Error interrupt enable register	EIER	8	8	2, 3 PCLK*3
0009 084Dh	CAN0*2	Error interrupt factor judge register	EIFR	8	8	2, 3 PCLK*3
0009 084Eh	CAN0*2	Receive error count register	RECR	8	8	2, 3 PCLK*3
0009 084Fh	CAN0*2	Transmit error count register	TECR	8	8	2, 3 PCLK*3
0009 0850h	CAN0*2	Error code store register	ECSR	8	8	2, 3 PCLK*3
0009 0851h	CAN0*2	Channel search support register	CSSR	8	8	2, 3 PCLK*3
0009 0852h	CAN0*2	Mailbox search status register	MSSR	8	8	2, 3 PCLK*3
0009 0853h	CAN0*2	Mailbox search mode register	MSMR	8	8	2, 3 PCLK*3
0009 0854h	CAN0*2	Time stamp register	TSR	16	8, 16	2, 3 PCLK*3
0009 0856h	CAN0*2	Acceptance filter support register	AFSR	16	8, 16	2, 3 PCLK*3
0009 0858h	CAN0*2	Test control register	TCR	8	8	2, 3 PCLK*3
0009 4001h	LIN0	LIN wake-up baud rate select register	LWBR	8	8	2, 3 PCLK*3
0009 4002h	LIN0	LIN baud rate prescaler 0 register	LBRP0	8	8, 16	2, 3 PCLK*3
0009 4003h	LIN0	LIN baud rate prescaler 1 register	LBRP1	8	8, 16	2, 3 PCLK*3
0009 4004h	LIN0	LIN self-test control register	LSTC	8	8	2, 3 PCLK*3
0009 4008h	LIN0	Mode register	L0MD	8	8, 16, 32	2, 3 PCLK*3
0009 4009h	LIN0	Break field setting register	L0BRK	8	8, 16, 32	2, 3 PCLK*3
0009 400Ah	LIN0	Space setting register	L0SPC	8	8, 16, 32	2, 3 PCLK*3
0009 400Bh	LIN0	Wake-up setting register	L0WUP	8	8, 16, 32	2, 3 PCLK*3
0009 400Ch	LIN0	Interrupt enable register	L0IE	8	8, 16	2, 3 PCLK*3
0009 400Dh	LIN0	Error detection enable register	L0EDE	8	8, 16	2, 3 PCLK*3
0009 400Eh	LIN0	Control register	L0C	8	8	2, 3 PCLK*3
0009 4010h	LIN0	Transmission control register	L0TC	8	8, 16, 32	2, 3 PCLK*3
0009 4011h	LIN0	Mode status register	L0MST	8	8, 16, 32	2, 3 PCLK*3
0009 4012h	LIN0	Status register	L0ST	8	8, 16, 32	2, 3 PCLK*3
0009 4013h	LIN0	Error status register	L0EST	8	8, 16, 32	2, 3 PCLK*3
0009 4014h	LIN0	Response field set register	L0RFC	8	8, 16	2, 3 PCLK*3
0009 4015h	LIN0	Buffer register	L0IDB	8	8, 16	2, 3 PCLK*3
0009 4016h	LIN0	Check sum buffer register	L0CBR	8	8	2, 3 PCLK*3
0009 4018h	LIN0	Data 1 buffer register	L0DB1	8	8, 16, 32	2, 3 PCLK*3

Table 4.1 List of I/O Registers (Address Order) (17 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000C 123Ah	MTU	Timer interrupt skipping mode register A	TITMRA	8	8	5 ICLK
000C 123Bh	MTU	Timer interrupt skipping set register 2A	TITCR2A	8	8	5 ICLK
000C 123Ch	MTU	Timer interrupt skipping counter 2A	TITCNT2A	8	8	5 ICLK
000C 1240h	MTU4	Timer A/D converter start request control register	TADCR	16	16	5 ICLK
000C 1244h	MTU4	Timer A/D converter start request cycle set register A	TADCORA	16	16, 32	5 ICLK
000C 1246h	MTU4	Timer A/D converter start request cycle set register B	TADCORB	16	16	5 ICLK
000C 1248h	MTU4	Timer A/D converter start request cycle set buffer register A	TADCOBRA	16	16, 32	5 ICLK
000C 124Ah	MTU4	Timer A/D converter start request cycle set buffer register B	TADCOBRB	16	16	5 ICLK
000C 1260h	MTU	Timer waveform control register A	TWCRA	8	8	5 ICLK
000C 1270h	MTU3	Timer mode register 2A	TMDR2A	8	8	5 ICLK
000C 1272h	MTU3	Timer general register E	TGRE	16	16	5 ICLK
000C 1274h	MTU4	Timer general register E	TGRE	16	16	5 ICLK
000C 1276h	MTU4	Timer general register F	TGRF	16	16	5 ICLK
000C 1280h	MTU	Timer start register A	TSTRA	8	8, 16	5 ICLK
000C 1281h	MTU	Timer synchronous register A	TSYRA	8	8	5 ICLK
000C 1282h	MTU	Timer counter synchronous start register	TCSYSTR	8	8	5 ICLK
000C 1284h	MTU	Timer read/write enable register A	TRWERA	8	8	5 ICLK
000C 1300h	MTU0	Timer control register	TCR	8	8, 16, 32	5 ICLK
000C 1301h	MTU0	Timer mode register 1	TMDR1	8	8	5 ICLK
000C 1302h	MTU0	Timer I/O control register H	TIORH	8	8, 16	5 ICLK
000C 1303h	MTU0	Timer I/O control register L	TIORL	8	8	5 ICLK
000C 1304h	MTU0	Timer interrupt enable register	TIER	8	8, 16, 32	5 ICLK
000C 1305h	MTU0	Timer status register	TSR	8	8	5 ICLK
000C 1306h	MTU0	Timer counter	TCNT	16	16	5 ICLK
000C 1308h	MTU0	Timer general register A	TGRA	16	16, 32	5 ICLK
000C 130Ah	MTU0	Timer general register B	TGRB	16	16	5 ICLK
000C 130Ch	MTU0	Timer general register C	TGRC	16	16, 32	5 ICLK
000C 130Eh	MTU0	Timer general register D	TGRD	16	16	5 ICLK
000C 1320h	MTU0	Timer general register E	TGRE	16	16, 32	5 ICLK
000C 1322h	MTU0	Timer general register F	TGRF	16	16	5 ICLK
000C 1324h	MTU0	Timer interrupt enable register 2	TIER2	8	8, 16	5 ICLK
000C 1325h	MTU0	Timer status register 2	TSR2	8	8	5 ICLK
000C 1326h	MTU0	Timer buffer operation transfer mode register	TBTM	8	8	5 ICLK
000C 1380h	MTU1	Timer control register	TCR	8	8, 16	5 ICLK
000C 1381h	MTU1	Timer mode register 1	TMDR1	8	8	5 ICLK
000C 1382h	MTU1	Timer I/O control register	TIOR	8	8	5 ICLK
000C 1384h	MTU1	Timer interrupt enable register	TIER	8	8, 16, 32	5 ICLK
000C 1385h	MTU1	Timer status register	TSR	8	8	5 ICLK
000C 1386h	MTU1	Timer counter	TCNT	16	16	5 ICLK
000C 1388h	MTU1	Timer general register A	TGRA	16	16, 32	5 ICLK
000C 138Ah	MTU1	Timer general register B	TGRB	16	16	5 ICLK

Table 4.1 List of I/O Registers (Address Order) (24 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000C 22B6h	GPT3	General PWM timer dead time control register	GTDTCR	16	16, 32	3 to 5 ICLK*4
000C 22B8h	GPT3	General PWM timer dead time value register	GTDVU	16	16, 32	3 to 5 ICLK*4
000C 22BAh	GPT3	General PWM timer dead time value register	GTDVD	16	16, 32	3 to 5 ICLK*4
000C 22BCh	GPT3	General PWM timer dead time buffer register	GTDBU	16	16, 32	3 to 5 ICLK*4
000C 22BEh	GPT3	General PWM timer dead time buffer register	GTDBD	16	16, 32	3 to 5 ICLK*4
000C 22C0h	GPT3	General PWM timer output protection function status register	GTSOS	16	16, 32	3 to 5 ICLK*4
000C 22C2h	GPT3	General PWM timer output protection temporary release register	GTSOTR	16	16, 32	3 to 5 ICLK*4
000C 2300h	GPT0	PWM output delay control register	GTDLYCR	16	16, 32	3 to 5 ICLK*4
000C 2302h	GPT1	PWM output delay control register	GTDLYCR	16	16, 32	3 to 5 ICLK*4
000C 2304h	GPT2	PWM output delay control register	GTDLYCR	16	16, 32	3 to 5 ICLK*4
000C 2306h	GPT3	PWM output delay control register	GTDLYCR	16	16, 32	3 to 5 ICLK*4
000C 2318h	GPT0	GTIOCA rising output delay register	GTDLYRA	16	16, 32	3 to 5 ICLK*4
000C 231Ah	GPT0	GTIOCB rising output delay register	GTDLYRB	16	16, 32	3 to 5 ICLK*4
000C 231Ch	GPT1	GTIOCA rising output delay register	GTDLYRA	16	16, 32	3 to 5 ICLK*4
000C 231Eh	GPT1	GTIOCB rising output delay register	GTDLYRB	16	16, 32	3 to 5 ICLK*4
000C 2320h	GPT2	GTIOCA rising output delay register	GTDLYRA	16	16, 32	3 to 5 ICLK*4
000C 2322h	GPT2	GTIOCB rising output delay register	GTDLYRB	16	16, 32	3 to 5 ICLK*4
000C 2324h	GPT3	GTIOCA falling output delay register	GTDLYRA	16	16, 32	3 to 5 ICLK*4
000C 2326h	GPT3	GTIOCB falling output delay register	GTDLYRB	16	16, 32	3 to 5 ICLK*4
000C 2328h	GPT0	GTIOCA falling output delay register	GTDLYFA	16	16, 32	3 to 5 ICLK*4
000C 232Ah	GPT0	GTIOCB falling output delay register	GTDLYFB	16	16, 32	3 to 5 ICLK*4
000C 232Ch	GPT1	GTIOCA falling output delay register	GTDLYFA	16	16, 32	3 to 5 ICLK*4
000C 232Eh	GPT1	GTIOCB falling output delay register	GTDLYFB	16	16, 32	3 to 5 ICLK*4
000C 2330h	GPT2	GTIOCA falling output delay register	GTDLYFA	16	16, 32	3 to 5 ICLK*4
000C 2332h	GPT2	GTIOCB falling output delay register	GTDLYFB	16	16, 32	3 to 5 ICLK*4
000C 2334h	GPT3	GTIOCA falling output delay register	GTDLYFA	16	16, 32	3 to 5 ICLK*4
000C 2336h	GPT3	GTIOCB falling output delay register	GTDLYFB	16	16, 32	3 to 5 ICLK*4
007F C402h	FLASH	Flash mode register	FMODR	8	8	2, 3 PCLK*3
007F C410h	FLASH	Flash access status register	FASTAT	8	8	2, 3 PCLK*3
007F C411h	FLASH	Flash access error interrupt enable register	FAEINT	8	8	2, 3 PCLK*3
007F C412h	FLASH	Flash ready interrupt enable register	FRDYIE	8	8	2, 3 PCLK*3
007F C440h	FLASH	Data flash read enable register 0	DFLRE0	16	16	2, 3 PCLK*3
007F C442h	FLASH	Data flash read enable register 1	DFLRE1	16	16	2, 3 PCLK*3
007F C450h	FLASH	Data flash programming/erasure enable register 0	DFLWE0	16	16	2, 3 PCLK*3
007F C452h	FLASH	Data flash programming/erasure enable register 1	DFLWE1	16	16	2, 3 PCLK*3
007F C454h	FLASH	FCU RAM enable register	FCURAME	16	16	2, 3 PCLK*3
007F FFB0h	FLASH	Flash status register 0	FSTATR0	8	8	2, 3 PCLK*3
007F FFB1h	FLASH	Flash status register 1	FSTATR1	8	8	2, 3 PCLK*3
007F FFB2h	FLASH	Flash P/E mode entry register	FENTRYR	16	16	2, 3 PCLK*3
007F FFB4h	FLASH	Flash protect register	FPROTR	16	16	2, 3 PCLK*3
007F FFB6h	FLASH	Flash reset register	FRESETR	16	16	2, 3 PCLK*3

Table 4.2 List of I/O Registers (Bit Order) (5 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
ICU	IR144	—	—	—	—	—	—	—	IR
ICU	IR145	—	—	—	—	—	—	—	IR
ICU	IR146	—	—	—	—	—	—	—	IR
ICU	IR149	—	—	—	—	—	—	—	IR
ICU	IR150	—	—	—	—	—	—	—	IR
ICU	IR151	—	—	—	—	—	—	—	IR
ICU	IR152	—	—	—	—	—	—	—	IR
ICU	IR153	—	—	—	—	—	—	—	IR
ICU	IR170	—	—	—	—	—	—	—	IR
ICU	IR171	—	—	—	—	—	—	—	IR
ICU	IR172	—	—	—	—	—	—	—	IR
ICU	IR173	—	—	—	—	—	—	—	IR
ICU	IR174	—	—	—	—	—	—	—	IR
ICU	IR175	—	—	—	—	—	—	—	IR
ICU	IR176	—	—	—	—	—	—	—	IR
ICU	IR177	—	—	—	—	—	—	—	IR
ICU	IR178	—	—	—	—	—	—	—	IR
ICU	IR179	—	—	—	—	—	—	—	IR
ICU	IR180	—	—	—	—	—	—	—	IR
ICU	IR181	—	—	—	—	—	—	—	IR
ICU	IR182	—	—	—	—	—	—	—	IR
ICU	IR183	—	—	—	—	—	—	—	IR
ICU	IR184	—	—	—	—	—	—	—	IR
ICU	IR186	—	—	—	—	—	—	—	IR
ICU	IR187	—	—	—	—	—	—	—	IR
ICU	IR188	—	—	—	—	—	—	—	IR
ICU	IR189	—	—	—	—	—	—	—	IR
ICU	IR190	—	—	—	—	—	—	—	IR
ICU	IR192	—	—	—	—	—	—	—	IR
ICU	IR193	—	—	—	—	—	—	—	IR
ICU	IR194	—	—	—	—	—	—	—	IR
ICU	IR195	—	—	—	—	—	—	—	IR
ICU	IR196	—	—	—	—	—	—	—	IR
ICU	IR214	—	—	—	—	—	—	—	IR
ICU	IR215	—	—	—	—	—	—	—	IR
ICU	IR216	—	—	—	—	—	—	—	IR
ICU	IR217	—	—	—	—	—	—	—	IR
ICU	IR218	—	—	—	—	—	—	—	IR
ICU	IR219	—	—	—	—	—	—	—	IR
ICU	IR220	—	—	—	—	—	—	—	IR
ICU	IR221	—	—	—	—	—	—	—	IR
ICU	IR222	—	—	—	—	—	—	—	IR
ICU	IR223	—	—	—	—	—	—	—	IR
ICU	IR224	—	—	—	—	—	—	—	IR
ICU	IR225	—	—	—	—	—	—	—	IR
ICU	IR246	—	—	—	—	—	—	—	IR
ICU	IR247	—	—	—	—	—	—	—	IR
ICU	IR248	—	—	—	—	—	—	—	IR
ICU	IR249	—	—	—	—	—	—	—	IR
ICU	IR254	—	—	—	—	—	—	—	IR
ICU	DTCER027	—	—	—	—	—	—	—	DTCE
ICU	DTCER028	—	—	—	—	—	—	—	DTCE

Table 4.2 List of I/O Registers (Bit Order) (7 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
ICU	DTCER180	—	—	—	—	—	—	—	DTCE
ICU	DTCER181	—	—	—	—	—	—	—	DTCE
ICU	DTCER182	—	—	—	—	—	—	—	DTCE
ICU	DTCER183	—	—	—	—	—	—	—	DTCE
ICU	DTCER184	—	—	—	—	—	—	—	DTCE
ICU	DTCER186	—	—	—	—	—	—	—	DTCE
ICU	DTCER187	—	—	—	—	—	—	—	DTCE
ICU	DTCER188	—	—	—	—	—	—	—	DTCE
ICU	DTCER189	—	—	—	—	—	—	—	DTCE
ICU	DTCER190	—	—	—	—	—	—	—	DTCE
ICU	DTCER192	—	—	—	—	—	—	—	DTCE
ICU	DTCER193	—	—	—	—	—	—	—	DTCE
ICU	DTCER194	—	—	—	—	—	—	—	DTCE
ICU	DTCER195	—	—	—	—	—	—	—	DTCE
ICU	DTCER196	—	—	—	—	—	—	—	DTCE
ICU	DTCER215	—	—	—	—	—	—	—	DTCE
ICU	DTCER216	—	—	—	—	—	—	—	DTCE
ICU	DTCER219	—	—	—	—	—	—	—	DTCE
ICU	DTCER220	—	—	—	—	—	—	—	DTCE
ICU	DTCER223	—	—	—	—	—	—	—	DTCE
ICU	DTCER224	—	—	—	—	—	—	—	DTCE
ICU	DTCER247	—	—	—	—	—	—	—	DTCE
ICU	DTCER248	—	—	—	—	—	—	—	DTCE
ICU	DTCER254	—	—	—	—	—	—	—	DTCE
ICU	IER02	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER03	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER05	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER07	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER08	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER0C	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER0D	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER0E	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER0F	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER10	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER11	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER12	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER13	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER15	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER16	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER17	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER18	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER1A	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER1B	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER1C	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER1E	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER1F	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	SWINTR	—	—	—	—	—	—	—	SWINT
ICU	FIR	FIEN	—	—	—	—	—	—	—
		FVCT[7:0]							
ICU	IPR00	—	—	—	—	IPR[3:0]			
ICU	IPR01	—	—	—	—	IPR[3:0]			
ICU	IPR02	—	—	—	—	IPR[3:0]			

Table 4.2 List of I/O Registers (Bit Order) (25 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
GPT0	GTDBU								
GPT0	GTDBD								
GPT0	GTSOS	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	SOS[1:0]	
GPT0	GTSOTR	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	SOTR
GPT1	GTIOR	OBHLD	OBDFLT			GTIOB[5:0]			
		OAHLD	OADFLT			GTIOA[5:0]			
GPT1	GTINTAD	ADTRBDEN	ADTRBUEN	ADTRADEN	ADTRAUEN	EINT	—	—	—
		GTINTPR[1:0]		GTINTF	GTINTE	GTINTD	GTINTC	GTINTB	GTINTA
GPT1	GTCR	—	—	CCLR[1:0]		—	—	TPCS[1:0]	
		—	—	—	—	—		MD[2:0]	
GPT1	GTBER	—	ADTDB	ADTTB[1:0]		—	ADTDA	ADTTA[1:0]	
		—	CCRSWT	PR[1:0]		CCRB[1:0]		CCRA[1:0]	
GPT1	GTUDC	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	UDF	UD
GPT1	GTITC	—	ADTBL	—	ADTAL	—		IVTT[2:0]	
		IVTC[1:0]		ITLF	ITLE	ITLD	ITLC	ITLB	ITLA
GPT1	GTST	TUCF	—	—	—	DTEF		ITCNT[2:0]	
		TCFPU	TCFPO	TCFF	TCFE	TCFD	TCFC	TCFB	TCFA
GPT1	GTCNT								
GPT1	GTCCRA								
GPT1	GTCCRB								
GPT1	GTCCRC								
GPT1	GTCCRD								
GPT1	GTCCRE								
GPT1	GTCCRF								
GPT1	GTPR								
GPT1	GTPBR								
GPT1	GTPDBR								
GPT1	GTADTRA								
GPT1	GTADTBRA								
GPT1	GTADTDBRA								
GPT1	GTADTRB								

Table 4.2 List of I/O Registers (Bit Order) (26 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
GPT1	GTADTBRB								
GPT1	GTADTDBRB								
GPT1	GTONCR	OBE	OAE	—	SWN	—	—	—	NFV
		NFS[3:0]				NVB	NVA	NEB	NEA
GPT1	GTDTCR	—	—	—	—	—	—	—	TDFER
		—	—	TDBDE	TDBUE	—	—	—	TDE
GPT1	GTDVU								
GPT1	GTDVD								
GPT1	GTDBU								
GPT1	GTDBD								
GPT1	GTSOS	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	SOS[1:0]	
GPT1	GTSOTR	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	SOTR
GPT2	GTIOR	OBHLD	OBDFLT	GTIOB[5:0]					
		OAHLD	OADFLT	GTIOA[5:0]					
GPT2	GTINTAD	ADTRBDEN	ADTRBUEN	ADTRADEN	ADTRAUEN	EINT	—	—	—
		GTINTPR[1:0]		GTINTF	GTINTE	GTINTD	GTINTC	GTINTB	GTINTA
GPT2	GTCR	—	—	CCLR[1:0]		—	—	TPCS[1:0]	
		—	—	—	—	—	MD[2:0]		
GPT2	GTBER	—	ADTDB	ADTTB[1:0]		—	ADTDA	ADTTA[1:0]	
		—	CCRSWT	PR[1:0]		CCRB[1:0]		CCRA[1:0]	
GPT2	GTUDC	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	UDF	UD
GPT2	GTITC	—	ADTBL	—	ADTAL	—	IVTT[2:0]		
		IVTC[1:0]		ITLF	ITLE	ITLD	ITLC	ITLB	ITLA
GPT2	GTST	TUCF	—	—	—	DTEF	ITCNT[2:0]		
		TCFPU	TCFPO	TCFF	TCFE	TCFD	TCFC	TCFB	TCFA
GPT2	GTCNT								
GPT2	GTCCRA								
GPT2	GTCCRB								
GPT2	GTCCRC								
GPT2	GTCCRD								
GPT2	GTCCRE								
GPT2	GTCCRF								
GPT2	GTPR								

Table 4.2 List of I/O Registers (Bit Order) (30 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
FLASH	FSTATR0	FRDY	ILGLERR	ERSERR	PRGERR	SUSRDY	—	ERSSPD	PRGSPD
FLASH	FSTATR1	FCUERR	—	—	FLOCKST	—	—	—	—
FLASH	FENTRYR	FEKEY[7:0]							
		FENTRYD	—	—	—	—	—	—	FENTRY0
FLASH	FPROTR	FPKEY[7:0]							
		—	—	—	—	—	—	—	FPROTCN
FLASH	FRESETR	FRKEY[7:0]							
		—	—	—	—	—	—	—	FRESET
FLASH	FCMDR	CMDR[7:0]							
		PCMDR[7:0]							
FLASH	FCPSR	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	ESUSPMD
FLASH	DFLBCCNT	—	—	—	—	—		BCADR[7:0]	
		BCADR[7:0]						—	BCSIZE
FLASH	FPESTAT	—	—	—	—	—	—	—	—
		PEERRST[7:0]							
FLASH	DFLBCSTAT	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	BCST
FLASH	PCKAR	—	—	—	—	—	—	—	—
		PCKA[7:0]							

Note: • In this, the I/O port related registers (0008 C001h to 0008 C116h) indicate the bit configuration of the 112-pin LQFP version. As the configuration of registers and bits differs depending on a package, see section 14, I/O Ports, for details in the User's manual: Hardware.

Note 1. This shows the bit configuration when ADDPR.DPSEL = 0 and ADDPR.DPPRC = 0 (The value has 10-bit accuracy and is padded at the LSB end).

Note 2. This shows the bit configuration when ADCER.ADRFMT = 0 (aligned to the LSB end) and ADCER.ADPRC[1:0] = 00b. For details, refer to section 28, 12-Bit A/D Converter (S12ADA) in the User's manual: Hardware.

Note 3. This function is not supported by the product without the CAN function.