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Details

Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I ² C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	44
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 4x10b, 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562t6edff-v1

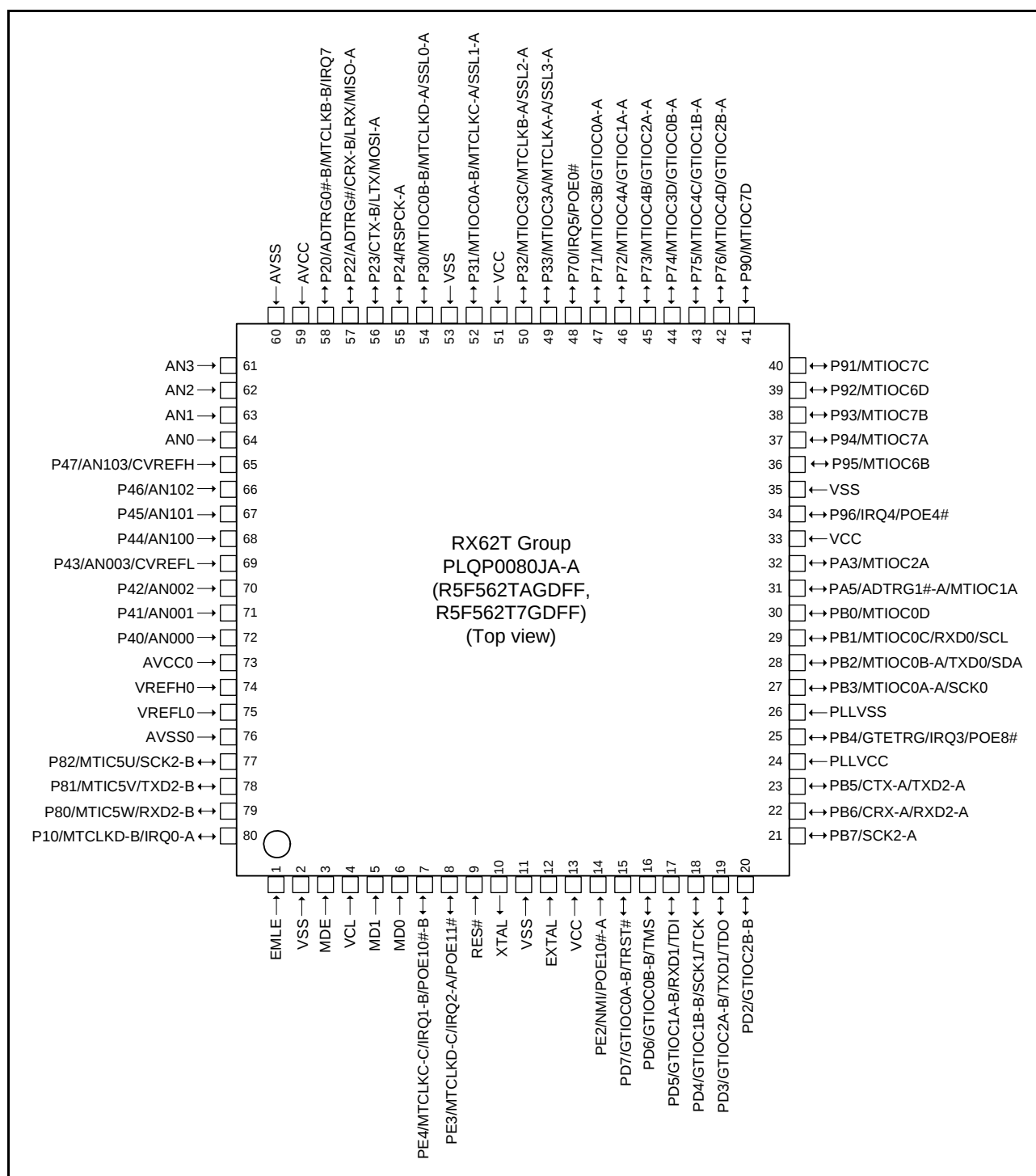


Figure 1.6 Pin Assignment of the 80-Pin LQFP (Two-Motor Control Supported Version)

Table 1.4 List of Pins and Pin Functions (112-Pin LQFP) (3 / 3)

Pin No. (112-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi- cation	Interrupt	POE	Debugging
80	AVCC							
81	VREF							
82	AVSS							
83		P63	AN3					
84		P62	AN2					
85		P61	AN1					
86		P60	AN0					
87		P55	AN11					
88		P54	AN10					
89		P53	AN9					
90		P52	AN8					
91		P51	AN7					
92		P50	AN6					
93		P47	AN103/ CVREFH					
94		P46	AN102					
95		P45	AN101					
96		P44	AN100					
97		P43	AN003/ CVREFL					
98		P42	AN002					
99		P41	AN001					
100		P40	AN000					
101	AVCC0							
102	VREFH0							
103	VREFL0							
104	AVSS0							
105		P82		MTIC5U	SCK2-B			
106		P81		MTIC5V	TXD2-B			
107		P80		MTIC5W	RXD2-B			
108				WDTOVF#				
109		P11		MTCLKC-B		IRQ1-A		
110		P10		MTCLKD-B		IRQ0-A		
111								TRST#
112								TMS

Table 1.5 List of Pins and Pin Functions (100-Pin LQFP) (1 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi- cation	Interrupt	POE	Debugging
1		PE5				IRQ0-B		
2	EMLE							
3	VSS							
4	MDE							
5	VCL							
6	MD1							
7	MD0							
8		PE4		MTCLKC-C		IRQ1-B	POE10#-B	
9		PE3		MTCLKD-C		IRQ2-A	POE11#	
10	RES#							
11	XTAL							
12	VSS							
13	EXTAL							
14	VCC							
15		PE2				NMI	POE10#-A	
16		PE1			SSL3-C			
17		PE0			CRX-C/ SSL2-C			
18		PD7		GTIOC0A-B	CTX-C/SSL1-C			TRST#
19		PD6		GTIOC0B-B	SSL0-C			TMS
20		PD5		GTIOC1A-B	RXD1			TDI
21		PD4		GTIOC1B-B	SCK1			TCK
22		PD3		GTIOC2A-B	TXD1			TDO
23		PD2		GTIOC2B-B	MOSI-C			TRCLK
24		PD1		GTIOC3A	MISO-C			TRDATA3
25		PD0		GTIOC3B	RSPCK-C			TRDATA2
26		PB7			SCK2-A			TRDATA1
27		PB6			CRX-A/ RXD2-A			TRDATA0
28		PB5			CTX-A/TXD2-A			TRSYNC
29	PLLVC							
30		PB4		GTETR		IRQ3	POE8#	
31	PLLVS							
32		PB3		MTIOC0A-A	SCK0			
33		PB2		MTIOC0B-A	TXD0/SDA			
34		PB1		MTIOC0C	RXD0/SCL			
35		PB0		MTIOC0D	MOSI-B			
36		PA5	ADTRG1#-A	MTIOC1A	MISO-B			
37		PA4	ADTRG0#-A	MTIOC1B	RSPCK-B			
38		PA3		MTIOC2A	SSL0-B			
39		PA2		MTIOC2B	SSL1-B			
40		PA1		MTIOC6A	SSL2-B			

Table 1.5 List of Pins and Pin Functions (100-Pin LQFP) (3 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi- cation	Interrupt	POE	Debugging
77		P60	AN0					
78		P55	AN11					
79		P54	AN10					
80		P53	AN9					
81		P52	AN8					
82		P51	AN7					
83		P50	AN6					
84		P47	AN103/ CVREFH					
85		P46	AN102					
86		P45	AN101					
87		P44	AN100					
88		P43	AN003/ CVREFL					
89		P42	AN002					
90		P41	AN001					
91		P40	AN000					
92	AVCC0							
93	VREFH0							
94	VREFL0							
95	AVSS0							
96		P82		MTIC5U	SCK2-B			
97		P81		MTIC5V	TXD2-B			
98		P80		MTIC5W	RXD2-B			
99		P11		MTCLKC-B		IRQ1-A		
100		P10		MTCLKD-B		IRQ0-A		

1.5 Pin Functions

Table 1.9 lists the pin functions.

Table 1.9 Pin Functions (1 / 4)

Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply.
	VCL	Input	Connect this pin to VSS via a 0.1-μF capacitor. The capacitor should be placed close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
	PLLVC	Input	Power supply pin for the PLL circuit. Connect it to the system power supply.
	PLLVSS	Input	Ground pin for the PLL circuit.
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
Operating mode control	MD0 MD1 MDE	Input	Pins for setting the operating mode. The signal levels on these pins must not be changed during operation.
System control	RES#	Input	Reset signal input pin. This LSI enters the reset state when this signal goes low.
	EMLE	Input	Input pin for the on-chip emulator enable signal. When the on-chip emulator is used, this pin should be driven high. When not used, it should be driven low.
On-chip emulator	TRST#	Input	On-chip emulator pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator.
	TMS	Input	
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TRCLK	Output	This pin outputs the clock for synchronization with the trace data. Not included in the 80-/64-pin versions.
	TRSYNC	Output	This pin indicates that output from the TRDATA0 to TRDATA3 pins is valid. Not included in the 80-/64-pin versions.
	TRDATA0 to TRDATA3	Output	These pins output the trace information. Not included in the 80-/64-pin versions.
Interrupt (ICU)	NMI	Input	Non-maskable interrupt request signal.
	IRQ0-A/IRQ0-B/IRQ0-C IRQ1-A/IRQ1-B/IRQ1-C IRQ2-A/IRQ2-B IRQ3 to IRQ7	Input	Interrupt request signals. The IRQ0-C/IRQ1-C/IRQ2-B pin is not included in the 100-pin version. The IRQ0-B/IRQ0-C/IRQ1-C/IRQ2-B pin is not included in the 80-pin version. The IRQ0-B/IRQ0-C/IRQ1-B/IRQ1-/IRQ2-A/IRQ2-B/IRQ4/IRQ6/IRQ7 pin is not included in the 64-pin version.

2. CPU

The RX CPU has sixteen general-purpose registers, nine control registers, and one accumulator used for DSP instructions.

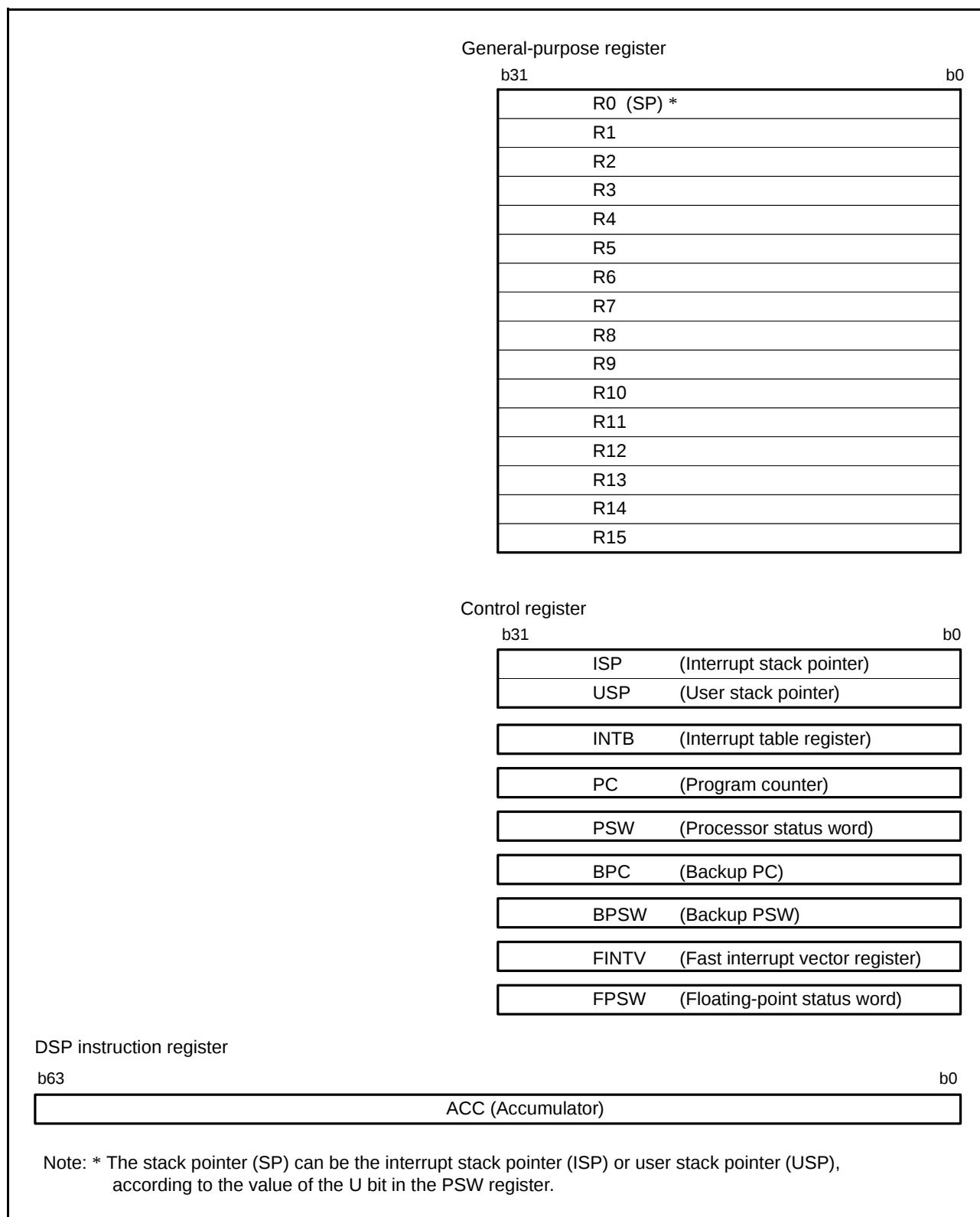


Figure 2.1 Register Set of the CPU

2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen general-purpose registers (R0 to R15). R1 to R15 can be used as data registers or address registers. R0, a general-purpose register, also functions as the stack pointer (SP). The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2 Control Registers

(1) Interrupt Stack Pointer (ISP)/User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).

Set the ISP or USP to a multiple of four, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(2) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the relocatable vector table starts. Set INTB to a multiple of four.

(3) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

(4) Processor Status Word (PSW)

The processor status word (PSW) indicates results of instruction execution or the state of the CPU.

(5) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.

After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC.

(6) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.

After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

(7) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.

The FINTV register specifies a branch destination address when a fast interrupt has been generated.

(8) Floating-Point Status Word (FPSW)

The floating-point status word (FPSW) indicates the results of floating-point operations.

When an exception handling enable bit (Ej) enables the exception handling (Ej = 1), the exception cause can be identified by checking the corresponding Cj flag in the exception handling routine. If the exception handling is masked (Ej = 0), the occurrence of exception can be checked by reading the Fj flag at the end of a series of processing. Once the Fj flag has been set to 1, this value is retained until it is cleared to 0 by software (j = X, U, Z, O, or V).

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 0000h	SYSTEM	Mode monitor register	MDMONR	16	16	3 ICLK
0008 0002h	SYSTEM	Mode status register	MDSR	16	16	3 ICLK
0008 0006h	SYSTEM	System control register 0	SYSCR0	16	16	3 ICLK
0008 0008h	SYSTEM	System control register 1	SYSCR1	16	16	3 ICLK
0008 000Ch	SYSTEM	Standby control register	SBYCR	16	16	3 ICLK
0008 0010h	SYSTEM	Module stop control register A	MSTPCRA	32	32	3 ICLK
0008 0014h	SYSTEM	Module stop control register B	MSTPCRB	32	32	3 ICLK
0008 0018h	SYSTEM	Module stop control register C	MSTPCRC	32	32	3 ICLK
0008 0020h	SYSTEM	System clock control register	SCKCR	32	32	3 ICLK
0008 0040h	SYSTEM	Oscillation stop detection control register	OSTDCR	16	16	3 ICLK
0008 1300h	BSC	Bus error status clear register	BERCLR	8	8	2 ICLK
0008 1304h	BSC	Bus error monitoring enable register	BEREN	8	8	2 ICLK
0008 1308h	BSC	Bus error status register 1	BERSR1	8	8	2 ICLK
0008 130Ah	BSC	Bus error status register 2	BERSR2	16	16	2 ICLK
0008 2400h	DTC	DTC control register	DTCCR	8	8	2 ICLK
0008 2404h	DTC	DTC vector base register	DTCVBR	32	32	2 ICLK
0008 2408h	DTC	DTC address mode register	DTCADMOD	8	8	2 ICLK
0008 240Ch	DTC	DTC module start register	DTCST	8	8	2 ICLK
0008 240Eh	DTC	DTC status register	DTCSTS	16	16	2 ICLK
0008 6400h	MPU	Region 0 start page-number register	RSPAGE0	32	32	1 ICLK
0008 6404h	MPU	Region 0 end page-number register	REPAGE0	32	32	1 ICLK
0008 6408h	MPU	Region 1 start page-number register	RSPAGE1	32	32	1 ICLK
0008 640Ch	MPU	Region 1 end page-number register	REPAGE1	32	32	1 ICLK
0008 6410h	MPU	Region 2 start page-number register	RSPAGE2	32	32	1 ICLK
0008 6414h	MPU	Region 2 end page-number register	REPAGE2	32	32	1 ICLK
0008 6418h	MPU	Region 3 start page-number register	RSPAGE3	32	32	1 ICLK
0008 641Ch	MPU	Region 3 end page-number register	REPAGE3	32	32	1 ICLK
0008 6420h	MPU	Region 4 start page-number register	RSPAGE4	32	32	1 ICLK
0008 6424h	MPU	Region 4 end page-number register	REPAGE4	32	32	1 ICLK
0008 6428h	MPU	Region 5 start page-number register	RSPAGE5	32	32	1 ICLK
0008 642Ch	MPU	Region 5 end page-number register	REPAGE5	32	32	1 ICLK
0008 6430h	MPU	Region 6 start page-number register	RSPAGE6	32	32	1 ICLK
0008 6434h	MPU	Region 6 end page-number register	REPAGE6	32	32	1 ICLK
0008 6438h	MPU	Region 7 start page-number register	RSPAGE7	32	32	1 ICLK
0008 643Ch	MPU	Region 7 end page-number register	REPAGE7	32	32	1 ICLK
0008 6500h	MPU	Memory-protection enable register	MPEN	32	32	1 ICLK
0008 6504h	MPU	Background access control register	MPBAC	32	32	1 ICLK
0008 6508h	MPU	Memory-protection error status-clearing register	MPECLR	32	32	1 ICLK
0008 650Ch	MPU	Memory-protection error status register	MPESTS	32	32	1 ICLK
0008 6514h	MPU	Data memory-protection error address register	MPDEA	32	32	1 ICLK
0008 6520h	MPU	Region search address register	MPSA	32	32	1 ICLK
0008 6524h	MPU	Region search operation register	MPOPS	16	16	1 ICLK

Table 4.1 List of I/O Registers (Address Order) (19 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000C 1A39h	MTU7	Timer buffer operation transfer mode register	TBTM	8	8	5 ICLK
000C 1A3Ah	MTU	Timer interrupt skipping mode register B	TITMRB	8	8	5 ICLK
000C 1A3Bh	MTU	Timer interrupt skipping set register 2B	TITCR2B	8	8	5 ICLK
000C 1A3Ch	MTU	Timer interrupt skipping counter 2B	TITCNT2B	8	8	5 ICLK
000C 1A40h	MTU7	Timer A/D converter start request control register	TADCR	16	16	5 ICLK
000C 1A44h	MTU7	Timer A/D converter start request cycle set register A	TADCORA	16	16, 32	5 ICLK
000C 1A46h	MTU7	Timer A/D converter start request cycle set register B	TADCORB	16	16	5 ICLK
000C 1A48h	MTU7	Timer A/D converter start request cycle set buffer register A	TADCOBRA	16	16, 32	5 ICLK
000C 1A4Ah	MTU7	Timer A/D converter start request cycle set buffer register B	TADCOBRB	16	16	5 ICLK
000C 1A50h	MTU6	Timer synchronous clear register	TSYCR	8	8	5 ICLK
000C 1A60h	MTU	Timer waveform control register B	TWCRB	8	8	5 ICLK
000C 1A70h	MTU	Timer mode register 2B	TMDR2B	8	8	5 ICLK
000C 1A72h	MTU6	Timer general register E	TGRE	16	16	5 ICLK
000C 1A74h	MTU7	Timer general register E	TGRE	16	16	5 ICLK
000C 1A76h	MTU7	Timer general register F	TGRF	16	16	5 ICLK
000C 1A80h	MTU	Timer start register B	TSTRB	8	8, 16	5 ICLK
000C 1A81h	MTU	Timer synchronous register B	TSYRB	8	8	5 ICLK
000C 1A84h	MTU	Timer read/write enable register B	TRWERB	8	8	5 ICLK
000C 1C80h	MTU5	Timer counter U	TCNTU	16	16, 32	5 ICLK
000C 1C82h	MTU5	Timer general register U	TGRU	16	16	5 ICLK
000C 1C84h	MTU5	Timer control register U	TCRU	8	8	5 ICLK
000C 1C86h	MTU5	Timer I/O control register U	TIORU	8	8	5 ICLK
000C 1C90h	MTU5	Timer counter V	TCNTV	16	16, 32	5 ICLK
000C 1C92h	MTU5	Timer general register V	TGRV	16	16	5 ICLK
000C 1C94h	MTU5	Timer control register V	TCRV	8	8	5 ICLK
000C 1C96h	MTU5	Timer I/O control register V	TIORV	8	8	5 ICLK
000C 1CA0h	MTU5	Timer counter W	TCNTW	16	16, 32	5 ICLK
000C 1CA2h	MTU5	Timer general register W	TGRW	16	16	5 ICLK
000C 1CA4h	MTU5	Timer control register W	TCRW	8	8	5 ICLK
000C 1CA6h	MTU5	Timer I/O control register W	TIORW	8	8	5 ICLK
000C 1CB0h	MTU5	Timer status register	TSR	8	8	5 ICLK
000C 1CB2h	MTU5	Timer interrupt enable register	TIER	8	8	5 ICLK
000C 1CB4h	MTU5	Timer start register	TSTR	8	8	5 ICLK
000C 1CB6h	MTU5	Timer compare match clear register	TCNTCMPCLR	8	8	5 ICLK
000C 2000h	GPT	General PWM timer software start register	GTSTR	16	8, 16, 32	3 to 5 ICLK*4
000C 2004h	GPT	General PWM timer hardware source start control register	GTHSCR	16	8, 16, 32	3 to 5 ICLK*4
000C 2006h	GPT	General PWM timer hardware source clear control register	GTHCCR	16	8, 16, 32	3 to 5 ICLK*4
000C 2008h	GPT	General PWM timer hardware start source select register	GTHSSR	16	8, 16, 32	3 to 5 ICLK*4

Table 4.1 List of I/O Registers (Address Order) (24 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000C 22B6h	GPT3	General PWM timer dead time control register	GTDTCR	16	16, 32	3 to 5 ICLK ^{*4}
000C 22B8h	GPT3	General PWM timer dead time value register	GTDVU	16	16, 32	3 to 5 ICLK ^{*4}
000C 22BAh	GPT3	General PWM timer dead time value register	GTDVD	16	16, 32	3 to 5 ICLK ^{*4}
000C 22BCh	GPT3	General PWM timer dead time buffer register	GTDBU	16	16, 32	3 to 5 ICLK ^{*4}
000C 22BEh	GPT3	General PWM timer dead time buffer register	GTDBD	16	16, 32	3 to 5 ICLK ^{*4}
000C 22C0h	GPT3	General PWM timer output protection function status register	GTSOS	16	16, 32	3 to 5 ICLK ^{*4}
000C 22C2h	GPT3	General PWM timer output protection temporary release register	GTSOTR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2300h	GPT0	PWM output delay control register	GTDLYCR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2302h	GPT1	PWM output delay control register	GTDLYCR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2304h	GPT2	PWM output delay control register	GTDLYCR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2306h	GPT3	PWM output delay control register	GTDLYCR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2318h	GPT0	GTIOCA rising output delay register	GTDLYRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 231Ah	GPT0	GTIOCB rising output delay register	GTDLYRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 231Ch	GPT1	GTIOCA rising output delay register	GTDLYRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 231Eh	GPT1	GTIOCB rising output delay register	GTDLYRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2320h	GPT2	GTIOCA rising output delay register	GTDLYRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 2322h	GPT2	GTIOCB rising output delay register	GTDLYRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2324h	GPT3	GTIOCA falling output delay register	GTDLYRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 2326h	GPT3	GTIOCB falling output delay register	GTDLYRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2328h	GPT0	GTIOCA falling output delay register	GTDLYFA	16	16, 32	3 to 5 ICLK ^{*4}
000C 232Ah	GPT0	GTIOCB falling output delay register	GTDLYFB	16	16, 32	3 to 5 ICLK ^{*4}
000C 232Ch	GPT1	GTIOCA falling output delay register	GTDLYFA	16	16, 32	3 to 5 ICLK ^{*4}
000C 232Eh	GPT1	GTIOCB falling output delay register	GTDLYFB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2330h	GPT2	GTIOCA falling output delay register	GTDLYFA	16	16, 32	3 to 5 ICLK ^{*4}
000C 2332h	GPT2	GTIOCB falling output delay register	GTDLYFB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2334h	GPT3	GTIOCA falling output delay register	GTDLYFA	16	16, 32	3 to 5 ICLK ^{*4}
000C 2336h	GPT3	GTIOCB falling output delay register	GTDLYFB	16	16, 32	3 to 5 ICLK ^{*4}
007F C402h	FLASH	Flash mode register	FMODR	8	8	2, 3 PCLK ^{*3}
007F C410h	FLASH	Flash access status register	FASTAT	8	8	2, 3 PCLK ^{*3}
007F C411h	FLASH	Flash access error interrupt enable register	FAEINT	8	8	2, 3 PCLK ^{*3}
007F C412h	FLASH	Flash ready interrupt enable register	FRDYIE	8	8	2, 3 PCLK ^{*3}
007F C440h	FLASH	Data flash read enable register 0	DFLRE0	16	16	2, 3 PCLK ^{*3}
007F C442h	FLASH	Data flash read enable register 1	DFLRE1	16	16	2, 3 PCLK ^{*3}
007F C450h	FLASH	Data flash programming/erasure enable register 0	DFLWE0	16	16	2, 3 PCLK ^{*3}
007F C452h	FLASH	Data flash programming/erasure enable register 1	DFLWE1	16	16	2, 3 PCLK ^{*3}
007F C454h	FLASH	FCU RAM enable register	FCURAME	16	16	2, 3 PCLK ^{*3}
007F FFB0h	FLASH	Flash status register 0	FSTATR0	8	8	2, 3 PCLK ^{*3}
007F FFB1h	FLASH	Flash status register 1	FSTATR1	8	8	2, 3 PCLK ^{*3}
007F FFB2h	FLASH	Flash P/E mode entry register	FENTRYR	16	16	2, 3 PCLK ^{*3}
007F FFB4h	FLASH	Flash protect register	FPROTR	16	16	2, 3 PCLK ^{*3}
007F FFB6h	FLASH	Flash reset register	FRESETR	16	16	2, 3 PCLK ^{*3}

Table 4.2 List of I/O Registers (Bit Order) (12 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
RSPi0	SSLP	—	—	—	—	SSLP3	SSLP2	SSLP1	SSLP0
RSPi0	SPPCR	—	—	MOIFE	MOIFV	—	—	SPLP2	SPLP
RSPi0	SPSR	SPRF	—	SPTEF	—	PERF	MODF	IDLNF	OVRF
RSPi0	SPDR	H[15:0]							
		H[15:0]							
		L[15:0]							
		L[15:0]							
RSPi0	SPSCR	—	—	—	—	—	—	SPSLN[2:0]	—
RSPi0	SPSSR	—	—	SPECM[2:0]	—	—	—	SPCP[2:0]	—
RSPi0	SPBR	SPR7	SPR6	SPR5	SPR4	SPR3	SPR2	SPR1	SPR0
RSPi0	SPDCR	—	—	SPLW	SPRDTD	SLSEL[1:0]	—	SPFC[1:0]	—
RSPi0	SPCKD	—	—	—	—	—	—	SCKDL[2:0]	—
RSPi0	SSLND	—	—	—	—	—	—	SLNDL[2:0]	—
RSPi0	SPND	—	—	—	—	—	—	SPNDL[2:0]	—
RSPi0	SPCR2	—	—	—	—	PTE	SPIIE	SPOE	SPPE
RSPi0	SPCMD0	SCKDEN	SLNDEN	SPNDEN	LSBF	—	—	SPB[3:0]	—
		SSLKP	—	SSLA[2:0]	—	BRDV[1:0]	—	CPOL	CPHA
RSPi0	SPCMD1	SCKDEN	SLNDEN	SPNDEN	LSBF	—	—	SPB[3:0]	—
		SSLKP	—	SSLA[2:0]	—	BRDV[1:0]	—	CPOL	CPHA
RSPi0	SPCMD2	SCKDEN	SLNDEN	SPNDEN	LSBF	—	—	SPB[3:0]	—
		SSLKP	—	SSLA[2:0]	—	BRDV[1:0]	—	CPOL	CPHA
RSPi0	SPCMD3	SCKDEN	SLNDEN	SPNDEN	LSBF	—	—	SPB[3:0]	—
		SSLKP	—	SSLA[2:0]	—	BRDV[1:0]	—	CPOL	CPHA
RSPi0	SPCMD4	SCKDEN	SLNDEN	SPNDEN	LSBF	—	—	SPB[3:0]	—
		SSLKP	—	SSLA[2:0]	—	BRDV[1:0]	—	CPOL	CPHA
RSPi0	SPCMD5	SCKDEN	SLNDEN	SPNDEN	LSBF	—	—	SPB[3:0]	—
		SSLKP	—	SSLA[2:0]	—	BRDV[1:0]	—	CPOL	CPHA
RSPi0	SPCMD6	SCKDEN	SLNDEN	SPNDEN	LSBF	—	—	SPB[3:0]	—
		SSLKP	—	SSLA[2:0]	—	BRDV[1:0]	—	CPOL	CPHA
RSPi0	SPCMD7	SCKDEN	SLNDEN	SPNDEN	LSBF	—	—	SPB[3:0]	—
		SSLKP	—	SSLA[2:0]	—	BRDV[1:0]	—	CPOL	CPHA
S12AD0	ADCSR	ADST	ADCS[1:0]	—	ADIE	—	CKS[1:0]	TRGE	EXTRG
S12AD0	ADANS	—	—	CH[1:0]	—	—	PG002SEL	PG001SEL	PG000SEL
		—	—	—	—	—	PG002EN	PG001EN	PG000EN
S12AD0	ADPG	—	—	—	—	—	PG002GAIN[3:0]	PG001GAIN[3:0]	PG000GAIN[3:0]
		—	—	—	—	—	PG002GAIN[3:0]	PG001GAIN[3:0]	PG000GAIN[3:0]
S12AD0	ADCER	ADRFMT	—	ADIEW	ADIE2	DIAGM	DIAGLD	DIAGVAL[1:0]	—
		—	—	ACE	—	—	ADPRC[1:0]	SHBYP	—
S12AD0	ADSTRGR	—	—	—	—	—	ADSTRS1[4:0]	ADSTRS0[4:0]	—
		—	—	—	—	—	ADSTRS1[4:0]	ADSTRS0[4:0]	—
S12AD	ADCMPMD0	—	—	CEN102[1:0]	—	CEN101[1:0]	—	CEN100[1:0]	—
		—	—	CEN002[1:0]	—	CEN001[1:0]	—	CEN000[1:0]	—
S12AD	ADCMPMD1	—	VSELL1	VSELH1	CSEL1	—	VSELL0	VSELH0	CSEL0
		—	—	REFH[2:0]	—	—	—	REFL[2:0]	—
S12AD	ADCMPNR0	—	—	—	—	—	C002NR[3:0]	C001NR[3:0]	C000NR[3:0]
		—	—	—	—	—	C002NR[3:0]	C001NR[3:0]	C000NR[3:0]
S12AD	ADCMPNR1	—	—	—	—	—	C102NR[3:0]	C101NR[3:0]	C100NR[3:0]
		—	—	—	—	—	C102NR[3:0]	C101NR[3:0]	C100NR[3:0]
S12AD	ADCMPFR	—	—	C102FLAG	C101FLAG	C100FLAG	C002FLAG	C001FLAG	C000FLAG
S12AD	ADCMPSEL	—	—	—	—	—	—	POERQ	IE
		—	—	SEL102	SEL101	SEL100	SEL002	SEL001	SEL000

Table 4.2 List of I/O Registers (Bit Order) (23 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
GPT	GTBDR	BD33	BD32	BD31	BD30	BD23	BD22	BD21	BD20
		BD13	BD12	BD11	BD10	BD03	BD02	BD01	BD00
GPT	GTSWP	—	—	—	—	—	—	—	—
		—	—	—	—	SWP3	SWP2	SWP1	SWP0
GPT	LCCR	LPSC[1:0]		TPSC[1:0]		LCNTAT		LCTQ[2:0]	
		—	LCINTO	LCINTD	LCINTC	—	LCNTS	LCNTCR	LCNTE
GPT	LCST	—	—	—	—	—	—	—	—
		—	—	—	—	—	LISO	LISD	LISC
GPT	LCNTA								
GPT	LCNT00								
GPT	LCNT01								
GPT	LCNT02								
GPT	LCNT03								
GPT	LCNT04								
GPT	LCNT05								
GPT	LCNT06								
GPT	LCNT07								
GPT	LCNT08								
GPT	LCNT09								
GPT	LCNT10								
GPT	LCNT11								
GPT	LCNT12								
GPT	LCNT13								
GPT	LCNT14								
GPT	LCNT15								
GPT	LCNTDU								
GPT	LCNTDL								
GPT0	GTIOR	OBHLD	OBDFLT			GTIOB[5:0]			
		OAHL	OADFLT			GTIOA[5:0]			
GPT0	GTINTAD	ADTRBDEN	ADTRBUEN	ADTRADEN	ADTRAUEN	EINT	—	—	—
		GTINTPR[1:0]		GTINTF	GTINTE	GTINTD	GTINTC	GTINTB	GTINTA

Table 4.2 List of I/O Registers (Bit Order) (28 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
GPT3	GTCCRB								
GPT3	GTCCRC								
GPT3	GTCCRD								
GPT3	GTCCRE								
GPT3	GTCCRF								
GPT3	GTPR								
GPT3	GTPBR								
GPT3	GTPDBR								
GPT3	GTADTRA								
GPT3	GTADTBRA								
GPT3	GTADTDBRA								
GPT3	GTADTRB								
GPT3	GTADTBRB								
GPT3	GTADTDBRB								
GPT3	GTONCR	OBE	OAE	—	SWN	—	—	—	NFV
				NFS[3:0]		NVB	NVA	NEB	NEA
GPT3	GTDTCR	—	—	—	—	—	—	—	TDFER
		—	—	TDBDE	TDBUE	—	—	—	TDE
GPT3	GTDVU								
GPT3	GTDVD								
GPT3	GTDBU								
GPT3	GTDBD	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	SOS[1:0]	—
GPT3	GTSOS	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	SOS[1:0]	—
GPT3	GTSOTR	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	SOTR
GPT0	GTDLYCR	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLYEN	DLYRST	DLLEN
GPT1	GTDLYCR	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLYEN	DLYRST	DLLEN

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Item		Symbol	Value	Unit
Power supply voltage		VCC PLLVCC	-0.3 to +6.5	V
Input voltage (except for ports 4 to 6)		V _{IN}	-0.3 to VCC+0.3	V
Input voltage (port 4)		V _{IN}	-0.3 to AVCC0+0.3	V
Input voltage (ports 5 and 6)		V _{IN}	-0.3 to AVCC+0.3	V
Analog power supply voltage		AVCC0, AVCC*1	-0.3 to +6.5	V
Reference power supply voltage		VREFH0*1	-0.3 to AVCC0+0.3	V
		VREF*1	-0.3 to AVCC+0.3	
Analog input voltage (port 4)		V _{AN}	-0.3 to AVCC0+0.3	V
Analog input voltage (ports 5 and 6)		V _{AN}	-0.3 to AVCC+0.3	V
Operating temperature	D version	T _{opr}	-40 to +85	°C
	G version	T _{opr}	-40 to +105	°C
Storage temperature		T _{stg}	-55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. Do not leave the AVCC0, VREFH0, VREFL0, AVSS0, AVCC, VREF, and AVSS pins open circuit even if the A/D converter is not to be used.

- When the 12-bit converter is not in use:
Connect the AVCC0 pin to AVCC (or VCC for a 64-pin product), the VREFH0 pin to VREF (or AVCC or VCC for an 80- or 64-pin product, respectively), and the AVSS0 and VREFL0 pins to VSS.
- When the 10-bit converter is not in use:
Connect the AVCC pin to AVCC0, the VREF pin to VREFH0, and the AVSS pin to AVSS0.
- When neither the 10- nor the 12-bit converter is in use:
Connect the AVCC0, VREFH0, AVCC, and VREF pins to VCC, and the AVSS0, VREFL0, and AVSS pins to VSS.

5.2 DC Characteristics

Table 5.2 DC Characteristics (1) (1 / 3)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	CAN input pin IRQ input pin MTU3 input pin POE3 input pin SCI input pin A/D trigger input pin NMI input pin GPT input pin LIN input pin RES#	V _{IH}	VCC×0.8	-	VCC+0.3	V	
		V _{IL}	-0.3	-	VCC×0.2		
		ΔV _T	VCC ×0.06	-	-		
	RIIC input pin (IICBus)	V _{IH}	VCC×0.7	-	VCC+0.3		
		V _{IL}	-0.3	-	VCC×0.3		
		ΔV _T	VCC ×0.05	-	-		
	Port 4*1 (also usable as an analog port)	V _{IH}	AVCC0 ×0.8	-	AVCC0 +0.3		
		V _{IL}	- 0.3	-	AVCC0 ×0.2		
		ΔV _T	AVCC0 ×0.06	-	-		
	Ports 5 and 6*1 (also usable as analog ports)	V _{IH}	AVCC ×0.8	-	AVCC +0.3		
		V _{IL}	-0.3	-	AVCC ×0.2		
		ΔV _T	AVCC ×0.06	-	-		
	Ports 1 to 3*1 Ports 7 to B*1 Ports D, E, and G*1	V _{IH}	VCC×0.8	-	VCC+0.3		
		V _{IL}	-0.3	-	VCC×0.2		
		ΔV _T	VCC ×0.06	-	-		
Input high voltage (except Schmitt trigger input pin)	MD pin, EMLE	V _{IH}	VCC×0.9	-	VCC+0.3	V	Conditions 1 and 2
	EXTAL RSPI input pin		VCC×0.8		VCC+0.3		
	RIIC input pin (SMBus)		2.1		VCC+0.3		
Input low voltage (except Schmitt trigger input pin)	MD pin, EMLE	V _{IL}	-0.3	-	VCC×0.1	V	Conditions 1 and 2
	EXTAL RSPI input pin		-0.3	-	VCC×0.2		
	RIIC input pin (SMBus)		-0.3	-	0.8		

5.3 AC Characteristics

Table 5.6 Operation Frequency Value

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit
Operating frequency	System clock (ICLK)	f	8	-	100	MHz
	Peripheral module clock (PCLK)		8	-	50	

5.3.1 Clock Timing

Table 5.7 Clock Timing

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Ta = Topr. Ta is the same under conditions 1 to 3.

Item	Symbol	Min.	Max.	Unit	Test Conditions
Oscillation settling time after reset (crystal)	t _{OSC1}	10	-	ms	Figure 5.1
Oscillation settling time after leaving software standby mode (crystal)	t _{OSC2}	10	-	ms	Figure 5.2
Oscillation settling time after leaving deep software standby mode (crystal)	t _{OSC3}	10	-	ms	Figure 5.3
EXTAL external clock output delay settling time	t _{DEXT}	1	-	ms	Figure 5.1
EXTAL external clock input low pulse width	t _{EXL}	35	-	ns	Figure 5.4
EXTAL external clock input high pulse width	t _{EXH}	35	-	ns	
EXTAL external clock rising time	t _{EXr}	-	5	ns	
EXTAL external clock falling time	t _{EXf}	-	5	ns	
On-chip oscillator (IWDTCCLK) oscillation frequency	f _{IWDTCCLK}	62.5	187.5	kHz	

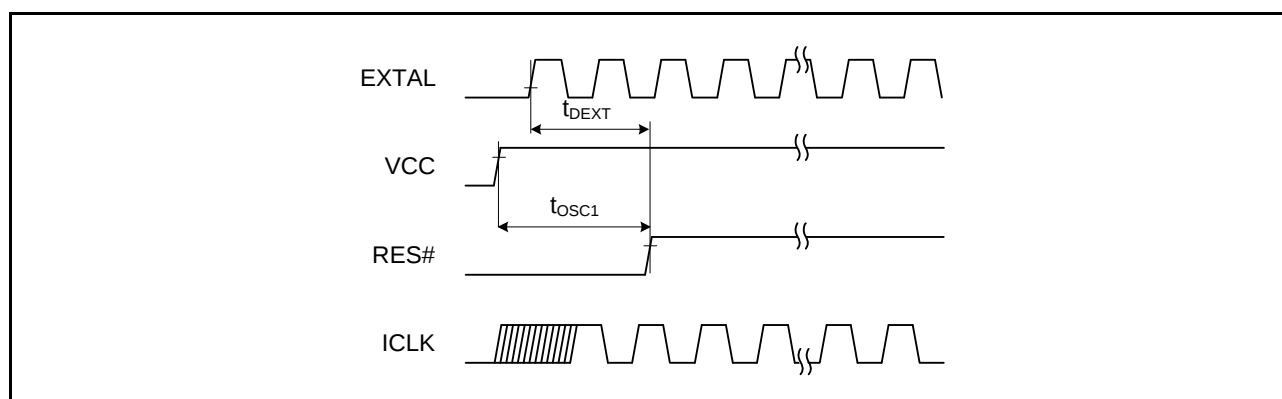


Figure 5.1 Oscillation Settling Timing

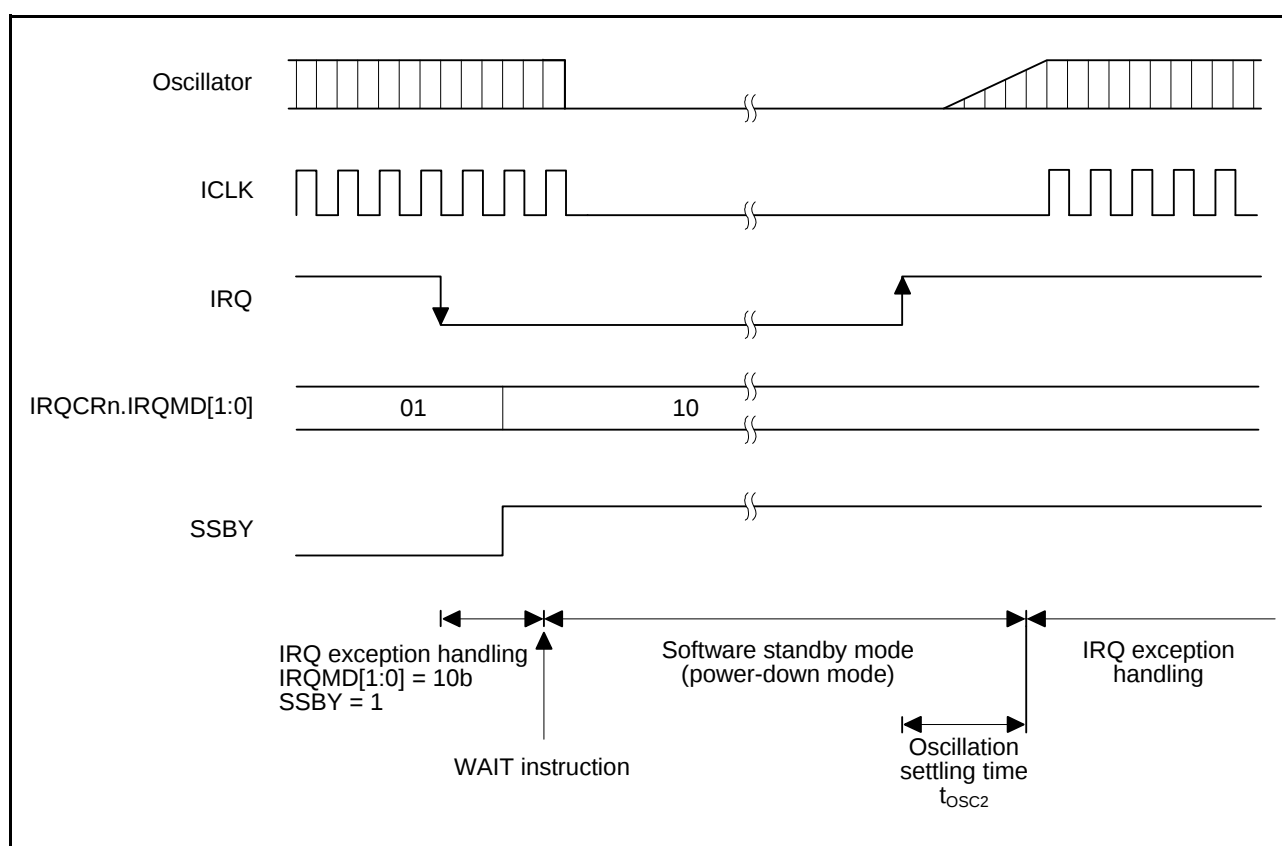


Figure 5.2 Oscillation Settling Timing after Software Standby Mode

Table 5.12 Timing of On-Chip Peripheral Modules (4)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

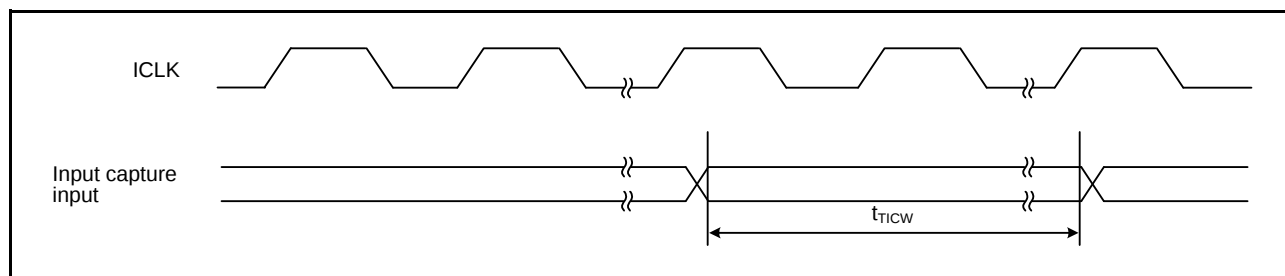
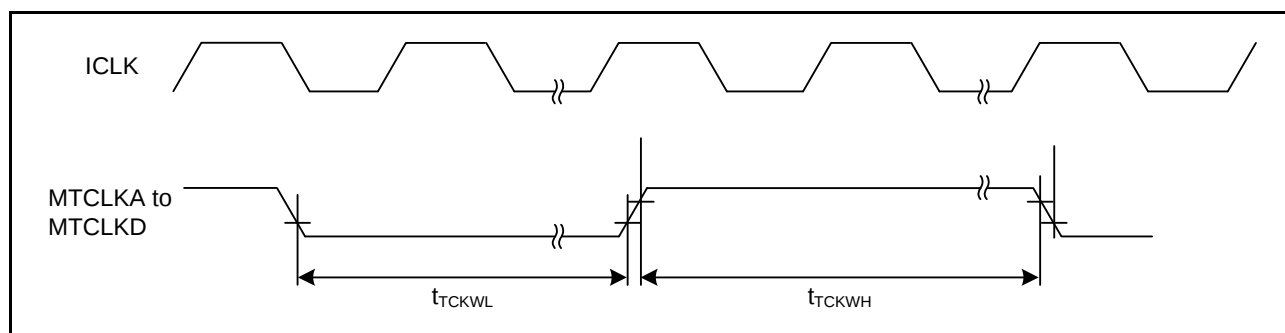
Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Max.	Unit	Test Conditions
MTU3	Input capture input pulse width (single-edge setting)	t_{TICW}	3.0	-	t_{Icyc}	Figure 5.16
	Input capture input pulse width (both-edge setting)	t_{TICW}	5.0	-	t_{Icyc}	
	Timer clock pulse width (single-edge setting)	$t_{TCKWH/L}$	3.0	-	t_{Icyc}	Figure 5.17
	Timer clock pulse width (both-edge setting)	$t_{TCKWH/L}$	5.0	-	t_{Icyc}	
	Timer clock pulse width (phase coefficient mode)	$t_{TCKWH/L}$	5.0	-	t_{Icyc}	
GPT	Input capture input pulse width (single-edge setting)	t_{GTICW}	3.0	-	t_{Icyc}	Figure 5.18
	Input capture input pulse width (both-edge setting)	t_{GTICW}	5.0	-	t_{Icyc}	

Note: • t_{Icyc} : ICLK cycle

**Figure 5.16 MTU3 Input/Output Timing****Figure 5.17 MTU3 Clock Input Timing**

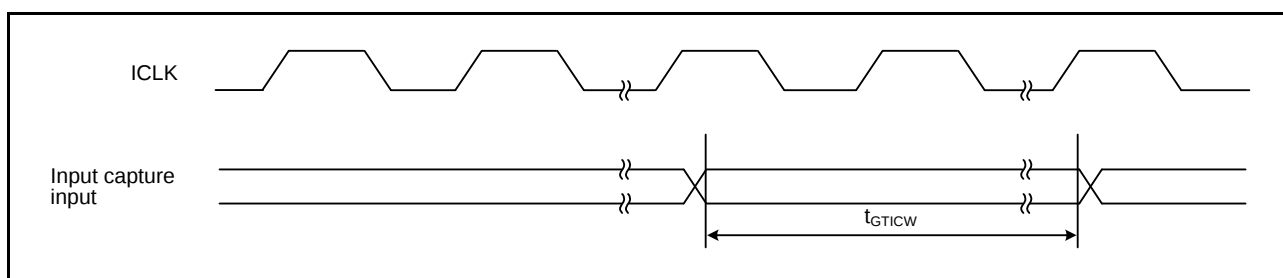


Figure 5.18 GPT Input/Output Timing

Table 5.13 Timing of On-Chip Peripheral Modules (5)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Max.	Unit	Test Conditions
POE3	POE# input pulse width	t _{POEW}	1.5	-	t _{Pcyc}	Figure 5.19

Note: • t_{Pcyc}: PCLK cycle

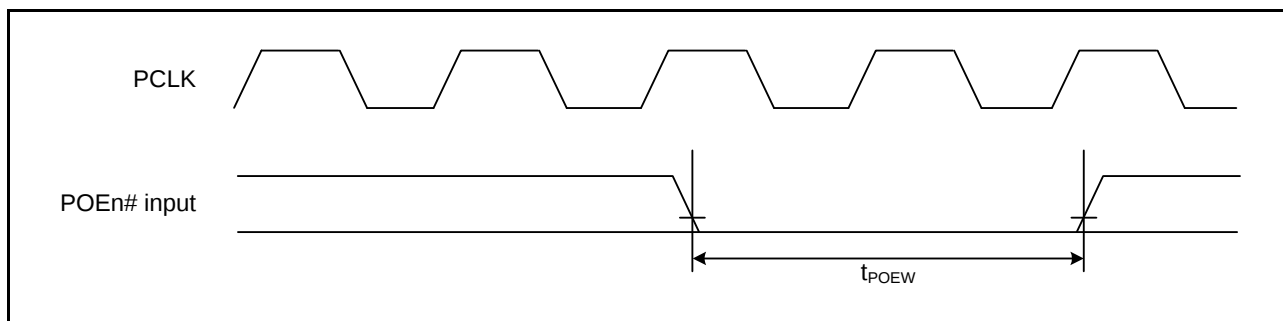


Figure 5.19 POE3# Clock Timing

5.3.4 Timing of PWM Delay Generation Circuit

Table 5.14 Timing of the PWM Delay Generation Circuit

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS = VREL0 = 0 V

AVCC = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Ta = Topr.

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Resolution	—	312.5	—	ps	ICLK = 100 MHz
DNL *1	—	±2.0	—	LSB	

Note 1. This value is correct when the difference between each code and the next is a resolution of one bit (1 LSB).

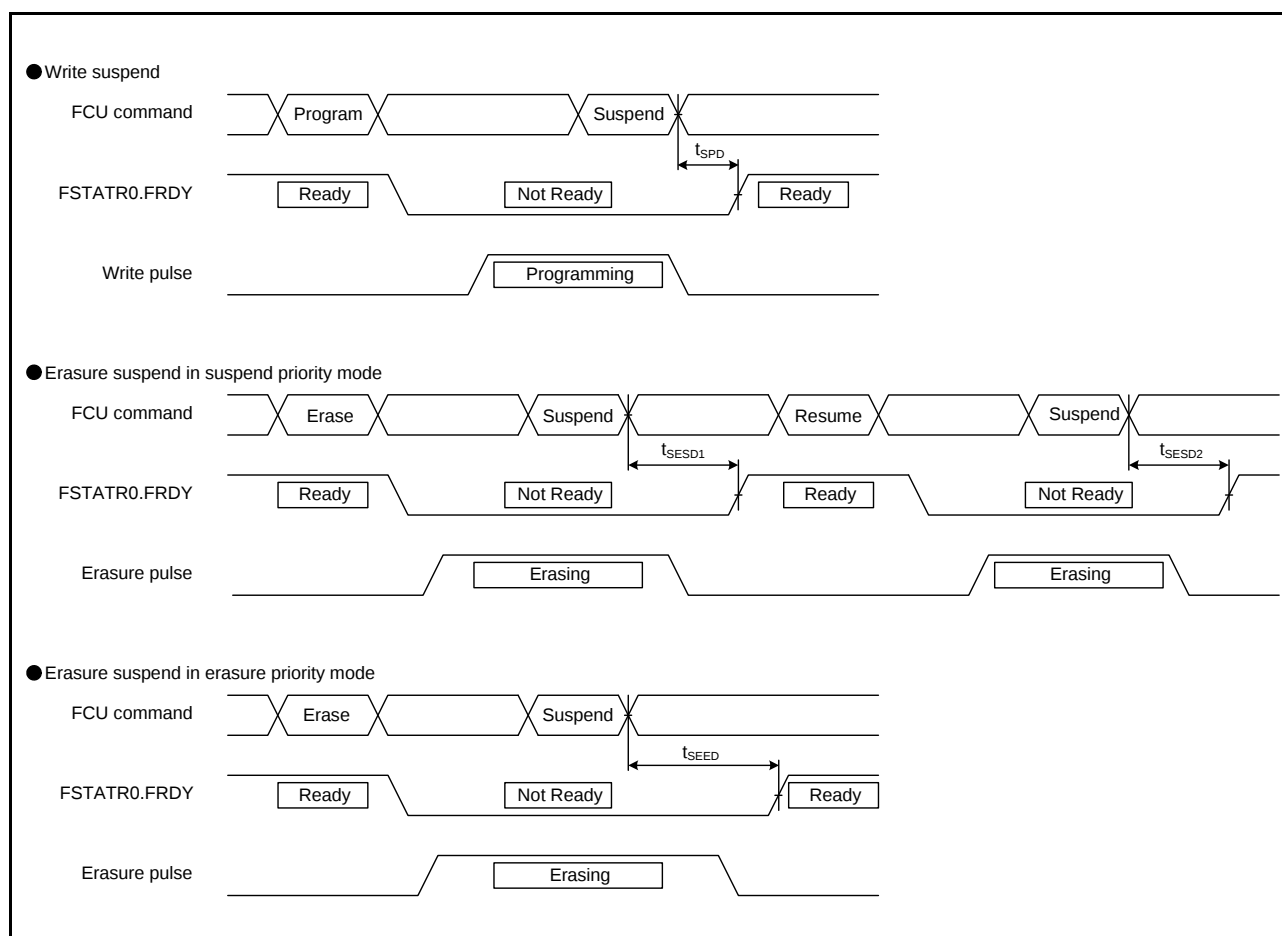


Figure 5.24 Flash Memory Write/Erase Suspend Timing