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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I ² C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	44
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 4x10b, 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562t6edff-v3

Table 1.1 Outline of Specifications (5 / 5)

Classification	Module/Function	Description
A/D converter	10-bit A/D converter (ADA)	• 10 bits (1 unit x 12 channels) • 10-bit resolution • Conversion time: 1.0 μs per channel (in operation with A/D conversion clock ADCLK at 50 MHz) for AVCC0 = 4.0 to 5.5 V 2.0 μs per channel (in operation with A/D conversion clock ADCLK at 25 MHz) for AVCC = 3.0 to 3.6 V • Two basic operating modes - Single mode and scan mode • Scan mode - One-cycle scan mode - Continuous scan mode • Sample-and-hold function - A common sample-and-hold circuit for both units is included. • A/D-conversion register settings for each input pin • Three ways to start A/D conversion - Conversion can be started by software, a conversion start trigger from a timer (MTU3 or GPT), or an external trigger signal. • Functionality for 8-bit precision output - Right-shifting the results of conversion for output by two bits is selectable. • Self-diagnostic function - The self-diagnostic function internally generates three analog input voltages (AVSS, VREF x 1/2, VREF).
CRC calculator (CRC)		• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$. • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.
Operating frequency		ICLK: 8 to 100 MHz PCLK: 8 to 50 MHz
Power supply voltage		• 3-V version - VCC = PLLVCC = 2.7 to 3.6V - AVCC0 = AVCC = 3.0 to 3.6V, or 4.0 to 5.5V - VREFH0 = 3.0 to AVCC0, or 4.0 to AVCC0 - VREF = 3.0 to AVCC, or 4.0 to AVCC • 5-V version - VCC = PLLVCC = 4.0 to 5.5V - AVCC0 = AVCC = 4.0 to 5.5V - VREFH0 = 4.0 to AVCC0 - VREF = 4.0 to AVCC
Operating temperature		D version: -40 to +85°C, G version: -40 to +105°C*1
Packages		112-pin LQFP (PLQP0112JA-A, 20x20-0.65-mm pitch) 100-pin LQFP (PLQP0100KB-A, 14x14-0.5-mm pitch) 80-pin LQFP (PLQP0080JA-A, 14x14-0.65-mm pitch) 64-pin LQFP (PLQP0064KB-A, 10x10-0.5-mm pitch) 64-pin LQFP (PLQP0064GA-A, 14x14-0.8mm pitch)

Note 1. Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

Table 1.3 List of Products (2 / 2)

Group	Part No.	Order Part No.	Package	ROM Capacity	RAM Capacity	Data Flash Capacity	Power Supply Voltage	CAN	Operating Temp. Range	
RX62T	R5F562T7EDFH	R5F562T7EDFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes	2.7 to 3.6 V	Not Supported	-40 to +85°C (D version)	
	R5F562T7EDFP	R5F562T7EDFP#V3	PLQP0100KB-A							
	R5F562T7EDFF	R5F562T7EDFF#V3	PLQP0080JA-A							
	R5F562T7EDFM	R5F562T7EDFM#V3	PLQP0064KB-A							
	R5F562T7EDFK	R5F562T7EDFK#V3	PLQP0064GA-A							
	R5F562T6EDFF	R5F562T6EDFF#V3	PLQP0080JA-A	64 Kbytes	8 Kbytes					
	R5F562T6EDFM	R5F562T6EDFM#V3	PLQP0064KB-A							
	R5F562T6EDFK	R5F562T6EDFK#V3	PLQP0064GA-A							
	R5F562TAAGFH	R5F562TAAGFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes	VCC/PLL VCC 4.0 to 5.5 V AVCC/AVCC0 4.0 to 5.5 V	Supported	-40 to +105°C (G version) *1	
	R5F562TAAGFP	R5F562TAAGFP#V3	PLQP0100KB-A							
	R5F562TAAGFF	R5F562TAAGFF#V3	PLQP0080JA-A							
	R5F562TAGGFF	R5F562TAGGFF#V3	PLQP0080JA-A							
	R5F562TAAGFM	R5F562TAAGFM#V3	PLQP0064KB-A							
	R5F562TAAGFK	R5F562TAAGFK#V3	PLQP0064GA-A							
	R5F562T7AGFH	R5F562T7AGFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes				
	R5F562T7AGFP	R5F562T7AGFP#V3	PLQP0100KB-A							
	R5F562T7AGFF	R5F562T7AGFF#V3	PLQP0080JA-A							
	R5F562T7GGFF	R5F562T7GGFF#V3	PLQP0080JA-A							
	R5F562T7AGFM	R5F562T7AGFM#V3	PLQP0064KB-A							
	R5F562T7AGFK	R5F562T7AGFK#V3	PLQP0064GA-A	64 Kbytes	8 Kbytes					
	R5F562T6AGFF	R5F562T6AGFF#V3	PLQP0080JA-A							
	R5F562T6AGFM	R5F562T6AGFM#V3	PLQP0064KB-A							
	R5F562T6AGFK	R5F562T6AGFK#V3	PLQP0064GA-A	256 Kbytes	16 Kbytes	32 Kbytes	VCC/PLL VCC 2.7 to 3.6 V AVCC/AVCC0 3.0 to 3.6 V or 4.0 to 5.5 V			
	R5F562TABGFH	R5F562TABGFH#V3	PLQP0112JA-A							
	R5F562TABGFP	R5F562TABGFP#V3	PLQP0100KB-A							
	R5F562TABGFF	R5F562TABGFF#V3	PLQP0080JA-A							
	R5F562TABGFM	R5F562TABGFM#V3	PLQP0064KB-A							
	R5F562TABGFK	R5F562TABGFK#V3	PLQP0064GA-A	128 Kbytes	8 Kbytes	8 Kbytes				
	R5F562T7BGFH	R5F562T7BGFH#V3	PLQP0112JA-A							
	R5F562T7BGFP	R5F562T7BGFP#V3	PLQP0100KB-A							
	R5F562T7BGFF	R5F562T7BGFF#V3	PLQP0080JA-A							
	R5F562T7BGFM	R5F562T7BGFM#V3	PLQP0064KB-A							
	R5F562T7BGFK	R5F562T7BGFK#V3	PLQP0064GA-A	64 Kbytes	8 Kbytes					
	R5F562T6BGFF	R5F562T6BGFF#V3	PLQP0080JA-A							
	R5F562T6BGFM	R5F562T6BGFM#V3	PLQP0064KB-A							
	R5F562T6BGFK	R5F562T6BGFK#V3	PLQP0064GA-A	RX62G	256 Kbytes	16 Kbytes	32 Kbytes	VCC/PLL VCC 4.0 to 5.5 V AVCC/AVCC0 4.0 to 5.5 V	Supported	-40 to +85°C (D version)
R5F562GAADFP	R5F562GAADFP#V3	PLQP0100KB-A								
R5F562G7ADFH	R5F562G7ADFH#V3	PLQP0112JA-A	128 Kbytes		8 Kbytes	8 Kbytes				
R5F562G7ADFP	R5F562G7ADFP#V3	PLQP0100KB-A								
R5F562GADDFH	R5F562GADDFH#V3	PLQP0112JA-A	256 Kbytes		16 Kbytes	32 Kbytes			Not Supported	
R5F562GADDFP	R5F562GADDFP#V3	PLQP0100KB-A								
R5F562G7DDFH	R5F562G7DDFH#V3	PLQP0112JA-A	128 Kbytes		8 Kbytes	8 Kbytes				
R5F562G7DDFP	R5F562G7DDFP#V3	PLQP0100KB-A								
R5F562GAAGFH	R5F562GAAGFH#V3	PLQP0112JA-A	256 Kbytes		16 Kbytes	32 Kbytes	VCC/PLL VCC 4.0 to 5.5 V AVCC/AVCC0 4.0 to 5.5 V	Supported	-40 to +105°C (G versio) *1	
R5F562GAAGFP	R5F562GAAGFP#V3	PLQP0100KB-A								
R5F562G7AGFH	R5F562G7AGFH#V3	PLQP0112JA-A	128 Kbytes		8 Kbytes	8 Kbytes				
R5F562G7AGFP	R5F562G7AGFP#V3	PLQP0100KB-A								

Note 1. Please contact us if you are using a G version.

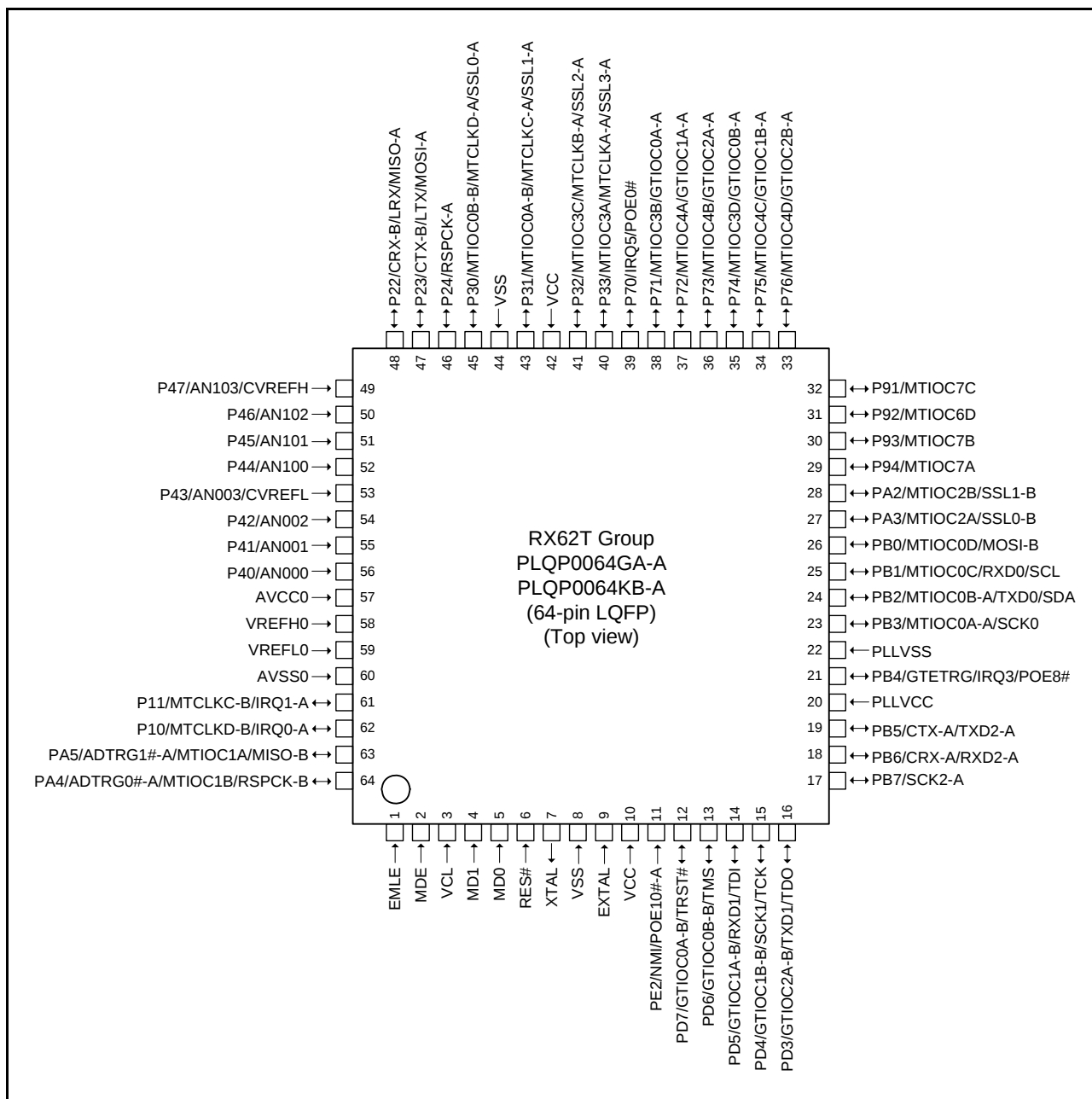


Figure 1.7 Pin Assignment of the 64-Pin LQFP

Table 1.5 List of Pins and Pin Functions (100-Pin LQFP) (2 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi- cation	Interrupt	POE	Debugging
41		PA0		MTIOC6C	SSL3-B			
42	VCC							
43		P96				IRQ4	POE4#	
44	VSS							
45		P95		MTIOC6B				
46		P94		MTIOC7A				
47		P93		MTIOC7B				
48		P92		MTIOC6D				
49		P91		MTIOC7C				
50		P90		MTIOC7D				
51		P76		MTIOC4D/ GTIOC2B-A				
52		P75		MTIOC4C/ GTIOC1B-A				
53		P74		MTIOC3D/ GTIOC0B-A				
54		P73		MTIOC4B/ GTIOC2A-A				
55		P72		MTIOC4A/ GTIOC1A-A				
56		P71		MTIOC3B/ GTIOC0A-A				
57		P70				IRQ5	POE0#	
58		P33		MTIOC3A/ MTCLKA-A	SSL3-A			
59		P32		MTIOC3C/ MTCLKB-A	SSL2-A			
60	VCC							
61		P31		MTIOC0A-B/ MTCLKC-A	SSL1-A			
62	VSS							
63		P30		MTIOC0B-B/ MTCLKD-A	SSL0-A			
64		P24			RSPCK-A			
65		P23			CTX-B/ LTX/ MOSI-A			
66		P22	ADTRG#		CRX-B/ LRX/ MISO-A			
67		P21	ADTRG1#-B	MTCLKA-B		IRQ6		
68		P20	ADTRG0#-B	MTCLKB-B		IRQ7		
69		P65	AN5					
70		P64	AN4					
71	AVCC							
72	VREF							
73	AVSS							
74		P63	AN3					
75		P62	AN2					
76		P61	AN1					

Table 1.6 List of Pins and Pin Functions (80-Pin LQFP) (1 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi- cation	Interrupt	POE	Debugging
1	EMLE							
2	VSS							
3	MDE							
4	VCL							
5	MD1							
6	MD0							
7		PE4		MTCLKC-C		IRQ1-B	POE10#-B	
8		PE3		MTCLKD-C		IRQ2-A	POE11#	
9	RES#							
10	XTAL							
11	VSS							
12	EXTAL							
13	VCC							
14		PE2				NMI	POE10#-A	
15		PE0			CRX-C			
16		PD7		GTIOC0A-B	CTX-C			TRST#
17		PD6		GTIOC0B-B				TMS
18		PD5		GTIOC1A-B	RXD1			TDI
19		PD4		GTIOC1B-B	SCK1			TCK
20		PD3		GTIOC2A-B	TXD1			TDO
21		PB7			SCK2-A			
22		PB6			CRX-A/ RXD2-A			
23		PB5			CTX-A/ TXD2-A			
24	PLL VCC							
25		PB4		GTETRG		IRQ3	POE8#	
26	PLL VSS							
27		PB3		MTIOC0A-A	SCK0			
28		PB2		MTIOC0B-A	TXD0/SDA			
29		PB1		MTIOC0C	RXD0/SCL			
30		PB0		MTIOC0D	MOSI-B			
31		PA3		MTIOC2A	SSL0-B			
32		PA2		MTIOC2B	SSL1-B			
33	VCC							
34		P96				IRQ4	POE4#	
35	VSS							
36		P95		MTIOC6B				
37		P94		MTIOC7A				
38		P93		MTIOC7B				
39		P92		MTIOC6D				
40		P91		MTIOC7C				
41		P76		MTIOC4D/ GTIOC2B-A				

Table 1.6 List of Pins and Pin Functions (80-Pin LQFP) (2 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi- cation	Interrupt	POE	Debugging
42		P75		MTIOC4C/ GTIOC1B-A				
43		P74		MTIOC3D/ GTIOC0B-A				
44		P73		MTIOC4B/ GTIOC2A-A				
45		P72		MTIOC4A/ GTIOC1A-A				
46		P71		MTIOC3B/ GTIOC0A-A				
47		P70				IRQ5	POE0#	
48		P33		MTIOC3A/ MTCLKA-A	SSL3-A			
49		P32		MTIOC3C/ MTCLKB-A	SSL2-A			
50	VCC							
51		P31		MTIOC0A-B/ MTCLKC-A	SSL1-A			
52	VSS							
53		P30		MTIOC0B-B/ MTCLKD-A	SSL0-A			
54		P24			RSPCK-A			
55		P23			CTX-B/ LTX/ MOSI-A			
56		P22	ADTRG#		CRX-B/ LRX/ MISO-A			
57		P21	ADTRG1#-B	MTCLKA-B		IRQ6		
58		P20	ADTRG0#-B	MTCLKB-B		IRQ7		
59	AVCC							
60	AVSS							
61		P63	AN3					
62		P62	AN2					
63		P61	AN1					
64		P60	AN0					
65		P47	AN103/ CVREFH					
66		P46	AN102					
67		P45	AN101					
68		P44	AN100					
69		P43	AN003/ CVREFL					
70		P42	AN002					
71		P41	AN001					
72		P40	AN000					
73	AVCC0							
74	VREFH0							
75	VREFL0							

Table 1.8 List of Pins and Pin Functions (64-Pin LQFP) (2 / 2)

Pin No. (64-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi- cation	Interrupt	POE	Debuggi ng
40		P33		MTIOC3A/ MTCLKA-A	SSL3-A			
41		P32		MTIOC3C/ MTCLKB-A	SSL2-A			
42	VCC							
43		P31		MTIOC0A-B/ MTCLKC-A	SSL1-A			
44	VSS							
45		P30		MTIOC0B-B/ MTCLKD-A	SSL0-A			
46		P24			RSPCK-A			
47		P23			CTX-B/ LTX/ MOSI-A			
48		P22			CRX-B/ LRX/ MISO-A			
49		P47	AN103/ CVREFH					
50		P46	AN102					
51		P45	AN101					
52		P44	AN100					
53		P43	AN003/ CVREFL					
54		P42	AN002					
55		P41	AN001					
56		P40	AN000					
57	AVCC0							
58	VREFH0							
59	VREFL0							
60	AVSS0							
61		P11		MTCLKC-B		IRQ1-A		
62		P10		MTCLKD-B		IRQ0-A		
63		PA5	ADTRG1#-A	MTIOC1A	MISO-B			
64		PA4	ADTRG0#-A	MTIOC1B	RSPCK-B			

- (a) Write to an I/O register.
- (b) Read the value from the I/O register to a general register.
- (c) Execute the operation using the value read.
- (d) Execute the subsequent instruction.

[Instruction examples]

- Byte-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.B #SFR_DATA, [R1]
CMP [R1].UB, R1
;; Next process
```

- Word-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.W #SFR_DATA, [R1]
CMP [R1].W, R1
;; Next process
```

- Longword-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.L #SFR_DATA, [R1]
CMP [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 0000h	SYSTEM	Mode monitor register	MDMONR	16	16	3 ICLK
0008 0002h	SYSTEM	Mode status register	MDSR	16	16	3 ICLK
0008 0006h	SYSTEM	System control register 0	SYSCR0	16	16	3 ICLK
0008 0008h	SYSTEM	System control register 1	SYSCR1	16	16	3 ICLK
0008 000Ch	SYSTEM	Standby control register	SBYCR	16	16	3 ICLK
0008 0010h	SYSTEM	Module stop control register A	MSTPCRA	32	32	3 ICLK
0008 0014h	SYSTEM	Module stop control register B	MSTPCRB	32	32	3 ICLK
0008 0018h	SYSTEM	Module stop control register C	MSTPCRC	32	32	3 ICLK
0008 0020h	SYSTEM	System clock control register	SCKCR	32	32	3 ICLK
0008 0040h	SYSTEM	Oscillation stop detection control register	OSTDCR	16	16	3 ICLK
0008 1300h	BSC	Bus error status clear register	BERCLR	8	8	2 ICLK
0008 1304h	BSC	Bus error monitoring enable register	BEREN	8	8	2 ICLK
0008 1308h	BSC	Bus error status register 1	BERSR1	8	8	2 ICLK
0008 130Ah	BSC	Bus error status register 2	BERSR2	16	16	2 ICLK
0008 2400h	DTC	DTC control register	DTCCR	8	8	2 ICLK
0008 2404h	DTC	DTC vector base register	DTCVBR	32	32	2 ICLK
0008 2408h	DTC	DTC address mode register	DTCADMOD	8	8	2 ICLK
0008 240Ch	DTC	DTC module start register	DTCST	8	8	2 ICLK
0008 240Eh	DTC	DTC status register	DTCSTS	16	16	2 ICLK
0008 6400h	MPU	Region 0 start page-number register	RSPAGE0	32	32	1 ICLK
0008 6404h	MPU	Region 0 end page-number register	REPAGE0	32	32	1 ICLK
0008 6408h	MPU	Region 1 start page-number register	RSPAGE1	32	32	1 ICLK
0008 640Ch	MPU	Region 1 end page-number register	REPAGE1	32	32	1 ICLK
0008 6410h	MPU	Region 2 start page-number register	RSPAGE2	32	32	1 ICLK
0008 6414h	MPU	Region 2 end page-number register	REPAGE2	32	32	1 ICLK
0008 6418h	MPU	Region 3 start page-number register	RSPAGE3	32	32	1 ICLK
0008 641Ch	MPU	Region 3 end page-number register	REPAGE3	32	32	1 ICLK
0008 6420h	MPU	Region 4 start page-number register	RSPAGE4	32	32	1 ICLK
0008 6424h	MPU	Region 4 end page-number register	REPAGE4	32	32	1 ICLK
0008 6428h	MPU	Region 5 start page-number register	RSPAGE5	32	32	1 ICLK
0008 642Ch	MPU	Region 5 end page-number register	REPAGE5	32	32	1 ICLK
0008 6430h	MPU	Region 6 start page-number register	RSPAGE6	32	32	1 ICLK
0008 6434h	MPU	Region 6 end page-number register	REPAGE6	32	32	1 ICLK
0008 6438h	MPU	Region 7 start page-number register	RSPAGE7	32	32	1 ICLK
0008 643Ch	MPU	Region 7 end page-number register	REPAGE7	32	32	1 ICLK
0008 6500h	MPU	Memory-protection enable register	MPEN	32	32	1 ICLK
0008 6504h	MPU	Background access control register	MPBAC	32	32	1 ICLK
0008 6508h	MPU	Memory-protection error status-clearing register	MPECLR	32	32	1 ICLK
0008 650Ch	MPU	Memory-protection error status register	MPESTS	32	32	1 ICLK
0008 6514h	MPU	Data memory-protection error address register	MPDEA	32	32	1 ICLK
0008 6520h	MPU	Region search address register	MPSA	32	32	1 ICLK
0008 6524h	MPU	Region search operation register	MPOPS	16	16	1 ICLK

Table 4.1 List of I/O Registers (Address Order) (4 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 70BCh	ICU	Interrupt request register 188	IR188	8	8	2 ICLK
0008 70BDh	ICU	Interrupt request register 189	IR189	8	8	2 ICLK
0008 70BEh	ICU	Interrupt request register 190	IR190	8	8	2 ICLK
0008 70C0h	ICU	Interrupt request register 192	IR192	8	8	2 ICLK
0008 70C1h	ICU	Interrupt request register 193	IR193	8	8	2 ICLK
0008 70C2h	ICU	Interrupt request register 194	IR194	8	8	2 ICLK
0008 70C3h	ICU	Interrupt request register 195	IR195	8	8	2 ICLK
0008 70C4h	ICU	Interrupt request register 196	IR196	8	8	2 ICLK
0008 70D6h	ICU	Interrupt request register 214	IR214	8	8	2 ICLK
0008 70D7h	ICU	Interrupt request register 215	IR215	8	8	2 ICLK
0008 70D8h	ICU	Interrupt request register 216	IR216	8	8	2 ICLK
0008 70D9h	ICU	Interrupt request register 217	IR217	8	8	2 ICLK
0008 70DAh	ICU	Interrupt request register 218	IR218	8	8	2 ICLK
0008 70DBh	ICU	Interrupt request register 219	IR219	8	8	2 ICLK
0008 70DCh	ICU	Interrupt request register 220	IR220	8	8	2 ICLK
0008 70DDh	ICU	Interrupt request register 221	IR221	8	8	2 ICLK
0008 70DEh	ICU	Interrupt request register 222	IR222	8	8	2 ICLK
0008 70DFh	ICU	Interrupt request register 223	IR223	8	8	2 ICLK
0008 70E0h	ICU	Interrupt request register 224	IR224	8	8	2 ICLK
0008 70E1h	ICU	Interrupt request register 225	IR225	8	8	2 ICLK
0008 70F6h	ICU	Interrupt request register 246	IR246	8	8	2 ICLK
0008 70F7h	ICU	Interrupt request register 247	IR247	8	8	2 ICLK
0008 70F8h	ICU	Interrupt request register 248	IR248	8	8	2 ICLK
0008 70F9h	ICU	Interrupt request register 249	IR249	8	8	2 ICLK
0008 70FEh	ICU	Interrupt request register 254	IR254	8	8	2 ICLK
0008 711Bh	ICU	DTC activation enable register 027	DTCER027	8	8	2 ICLK
0008 711Ch	ICU	DTC activation enable register 028	DTCER028	8	8	2 ICLK
0008 711Dh	ICU	DTC activation enable register 029	DTCER029	8	8	2 ICLK
0008 711Eh	ICU	DTC activation enable register 030	DTCER030	8	8	2 ICLK
0008 711Fh	ICU	DTC activation enable register 031	DTCER031	8	8	2 ICLK
0008 712Dh	ICU	DTC activation enable register 045	DTCER045	8	8	2 ICLK
0008 712Eh	ICU	DTC activation enable register 046	DTCER046	8	8	2 ICLK
0008 7140h	ICU	DTC activation enable register 064	DTCER064	8	8	2 ICLK
0008 7141h	ICU	DTC activation enable register 065	DTCER065	8	8	2 ICLK
0008 7142h	ICU	DTC activation enable register 066	DTCER066	8	8	2 ICLK
0008 7143h	ICU	DTC activation enable register 067	DTCER067	8	8	2 ICLK
0008 7144h	ICU	DTC activation enable register 068	DTCER068	8	8	2 ICLK
0008 7145h	ICU	DTC activation enable register 069	DTCER069	8	8	2 ICLK
0008 7146h	ICU	DTC activation enable register 070	DTCER070	8	8	2 ICLK
0008 7147h	ICU	DTC activation enable register 071	DTCER071	8	8	2 ICLK
0008 7162h	ICU	DTC activation enable register 098	DTCER098	8	8	2 ICLK
0008 7166h	ICU	DTC activation enable register 102	DTCER102	8	8	2 ICLK
0008 7167h	ICU	DTC activation enable register 103	DTCER103	8	8	2 ICLK
0008 716Ah	ICU	DTC activation enable register 106	DTCER106	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (16 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0009 4019h	LIN0	Data 2 buffer register	L0DB2	8	8, 16, 32	2, 3 PCLK* ³
0009 401Ah	LIN0	Data 3 buffer register	L0DB3	8	8, 16, 32	2, 3 PCLK* ³
0009 401Bh	LIN0	Data 4 buffer register	L0DB4	8	8, 16, 32	2, 3 PCLK* ³
0009 401Ch	LIN0	Data 5 buffer register	L0DB5	8	8, 16, 32	2, 3 PCLK* ³
0009 401Dh	LIN0	Data 6 buffer register	L0DB6	8	8, 16, 32	2, 3 PCLK* ³
0009 401Eh	LIN0	Data 7 buffer register	L0DB7	8	8, 16, 32	2, 3 PCLK* ³
0009 401Fh	LIN0	Data 8 buffer register	L0DB8	8	8, 16, 32	2, 3 PCLK* ³
000C 1200h	MTU3	Timer control register	TCR	8	8, 16, 32	5 ICLK
000C 1201h	MTU4	Timer control register	TCR	8	8	5 ICLK
000C 1202h	MTU3	Timer mode register 1	TMDR1	8	8, 16	5 ICLK
000C 1203h	MTU4	Timer mode register 1	TMDR1	8	8	5 ICLK
000C 1204h	MTU3	Timer I/O control register H	TIORH	8	8, 16, 32	5 ICLK
000C 1205h	MTU3	Timer I/O control register L	TIORL	8	8	5 ICLK
000C 1206h	MTU4	Timer I/O control register H	TIORH	8	8, 16	5 ICLK
000C 1207h	MTU4	Timer I/O control register L	TIORL	8	8	5 ICLK
000C 1208h	MTU3	Timer interrupt enable register	TIER	8	8, 16	5 ICLK
000C 1209h	MTU4	Timer interrupt enable register	TIER	8	8	5 ICLK
000C 120Ah	MTU	Timer output master enable register A	TOERA	8	8	5 ICLK
000C 120Dh	MTU	Timer gate control register A	TGCRA	8	8	5 ICLK
000C 120Eh	MTU	Timer output control register 1A	TOCR1A	8	8, 16	5 ICLK
000C 120Fh	MTU	Timer output control register 2A	TOCR2A	8	8	5 ICLK
000C 1210h	MTU3	Timer counter	TCNT	16	16, 32	5 ICLK
000C 1212h	MTU4	Timer counter	TCNT	16	16	5 ICLK
000C 1214h	MTU	Timer cycle data register A	TCDRA	16	16, 32	5 ICLK
000C 1216h	MTU	Timer dead time data register A	TDDRA	16	16	5 ICLK
000C 1218h	MTU3	Timer general register A	TGRA	16	16, 32	5 ICLK
000C 121Ah	MTU3	Timer general register B	TGRB	16	16	5 ICLK
000C 121Ch	MTU4	Timer general register A	TGRA	16	16, 32	5 ICLK
000C 121Eh	MTU4	Timer general register B	TGRB	16	16	5 ICLK
000C 1220h	MTU	Timer subcounter A	TCNTSA	16	16, 32	5 ICLK
000C 1222h	MTU	Timer cycle buffer register A	TCBRA	16	16	5 ICLK
000C 1224h	MTU3	Timer general register C	TGRC	16	16, 32	5 ICLK
000C 1226h	MTU3	Timer general register D	TGRD	16	16	5 ICLK
000C 1228h	MTU4	Timer general register C	TGRC	16	16, 32	5 ICLK
000C 122Ah	MTU4	Timer general register D	TGRD	16	16	5 ICLK
000C 122Ch	MTU3	Timer status register	TSR	8	8, 16	5 ICLK
000C 122Dh	MTU4	Timer status register	TSR	8	8	5 ICLK
000C 1230h	MTU	Timer interrupt skipping set register 1A	TITCR1A	8	8, 16	5 ICLK
000C 1231h	MTU	Timer interrupt skipping counter 1A	TITCNT1A	8	8	5 ICLK
000C 1232h	MTU	Timer buffer transfer set register A	TBTERA	8	8	5 ICLK
000C 1234h	MTU	Timer dead time enable register A	TDERA	8	8	5 ICLK
000C 1236h	MTU	Timer output level buffer register A	TOLBRA	8	8	5 ICLK
000C 1238h	MTU3	Timer buffer operation transfer mode register	TBTM	8	8, 16	5 ICLK
000C 1239h	MTU4	Timer buffer operation transfer mode register	TBTM	8	8	5 ICLK

Table 4.1 List of I/O Registers (Address Order) (21 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000C 2116h	GPT0	General PWM timer compare capture register D	GTCCRD	16	16, 32	3 to 5 ICLK ^{*4}
000C 2118h	GPT0	General PWM timer compare capture register E	GTCCRE	16	16, 32	3 to 5 ICLK ^{*4}
000C 211Ah	GPT0	General PWM timer compare capture register F	GTCCRF	16	16, 32	3 to 5 ICLK ^{*4}
000C 211Ch	GPT0	General PWM timer cycle setting register	GTPR	16	16, 32	3 to 5 ICLK ^{*4}
000C 211Eh	GPT0	General PWM timer cycle setting buffer register	GTPBR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2120h	GPT0	General PWM timer cycle setting double-buffer register	GTPDBR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2124h	GPT0	A/D converter start request timing register A	GTADTRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 2126h	GPT0	A/D converter start request timing buffer register A	GTADTBRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 2128h	GPT0	A/D converter start request timing double-buffer register A	GTADTBRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 212Ch	GPT0	A/D converter start request timing register B	GTADTRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 212Eh	GPT0	A/D converter start request timing buffer register B	GTADTRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2130h	GPT0	A/D converter start request timing double-buffer register B	GTADTRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2134h	GPT0	General PWM timer output negate control register	GTONCR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2136h	GPT0	General PWM timer dead time control register	GTDTCR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2138h	GPT0	General PWM timer dead time value register	GTDVU	16	16, 32	3 to 5 ICLK ^{*4}
000C 213Ah	GPT0	General PWM timer dead time value register	GTDVD	16	16, 32	3 to 5 ICLK ^{*4}
000C 213Ch	GPT0	General PWM timer dead time buffer register	GTDBU	16	16, 32	3 to 5 ICLK ^{*4}
000C 213Eh	GPT0	General PWM timer dead time buffer register	GTDBD	16	16, 32	3 to 5 ICLK ^{*4}
000C 2140h	GPT0	General PWM timer output protection function status register	GTSOS	16	16, 32	3 to 5 ICLK ^{*4}
000C 2142h	GPT0	General PWM timer output protection function temporary release register	GTSOTR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2180h	GPT1	General PWM timer I/O control register	GTIOR	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2182h	GPT1	General PWM timer interrupt output setting register	GTINTAD	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2184h	GPT1	General PWM timer control register	GTCR	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2186h	GPT1	General PWM timer buffer enable register	GTBER	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2188h	GPT1	General PWM timer count direction register	GTUDC	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 218Ah	GPT1	General PWM timer interrupt and A/D converter start request skipping setting register	GTITC	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 218Ch	GPT1	General PWM timer status register	GTST	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 218Eh	GPT1	General PWM timer counter	GTCNT	16	16	3 to 5 ICLK ^{*4}
000C 2190h	GPT1	General PWM timer compare capture register A	GTCCRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 2192h	GPT1	General PWM timer compare capture register B	GTCCRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2194h	GPT1	General PWM timer compare capture register C	GTCCRC	16	16, 32	3 to 5 ICLK ^{*4}
000C 2196h	GPT1	General PWM timer compare capture register D	GTCCRD	16	16, 32	3 to 5 ICLK ^{*4}
000C 2198h	GPT1	General PWM timer compare capture register E	GTCCRE	16	16, 32	3 to 5 ICLK ^{*4}
000C 219Ah	GPT1	General PWM timer compare capture register F	GTCCRF	16	16, 32	3 to 5 ICLK ^{*4}
000C 219Ch	GPT1	General PWM timer cycle setting register	GTPR	16	16, 32	3 to 5 ICLK ^{*4}
000C 219Eh	GPT1	General PWM timer cycle setting buffer register	GTPBR	16	16, 32	3 to 5 ICLK ^{*4}

Table 4.1 List of I/O Registers (Address Order) (23 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000C 222Ch	GPT2	A/D converter start request timing register B	GTADTRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 222Eh	GPT2	A/D converter start request timing buffer register B	GTADTBRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2230h	GPT2	A/D converter start request timing double-buffer register B	GTADTDBRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2234h	GPT2	General PWM timer output negate control register	GTONCR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2236h	GPT2	General PWM timer dead time control register	GTDTCR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2238h	GPT2	General PWM timer dead time value register	GTDVU	16	16, 32	3 to 5 ICLK ^{*4}
000C 223Ah	GPT2	General PWM timer dead time value register	GTDVD	16	16, 32	3 to 5 ICLK ^{*4}
000C 223Ch	GPT2	General PWM timer dead time buffer register	GTDBU	16	16, 32	3 to 5 ICLK ^{*4}
000C 223Eh	GPT2	General PWM timer dead time buffer register	GTDBD	16	16, 32	3 to 5 ICLK ^{*4}
000C 2240h	GPT2	General PWM timer output protection function status register	GTSOS	16	16, 32	3 to 5 ICLK ^{*4}
000C 2242h	GPT2	General PWM timer output protection temporary release register	GTSOTR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2280h	GPT3	General PWM timer I/O control register	GTIOR	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2282h	GPT3	General PWM timer interrupt output setting register	GTINTAD	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2284h	GPT3	General PWM timer control register	GTCR	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2286h	GPT3	General PWM timer buffer enable register	GTBER	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2288h	GPT3	General PWM timer count direction register	GTUDC	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 228Ah	GPT3	General PWM timer interrupt and A/D converter start request skipping setting register	GTITC	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 228Ch	GPT3	General PWM timer status register	GTST	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 228Eh	GPT3	General PWM timer counter	GTCNT	16	16	3 to 5 ICLK ^{*4}
000C 2290h	GPT3	General PWM timer compare capture register A	GTCCRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 2292h	GPT3	General PWM timer compare capture register B	GTCCRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2294h	GPT3	General PWM timer compare capture register C	GTCCRC	16	16, 32	3 to 5 ICLK ^{*4}
000C 2296h	GPT3	General PWM timer compare capture register D	GTCCRD	16	16, 32	3 to 5 ICLK ^{*4}
000C 2298h	GPT3	General PWM timer compare capture register E	GTCCRE	16	16, 32	3 to 5 ICLK ^{*4}
000C 229Ah	GPT3	General PWM timer compare capture register F	GTCCRF	16	16, 32	3 to 5 ICLK ^{*4}
000C 229Ch	GPT3	General PWM timer cycle setting register	GTPR	16	16, 32	3 to 5 ICLK ^{*4}
000C 229Eh	GPT3	General PWM timer cycle setting buffer register	GTPBR	16	16, 32	3 to 5 ICLK ^{*4}
000C 22A0h	GPT3	General PWM timer cycle setting double-buffer register	GTPDBR	16	16, 32	3 to 5 ICLK ^{*4}
000C 22A4h	GPT3	A/D converter start request timing register A	GTADTRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 22A6h	GPT3	A/D converter start request timing buffer register A	GTADTBRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 22A8h	GPT3	A/D converter start request timing double-buffer register A	GTADTDBRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 22ACh	GPT3	A/D converter start request timing register B	GTADTRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 22AEh	GPT3	A/D converter start request timing buffer register B	GTADTBRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 22B0h	GPT3	A/D converter start request timing double-buffer register B	GTADTDBRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 22B4h	GPT3	General PWM timer output negate control register	GTONCR	16	16, 32	3 to 5 ICLK ^{*4}

Table 4.2 **List of I/O Registers (Bit Order) (9 / 30)**

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
ICU	IRQCR0	—	—	—	—		IRQMD[1:0]	—	—
ICU	IRQCR1	—	—	—	—		IRQMD[1:0]	—	—
ICU	IRQCR2	—	—	—	—		IRQMD[1:0]	—	—
ICU	IRQCR3	—	—	—	—		IRQMD[1:0]	—	—
ICU	IRQCR4	—	—	—	—		IRQMD[1:0]	—	—
ICU	IRQCR5	—	—	—	—		IRQMD[1:0]	—	—
ICU	IRQCR6	—	—	—	—		IRQMD[1:0]	—	—
ICU	IRQCR7	—	—	—	—		IRQMD[1:0]	—	—
ICU	NMISR	—	—	—	—	—	OSTST	LV DST	NMIST
ICU	NMIER	—	—	—	—	—	OSTEN	LV DEN	NMIEN
ICU	NMICLR	—	—	—	—	—	OSTCLR	—	NMICLR
ICU	NMICR	—	—	—	—	NMIMD	—	—	—
CMT	CMSTR0	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	STR1	STR0
CMT0	CMCR	—	—	—	—	—	—	—	—
		—	CMIE	—	—	—	—	CKS[1:0]	
CMT0	CMCNT								
CMT0	CMCOR								
CMT1	CMCR	—	—	—	—	—	—	—	—
		—	CMIE	—	—	—	—	CKS[1:0]	
CMT1	CMCNT								
CMT1	CMCOR								
CMT	CMSTR1	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	STR3	STR2
CMT2	CMCR	—	—	—	—	—	—	—	—
		—	CMIE	—	—	—	—	CKS[1:0]	
CMT2	CMCNT								
CMT2	CMCOR								
CMT3	CMCR	—	—	—	—	—	—	—	—
		—	CMIE	—	—	—	—	CKS[1:0]	
CMT3	CMCNT								
CMT3	CMCOR								
WDT	TCSR	—	TMS	TME	—	—		CKS[2:0]	
WDT	WINA								
WDT	TCNT								
WDT	WINB								
WDT	RSTCSR	WOVF	RSTE	—	—	—	—	—	—
IWD	IWDTCR	—	—	—	—	—	—	—	—
			CKS[3:0]			—	—	TOPS[1:0]	
IWD	IWDTSR	—	UNDF			CNTVAL[13:0]			
						CNTVAL[13:0]			
AD0	ADDR ^{A1}	—	—	—	—	—	—		

Table 4.2 List of I/O Registers (Bit Order) (28 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
GPT3	GTCCRB								
GPT3	GTCCRC								
GPT3	GTCCRD								
GPT3	GTCCRE								
GPT3	GTCCRF								
GPT3	GTPR								
GPT3	GTPBR								
GPT3	GTPDBR								
GPT3	GTADTRA								
GPT3	GTADTBRA								
GPT3	GTADTDBRA								
GPT3	GTADTRB								
GPT3	GTADTBRB								
GPT3	GTADTDBRB								
GPT3	GTONCR	OBE	OAE	—	SWN	—	—	—	NFV
		NFS[3:0]				NVB	NVA	NEB	NEA
GPT3	GTDTCR	—	—	—	—	—	—	—	TDFER
		—	—	TDBDE	TDBUE	—	—	—	TDE
GPT3	GTDVU								
GPT3	GTDVD								
GPT3	GTDBU								
GPT3	GTDBD	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	SOS[1:0]	—
GPT3	GTSOS	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	SOS[1:0]	—
GPT3	GTSOTR	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	SOTR
GPT0	GTDLYCR	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLYEN	DLYRST	DLLEN
GPT1	GTDLYCR	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLYEN	DLYRST	DLLEN

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Item		Symbol	Value	Unit
Power supply voltage		VCC PLLVCC	-0.3 to +6.5	V
Input voltage (except for ports 4 to 6)		V _{IN}	-0.3 to VCC+0.3	V
Input voltage (port 4)		V _{IN}	-0.3 to AVCC0+0.3	V
Input voltage (ports 5 and 6)		V _{IN}	-0.3 to AVCC+0.3	V
Analog power supply voltage		AVCC0, AVCC*1	-0.3 to +6.5	V
Reference power supply voltage		VREFH0*1	-0.3 to AVCC0+0.3	V
		VREF*1	-0.3 to AVCC+0.3	
Analog input voltage (port 4)		V _{AN}	-0.3 to AVCC0+0.3	V
Analog input voltage (ports 5 and 6)		V _{AN}	-0.3 to AVCC+0.3	V
Operating temperature	D version	T _{opr}	-40 to +85	°C
	G version	T _{opr}	-40 to +105	°C
Storage temperature		T _{stg}	-55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. Do not leave the AVCC0, VREFH0, VREFL0, AVSS0, AVCC, VREF, and AVSS pins open circuit even if the A/D converter is not to be used.

- When the 12-bit converter is not in use:
Connect the AVCC0 pin to AVCC (or VCC for a 64-pin product), the VREFH0 pin to VREF (or AVCC or VCC for an 80- or 64-pin product, respectively), and the AVSS0 and VREFL0 pins to VSS.
- When the 10-bit converter is not in use:
Connect the AVCC pin to AVCC0, the VREF pin to VREFH0, and the AVSS pin to AVSS0.
- When neither the 10- nor the 12-bit converter is in use:
Connect the AVCC0, VREFH0, AVCC, and VREF pins to VCC, and the AVSS0, VREFL0, and AVSS pins to VSS.

5.2 DC Characteristics

Table 5.2 DC Characteristics (1) (1 / 3)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	CAN input pin IRQ input pin MTU3 input pin POE3 input pin SCI input pin A/D trigger input pin NMI input pin GPT input pin LIN input pin RES#	V _{IH}	VCC×0.8	-	VCC+0.3	V	
		V _{IL}	-0.3	-	VCC×0.2		
		ΔV _T	VCC ×0.06	-	-		
	RIIC input pin (IICBus)	V _{IH}	VCC×0.7	-	VCC+0.3		
		V _{IL}	-0.3	-	VCC×0.3		
		ΔV _T	VCC ×0.05	-	-		
	Port 4*1 (also usable as an analog port)	V _{IH}	AVCC0 ×0.8	-	AVCC0 +0.3		
		V _{IL}	- 0.3	-	AVCC0 ×0.2		
		ΔV _T	AVCC0 ×0.06	-	-		
	Ports 5 and 6*1 (also usable as analog ports)	V _{IH}	AVCC ×0.8	-	AVCC +0.3		
		V _{IL}	-0.3	-	AVCC ×0.2		
		ΔV _T	AVCC ×0.06	-	-		
	Ports 1 to 3*1 Ports 7 to B*1 Ports D, E, and G*1	V _{IH}	VCC×0.8	-	VCC+0.3		
		V _{IL}	-0.3	-	VCC×0.2		
		ΔV _T	VCC ×0.06	-	-		
Input high voltage (except Schmitt trigger input pin)	MD pin, EMLE	V _{IH}	VCC×0.9	-	VCC+0.3	V	Conditions 1 and 2
	EXTAL RSPI input pin		VCC×0.8		VCC+0.3		
	RIIC input pin (SMBus)		2.1		VCC+0.3		
Input low voltage (except Schmitt trigger input pin)	MD pin, EMLE	V _{IL}	-0.3	-	VCC×0.1	V	Conditions 1 and 2
	EXTAL RSPI input pin		-0.3	-	VCC×0.2		
	RIIC input pin (SMBus)		-0.3	-	0.8		

Table 5.18 Comparator Characteristics

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Ta = Topr. Ta is the same under conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog input capacitance	Cin	-	-	6	pF	
REFH pin offset voltage	Voff	-	-	5	mV	
REFL pin offset voltage		-	-	5	mV	
REFH input voltage range	Vin	1.7	-	AVcc – 0.3	V	
REFL input voltage range		0.3	-	AVcc – 1.7	V	
REFH reply time	tCR	-	-	1	μs	
REFL reply time	tCF	-	-	1	μs	

5.5 Power-on Reset Circuit, Voltage Detection Circuit Characteristics

Table 5.19 Power-on Reset Circuit, Voltage Detection Circuit Characteristics

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

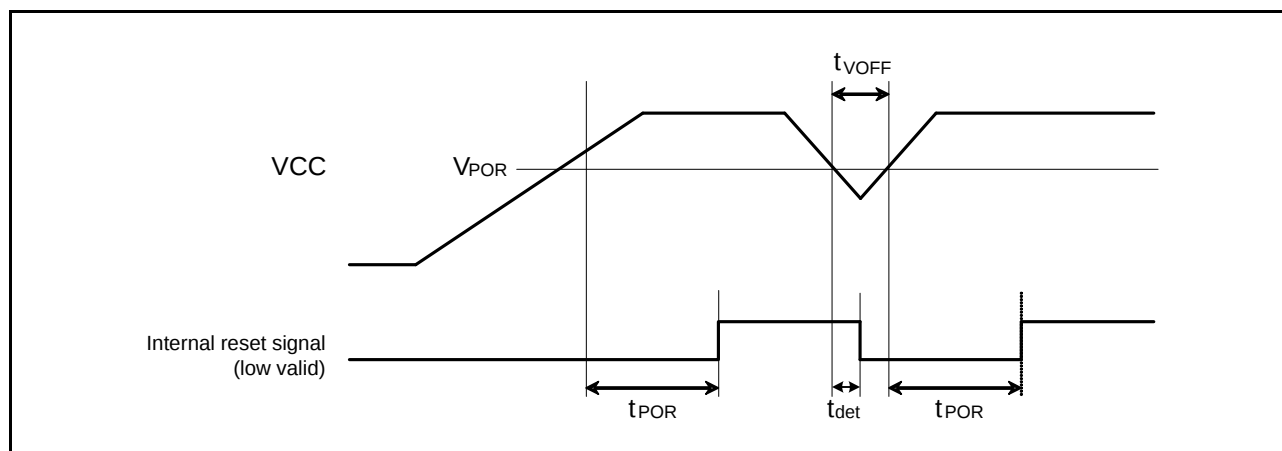
Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 and 2.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V _{POR}	2.48	2.60	2.72	V	Figure 5.20
	Voltage detection circuit (LVD)	V _{det1}	2.68	2.80	2.92		Figure 5.21
		V _{det2}	2.98	3.10	3.22		Figure 5.22
Internal reset time		t _{POR}	20	35	50	ms	Figure 5.21 and Figure 5.22
Min. VCC down time ^{*1}		t _{VOFF}	200	-	-	us	Figure 5.20 to Figure 5.22
Reply delay time		t _{det}	-	-	200	us	

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V _{POR}	3.70	3.90	4.10	V	Figure 5.20
	Voltage detection circuit (LVD)	V _{det1}	3.95	4.15	4.35		Figure 5.21
		V _{det2}	4.40	4.60	4.80		Figure 5.22
Internal reset time		t _{POR}	20	35	50	ms	Figure 5.21 and Figure 5.22
Min. VCC down time*1		t _{VOFF}	200	-	-	us	Figure 5.20 to Figure 5.22
Reply delay time		t _{det}	-	-	200	us	

Note 1. The power-off time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det1}, and V_{det2} for the POR/ LVD.


Figure 5.20 Power-on Reset Timing

Appendix 1. Package Dimensions

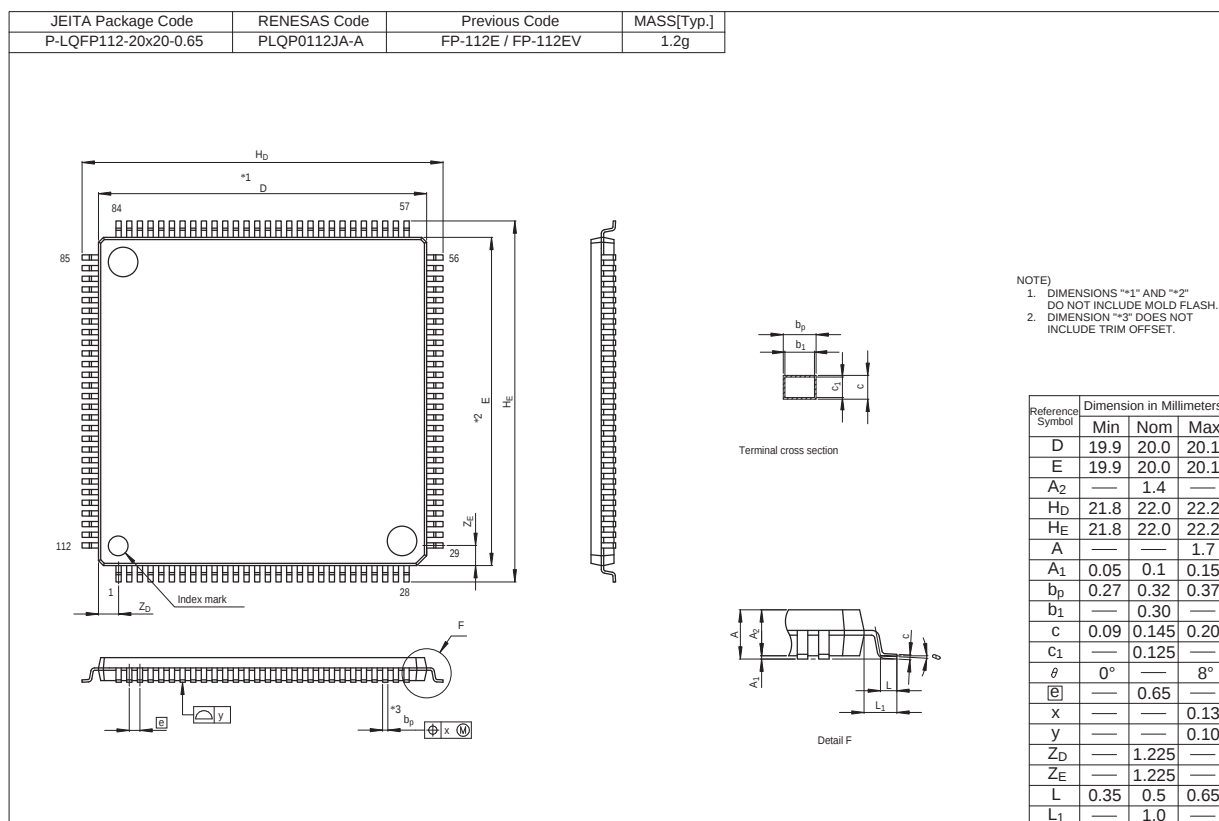


Figure A 112-Pin LQFP (PLQP0112JA-A) Package Dimensions