Renesas Electronics America Inc - R5F562T6EDFK#V1 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562t6edfk-v1

Table 1.1 Outline of Specifications (2 / 5)

Classification	Module/Function	Description
Interrupt	Interrupt controller (ICU)	• Peripheral function interrupts: 101 sources • External interrupts: 9 (NMI and IRQ0 to IRQ7 pins) • Non-maskable interrupts: 3 (the NMI pin, oscillation stop detection interrupt, and voltage-monitoring interrupt) • 16 levels specifiable for the order of priority
Data transfer	Data transfer controller (DTC)	• Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
I/O ports	Programmable I/O ports	I/O port pins for devices in the 112-pin LQFP/100-pin LQFP/ 80-pin LQFP (R5F562TxGDFF)/80-pin LQFP (except R5F562TxGDFF)/64-pin LQFP • I/O: 61/55/44/44/37 • Input only: 21/21/13/13/9 • Open-drain outputs: 2/2/2/2/2 (I^2C bus interface pins) • Large-current outputs: 12/12/12/6/6(0) (MTU3 and GPT pins) The 5-V version of the 64-pin product does not have large-current outputs. • Reading out the states of pins is always possible.
Timers	Multi-function timer pulse unit 3 (MTU3)	• 16 bits x 8 channels • Up to 24 pulse inputs/outputs and three pulse inputs • Select from among six to eight counter-input clock signals for each channel (ICLK/1, ICLK/4, ICLK/16, ICLK/64, ICLK/256, ICLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available. • 24 output compare or input capture registers • Counter clearing (clearing is synchronizable with compare match or input capture) • Simultaneous writing to multiple timer counters (TCNT) • Input to and output from all registers in synchronization with counter operation • Buffered operation • Cascade-connected operation • 38 kinds of interrupt source • Automatic transfer of register data • Pulse output modes Toggled, PWM, complementary PWM, and reset synchronous PWM • Complementary PWM output mode Outputs non-overlapping waveforms for controlling 3-phase inverters Automatic specification of dead times PWM duty cycle: Selectable as any value from 0% to 100% Delay can be applied to requests for A/D conversion. Non-generation of interrupt requests at peak or trough values of counters can be selected. Double buffering • Reset-synchronous PWM mode Three PWM waveforms and corresponding inverse waveforms are output with the desired duty cycles. • Phase-counting mode • Counter functionality for dead-time compensation • Generation of triggers for A/D converters • Differential timing for initiation of A/D conversion
	Port output enable 3 (POE3)	• Control of the high-impedance state of the MTU3 and GPT's waveform output pins 5 pins for input from signal sources: POE0, POE4, POE8, POE10, POE11 Initiation on detection of short-circuited outputs (detection of simultaneous switching of large-current pins to the active level) Initiation by comparator-detection of analog level input to the 12-bit A/D converter Initiation by oscillation-stoppage detection Initiation by software • Selection of which output pins should be placed in the high-impedance state at the time of each POE input or comparator detection

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no.

Table 1.3 List of Products (1 / 2)

Group	Part No.	Order Part No.	Package	ROM Capacity	RAM Capacity	Data Flash Capacity	Power Supply Voltage	CAN	Operating Temp. Range
RX62T	R5F562TAADFH	R5F562TAADFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes	VCC/PLLVCC 4.0 to 5.5 V AVCC/AVCC0 4.0 to 5.5 V	Support-ed	-40 to +85°C (D version)
	R5F562TAADFP	R5F562TAADFP#V3	PLQP0100KB-A						
	R5F562TAADFF	R5F562TAADFF#V3	PLQP0080JA-A						
	R5F562TAGDFF	R5F562TAGDFF#V3	PLQP0080JA-A						
	R5F562TAADFM	R5F562TAADFM#V3	PLQP0064KB-A						
	R5F562TAADFK	R5F562TAADFK#V3	PLQP0064GA-A						
	R5F562T7ADFH	R5F562T7ADFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes			
	R5F562T7ADFP	R5F562T7ADFP#V3	PLQP0100KB-A						
	R5F562T7ADFF	R5F562T7ADFF#V3	PLQP0080JA-A						
	R5F562T7GDFF	R5F562T7GDFF#V3	PLQP0080JA-A						
	R5F562T7ADFM	R5F562T7ADFM#V3	PLQP0064KB-A						
	R5F562T7ADFK	R5F562T7ADFK#V3	PLQP0064GA-A						
	R5F562T6ADFF	R5F562T6ADFF#V3	PLQP0080JA-A	64 Kbytes	8 Kbytes				
	R5F562T6ADFM	R5F562T6ADFM#V3	PLQP0064KB-A						
	R5F562T6ADFK	R5F562T6ADFK#V3	PLQP0064GA-A						
	R5F562TABDFH	R5F562TABDFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes	VCC/PLLVCC 2.7 to 3.6 V AVCC/AVCC0 3.0 to 3.6 V or 4.0 to 5.5 V		
	R5F562TABDFP	R5F562TABDFP#V3	PLQP0100KB-A						
	R5F562TABDFF	R5F562TABDFF#V3	PLQP0080JA-A						
	R5F562TABDFM	R5F562TABDFM#V3	PLQP0064KB-A						
	R5F562TABDFK	R5F562TABDFK#V3	PLQP0064GA-A						
	R5F562T7BDFH	R5F562T7BDFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes			
	R5F562T7BDFP	R5F562T7BDFP#V3	PLQP0100KB-A						
	R5F562T7BDFF	R5F562T7BDFF#V3	PLQP0080JA-A						
	R5F562T7BDFM	R5F562T7BDFM#V3	PLQP0064KB-A						
	R5F562T7BDFK	R5F562T7BDFK#V3	PLQP0064GA-A						
	R5F562T6BDFF	R5F562T6BDFF#V3	PLQP0080JA-A	64 Kbytes	8 Kbytes				
	R5F562T6BDFM	R5F562T6BDFM#V3	PLQP0064KB-A						
	R5F562T6BDFK	R5F562T6BDFK#V3	PLQP0064GA-A						
	R5F562TADDFH	R5F562TADDFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes	4.0 to 5.5 V	Not Support-ed	
	R5F562TADDFP	R5F562TADDFP#V3	PLQP0100KB-A						
	R5F562TADDFF	R5F562TADDFF#V3	PLQP0080JA-A						
	R5F562TADDFM	R5F562TADDFM#V3	PLQP0064KB-A						
	R5F562TADDFK	R5F562TADDFK#V3	PLQP0064GA-A						
	R5F562T7DDFH	R5F562T7DDFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes			
	R5F562T7DDFP	R5F562T7DDFP#V3	PLQP0100KB-A						
	R5F562T7DDFF	R5F562T7DDFF#V3	PLQP0080JA-A						
	R5F562T7DDFM	R5F562T7DDFM#V3	PLQP0064KB-A						
	R5F562T7DDFK	R5F562T7DDFK#V3	PLQP0064GA-A						
	R5F562T6DDFF	R5F562T6DDFF#V3	PLQP0080JA-A	64 Kbytes	8 Kbytes				
	R5F562T6DDFM	R5F562T6DDFM#V3	PLQP0064KB-A						
	R5F562T6DDFK	R5F562T6DDFK#V3	PLQP0064GA-A						
	R5F562TAEDFH	R5F562TAEDFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes	2.7 to 3.6 V		
	R5F562TAEDFP	R5F562TAEDFP#V3	PLQP0100KB-A						
	R5F562TAEDFF	R5F562TAEDFF#V3	PLQP0080JA-A						
	R5F562TAEDFM	R5F562TAEDFM#V3	PLQP0064KB-A						
	R5F562TAEDFK	R5F562TAEDFK#V3	PLQP0064GA-A						

Table 1.3 List of Products (2 / 2)

Group	Part No.	Order Part No.	Package	ROM Capacity	RAM Capacity	Data Flash Capacity	Power Supply Voltage	CAN	Operating Temp. Range
RX62T	R5F562T7EDFH	R5F562T7EDFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes	2.7 to 3.6 V	Not Support-ed	-40 to +85°C (D version)
	R5F562T7EDFP	R5F562T7EDFP#V3	PLQP0100KB-A						
	R5F562T7EDFF	R5F562T7EDFF#V3	PLQP0080JA-A						
	R5F562T7EDFM	R5F562T7EDFM#V3	PLQP0064KB-A						
	R5F562T7EDFK	R5F562T7EDFK#V3	PLQP0064GA-A						
	R5F562T6EDFF	R5F562T6EDFF#V3	PLQP0080JA-A	64 Kbytes	8 Kbytes				
	R5F562T6EDFM	R5F562T6EDFM#V3	PLQP0064KB-A						
	R5F562T6EDFK	R5F562T6EDFK#V3	PLQP0064GA-A						
	R5F562TAAGFH	R5F562TAAGFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes	VCC/PLLVCC 4.0 to 5.5 V AVCC/AVCC0 4.0 to 5.5 V	Support-ed	-40 to +105°C (G version) *1
	R5F562TAAGFP	R5F562TAAGFP#V3	PLQP0100KB-A						
	R5F562TAAGFF	R5F562TAAGFF#V3	PLQP0080JA-A						
	R5F562TAGGFF	R5F562TAGGFF#V3	PLQP0080JA-A						
	R5F562TAAGFM	R5F562TAAGFM#V3	PLQP0064KB-A						
	R5F562TAAGFK	R5F562TAAGFK#V3	PLQP0064GA-A						
	R5F562T7AGFH	R5F562T7AGFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes			
	R5F562T7AGFP	R5F562T7AGFP#V3	PLQP0100KB-A						
	R5F562T7AGFF	R5F562T7AGFF#V3	PLQP0080JA-A						
	R5F562T7GGFF	R5F562T7GGFF#V3	PLQP0080JA-A						
	R5F562T7AGFM	R5F562T7AGFM#V3	PLQP0064KB-A						
	R5F562T7AGFK	R5F562T7AGFK#V3	PLQP0064GA-A						
	R5F562T6AGFF	R5F562T6AGFF#V3	PLQP0080JA-A	64 Kbytes	8 Kbytes				
	R5F562T6AGFM	R5F562T6AGFM#V3	PLQP0064KB-A						
	R5F562T6AGFK	R5F562T6AGFK#V3	PLQP0064GA-A						
	R5F562TABGFH	R5F562TABGFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes	VCC/PLLVCC 2.7 to 3.6 V AVCC/AVCC0 3.0 to 3.6 V or 4.0 to 5.5 V		
	R5F562TABGFP	R5F562TABGFP#V3	PLQP0100KB-A						
	R5F562TABGFF	R5F562TABGFF#V3	PLQP0080JA-A						
	R5F562TABGFM	R5F562TABGFM#V3	PLQP0064KB-A						
	R5F562TABGFK	R5F562TABGFK#V3	PLQP0064GA-A						
	R5F562T7BGFH	R5F562T7BGFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes			
	R5F562T7BGFP	R5F562T7BGFP#V3	PLQP0100KB-A						
	R5F562T7BGFF	R5F562T7BGFF#V3	PLQP0080JA-A						
	R5F562T7BGFM	R5F562T7BGFM#V3	PLQP0064KB-A						
	R5F562T7BGFK	R5F562T7BGFK#V3	PLQP0064GA-A						
	R5F562T6BGFF	R5F562T6BGFF#V3	PLQP0080JA-A	64 Kbytes	8 Kbytes				
	R5F562T6BGFM	R5F562T6BGFM#V3	PLQP0064KB-A						
	R5F562T6BGFK	R5F562T6BGFK#V3	PLQP0064GA-A						
RX62G	R5F562GAADFH	R5F562GAADFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes	VCC/PLLVCC 4.0 to 5.5 V AVCC/AVCC0 4.0 to 5.5 V	Support-ed	-40 to +85°C (D version)
	R5F562GAADFP	R5F562GAADFP#V3	PLQP0100KB-A						
	R5F562G7ADFH	R5F562G7ADFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes			
	R5F562G7ADFP	R5F562G7ADFP#V3	PLQP0100KB-A						
	R5F562GADDFH	R5F562GADDFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes		Not Support-ed	
	R5F562GADDFP	R5F562GADDFP#V3	PLQP0100KB-A						
	R5F562G7DDFH	R5F562G7DDFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes			
	R5F562G7DDFP	R5F562G7DDFP#V3	PLQP0100KB-A						
	R5F562GAAGFH	R5F562GAAGFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes	VCC/PLLVCC 4.0 to 5.5 V AVCC/AVCC0 4.0 to 5.5 V	Support-ed	-40 to +105°C (G versio) *1
	R5F562GAAGFP	R5F562GAAGFP#V3	PLQP0100KB-A						
	R5F562G7AGFH	R5F562G7AGFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes			
	R5F562G7AGFP	R5F562G7AGFP#V3	PLQP0100KB-A						

Note 1. Please contact us if you are using a G version.

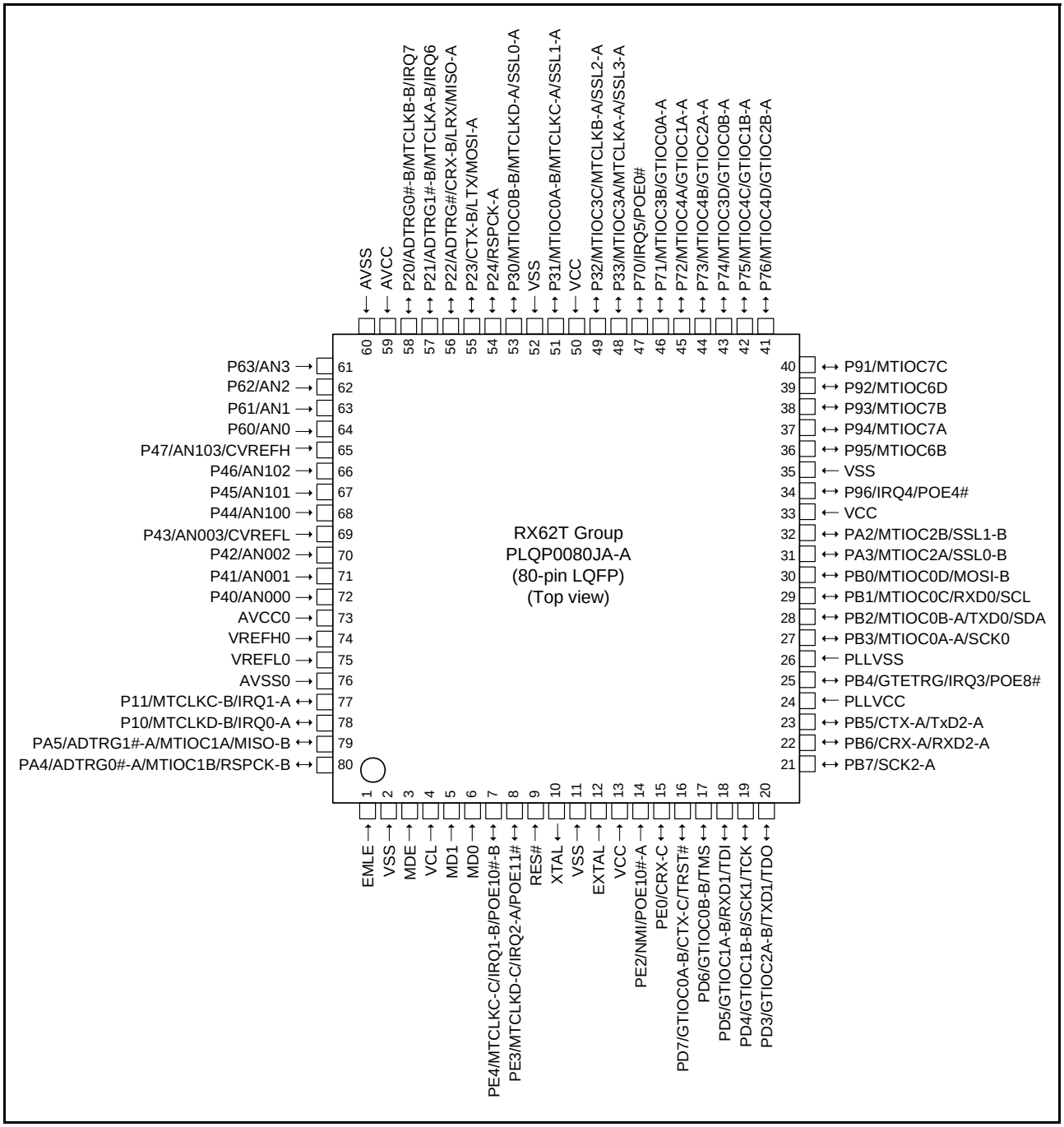

Figure 1.5 Pin Assignment of the 80-Pin LQFP

Table 1.4 List of Pins and Pin Functions (112-Pin LQFP) (1 / 3)

Pin No. (112-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi-cation	Interrupt	POE	Debugging
1		PE5				IRQ0-B		
2	EMLE							
3	VSS							
4	MDE							
5	VCL							
6	MD1							
7	MD0							
8		PE4		MTCLKC-C		IRQ1-B	POE10#-B	
9		PE3		MTCLKD-C		IRQ2-A	POE11#	
10	RES#							
11	XTAL							
12	VSS							
13	EXTAL							
14	VCC							
15		PE2				NMI	POE10#-A	
16		PE1			SSL3-C			
17		PE0			CRX-C/ SSL2-C			
18		PD7		GTIOC0A-B	CTX-C/ SSL1-C			
19		PD6		GTIOC0B-B	SSL0-C			
20		PD5		GTIOC1A-B	RXD1			
21		PD4		GTIOC1B-B	SCK1			
22		PD3		GTIOC2A-B	TXD1			
23		PD2		GTIOC2B-B	MOSI-C			
24		PD1		GTIOC3A	MISO-C			
25		PD0		GTIOC3B	RSPCK-C			
26								TDI
27								TCK
28								TDO
29		PB7			SCK2-A			
30		PB6			CRX-A/ RXD2-A			
31		PB5			CTX-A/ TXD2-A			
32	PLLVCC							
33		PB4		GTETRG		IRQ3	POE8#	
34	PLLVSS							
35		PB3		MTIOC0A-A	SCK0			
36		PB2		MTIOC0B-A	TXD0/SDA			
37		PB1		MTIOC0C	RXD0/SCL			
38		PB0		MTIOC0D	MOSI-B			
39		PA5	ADTRG1#-A	MTIOC1A	MISO-B			
40		PA4	ADTRG0#-A	MTIOC1B	RSPCK-B			
41		PA3		MTIOC2A	SSL0-B			
42		PA2		MTIOC2B	SSL1-B			
43		PA1		MTIOC6A	SSL2-B			

Table 1.7 List of Pins and Pin Functions (80-Pin LQFP: R5F562TxGDFF) (3 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communication	Interrupt	POE	Debugging
76	AVSS0							
77		P82		MTIC5U	SCK2-B			
78		P81		MTIC5V	TXD2-B			
79		P80		MTIC5W	RXD2-B			
80		P10		MTCLKD-B		IRQ0-A		

Table 1.9 Pin Functions (3 / 4)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCIb)	TXD0, TXD1, TXD2-A/TXD2-B	Output	Output pins for data transmission. The TXD2-B pin is not included in the 80-/64-pin versions.
	RXD0, RXD1, RXD2-A/ RXD2-B	Input	Input pins for data reception. The RXD2-B pin is not included in the 80-/64-pin versions.
	SCK0, SCK1, SCK2-A/ SCK2-B	I/O	Input/output pins for clock signals. The SCK2-B pin is not included in the 80-/64-pin versions.
I^2C bus interface (RIIC)	SCL	I/O	Input/output pin for I^2C bus interface clocks. Bus can be directly driven by the NMOS open drain output.
	SDA	I/O	Input/output pin for I^2C bus interface data. Bus can be directly driven by the NMOS open drain output.
CAN module (CAN) (as an optional function)	CRX-A/CRX-B/CRX-C	Input	Input pin for the CAN. The CRX-C pin is not included in the 64-pin version.
	CTX-A/CTX-B/CTX-C	Output	Output pin for the CAN. The CTX-C pin is not included in the 64-pin version.
LIN module (LIN)	LRX	Input	Input pin for the LIN.
	LTX	Output	Output pin for the LIN.
Serial peripheral interface (RSPI)	RSPCK-A/RSPCK-B/ RSPCK-C	I/O	Clock input/output pin for the RSPI. The RSPCK-C pin is not included in the 80-/64-pin versions.
	MOSI-A/MOSI-B/MOSI-C	I/O	Inputs or outputs data output from the master for the RSPI. The MOSI-C pin is not included in the 80-/64-pin versions.
	MISO-A/MISO-B/MISO-C	I/O	Inputs or outputs data output from the slave for the RSPI. The MISO-C pin is not included in the 80-/64-pin versions.
	SSL0-A/SSL0-B/SSL0-C	I/O	Select the slave for the RSPI. The SSL0-C/SSL1-C/SSL2-C/ SSL3-C pin is not included in the 80-/64-pin versions.
	SSL1-A/SSL1-B/SSL1-C SSL2-A/SSL2-B/SSL2-C SSL3-A/SSL3-B/SSL3-C	Output	
A/D converter	AN000 to AN003 AN100 to AN103	Input	Input pins for the analog signals to be processed by the 12-bit A/D converter.
	AN0 to AN11	Input	Input pins for the analog signals to be processed by the 10-bit A/D converter. The AN4 to AN11 pins are not included in the 80-pin version. Not included in the 64-pin version.
	ADTRG0#-A/ADTRG0#-B ADTRG1#-A/ADTRG1#-B ADTRG#	Input	Input pins for the external trigger signals that start the A/D conversion. The ADTRG0#-B/ADTRG1#-B/ADTRG# pin is not included in the 64-pin version.
	CVREFH	Input	Input pin for the high-level reference voltage to the comparator
	CVREFL	Input	Input pin for the low-level reference voltage to the comparator
Analog power supply	AVCC0	Input	Analog power supply pin for the 12-bit A/D converter. When the A/D converter is not in use, connect this pin to the system power supply.
	AVSS0	Input	Ground pin for the 12-bit A/D converter. Connect this pin to the system power supply (0 V).
	VREFH0	Input	Reference power supply pin for the 12-bit A/D converter. When the 12-bit A/D converter is not in use, connect this pin to the system power supply.
	VREFL0	Input	Ground pin of the reference power supply pin for the 12-bit A/D converter. When the 12-bit A/D converter is not in use, connect this pin to the system power supply (0 V).
	AVCC	Input	Analog power supply pin for the 10-bit A/D converter. When the A/D converter is not in use, connect this pin to the system power supply. Not included in the 64-pin version.
	AVSS	Input	Ground pin for the 10-bit A/D converter. Connect this pin to the system power supply (0 V). Not included in the 64-pin version.
	VREF	Input	Reference power supply pin for the 10-bit A/D converter. When the 10-bit A/D converter is not in use, connect this pin to the system power supply. Not included in the 80-/64-pin versions.

(a) Write to an I/O register.

(b) Read the value from the I/O register to a general register.

(c) Execute the operation using the value read.

(d) Execute the subsequent instruction.

[Instruction examples]

- Byte-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.B  #SFR_DATA, [R1]
CMP    [R1].UB, R1
;; Next process
```

- Word-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.W  #SFR_DATA, [R1]
CMP    [R1].W, R1
;; Next process
```

- Longword-size I/O registers

```
MOV.L  #SFR_ADDR, R1
MOV.L  #SFR_DATA, [R1]
CMP    [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

(4) Number of Access Cycles to I/O Registers

The number of access cycles to I/O registers is obtained by following equation.*

Number of access cycles to I/O registers = Number of bus cycles for internal main bus 1 +
Number of divided cycles for clock synchronization +
Number of bus cycles for internal peripheral buses 1, 2, 4, and 6

The number of bus cycles for internal peripheral buses 1, 2, 4, and 6 differs according to the register to be accessed. For the number of access cycles to each I/O register, see Table 4.1, List of I/O Registers.

When peripheral functions connected to internal peripheral bus 6 are accessed, the number of divided cycles for clock synchronization is added.

Although the number of divided cycles for clock synchronization differs depending on the number of frequency ratio between ICLK and PCLK or bus access timing, the sum of the number of bus cycles for internal main bus 1 and the number of divided cycles for clock synchronization will be one PCLK at a maximum. Therefore, one PCLK is added to the number of access cycles shown in Table 4.1.

Note: • This applies to the number of cycles when the access from the CPU does not conflict with the instruction fetching to the external memory or bus access from the different bus master (DTC).

Table 4.1 List of I/O Registers (Address Order) (11 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 8383h	RSPI	RSPI status register	SPSR	8	8	2, 3 PCLK*3
0008 8384h	RSPI	RSPI data register	SPDR	16, 32	16, 32	2, 3 PCLK*3
0008 8388h	RSPI	RSPI sequence control register	SPSCR	8	8	2, 3 PCLK*3
0008 8389h	RSPI	RSPI sequence status register	SPSSR	8	8	2, 3 PCLK*3
0008 838Ah	RSPI	RSPI bit rate register	SPBR	8	8	2, 3 PCLK*3
0008 838Bh	RSPI	RSPI data control register	SPDCR	8	8	2, 3 PCLK*3
0008 838Ch	RSPI	RSPI clock delay register	SPCKD	8	8	2, 3 PCLK*3
0008 838Dh	RSPI	RSPI slave select negation delay register	SSLND	8	8	2, 3 PCLK*3
0008 838Eh	RSPI	RSPI next-access delay register	SPND	8	8	2, 3 PCLK*3
0008 838Fh	RSPI	RSPI control register 2	SPCR2	8	8	2, 3 PCLK*3
0008 8390h	RSPI	RSPI command register 0	SPCMD0	16	16	2, 3 PCLK*3
0008 8392h	RSPI	RSPI command register 1	SPCMD1	16	16	2, 3 PCLK*3
0008 8394h	RSPI	RSPI command register 2	SPCMD2	16	16	2, 3 PCLK*3
0008 8396h	RSPI	RSPI command register 3	SPCMD3	16	16	2, 3 PCLK*3
0008 8398h	RSPI	RSPI command register 4	SPCMD4	16	16	2, 3 PCLK*3
0008 839Ah	RSPI	RSPI command register 5	SPCMD5	16	16	2, 3 PCLK*3
0008 839Ch	RSPI	RSPI command register 6	SPCMD6	16	16	2, 3 PCLK*3
0008 839Eh	RSPI	RSPI command register 7	SPCMD7	16	16	2, 3 PCLK*3
0008 9000h	S12AD0	A/D control register	ADCSR	8	8	2, 3 PCLK*3
0008 9004h	S12AD0	A/D channel select register	ADANS	16	16	2, 3 PCLK*3
0008 900Ah	S12AD0	A/D programmable gain amplifier register	ADPG	16	16	2, 3 PCLK*3
0008 900Eh	S12AD0	A/D control extended register	ADCER	16	16	2, 3 PCLK*3
0008 9010h	S12AD0	A/D start trigger select register	ADSTRGR	16	16	2, 3 PCLK*3
0008 9012h	S12AD	Comparator operating mode select register 0	ADCMPMD0	16	16	2, 3 PCLK*3
0008 9014h	S12AD	Comparator operating mode select register 1	ADCMPMD1	16	16	2, 3 PCLK*3
0008 9016h	S12AD	Comparator filter mode register 0	ADCMPNR0	16	16	2, 3 PCLK*3
0008 9018h	S12AD	Comparator filter mode register 1	ADCMPNR1	16	16	2, 3 PCLK*3
0008 901Ah	S12AD	Comparator detection flag register	ADCMPFR	8	8	2, 3 PCLK*3
0008 901Ch	S12AD	Comparator interrupt select register	ADCMPSEL	16	16	2, 3 PCLK*3
0008 901Eh	S12AD0	A/D data register Diag	ADRD	16	16	2, 3 PCLK*3
0008 9020h	S12AD0	A/D data register 0A	ADDR0A	16	16	2, 3 PCLK*3
0008 9022h	S12AD0	A/D data register 1	ADDR1	16	16	2, 3 PCLK*3
0008 9024h	S12AD0	A/D data register 2	ADDR2	16	16	2, 3 PCLK*3
0008 9026h	S12AD0	A/D data register 3	ADDR3	16	16	2, 3 PCLK*3
0008 9030h	S12AD0	A/D data register 0B	ADDR0B	16	16	2, 3 PCLK*3
0008 9060h	S12AD0	A/D sampling state register	ADSSTR	8	8	2, 3 PCLK*3
0008 9080h	S12AD1	A/D control register	ADCSR	8	8	2, 3 PCLK*3
0008 9084h	S12AD1	A/D channel select register	ADANS	16	16	2, 3 PCLK*3
0008 908Ah	S12AD1	A/D programmable gain amplifier register	ADPG	16	16	2, 3 PCLK*3
0008 908Eh	S12AD1	A/D control extended register	ADCER	16	16	2, 3 PCLK*3
0008 9090h	S12AD1	A/D start trigger select register	ADSTRGR	16	16	2, 3 PCLK*3
0008 909Eh	S12AD1	A/D data register Diag	ADRD	16	16	2, 3 PCLK*3
0008 90A0h	S12AD1	A/D data register 0A	ADDR0A	16	16	2, 3 PCLK*3
0008 90A2h	S12AD1	A/D data register 1	ADDR1	16	16	2, 3 PCLK*3

Table 4.1 List of I/O Registers (Address Order) (23 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000C 222Ch	GPT2	A/D converter start request timing register B	GTADTRB	16	16, 32	3 to 5 ICLK*4
000C 222Eh	GPT2	A/D converter start request timing buffer register B	GTADTBRB	16	16, 32	3 to 5 ICLK*4
000C 2230h	GPT2	A/D converter start request timing double-buffer register B	GTADTDBRB	16	16, 32	3 to 5 ICLK*4
000C 2234h	GPT2	General PWM timer output negate control register	GTONCR	16	16, 32	3 to 5 ICLK*4
000C 2236h	GPT2	General PWM timer dead time control register	GTDTCR	16	16, 32	3 to 5 ICLK*4
000C 2238h	GPT2	General PWM timer dead time value register	GTDVU	16	16, 32	3 to 5 ICLK*4
000C 223Ah	GPT2	General PWM timer dead time value register	GTDVD	16	16, 32	3 to 5 ICLK*4
000C 223Ch	GPT2	General PWM timer dead time buffer register	GTDBU	16	16, 32	3 to 5 ICLK*4
000C 223Eh	GPT2	General PWM timer dead time buffer register	GTDBD	16	16, 32	3 to 5 ICLK*4
000C 2240h	GPT2	General PWM timer output protection function status register	GTSOS	16	16, 32	3 to 5 ICLK*4
000C 2242h	GPT2	General PWM timer output protection temporary release register	GTSOTR	16	16, 32	3 to 5 ICLK*4
000C 2280h	GPT3	General PWM timer I/O control register	GTIOR	16	8, 16, 32	3 to 5 ICLK*4
000C 2282h	GPT3	General PWM timer interrupt output setting register	GTINTAD	16	8, 16, 32	3 to 5 ICLK*4
000C 2284h	GPT3	General PWM timer control register	GTCR	16	8, 16, 32	3 to 5 ICLK*4
000C 2286h	GPT3	General PWM timer buffer enable register	GTBER	16	8, 16, 32	3 to 5 ICLK*4
000C 2288h	GPT3	General PWM timer count direction register	GTUDC	16	8, 16, 32	3 to 5 ICLK*4
000C 228Ah	GPT3	General PWM timer interrupt and A/D converter start request skipping setting register	GTITC	16	8, 16, 32	3 to 5 ICLK*4
000C 228Ch	GPT3	General PWM timer status register	GTST	16	8, 16, 32	3 to 5 ICLK*4
000C 228Eh	GPT3	General PWM timer counter	GTCNT	16	16	3 to 5 ICLK*4
000C 2290h	GPT3	General PWM timer compare capture register A	GTCCRA	16	16, 32	3 to 5 ICLK*4
000C 2292h	GPT3	General PWM timer compare capture register B	GTCCRB	16	16, 32	3 to 5 ICLK*4
000C 2294h	GPT3	General PWM timer compare capture register C	GTCCRC	16	16, 32	3 to 5 ICLK*4
000C 2296h	GPT3	General PWM timer compare capture register D	GTCCRD	16	16, 32	3 to 5 ICLK*4
000C 2298h	GPT3	General PWM timer compare capture register E	GTCCRE	16	16, 32	3 to 5 ICLK*4
000C 229Ah	GPT3	General PWM timer compare capture register F	GTCCRF	16	16, 32	3 to 5 ICLK*4
000C 229Ch	GPT3	General PWM timer cycle setting register	GTPR	16	16, 32	3 to 5 ICLK*4
000C 229Eh	GPT3	General PWM timer cycle setting buffer register	GTPBR	16	16, 32	3 to 5 ICLK*4
000C 22A0h	GPT3	General PWM timer cycle setting double-buffer register	GTPDBR	16	16, 32	3 to 5 ICLK*4
000C 22A4h	GPT3	A/D converter start request timing register A	GTADTRA	16	16, 32	3 to 5 ICLK*4
000C 22A6h	GPT3	A/D converter start request timing buffer register A	GTADTBRA	16	16, 32	3 to 5 ICLK*4
000C 22A8h	GPT3	A/D converter start request timing double-buffer register A	GTADTDBRA	16	16, 32	3 to 5 ICLK*4
000C 22ACh	GPT3	A/D converter start request timing register B	GTADTRB	16	16, 32	3 to 5 ICLK*4
000C 22AEh	GPT3	A/D converter start request timing buffer register B	GTADTBRB	16	16, 32	3 to 5 ICLK*4
000C 22B0h	GPT3	A/D converter start request timing double-buffer register B	GTADTDBRB	16	16, 32	3 to 5 ICLK*4
000C 22B4h	GPT3	General PWM timer output negate control register	GTONCR	16	16, 32	3 to 5 ICLK*4

Table 4.1 List of I/O Registers (Address Order) (25 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
007F FFBAh	FLASH	FCU command register	FCMDR	16	16	2, 3 PCLK*3
007F FFC8h	FLASH	FCU processing switching register	FCPSR	16	16	2, 3 PCLK*3
007F FFCAh	FLASH	Data flash blank check control register	DFLBCCNT	16	16	2, 3 PCLK*3
007F FFCCh	FLASH	Flash P/E status register	FPESTAT	16	16	2, 3 PCLK*3
007F FFCEh	FLASH	Data flash blank check status register	DFLBCSTAT	16	16	2, 3 PCLK*3
007F FFE8h	FLASH	Peripheral clock notification register	PCKAR	16	16	2, 3 PCLK*3

Note 1. This register is not supported by the 100-pin LQFP version.
Note 2. This register is not supported by the product without the CAN function.
Note 3. The number of access states depends on the number of divided cycles for clock synchronization (0 to 1 PCLK).
Note 4. Reading the registers takes 3 cycles of ICLK and writing to the registers takes 5 cycles of ICLK.

Table 4.2 List of I/O Registers (Bit Order) (9 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
ICU	IRQCR0	—	—	—	—	IRQMD[1:0]		—	—
ICU	IRQCR1	—	—	—	—	IRQMD[1:0]		—	—
ICU	IRQCR2	—	—	—	—	IRQMD[1:0]		—	—
ICU	IRQCR3	—	—	—	—	IRQMD[1:0]		—	—
ICU	IRQCR4	—	—	—	—	IRQMD[1:0]		—	—
ICU	IRQCR5	—	—	—	—	IRQMD[1:0]		—	—
ICU	IRQCR6	—	—	—	—	IRQMD[1:0]		—	—
ICU	IRQCR7	—	—	—	—	IRQMD[1:0]		—	—
ICU	NMISR	—	—	—	—	—	OSTST	LVDST	NMIST
ICU	NMIER	—	—	—	—	—	OSTEN	LVDEN	NMIEN
ICU	NMICLR	—	—	—	—	—	OSTCLR	—	NMICLR
ICU	NMICR	—	—	—	—	NMIMD	—	—	—
CMT	CMSTR0	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	STR1	STR0
CMT0	CMCR	—	—	—	—	—	—	—	—
		—	CMIE	—	—	—	—	CKS[1:0]	
CMT0	CMCNT								
CMT0	CMCOR								
CMT1	CMCR	—	—	—	—	—	—	—	—
		—	CMIE	—	—	—	—	CKS[1:0]	
CMT1	CMCNT								
CMT1	CMCOR								
CMT	CMSTR1	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	STR3	STR2
CMT2	CMCR	—	—	—	—	—	—	—	—
		—	CMIE	—	—	—	—	CKS[1:0]	
CMT2	CMCNT								
CMT2	CMCOR								
CMT3	CMCR	—	—	—	—	—	—	—	—
		—	CMIE	—	—	—	—	CKS[1:0]	
CMT3	CMCNT								
CMT3	CMCOR								
WDT	TCSR	—	TMS	TME	—	—		CKS[2:0]	
WDT	WINA								
WDT	TCNT								
WDT	WINB								
WDT	RSTCSR	WOVF	RSTE	—	—	—	—	—	—
IWDT	IWDTCR	—	—	—	—	—	—	—	—
			CKS[3:0]			—	—	TOPS[1:0]	
IWDT	IWDTSR	—	UNDFF			CNTVAL[13:0]			
					CNTVAL[13:0]				
AD0	ADDRA*1	—	—	—	—	—	—		

Table 4.2 List of I/O Registers (Bit Order) (10 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
AD0	ADDRB*1	—	—	—	—	—	—		
AD0	ADDRC*1	—	—	—	—	—	—		
AD0	ADDRD*1	—	—	—	—	—	—		
AD0	ADDRE*1	—	—	—	—	—	—		
AD0	ADDRF*1	—	—	—	—	—	—		
AD0	ADDRG*1	—	—	—	—	—	—		
AD0	ADDRH*1	—	—	—	—	—	—		
AD0	ADCSR	—	ADIE	ADST	—		CH[3:0]		
AD0	ADCR	—	—	—	—	CKS[1:0]		MODE[1:0]	
AD0	ADSSTR								
AD0	ADDIAGR	—	—	—	—	—	—	DIAG[1:0]	
AD0	ADDRI*1	—	—	—	—	—	—		
AD0	ADDRJ*1	—	—	—	—	—	—		
AD0	ADDRK *1	—	—	—	—	—	—		
AD0	ADDRL*1	—	—	—	—	—	—		
AD0	ADSTRGR	—	—	—			ADSTRS[4:0]		
AD0	ADDPR	DPSEL	—	—	—	—	—	—	DPPRC
SCI0	SMR	CM	CHR	PE	PM	STOP	MP	CKS[1:0]	
SCI0	BRR								
SCI0	SCR	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
SCI0	TDR								
SCI0	SSR	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
SCI0	RDR								
SCI0	SCMR	BCP2	—	—	—	SDIR	SINV	—	SMIF
SCI0	SEMR	—	—	NFEN	ABCS	—	—	—	—
SMCI0	SMR	GM	BLK	PE	PM	(BCP[1:0])		CKS[1:0]	
SMCI0	BRR								
SMCI0	SCR	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
SMCI0	TDR								
SMCI0	SSR	TDRE	RDRF	ORER	ERS	PER	TEND	MPB	MPBT
SMCI0	RDR								
SMCI0	SCMR	BCP2	—	—	—	SDIR	SINV	—	SMIF
SCI1	SMR	CM	CHR	PE	PM	STOP	MP	CKS[1:0]	
SCI1	BRR								
SCI1	SCR	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
SCI1	TDR								
SCI1	SSR	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
SCI1	RDR								
SCI1	SCMR	BCP2	—	—	—	SDIR	SINV	—	SMIF

Table 4.2 List of I/O Registers (Bit Order) (13 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
S12AD0	ADRD*2	DIAGST[1:0]		—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD0	ADDR0A*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD0	ADDR1*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD0	ADDR2*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD0	ADDR3*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD0	ADDR0B*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD0	ADSSTR								
S12AD1	ADCSR	ADST	ADCS[1:0]		ADIE	CKS[1:0]		TRGE	EXTRG
S12AD1	ADANS	—	—	CH[1:0]		—	PG102SEL	PG101SEL	PG100SEL
		—	—	—	—	—	PG102EN	PG101EN	PG100EN
S12AD1	ADPG	—	—	—	—	PG102GAIN[3:0]			
		PG101GAIN[3:0]				PG100GAIN[3:0]			
S12AD1	ADCER	ADRFMT	—	ADIEW	ADIE2	DIAGM	DIAGLD	DIAGVAL[1:0]	
		—	—	ACE	—	—	ADPRC[1:0]		SHBYP
S12AD1	ADSTRGR	—	—	—	ADSTRS1[4:0]				
		—	—	—	ADSTRS0[4:0]				
S12AD1	ADRD*2	DIAGST[1:0]		—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD1	ADDR0A*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD1	ADDR1*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD1	ADDR2*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD1	ADDR3*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD1	ADDR0B*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD1	ADSSTR								
PORT1	DDR	—	—	—	—	—	—	B1	B0
PORT2	DDR	—	—	—	B4	B3	B2	B1	B0
PORT3	DDR	—	—	—	—	B3	B2	B1	B0
PORT7	DDR	—	B6	B5	B4	B3	B2	B1	B0
PORT8	DDR	—	—	—	—	—	B2	B1	B0
PORT9	DDR	—	B6	B5	B4	B3	B2	B1	B0
PORTA	DDR	—	—	B5	B4	B3	B2	B1	B0
PORTB	DDR	B7	B6	B5	B4	B3	B2	B1	B0
PORTD	DDR	B7	B6	B5	B4	B3	B2	B1	B0
PORTE	DDR	—	—	B5	B4	B3	—	B1	B0
PORTG	DDR	—	—	B5	B4	B3	B2	B1	B0
PORT1	DR	—	—	—	—	—	—	B1	B0
PORT2	DR	—	—	—	B4	B3	B2	B1	B0
PORT3	DR	—	—	—	—	B3	B2	B1	B0
PORT7	DR	—	B6	B5	B4	B3	B2	B1	B0

Table 4.2 List of I/O Registers (Bit Order) (15 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
SYSTEM	DPSIFR	DNMIF	—	—	DLVDF	—	—	DIRQ1F	DIRQ0F
SYSTEM	DPSIEGR	DNMIEG	—	—	—	—	—	DIRQ1EG	DIRQ0EG
SYSTEM	RSTSR	DPSRSTF	—	—	—	—	LVD2F	LVD1F	PORF
FLASH	FWEPROR	—	—	—	—	—	—	FLWE[1:0]	
SYSTEM	LVDKEYR	KEY[7:0]							
SYSTEM	LVDCR	LVD2E	LVD2RI	—	—	LVD1E	LVD1RI	—	—
SYSTEM	DPSBKR0								
SYSTEM	DPSBKR1								
SYSTEM	DPSBKR2								
SYSTEM	DPSBKR3								
SYSTEM	DPSBKR4								
SYSTEM	DPSBKR5								
SYSTEM	DPSBKR6								
SYSTEM	DPSBKR7								
SYSTEM	DPSBKR8								
SYSTEM	DPSBKR9								
SYSTEM	DPSBKR10								
SYSTEM	DPSBKR11								
SYSTEM	DPSBKR12								
SYSTEM	DPSBKR13								
SYSTEM	DPSBKR14								
SYSTEM	DPSBKR15								
SYSTEM	DPSBKR16								
SYSTEM	DPSBKR17								
SYSTEM	DPSBKR18								
SYSTEM	DPSBKR19								
SYSTEM	DPSBKR20								
SYSTEM	DPSBKR21								
SYSTEM	DPSBKR22								
SYSTEM	DPSBKR23								
SYSTEM	DPSBKR24								
SYSTEM	DPSBKR25								
SYSTEM	DPSBKR26								
SYSTEM	DPSBKR27								
SYSTEM	DPSBKR28								
SYSTEM	DPSBKR29								
SYSTEM	DPSBKR30								
SYSTEM	DPSBKR31								
POE	ICSR1	—	—	—	POE0F	—	—	—	PIE1
		—	—	—	—	—	—	POE0M[1:0]	
POE	OCSR1	OSF1	—	—	—	—	—	OCE1	OIE1
		—	—	—	—	—	—	—	—
POE	ICSR2	—	—	—	POE4F	—	—	—	PIE2
		—	—	—	—	—	—	POE4M[1:0]	
POE	OCSR2	OSF2	—	—	—	—	—	OCE2	OIE2
		—	—	—	—	—	—	—	—
POE	ICSR3	—	—	—	POE8F	—	—	POE8E	PIE3
		—	—	—	—	—	—	POE8M[1:0]	
POE	SPOER	—	—	—	GPT23HIZ	GPT01HIZ	MTUCH0HIZ	MTUCH67HIZ	MTUCH34HIZ
POE	POECR1	—	—	—	—	MTU0DZE	MTU0CZE	MTU0BZE	MTU0AZE

Table 4.2 List of I/O Registers (Bit Order) (23 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
GPT	GTBDR	BD33	BD32	BD31	BD30	BD23	BD22	BD21	BD20
		BD13	BD12	BD11	BD10	BD03	BD02	BD01	BD00
GPT	GTSWP	—	—	—	—	—	—	—	—
		—	—	—	—	SWP3	SWP2	SWP1	SWP0
GPT	LCCR	LPSC[1:0]		TPSC[1:0]		LCNTAT		LCTO[2:0]	
		—	LCINTO	LCINTD	LCINTC	—	LCNTS	LCNTCR	LCNTE
GPT	LCST	—	—	—	—	—	—	—	—
		—	—	—	—	—	LISO	LISD	LISC
GPT	LCNTA								
GPT	LCNT00								
GPT	LCNT01								
GPT	LCNT02								
GPT	LCNT03								
GPT	LCNT04								
GPT	LCNT05								
GPT	LCNT06								
GPT	LCNT07								
GPT	LCNT08								
GPT	LCNT09								
GPT	LCNT10								
GPT	LCNT11								
GPT	LCNT12								
GPT	LCNT13								
GPT	LCNT14								
GPT	LCNT15								
GPT	LCNTDU								
GPT	LCNTDL								
GPT0	GTIOR	OBHLD	OBDFLT			GTIOB[5:0]			
		OAHLD	OADFLT			GTIOA[5:0]			
GPT0	GTINTAD	ADTRBDEN	ADTRBUEN	ADTRADEN	ADTRAUEN	EINT	—	—	—
		GTINTPR[1:0]		GTINTF	GTINTE	GTINTD	GTINTC	GTINTB	GTINTA

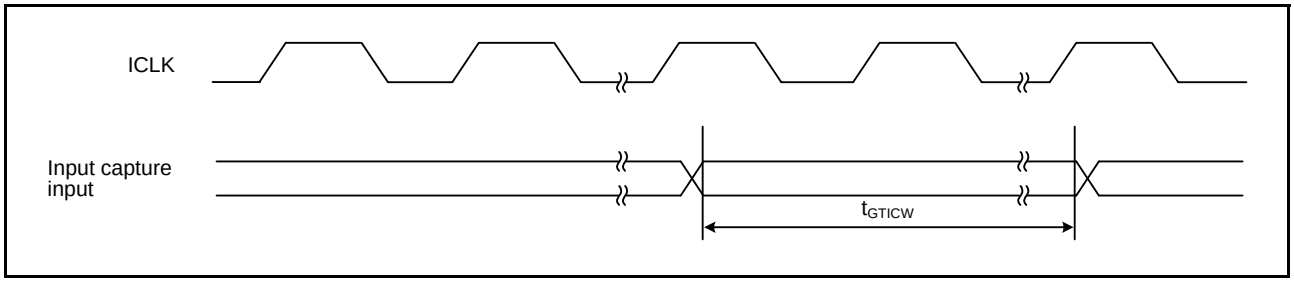

Figure 5.18 GPT Input/Output Timing

Table 5.13 Timing of On-Chip Peripheral Modules (5)

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Max.	Unit	Test Conditions
POE3	POE# input pulse width	t_{POEW}	1.5	-	t_{Pcyc}	Figure 5.19

Note: • t_{Pcyc}: PCLK cycle

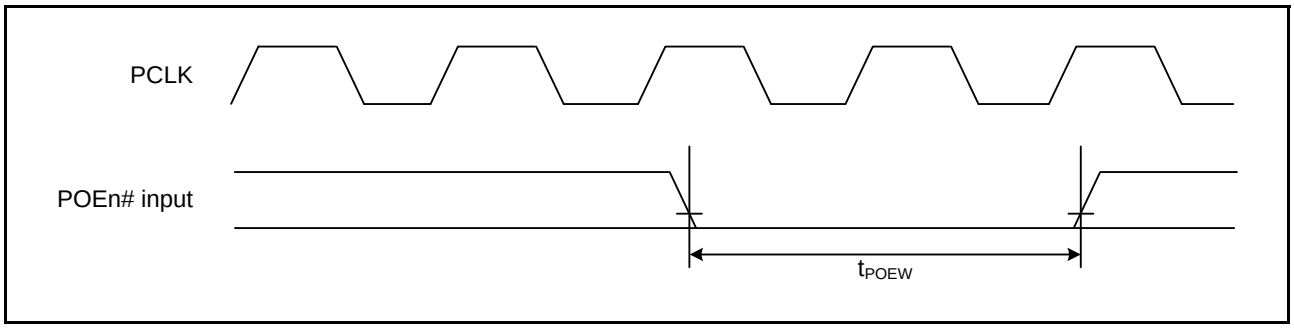

Figure 5.19 POE3# Clock Timing

5.3.4 Timing of PWM Delay Generation Circuit

Table 5.14 Timing of the PWM Delay Generation Circuit

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS = VREL0 = 0 V
AVCC = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr.

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Resolution	—	312.5	—	ps	ICLK = 100 MHz
DNL*1	—	±2.0	—	LSB	

Note 1. This value is correct when the difference between each code and the next is a resolution of one bit (1 LSB).

5.5 Power-on Reset Circuit, Voltage Detection Circuit Characteristics

Table 5.19 Power-on Reset Circuit, Voltage Detection Circuit Characteristics

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 and 2.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	2.48	2.60	2.72	V	Figure 5.20
	Voltage detection circuit (LVD)	Vdet1	2.68	2.80	2.92		Figure 5.21
		Vdet2	2.98	3.10	3.22		Figure 5.22
Internal reset time		t_{POR}	20	35	50	ms	Figure 5.21 and Figure 5.22
Min. VCC down time*1		t_{VOFF}	200	-	-	us	Figure 5.20 to Figure 5.22
Reply delay time		tdet	-	-	200	us	

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	3.70	3.90	4.10	V	Figure 5.20
	Voltage detection circuit (LVD)	Vdet1	3.95	4.15	4.35		Figure 5.21
		Vdet2	4.40	4.60	4.80		Figure 5.22
Internal reset time		t_{POR}	20	35	50	ms	Figure 5.21 and Figure 5.22
Min. VCC down time*1		t_{VOFF}	200	-	-	us	Figure 5.20 to Figure 5.22
Reply delay time		tdet	-	-	200	us	

Note 1. The power-off time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det1}, and V_{det2} for the POR/ LVD.

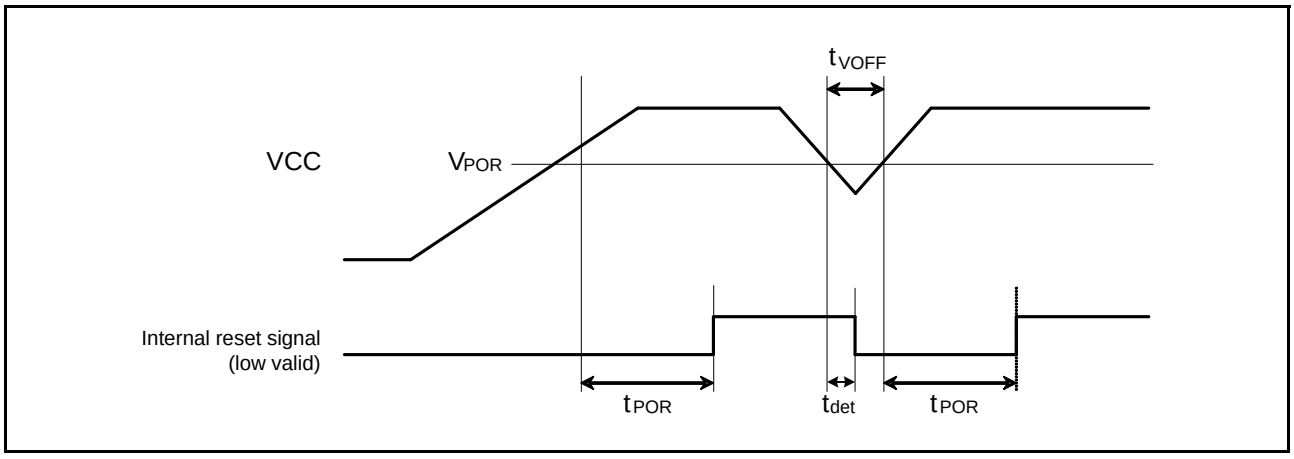

Figure 5.20 Power-on Reset Timing

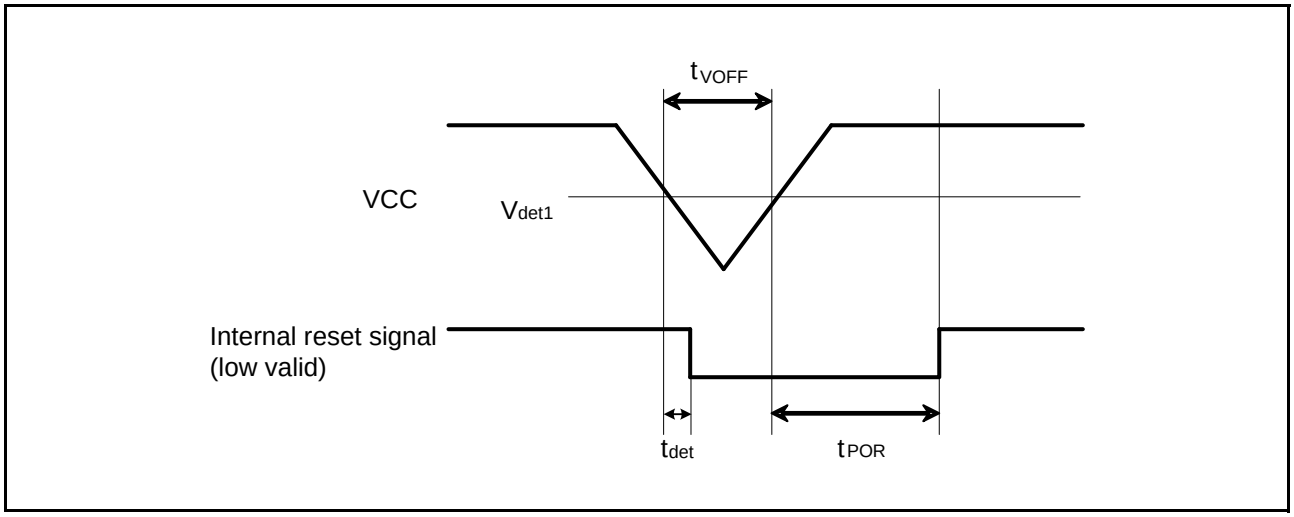

Figure 5.21 Voltage Detection Circuit Timing (Vdet1)

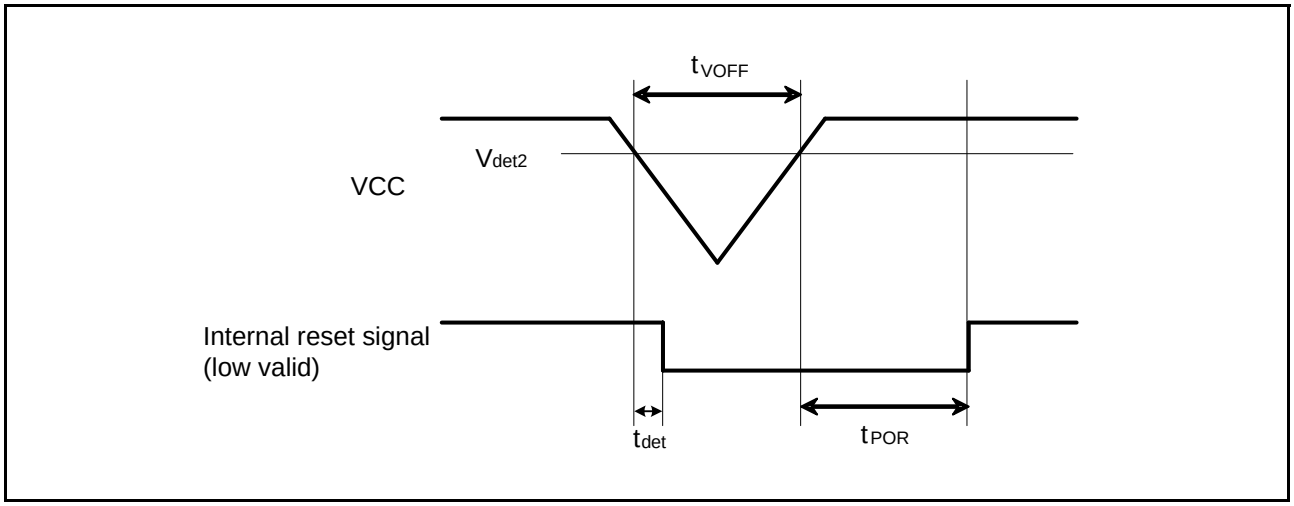

Figure 5.22 Voltage Detection Circuit Timing (Vdet2)