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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562t7bdfk-v1

Table 1.1 Outline of Specifications (2 / 5)

Classification	Module/Function	Description
Interrupt	Interrupt controller (ICU)	• Peripheral function interrupts: 101 sources • External interrupts: 9 (NMI and IRQ0 to IRQ7 pins) • Non-maskable interrupts: 3 (the NMI pin, oscillation stop detection interrupt, and voltage-monitoring interrupt) • 16 levels specifiable for the order of priority
Data transfer	Data transfer controller (DTC)	• Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
I/O ports	Programmable I/O ports	I/O port pins for devices in the 112-pin LQFP/100-pin LQFP/ 80-pin LQFP (R5F562TxGDFF)/80-pin LQFP (except R5F562TxGDFF)/64-pin LQFP • I/O: 61/55/44/44/37 • Input only: 21/21/13/13/9 • Open-drain outputs: 2/2/2/2/2 (I^2C bus interface pins) • Large-current outputs: 12/12/12/6/6(0) (MTU3 and GPT pins) The 5-V version of the 64-pin product does not have large-current outputs. • Reading out the states of pins is always possible.
Timers	Multi-function timer pulse unit 3 (MTU3)	• 16 bits x 8 channels • Up to 24 pulse inputs/outputs and three pulse inputs • Select from among six to eight counter-input clock signals for each channel (ICLK/1, ICLK/4, ICLK/16, ICLK/64, ICLK/256, ICLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available. • 24 output compare or input capture registers • Counter clearing (clearing is synchronizable with compare match or input capture) • Simultaneous writing to multiple timer counters (TCNT) • Input to and output from all registers in synchronization with counter operation • Buffered operation • Cascade-connected operation • 38 kinds of interrupt source • Automatic transfer of register data • Pulse output modes Toggled, PWM, complementary PWM, and reset synchronous PWM • Complementary PWM output mode Outputs non-overlapping waveforms for controlling 3-phase inverters Automatic specification of dead times PWM duty cycle: Selectable as any value from 0% to 100% Delay can be applied to requests for A/D conversion. Non-generation of interrupt requests at peak or trough values of counters can be selected. Double buffering • Reset-synchronous PWM mode Three PWM waveforms and corresponding inverse waveforms are output with the desired duty cycles. • Phase-counting mode • Counter functionality for dead-time compensation • Generation of triggers for A/D converters • Differential timing for initiation of A/D conversion
	Port output enable 3 (POE3)	• Control of the high-impedance state of the MTU3 and GPT's waveform output pins 5 pins for input from signal sources: POE0, POE4, POE8, POE10, POE11 Initiation on detection of short-circuited outputs (detection of simultaneous switching of large-current pins to the active level) Initiation by comparator-detection of analog level input to the 12-bit A/D converter Initiation by oscillation-stoppage detection Initiation by software • Selection of which output pins should be placed in the high-impedance state at the time of each POE input or comparator detection

Table 1.2 Functions of RX62T Group and RX62G Group Products (2 / 2)

Functions	RX62G Group		RX62T Group				
Pin number	**112 Pins**	**100 Pins**	**112 Pins**	**100 Pins**	**80 Pins (R5F562T xGDFF)**	**80 Pins**	**64 Pins**
Package	LQFP2020 (0.65-mm pitch)	LQFP1414 (0.5-mm pitch)	LQFP2020 (0.65-mm pitch)	LQFP1414 (0.5-mm pitch)	LQFP1414 (0.65-mm pitch)	LQFP1414 (0.65-mm pitch)	LQFP1010 (0.5-mm pitch) LQFP1414 (0.8-mm pitch)

O: Supported, —: Not supported

Note 1. For the MTU and GPT, the number of pins will differ with the package. See the list of pins and pin functions for details. In addition, the CAN module is an optional function. See Table 1.3 for details.

Table 1.5 List of Pins and Pin Functions (100-Pin LQFP) (2 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi-cation	Interrupt	POE	Debugging
41		PA0		MTIOC6C	SSL3-B			
42	VCC							
43		P96				IRQ4	POE4#	
44	VSS							
45		P95		MTIOC6B				
46		P94		MTIOC7A				
47		P93		MTIOC7B				
48		P92		MTIOC6D				
49		P91		MTIOC7C				
50		P90		MTIOC7D				
51		P76		MTIOC4D/ GTIOC2B-A				
52		P75		MTIOC4C/ GTIOC1B-A				
53		P74		MTIOC3D/ GTIOC0B-A				
54		P73		MTIOC4B/ GTIOC2A-A				
55		P72		MTIOC4A/ GTIOC1A-A				
56		P71		MTIOC3B/ GTIOC0A-A				
57		P70				IRQ5	POE0#	
58		P33		MTIOC3A/ MTCLKA-A	SSL3-A			
59		P32		MTIOC3C/ MTCLKB-A	SSL2-A			
60	VCC							
61		P31		MTIOC0A-B/ MTCLKC-A	SSL1-A			
62	VSS							
63		P30		MTIOC0B-B/ MTCLKD-A	SSL0-A			
64		P24			RSPCK-A			
65		P23			CTX-B/ LTX/ MOSI-A			
66		P22	ADTRG#		CRX-B/ LRX/ MISO-A			
67		P21	ADTRG1#-B	MTCLKA-B		IRQ6		
68		P20	ADTRG0#-B	MTCLKB-B		IRQ7		
69		P65	AN5					
70		P64	AN4					
71	AVCC							
72	VREF							
73	AVSS							
74		P63	AN3					
75		P62	AN2					
76		P61	AN1					

Table 1.7 List of Pins and Pin Functions (80-Pin LQFP: R5F562TxGDFF) (1 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communication	Interrupt	POE	Debugging
1	EMLE							
2	VSS							
3	MDE							
4	VCL							
5	MD1							
6	MD0							
7		PE4		MTCLKC-C		IRQ1-B	POE10#-B	
8		PE3		MTCLKD-C		IRQ2-A	POE11#	
9	RES#							
10	XTAL							
11	VSS							
12	EXTAL							
13	VCC							
14		PE2				NMI	POE10#-A	
15		PD7		GTIOC0A-B				TRST#
16		PD6		GTIOC0B-B				TMS
17		PD5		GTIOC1A-B	RXD1			TDI
18		PD4		GTIOC1B-B	SCK1			TCK
19		PD3		GTIOC2A-B	TXD1			TDO
20		PD2		GTIOC2B-B				
21		PB7			SCK2-A			
22		PB6			CRX-A/ RXD2-A			
23		PB5			CTX-A/ TXD2-A			
24	PLLVCC							
25		PB4		GTETRG		IRQ3	POE8#	
26	PLLVSS							
27		PB3		MTIOC0A-A	SCK0			
28		PB2		MTIOC0B-A	TXD0/SDA			
29		PB1		MTIOC0C	RXD0/SCL			
30		PB0		MTIOC0D				
31		PA5	ADTRG1#-A	MTIOC1A				
32		PA3		MTIOC2A				
33	VCC							
34		P96				IRQ4	POE4#	
35	VSS							
36		P95		MTIOC6B				
37		P94		MTIOC7A				
38		P93		MTIOC7B				
39		P92		MTIOC6D				
40		P91		MTIOC7C				
41		P90		MTIOC7D				

Table 1.7 List of Pins and Pin Functions (80-Pin LQFP: R5F562TxGDFF) (3 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communication	Interrupt	POE	Debugging
76	AVSS0							
77		P82		MTIC5U	SCK2-B			
78		P81		MTIC5V	TXD2-B			
79		P80		MTIC5W	RXD2-B			
80		P10		MTCLKD-B		IRQ0-A		

Table 1.9 Pin Functions (4 / 4)

Classifications	Pin Name	I/O	Description
I/O ports	P10, P11	I/O	2-bit input/output pins.
	P20 to P24	I/O	5-bit input/output pins. The P20/P21 pin is not included in the 64-pin version.
	P30 to P33	I/O	4-bit input/output pins.
	P40 to P47	Input	8-bit input pins.
	P50 to P55	Input	6-bit input pins. Not included in the 80-/64-pin versions.
	P60 to P65	Input	6-bit input pins. The P64/P6 pin is not included in the 80-pin version. Not included in the 64-pin version.
	P70 to P76	I/O	7-bit input/output pins.
	P80 to P82	I/O	3-bit input/output pins. Not included in the 80-/64-pin versions.
	P90 to P96	I/O	7-bit input/output pins. The P90 pin is not included in the 80-pin version. The P90/P95/P96 pin is not included in the 64-pin version.
	PA0 to PA5	I/O	6-bit input/output pins. The PA0/PA1 pin is not included in the 80-/64-pin versions.
	PB0 to PB7	I/O	8-bit input/output pins.
	PD0 to PD7	I/O	8-bit input/output pins. The PD0/PD1/PD2 pin is not included in the 80-/64-pin versions.
	PE0, PE1, PE3 to PE5	I/O	5-bit input/output pins. The PE1/PE5 pin is not included in the 80-pin version. Not included in the 64-pin version.
	PE2	Input	1-bit input pin.
	PG0 to PG5	I/O	6-bit input/output pins. Not included in the 100-/80-/64-pin versions.

Note: • Which pins are and are not incorporated depends on the package.
For details, see the list of pins and pin functions in Table 1.4 to Table 1.8.

2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen general-purpose registers (R0 to R15). R1 to R15 can be used as data registers or address registers. R0, a general-purpose register, also functions as the stack pointer (SP). The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2 Control Registers

(1) Interrupt Stack Pointer (ISP)/User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).
Set the ISP or USP to a multiple of four, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(2) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the relocatable vector table starts.
Set INTB to a multiple of four.

(3) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

(4) Processor Status Word (PSW)

The processor status word (PSW) indicates results of instruction execution or the state of the CPU.

(5) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC.

(6) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

(7) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.
The FINTV register specifies a branch destination address when a fast interrupt has been generated.

(8) Floating-Point Status Word (FPSW)

The floating-point status word (FPSW) indicates the results of floating-point operations.
When an exception handling enable bit (Ej) enables the exception handling (Ej = 1), the exception cause can be identified by checking the corresponding Cj flag in the exception handling routine. If the exception handling is masked (Ej = 0), the occurrence of exception can be checked by reading the Fj flag at the end of a series of processing. Once the Fj flag has been set to 1, this value is retained until it is cleared to 0 by software (j = X, U, Z, O, or V).

(4) Number of Access Cycles to I/O Registers

The number of access cycles to I/O registers is obtained by following equation.*

Number of access cycles to I/O registers = Number of bus cycles for internal main bus 1 +
Number of divided cycles for clock synchronization +
Number of bus cycles for internal peripheral buses 1, 2, 4, and 6

The number of bus cycles for internal peripheral buses 1, 2, 4, and 6 differs according to the register to be accessed. For the number of access cycles to each I/O register, see Table 4.1, List of I/O Registers.

When peripheral functions connected to internal peripheral bus 6 are accessed, the number of divided cycles for clock synchronization is added.

Although the number of divided cycles for clock synchronization differs depending on the number of frequency ratio between ICLK and PCLK or bus access timing, the sum of the number of bus cycles for internal main bus 1 and the number of divided cycles for clock synchronization will be one PCLK at a maximum. Therefore, one PCLK is added to the number of access cycles shown in Table 4.1.

Note: • This applies to the number of cycles when the access from the CPU does not conflict with the instruction fetching to the external memory or bus access from the different bus master (DTC).

Table 4.1 List of I/O Registers (Address Order) (5 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 7172h	ICU	DTC activation enable register 114	DTCER114	8	8	2 ICLK
0008 7173h	ICU	DTC activation enable register 115	DTCER115	8	8	2 ICLK
0008 7174h	ICU	DTC activation enable register 116	DTCER116	8	8	2 ICLK
0008 7175h	ICU	DTC activation enable register 117	DTCER117	8	8	2 ICLK
0008 7179h	ICU	DTC activation enable register 121	DTCER121	8	8	2 ICLK
0008 717Ah	ICU	DTC activation enable register 122	DTCER122	8	8	2 ICLK
0008 717Dh	ICU	DTC activation enable register 125	DTCER125	8	8	2 ICLK
0008 717Eh	ICU	DTC activation enable register 126	DTCER126	8	8	2 ICLK
0008 7181h	ICU	DTC activation enable register 129	DTCER129	8	8	2 ICLK
0008 7182h	ICU	DTC activation enable register 130	DTCER130	8	8	2 ICLK
0008 7183h	ICU	DTC activation enable register 131	DTCER131	8	8	2 ICLK
0008 7184h	ICU	DTC activation enable register 132	DTCER132	8	8	2 ICLK
0008 7186h	ICU	DTC activation enable register 134	DTCER134	8	8	2 ICLK
0008 7187h	ICU	DTC activation enable register 135	DTCER135	8	8	2 ICLK
0008 7188h	ICU	DTC activation enable register 136	DTCER136	8	8	2 ICLK
0008 7189h	ICU	DTC activation enable register 137	DTCER137	8	8	2 ICLK
0008 718Ah	ICU	DTC activation enable register 138	DTCER138	8	8	2 ICLK
0008 718Bh	ICU	DTC activation enable register 139	DTCER139	8	8	2 ICLK
0008 718Ch	ICU	DTC activation enable register 140	DTCER140	8	8	2 ICLK
0008 718Dh	ICU	DTC activation enable register 141	DTCER141	8	8	2 ICLK
0008 718Eh	ICU	DTC activation enable register 142	DTCER142	8	8	2 ICLK
0008 718Fh	ICU	DTC activation enable register 143	DTCER143	8	8	2 ICLK
0008 7190h	ICU	DTC activation enable register 144	DTCER144	8	8	2 ICLK
0008 7191h	ICU	DTC activation enable register 145	DTCER145	8	8	2 ICLK
0008 7195h	ICU	DTC activation enable register 149	DTCER149	8	8	2 ICLK
0008 7196h	ICU	DTC activation enable register 150	DTCER150	8	8	2 ICLK
0008 7197h	ICU	DTC activation enable register 151	DTCER151	8	8	2 ICLK
0008 7198h	ICU	DTC activation enable register 152	DTCER152	8	8	2 ICLK
0008 7199h	ICU	DTC activation enable register 153	DTCER153	8	8	2 ICLK
0008 71AEh	ICU	DTC activation enable register 174	DTCER174	8	8	2 ICLK
0008 71AFh	ICU	DTC activation enable register 175	DTCER175	8	8	2 ICLK
0008 71B0h	ICU	DTC activation enable register 176	DTCER176	8	8	2 ICLK
0008 71B1h	ICU	DTC activation enable register 177	DTCER177	8	8	2 ICLK
0008 71B2h	ICU	DTC activation enable register 178	DTCER178	8	8	2 ICLK
0008 71B3h	ICU	DTC activation enable register 179	DTCER179	8	8	2 ICLK
0008 71B4h	ICU	DTC activation enable register 180	DTCER180	8	8	2 ICLK
0008 71B5h	ICU	DTC activation enable register 181	DTCER181	8	8	2 ICLK
0008 71B6h	ICU	DTC activation enable register 182	DTCER182	8	8	2 ICLK
0008 71B7h	ICU	DTC activation enable register 183	DTCER183	8	8	2 ICLK
0008 71B8h	ICU	DTC activation enable register 184	DTCER184	8	8	2 ICLK
0008 71BAh	ICU	DTC activation enable register 186	DTCER186	8	8	2 ICLK
0008 71BBh	ICU	DTC activation enable register 187	DTCER187	8	8	2 ICLK
0008 71BCh	ICU	DTC activation enable register 188	DTCER188	8	8	2 ICLK
0008 71BDh	ICU	DTC activation enable register 189	DTCER189	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (7 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 7305h	ICU	Interrupt source priority register 05	IPR05	8	8	2 ICLK
0008 7306h	ICU	Interrupt source priority register 06	IPR06	8	8	2 ICLK
0008 7307h	ICU	Interrupt source priority register 07	IPR07	8	8	2 ICLK
0008 7314h	ICU	Interrupt source priority register 14	IPR14	8	8	2 ICLK
0008 7318h	ICU	Interrupt source priority register 18	IPR18	8	8	2 ICLK
0008 7320h	ICU	Interrupt source priority register 20	IPR20	8	8	2 ICLK
0008 7321h	ICU	Interrupt source priority register 21	IPR21	8	8	2 ICLK
0008 7322h	ICU	Interrupt source priority register 22	IPR22	8	8	2 ICLK
0008 7323h	ICU	Interrupt source priority register 23	IPR23	8	8	2 ICLK
0008 7324h	ICU	Interrupt source priority register 24	IPR24	8	8	2 ICLK
0008 7325h	ICU	Interrupt source priority register 25	IPR25	8	8	2 ICLK
0008 7326h	ICU	Interrupt source priority register 26	IPR26	8	8	2 ICLK
0008 7327h	ICU	Interrupt source priority register 27	IPR27	8	8	2 ICLK
0008 7340h	ICU	Interrupt source priority register 40	IPR40	8	8	2 ICLK
0008 7344h	ICU	Interrupt source priority register 44	IPR44	8	8	2 ICLK
0008 7348h	ICU	Interrupt source priority register 48	IPR48	8	8	2 ICLK
0008 7349h	ICU	Interrupt source priority register 49	IPR49	8	8	2 ICLK
0008 7351h	ICU	Interrupt source priority register 51	IPR51	8	8	2 ICLK
0008 7352h	ICU	Interrupt source priority register 52	IPR52	8	8	2 ICLK
0008 7353h	ICU	Interrupt source priority register 53	IPR53	8	8	2 ICLK
0008 7354h	ICU	Interrupt source priority register 54	IPR54	8	8	2 ICLK
0008 7355h	ICU	Interrupt source priority register 55	IPR55	8	8	2 ICLK
0008 7356h	ICU	Interrupt source priority register 56	IPR56	8	8	2 ICLK
0008 7357h	ICU	Interrupt source priority register 57	IPR57	8	8	2 ICLK
0008 7358h	ICU	Interrupt source priority register 58	IPR58	8	8	2 ICLK
0008 7359h	ICU	Interrupt source priority register 59	IPR59	8	8	2 ICLK
0008 735Ah	ICU	Interrupt source priority register 5A	IPR5A	8	8	2 ICLK
0008 735Bh	ICU	Interrupt source priority register 5B	IPR5B	8	8	2 ICLK
0008 735Ch	ICU	Interrupt source priority register 5C	IPR5C	8	8	2 ICLK
0008 735Dh	ICU	Interrupt source priority register 5D	IPR5D	8	8	2 ICLK
0008 735Eh	ICU	Interrupt source priority register 5E	IPR5E	8	8	2 ICLK
0008 735Fh	ICU	Interrupt source priority register 5F	IPR5F	8	8	2 ICLK
0008 7360h	ICU	Interrupt source priority register 60	IPR60	8	8	2 ICLK
0008 7367h	ICU	Interrupt source priority register 67	IPR67	8	8	2 ICLK
0008 7368h	ICU	Interrupt source priority register 68	IPR68	8	8	2 ICLK
0008 7369h	ICU	Interrupt source priority register 69	IPR69	8	8	2 ICLK
0008 736Ah	ICU	Interrupt source priority register 6A	IPR6A	8	8	2 ICLK
0008 736Bh	ICU	Interrupt source priority register 6B	IPR6B	8	8	2 ICLK
0008 736Ch	ICU	Interrupt source priority register 6C	IPR6C	8	8	2 ICLK
0008 736Dh	ICU	Interrupt source priority register 6D	IPR6D	8	8	2 ICLK
0008 736Eh	ICU	Interrupt source priority register 6E	IPR6E	8	8	2 ICLK
0008 736Fh	ICU	Interrupt source priority register 6F	IPR6F	8	8	2 ICLK
0008 7380h	ICU	Interrupt source priority register 80	IPR80	8	8	2 ICLK
0008 7381h	ICU	Interrupt source priority register 81	IPR81	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (25 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
007F FFBAh	FLASH	FCU command register	FCMDR	16	16	2, 3 PCLK*3
007F FFC8h	FLASH	FCU processing switching register	FCPSR	16	16	2, 3 PCLK*3
007F FFCAh	FLASH	Data flash blank check control register	DFLBCCNT	16	16	2, 3 PCLK*3
007F FFCCh	FLASH	Flash P/E status register	FPESTAT	16	16	2, 3 PCLK*3
007F FFCEh	FLASH	Data flash blank check status register	DFLBCSTAT	16	16	2, 3 PCLK*3
007F FFE8h	FLASH	Peripheral clock notification register	PCKAR	16	16	2, 3 PCLK*3

Note 1. This register is not supported by the 100-pin LQFP version.
Note 2. This register is not supported by the product without the CAN function.
Note 3. The number of access states depends on the number of divided cycles for clock synchronization (0 to 1 PCLK).
Note 4. Reading the registers takes 3 cycles of ICLK and writing to the registers takes 5 cycles of ICLK.

4.2 I/O Register Bits

Register addresses and bit names of the peripheral modules are described below.
Each line cover eight bits, and 16-bit and 32-bit registers are shown as 2 or 4 lines, respectively.

Table 4.2 List of I/O Registers (Bit Order) (1 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
SYSTEM	MDMONR	—	—	—	—	—	—	—	—
		MDE	—	—	—	—	—	MD1	MD0
SYSTEM	MDSR	—	—	—	—	—	—	—	—
		—	—	—	BOTS	—	—	—	IROM
SYSTEM	SYSCR0	KEY[7:0]							
		—	—	—	—	—	—	—	ROME
SYSTEM	SYSCR1	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	RAME
SYSTEM	SBYCR	SSBY	—	—			STS[4:0]		
		—	—	—	—	—	—	—	—
SYSTEM	MSTPCRA	ACSE	—	—	MSTPA28	—	—	—	MSTPA24
		MSTPA23	—	—	—	—	—	MSTPA17	MSTPA16
		MSTPA15	MSTPA14	—	—	—	—	MSTPA9	—
		MSTPA7	—	—	—	—	—	—	—
SYSTEM	MSTPCRB	MSTPB31	MSTPB30	MSTPB29	—	—	—	—	—
		MSTPB23	—	MSTPB21	—	—	—	MSTPB17	—
		—	—	—	—	—	—	—	—
		MSTPB7	—	—	—	—	—	—	MSTPB0
SYSTEM	MSTPCRC	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	MSTPC0
SYSTEM	SCKCR	—	—	—	—			ICK[3:0]	
		—	—	—	—	—	—	—	—
		—	—	—	—			PCK[3:0]	
		—	—	—	—	—	—	—	—
SYSTEM	OSTDCR	KEY[7:0]							
		OSTDE	OSTDF	—	—	—	—	—	—
BSC	BERCLR	—	—	—	—	—	—	—	STSCLR
BSC	BEREN	—	—	—	—	—	—	—	IGAEN
BSC	BERSR1	—		MST[2:0]		—	—	—	IA
BSC	BERSR2	ADDR[12:0]							
				ADDR[12:0]			—	—	—
DTC	DTCCR	—	—	—	RRS	—	—	—	—
DTC	DTCVBR								
DTC	DTCADMOD	—	—	—	—	—	—	—	SHORT
DTC	DTCST	—	—	—	—	—	—	—	DTCST
DTC	DTCSTS	ACT	—	—	—	—	—	—	—
					VECN[7:0]				
MPU	RSPAGE0				RSPN[27:0]				
					RSPN[27:0]				
					RSPN[27:0]				
				RSPN[27:0]		—	—	—	—

Table 4.2 List of I/O Registers (Bit Order) (25 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
GPT0	GTDBU								
GPT0	GTDBD								
GPT0	GTSOS	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	SOS[1:0]	
GPT0	GTSOTR	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	SOTR
GPT1	GTIOR	OBHLD	OBDFLT			GTIOB[5:0]			
		OAHLD	OADFLT			GTIOA[5:0]			
GPT1	GTINTAD	ADTRBDEN	ADTRBUEN	ADTRADEN	ADTRAUEN	EINT	—	—	—
		GTINTPR[1:0]		GTINTF	GTINTE	GTINTD	GTINTC	GTINTB	GTINTA
GPT1	GTCR	—	—	CCLR[1:0]		—	—	TPCS[1:0]	
		—	—	—	—	—		MD[2:0]	
GPT1	GTBER	—	ADTDB	ADTTB[1:0]		—	ADTDA	ADTTA[1:0]	
		—	CCRSWT	PR[1:0]		CCRB[1:0]		CCRA[1:0]	
GPT1	GTUDC	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	UDF	UD
GPT1	GTITC	—	ADTBL	—	ADTAL	—		IVTT[2:0]	
		IVTC[1:0]		ITLF	ITLE	ITLD	ITLC	ITLB	ITLA
GPT1	GTST	TUCF	—	—	—	DTEF		ITCNT[2:0]	
		TCFPU	TCFPO	TCFF	TCFE	TCFD	TCFC	TCFB	TCFA
GPT1	GTCNT								
GPT1	GTCCRA								
GPT1	GTCCRB								
GPT1	GTCCRC								
GPT1	GTCCRD								
GPT1	GTCCRE								
GPT1	GTCCRF								
GPT1	GTPR								
GPT1	GTPBR								
GPT1	GTPDBR								
GPT1	GTADTRA								
GPT1	GTADTBRA								
GPT1	GTADTDBRA								
GPT1	GTADTRB								

Table 4.2 List of I/O Registers (Bit Order) (30 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
FLASH	FSTATR0	FRDY	ILGLERR	ERSERR	PRGERR	SUSRDY	—	ERSSPD	PRGSPD
FLASH	FSTATR1	FCUERR	—	—	FLOCKST	—	—	—	—
FLASH	FENTRYR	FEKEY[7:0]							
		FENTRYD	—	—	—	—	—	—	FENTRY0
FLASH	FPROTR	FPKEY[7:0]							
		—	—	—	—	—	—	—	FPROTCN
FLASH	FRESETR	FRKEY[7:0]							
		—	—	—	—	—	—	—	FRESET
FLASH	FCMDR	CMDR[7:0]							
		PCMDR[7:0]							
FLASH	FCPSR	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	ESUSPMD
FLASH	DFLBCCNT	—	—	—	—	—		BCADR[7:0]	
		BCADR[7:0]						—	BCSIZE
FLASH	FPESTAT	—	—	—	—	—	—	—	—
		PEERRST[7:0]							
FLASH	DFLBCSTAT	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	BCST
FLASH	PCKAR	—	—	—	—	—	—	—	—
		PCKA[7:0]							

Note: • In this, the I/O port related registers (0008 C001h to 0008 C116h) indicate the bit configuration of the 112-pin LQFP version. As the configuration of registers and bits differs depending on a package, see section 14, I/O Ports, for details in the User's manual: Hardware.

Note 1. This shows the bit configuration when ADDPR.DPSEL = 0 and ADDPR.DPPRC = 0 (The value has 10-bit accuracy and is padded at the LSB end).

Note 2. This shows the bit configuration when ADCER.ADRFMT = 0 (aligned to the LSB end) and ADCER.ADPRC[1:0] = 00b. For details, refer to section 28, 12-Bit A/D Converter (S12ADA) in the User's manual: Hardware.

Note 3. This function is not supported by the product without the CAN function.

5.2 DC Characteristics

Table 5.2 DC Characteristics (1) (1 / 3)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	CAN input pin IRQ input pin MTU3 input pin POE3 input pin SCI input pin A/D trigger input pin NMI input pin GPT input pin LIN input pin RES#	V_{IH}	VCC×0.8	-	VCC+0.3	V	
		V_{IL}	-0.3	-	VCC×0.2		
		ΔV_T	VCC ×0.06	-	-		
	RIIC input pin (IICBus)	V_{IH}	VCC×0.7	-	VCC+0.3		
		V_{IL}	-0.3	-	VCC×0.3		
		ΔV_T	VCC ×0.05	-	-		
	Port 4*1 (also usable as an analog port)	V_{IH}	AVCC0 ×0.8	-	AVCC0 +0.3		
		V_{IL}	- 0.3	-	AVCC0 ×0.2		
		ΔV_T	AVCC0 ×0.06	-	-		
	Ports 5 and 6*1 (also usable as analog ports)	V_{IH}	AVCC ×0.8	-	AVCC +0.3		
		V_{IL}	-0.3	-	AVCC ×0.2		
		ΔV_T	AVCC ×0.06	-	-		
	Ports 1 to 3*1 Ports 7 to B*1 Ports D, E, and G*1	V_{IH}	VCC×0.8	-	VCC+0.3		
		V_{IL}	-0.3	-	VCC×0.2		
		ΔV_T	VCC ×0.06	-	-		
Input high voltage (except Schmitt trigger input pin)	MD pin, EMLE	V_{IH}	VCC×0.9	-	VCC+0.3	V	
	EXTAL RSPI input pin		VCC×0.8		VCC+0.3		
	RIIC input pin (SMBus)		2.1		VCC+0.3		Conditions 1 and 2
Input low voltage (except Schmitt trigger input pin)	MD pin, EMLE	V_{IL}	-0.3	-	VCC×0.1	V	
	EXTAL RSPI input pin		-0.3	-	VCC×0.2		
	RIIC input pin (SMBus)		-0.3	-	0.8		Conditions 1 and 2

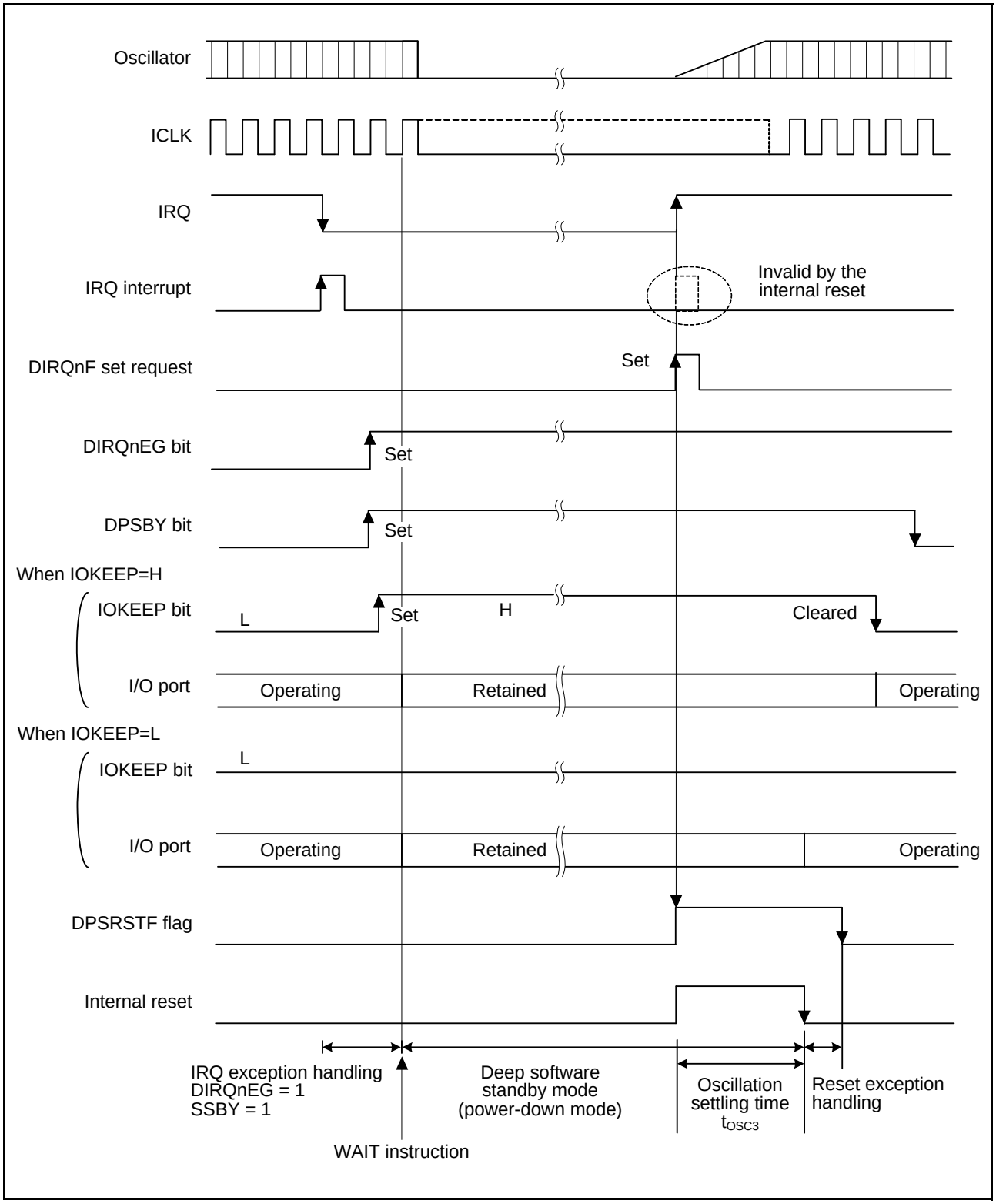

Figure 5.3 Oscillation Settling Timing after Deep Software Standby Mode

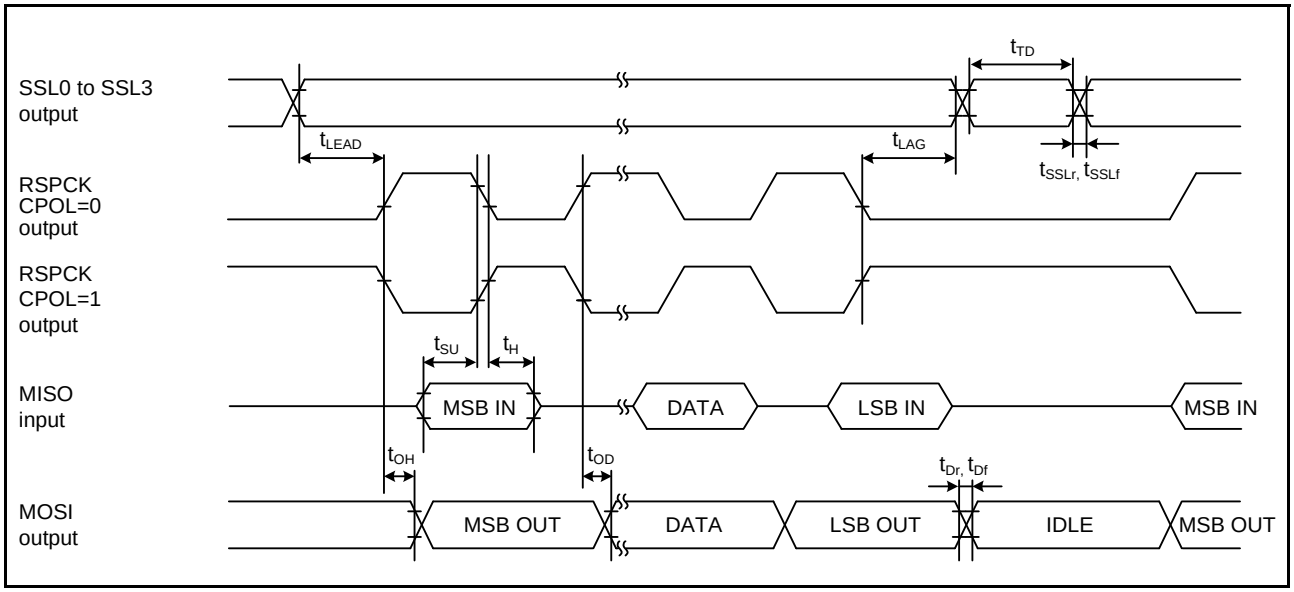

Figure 5.13 RSPI Timing (Master, CPHA = 1)

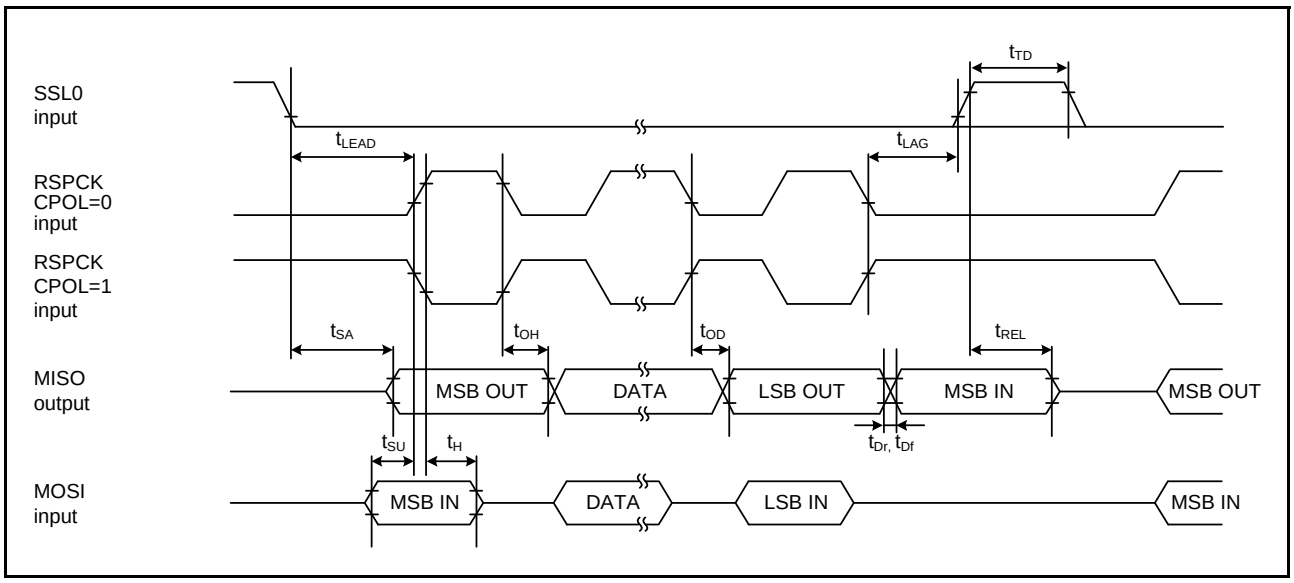

Figure 5.14 RSPI Timing (Slave, CPHA = 0)

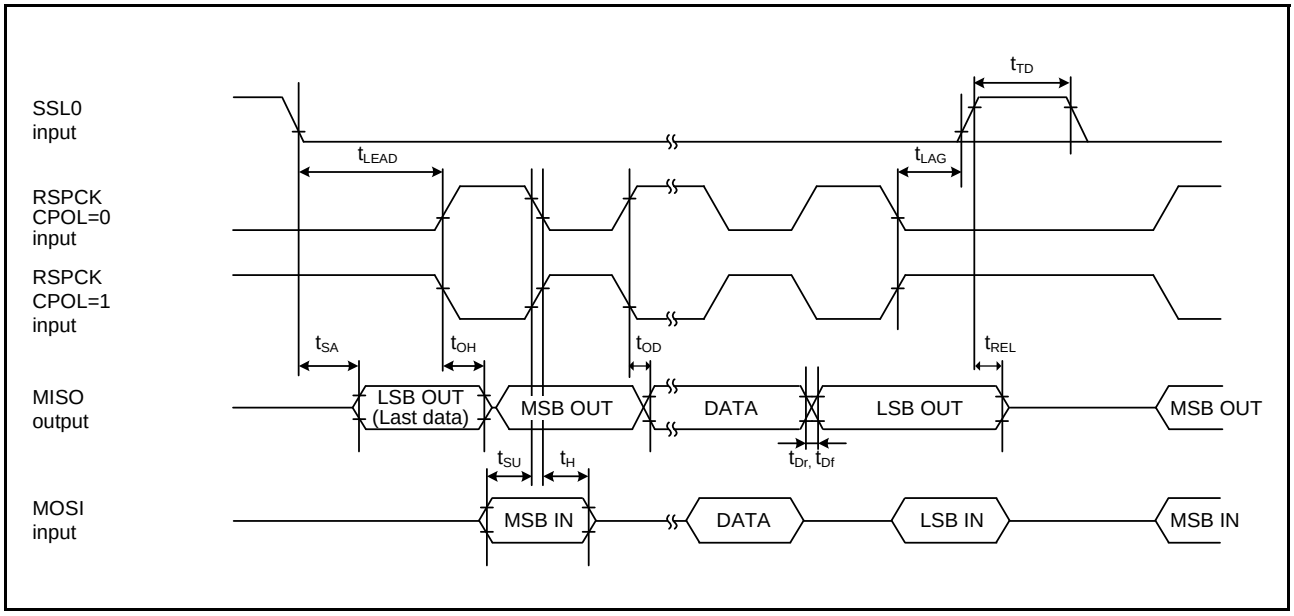

Figure 5.15 RSPI Timing (Slave, CPHA = 1)

Table 5.18 Comparator Characteristics

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC
Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog input capacitance	Cin	-	-	6	pF	
REFH pin offset voltage	Voff	-	-	5	mV	
REFL pin offset voltage		-	-	5	mV	
REFH input voltage range	Vin	1.7	-	AVcc – 0.3	V	
REFL input voltage range		0.3	-	AVcc – 1.7	V	
REFH reply time	tCR	-	-	1	µs	
REFL reply time	tCF	-	-	1	µs	

5.7 ROM (Flash Memory for Code Storage) Characteristics

Table 5.21 ROM (Flash Memory for Code Storage) Characteristics (1)

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Temperature range for the programming/erasure operation:
Ta = Topr. Ta is the same under conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Rewrite/erase cycle*1	N_{PEC}	1000	—	—	Times	
Data hold time	t_{DRP}	30*2	—	—	Year	Ta = +85C°

Note 1. Definition of rewrite/erase cycle:
The rewrite/erase cycle is the number of erasing for each block. When the rewrite/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 256-byte writing is performed 16 times for different addresses in 4-Kbyte block and then the entire block is erased, the rewrite/erase cycle is counted as one. However, writing to the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. The value is obtained from the reliability test.

Table 5.22 ROM (Flash Memory for Code Storage) Characteristics (2)

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Temperature range for the programming/erasure operation:
Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Programming time	256 bytes	t_{P256}	—	2	12	ms	PCLK = 50 MHz $N_{PEC} \leq 100$
	4 Kbytes	t_{P4K}	—	23	50	ms	
	16 Kbytes	t_{P16K}	—	90	200	ms	
	256 byte	t_{P256}	—	2.4	14.4	ms	PCLK = 50 MHz $N_{PEC} > 100$
	4 Kbytes	t_{P4K}	—	27.6	60	ms	
	16 Kbytes	t_{P16K}	—	108	240	ms	
Erasure time	4 Kbytes	t_{E4K}	—	25	60	ms	PCLK = 50 MHz $N_{PEC} \leq 100$
	16 Kbytes	t_{E16K}	—	100	240	ms	
	4 Kbytes	t_{E4K}	—	30	72	ms	PCLK = 50 MHz $N_{PEC} > 100$
	16 Kbytes	t_{E16K}	—	120	288	ms	
Suspend delay time during writing		t_{SPD}	—	—	120	µs	Figure 5.24 PCLK = 50 MHz
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	120	µs	
Second suspend delay time during erasing (in suspend priority mode)		t_{SESD2}	—	—	1.7	ms	
Suspend delay time during erasing (in erasure priority mode)		t_{SEED}	—	—	1.7	ms	