Renesas Electronics America Inc - R5F562T7BDFK#V3 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562t7bdfk-v3

Table 1.1 Outline of Specifications (4 / 5)

Classification	Module/Function	Description
Communications	CAN module (CAN) (as an optional function)	• 1 channel • 32 mailboxes
	Serial peripheral interface (RSPI)	• 1 unit • RSPI transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPI clock (RSPCK) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) Capable of handling serial transfer as a master or slave • Data formats Switching between MSB first and LSB first The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Buffered structure • Double buffers for both transmission and reception
	LIN module (LIN)	• 1 channel (LIN master) • Supports revisions 1.3, 2.0, and 2.1 of the LIN protocol
A/D converter	12-bit A/D converter (S12ADA)	• 12 bits (2 units x 4 channels) • 12-bit resolution • Conversion time: 1.0 μs per channel (in operation with A/D conversion clock ADCLK at 50 MHz) for AVCC = 4.0 to 5.5 V 2.0 μs per channel (in operation with A/D conversion clock ADCLK at 25 MHz) for AVCC0 = 3.0 to 3.6 V • Two basic operating modes Single mode and scan mode • Scan mode One-cycle scan mode Continuous scan mode 2-channel scan mode (Input ports of the A/D unit are divided into two groups in this mode, and the activation sources are separately selectable for each group.) • Sample-and-hold function A common sample-and-hold circuit for both units is included. Additionally, sample-and-hold circuit for each unit is included. (three channels per unit) • A/D-conversion register settings for each input pin. • Two registers for the result of conversion are provided for a single analog input pin of each unit (AN000 and AN100). • Three ways to start A/D conversion Conversion can be started by software, a conversion start trigger from a timer (MTU3 or GPT), or an external trigger signal. • Functionality for 8- or 10-bit precision output Right-shifting of the results of conversion for output by two or four bits is selectable. • Self-diagnostic function The self-diagnostic function internally generates three analog input voltages (VREFL0, VREFH0 x 1/2, VREFH0). • Amplification of input signals by a programmable gain amplifier (three channels per unit) Amplification rate: 2.0-, 2.5-, 3.077-, 3.636-, 4.0-, 4.444-, 5.0-, 5.714-, 6.667-, 10.0-, or 13.333-times amplification (a total of 11 steps) • Window comparators (three channels per unit)

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no.

Table 1.3 List of Products (1 / 2)

Group	Part No.	Order Part No.	Package	ROM Capacity	RAM Capacity	Data Flash Capacity	Power Supply Voltage	CAN	Operating Temp. Range
RX62T	R5F562TAADFH	R5F562TAADFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes	VCC/PLLVCC 4.0 to 5.5 V AVCC/AVCC0 4.0 to 5.5 V	Support-ed	-40 to +85°C (D version)
	R5F562TAADFP	R5F562TAADFP#V3	PLQP0100KB-A						
	R5F562TAADFF	R5F562TAADFF#V3	PLQP0080JA-A						
	R5F562TAGDFF	R5F562TAGDFF#V3	PLQP0080JA-A						
	R5F562TAADFM	R5F562TAADFM#V3	PLQP0064KB-A						
	R5F562TAADFK	R5F562TAADFK#V3	PLQP0064GA-A						
	R5F562T7ADFH	R5F562T7ADFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes			
	R5F562T7ADFP	R5F562T7ADFP#V3	PLQP0100KB-A						
	R5F562T7ADFF	R5F562T7ADFF#V3	PLQP0080JA-A						
	R5F562T7GDFF	R5F562T7GDFF#V3	PLQP0080JA-A						
	R5F562T7ADFM	R5F562T7ADFM#V3	PLQP0064KB-A						
	R5F562T7ADFK	R5F562T7ADFK#V3	PLQP0064GA-A						
	R5F562T6ADFF	R5F562T6ADFF#V3	PLQP0080JA-A	64 Kbytes	8 Kbytes				
	R5F562T6ADFM	R5F562T6ADFM#V3	PLQP0064KB-A						
	R5F562T6ADFK	R5F562T6ADFK#V3	PLQP0064GA-A						
	R5F562TABDFH	R5F562TABDFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes	VCC/PLLVCC 2.7 to 3.6 V AVCC/AVCC0 3.0 to 3.6 V or 4.0 to 5.5 V		
	R5F562TABDFP	R5F562TABDFP#V3	PLQP0100KB-A						
	R5F562TABDFF	R5F562TABDFF#V3	PLQP0080JA-A						
	R5F562TABDFM	R5F562TABDFM#V3	PLQP0064KB-A						
	R5F562TABDFK	R5F562TABDFK#V3	PLQP0064GA-A						
	R5F562T7BDFH	R5F562T7BDFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes			
	R5F562T7BDFP	R5F562T7BDFP#V3	PLQP0100KB-A						
	R5F562T7BDFF	R5F562T7BDFF#V3	PLQP0080JA-A						
	R5F562T7BDFM	R5F562T7BDFM#V3	PLQP0064KB-A						
	R5F562T7BDFK	R5F562T7BDFK#V3	PLQP0064GA-A						
	R5F562T6BDFF	R5F562T6BDFF#V3	PLQP0080JA-A	64 Kbytes	8 Kbytes				
	R5F562T6BDFM	R5F562T6BDFM#V3	PLQP0064KB-A						
	R5F562T6BDFK	R5F562T6BDFK#V3	PLQP0064GA-A						
	R5F562TADDFH	R5F562TADDFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes	4.0 to 5.5 V	Not Support-ed	
	R5F562TADDFP	R5F562TADDFP#V3	PLQP0100KB-A						
	R5F562TADDFF	R5F562TADDFF#V3	PLQP0080JA-A						
	R5F562TADDFM	R5F562TADDFM#V3	PLQP0064KB-A						
	R5F562TADDFK	R5F562TADDFK#V3	PLQP0064GA-A						
	R5F562T7DDFH	R5F562T7DDFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes			
	R5F562T7DDFP	R5F562T7DDFP#V3	PLQP0100KB-A						
	R5F562T7DDFF	R5F562T7DDFF#V3	PLQP0080JA-A						
	R5F562T7DDFM	R5F562T7DDFM#V3	PLQP0064KB-A						
	R5F562T7DDFK	R5F562T7DDFK#V3	PLQP0064GA-A						
	R5F562T6DDFF	R5F562T6DDFF#V3	PLQP0080JA-A	64 Kbytes	8 Kbytes				
	R5F562T6DDFM	R5F562T6DDFM#V3	PLQP0064KB-A						
	R5F562T6DDFK	R5F562T6DDFK#V3	PLQP0064GA-A						
	R5F562TAEDFH	R5F562TAEDFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes	2.7 to 3.6 V		
	R5F562TAEDFP	R5F562TAEDFP#V3	PLQP0100KB-A						
	R5F562TAEDFF	R5F562TAEDFF#V3	PLQP0080JA-A						
	R5F562TAEDFM	R5F562TAEDFM#V3	PLQP0064KB-A						
	R5F562TAEDFK	R5F562TAEDFK#V3	PLQP0064GA-A						

1.4 Pin Assignments

Figure 1.3 to Figure 1.7 show the pins assignments. Table 1.4 to Table 1.8 show the list of pins and pin functions.

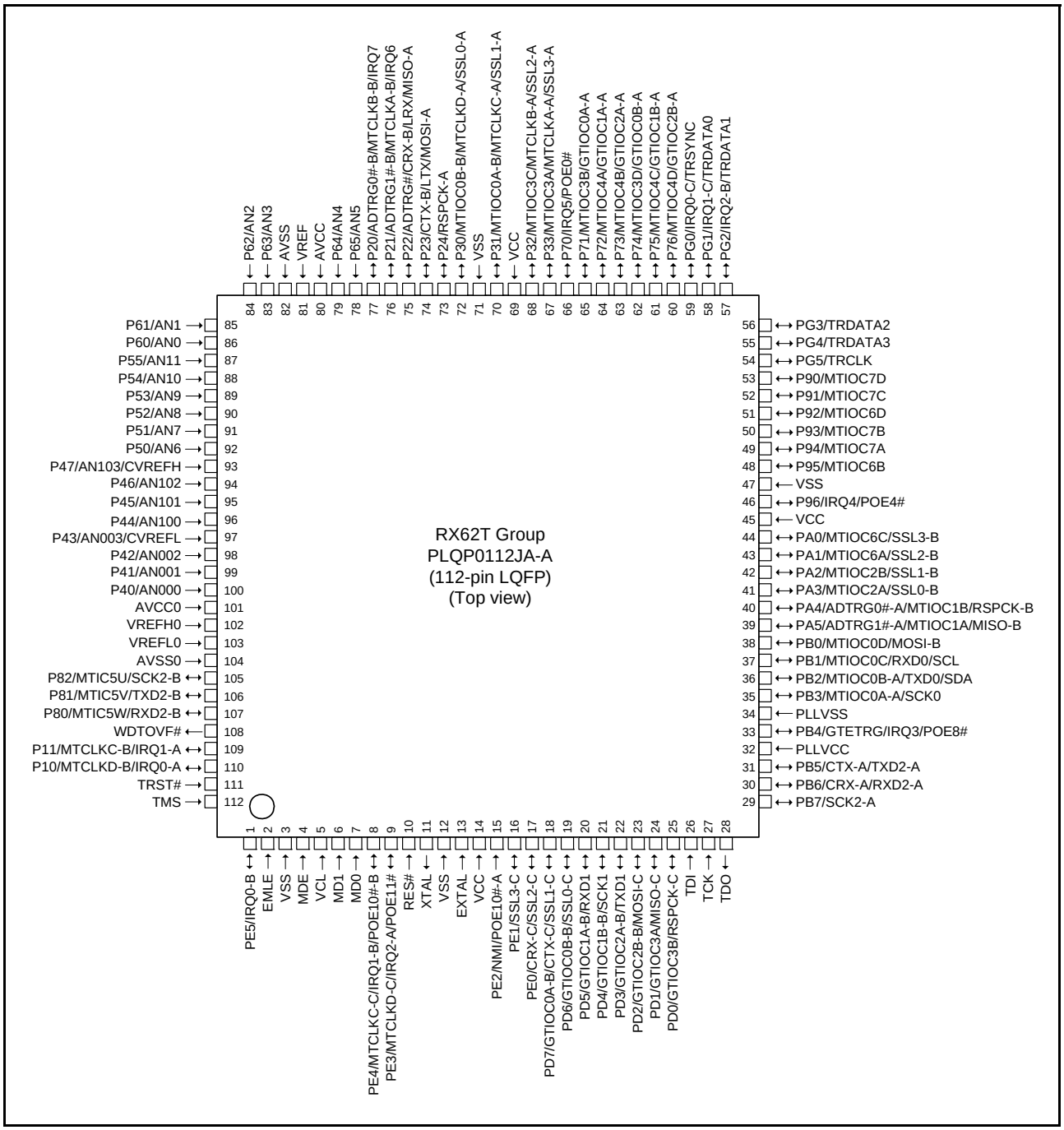


Figure 1.3 Pin Assignment of the 112-Pin LQFP

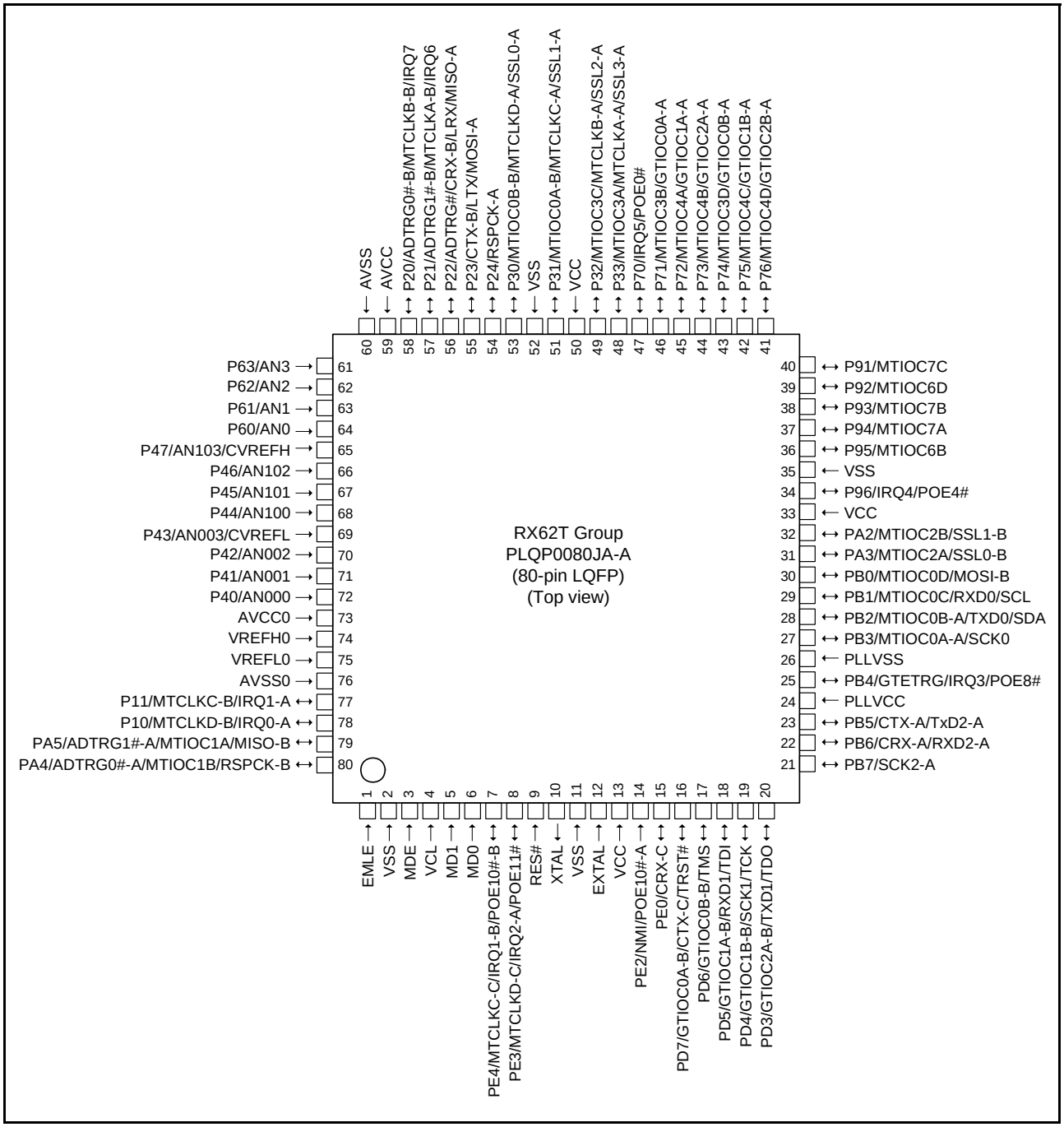


Figure 1.5 Pin Assignment of the 80-Pin LQFP

Table 1.5 List of Pins and Pin Functions (100-Pin LQFP) (1 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi-cation	Interrupt	POE	Debugging
1		PE5				IRQ0-B		
2	EMLE							
3	VSS							
4	MDE							
5	VCL							
6	MD1							
7	MD0							
8		PE4		MTCLKC-C		IRQ1-B	POE10#-B	
9		PE3		MTCLKD-C		IRQ2-A	POE11#	
10	RES#							
11	XTAL							
12	VSS							
13	EXTAL							
14	VCC							
15		PE2				NMI	POE10#-A	
16		PE1			SSL3-C			
17		PE0			CRX-C/ SSL2-C			
18		PD7		GTIOC0A-B	CTX-C/ SSL1-C			TRST#
19		PD6		GTIOC0B-B	SSL0-C			TMS
20		PD5		GTIOC1A-B	RXD1			TDI
21		PD4		GTIOC1B-B	SCK1			TCK
22		PD3		GTIOC2A-B	TXD1			TDO
23		PD2		GTIOC2B-B	MOSI-C			TRCLK
24		PD1		GTIOC3A	MISO-C			TRDATA3
25		PD0		GTIOC3B	RSPCK-C			TRDATA2
26		PB7			SCK2-A			TRDATA1
27		PB6			CRX-A/ RXD2-A			TRDATA0
28		PB5			CTX-A/ TXD2-A			TRSYNC
29	PLLVCC							
30		PB4		GTETRG		IRQ3	POE8#	
31	PLLVSS							
32		PB3		MTIOC0A-A	SCK0			
33		PB2		MTIOC0B-A	TXD0/SDA			
34		PB1		MTIOC0C	RXD0/SCL			
35		PB0		MTIOC0D	MOSI-B			
36		PA5	ADTRG1#-A	MTIOC1A	MISO-B			
37		PA4	ADTRG0#-A	MTIOC1B	RSPCK-B			
38		PA3		MTIOC2A	SSL0-B			
39		PA2		MTIOC2B	SSL1-B			
40		PA1		MTIOC6A	SSL2-B			

Table 1.7 List of Pins and Pin Functions (80-Pin LQFP: R5F562TxGDFF) (1 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communication	Interrupt	POE	Debugging
1	EMLE							
2	VSS							
3	MDE							
4	VCL							
5	MD1							
6	MD0							
7		PE4		MTCLKC-C		IRQ1-B	POE10#-B	
8		PE3		MTCLKD-C		IRQ2-A	POE11#	
9	RES#							
10	XTAL							
11	VSS							
12	EXTAL							
13	VCC							
14		PE2				NMI	POE10#-A	
15		PD7		GTIOC0A-B				TRST#
16		PD6		GTIOC0B-B				TMS
17		PD5		GTIOC1A-B	RXD1			TDI
18		PD4		GTIOC1B-B	SCK1			TCK
19		PD3		GTIOC2A-B	TXD1			TDO
20		PD2		GTIOC2B-B				
21		PB7			SCK2-A			
22		PB6			CRX-A/ RXD2-A			
23		PB5			CTX-A/ TXD2-A			
24	PLLVCC							
25		PB4		GTETRG		IRQ3	POE8#	
26	PLLVSS							
27		PB3		MTIOC0A-A	SCK0			
28		PB2		MTIOC0B-A	TXD0/SDA			
29		PB1		MTIOC0C	RXD0/SCL			
30		PB0		MTIOC0D				
31		PA5	ADTRG1#-A	MTIOC1A				
32		PA3		MTIOC2A				
33	VCC							
34		P96				IRQ4	POE4#	
35	VSS							
36		P95		MTIOC6B				
37		P94		MTIOC7A				
38		P93		MTIOC7B				
39		P92		MTIOC6D				
40		P91		MTIOC7C				
41		P90		MTIOC7D				

Table 1.8 List of Pins and Pin Functions (64-Pin LQFP) (1 / 2)

Pin No. (64-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi-cation	Interrupt	POE	Debugging
1	EMLE							
2	MDE							
3	VCL							
4	MD1							
5	MD0							
6	RES#							
7	XTAL							
8	VSS							
9	EXTAL							
10	VCC							
11		PE2				NMI	POE10#-A	
12		PD7		GTIOC0A-B				TRST#
13		PD6		GTIOC0B-B				TMS
14		PD5		GTIOC1A-B	RXD1			TDI
15		PD4		GTIOC1B-B	SCK1			TCK
16		PD3		GTIOC2A-B	TXD1			TDO
17		PB7			SCK2-A			
18		PB6			CRX-A/ RXD2-A			
19		PB5			CTX-A/ TXD2-A			
20	PLLVCC							
21		PB4		GTETRG		IRQ3	POE8#	
22	PLLVSS							
23		PB3		MTIOC0A-A	SCK0			
24		PB2		MTIOC0B-A	TXD0/SDA			
25		PB1		MTIOC0C	RXD0/SCL			
26		PB0		MTIOC0D	MOSI-B			
27		PA3		MTIOC2A	SSL0-B			
28		PA2		MTIOC2B	SSL1-B			
29		P94		MTIOC7A				
30		P93		MTIOC7B				
31		P92		MTIOC6D				
32		P91		MTIOC7C				
33		P76		MTIOC4D/ GTIOC2B-A				
34		P75		MTIOC4C/ GTIOC1B-A				
35		P74		MTIOC3D/ GTIOC0B-A				
36		P73		MTIOC4B/ GTIOC2A-A				
37		P72		MTIOC4A/ GTIOC1A-A				
38		P71		MTIOC3B/ GTIOC0A-A				
39		P70				IRQ5	POE0#	

1.5 Pin Functions

Table 1.9 lists the pin functions.

Table 1.9 Pin Functions (1 / 4)

Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply.
	VCL	Input	Connect this pin to VSS via a 0.1-μF capacitor. The capacitor should be placed close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
	PLLVCC	Input	Power supply pin for the PLL circuit. Connect it to the system power supply.
	PLLVSS	Input	Ground pin for the PLL circuit.
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
Operating mode control	MD0 MD1 MDE	Input	Pins for setting the operating mode. The signal levels on these pins must not be changed during operation.
System control	RES#	Input	Reset signal input pin. This LSI enters the reset state when this signal goes low.
	EMLE	Input	Input pin for the on-chip emulator enable signal. When the on-chip emulator is used, this pin should be driven high. When not used, it should be driven low.
On-chip emulator	TRST#	Input	On-chip emulator pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator.
	TMS	Input	
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TRCLK	Output	This pin outputs the clock for synchronization with the trace data. Not included in the 80-/64-pin versions.
	TRSYNC	Output	This pin indicates that output from the TRDATA0 to TRDATA3 pins is valid. Not included in the 80-/64-pin versions.
	TRDATA0 to TRDATA3	Output	These pins output the trace information. Not included in the 80-/64-pin versions.
Interrupt (ICU)	NMI	Input	Non-maskable interrupt request signal.
	IRQ0-A/IRQ0-B/IRQ0-C IRQ1-A/IRQ1-B/IRQ1-C IRQ2-A/IRQ2-B IRQ3 to IRQ7	Input	Interrupt request signals. The IRQ0-C/IRQ1-C/IRQ2-B pin is not included in the 100-pin version. The IRQ0-B/IRQ0-C/IRQ1-C/IRQ2-B pin is not included in the 80-pin version. The IRQ0-B/IRQ0-C/IRQ1-B/IRQ1-/IRQ2-A/IRQ2-B/IRQ4/IRQ6/IRQ7 pin is not included in the 64-pin version.

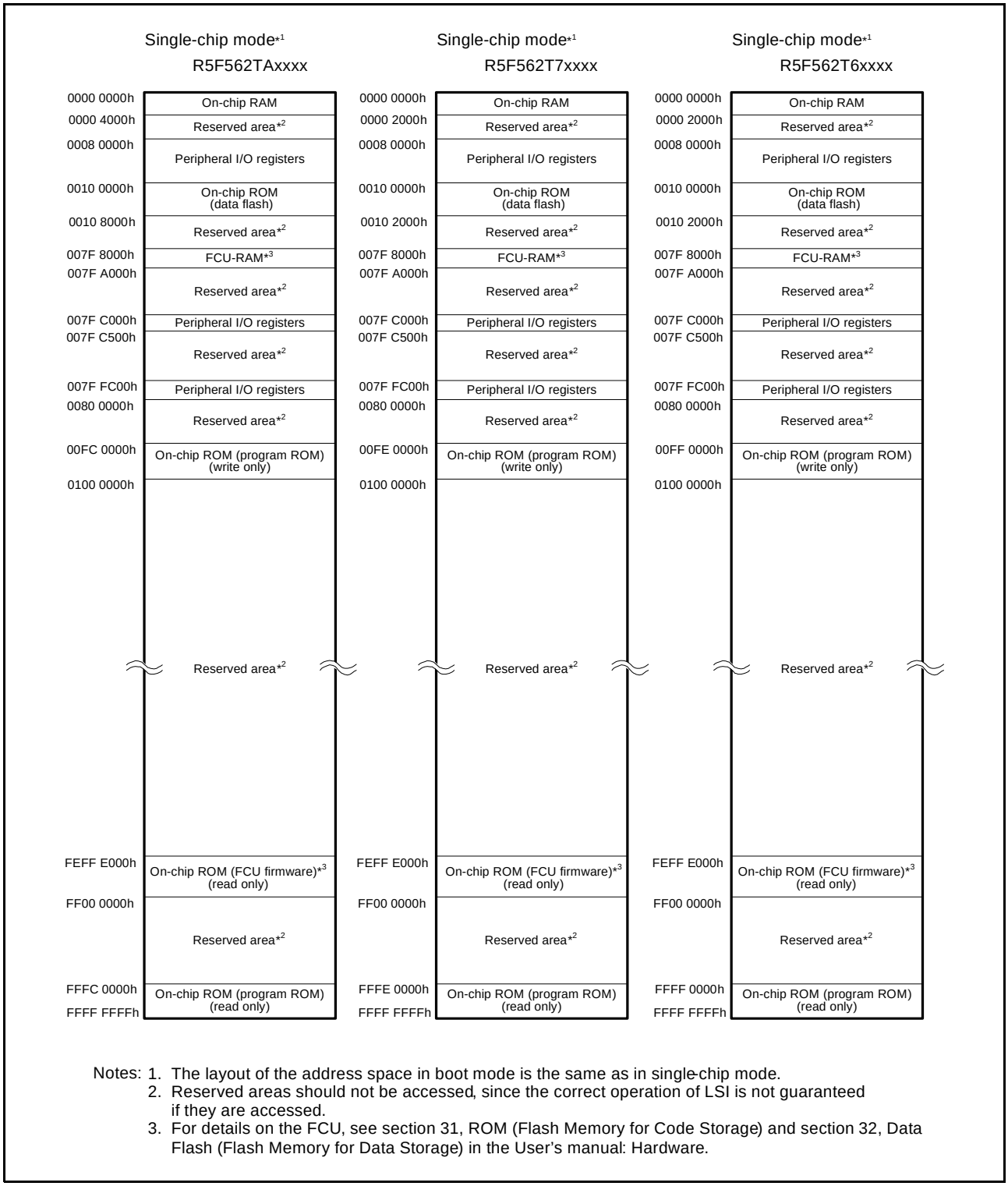
Table 1.9 Pin Functions (3 / 4)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCIb)	TXD0, TXD1, TXD2-A/TXD2-B	Output	Output pins for data transmission. The TXD2-B pin is not included in the 80-/64-pin versions.
	RXD0, RXD1, RXD2-A/ RXD2-B	Input	Input pins for data reception. The RXD2-B pin is not included in the 80-/64-pin versions.
	SCK0, SCK1, SCK2-A/ SCK2-B	I/O	Input/output pins for clock signals. The SCK2-B pin is not included in the 80-/64-pin versions.
I^2C bus interface (RIIC)	SCL	I/O	Input/output pin for I^2C bus interface clocks. Bus can be directly driven by the NMOS open drain output.
	SDA	I/O	Input/output pin for I^2C bus interface data. Bus can be directly driven by the NMOS open drain output.
CAN module (CAN) (as an optional function)	CRX-A/CRX-B/CRX-C	Input	Input pin for the CAN. The CRX-C pin is not included in the 64-pin version.
	CTX-A/CTX-B/CTX-C	Output	Output pin for the CAN. The CTX-C pin is not included in the 64-pin version.
LIN module (LIN)	LRX	Input	Input pin for the LIN.
	LTX	Output	Output pin for the LIN.
Serial peripheral interface (RSPI)	RSPCK-A/RSPCK-B/ RSPCK-C	I/O	Clock input/output pin for the RSPI. The RSPCK-C pin is not included in the 80-/64-pin versions.
	MOSI-A/MOSI-B/MOSI-C	I/O	Inputs or outputs data output from the master for the RSPI. The MOSI-C pin is not included in the 80-/64-pin versions.
	MISO-A/MISO-B/MISO-C	I/O	Inputs or outputs data output from the slave for the RSPI. The MISO-C pin is not included in the 80-/64-pin versions.
	SSL0-A/SSL0-B/SSL0-C	I/O	Select the slave for the RSPI. The SSL0-C/SSL1-C/SSL2-C/ SSL3-C pin is not included in the 80-/64-pin versions.
	SSL1-A/SSL1-B/SSL1-C SSL2-A/SSL2-B/SSL2-C SSL3-A/SSL3-B/SSL3-C	Output	
A/D converter	AN000 to AN003 AN100 to AN103	Input	Input pins for the analog signals to be processed by the 12-bit A/D converter.
	AN0 to AN11	Input	Input pins for the analog signals to be processed by the 10-bit A/D converter. The AN4 to AN11 pins are not included in the 80-pin version. Not included in the 64-pin version.
	ADTRG0#-A/ADTRG0#-B ADTRG1#-A/ADTRG1#-B ADTRG#	Input	Input pins for the external trigger signals that start the A/D conversion. The ADTRG0#-B/ADTRG1#-B/ADTRG# pin is not included in the 64-pin version.
	CVREFH	Input	Input pin for the high-level reference voltage to the comparator
	CVREFL	Input	Input pin for the low-level reference voltage to the comparator
Analog power supply	AVCC0	Input	Analog power supply pin for the 12-bit A/D converter. When the A/D converter is not in use, connect this pin to the system power supply.
	AVSS0	Input	Ground pin for the 12-bit A/D converter. Connect this pin to the system power supply (0 V).
	VREFH0	Input	Reference power supply pin for the 12-bit A/D converter. When the 12-bit A/D converter is not in use, connect this pin to the system power supply.
	VREFL0	Input	Ground pin of the reference power supply pin for the 12-bit A/D converter. When the 12-bit A/D converter is not in use, connect this pin to the system power supply (0 V).
	AVCC	Input	Analog power supply pin for the 10-bit A/D converter. When the A/D converter is not in use, connect this pin to the system power supply. Not included in the 64-pin version.
	AVSS	Input	Ground pin for the 10-bit A/D converter. Connect this pin to the system power supply (0 V). Not included in the 64-pin version.
	VREF	Input	Reference power supply pin for the 10-bit A/D converter. When the 10-bit A/D converter is not in use, connect this pin to the system power supply. Not included in the 80-/64-pin versions.

3. Address Space

3.1 Address Space

This LSI has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas. Figure 3.1 shows the memory maps.



Notes: 1. The layout of the address space in boot mode is the same as in single-chip mode.
2. Reserved areas should not be accessed, since the correct operation of LSI is not guaranteed if they are accessed.
3. For details on the FCU, see section 31, ROM (Flash Memory for Code Storage) and section 32, Data Flash (Flash Memory for Data Storage) in the User's manual: Hardware.

Figure 3.1 Memory Map (RX62T Group)

4. I/O Registers

This section gives information on the on-chip I/O register addresses and bit configurations. The information is given as shown below. Notes on writing to registers are also given at the end.

(1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to functional modules (abbreviations).
- The number of access cycles indicates the number of states based on the specified reference clock.
- Among the I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.
- A unit of access is specified for each register. Access other than in the specified unit is prohibited.

(2) I/O register bits

- Bit configurations of the registers are listed in the same order as the register addresses.
- Reserved bits are indicated by "—" in the bit name column.
- Space in the bit name field indicates that the entire register is allocated to either the counter or data.
- For the registers of 16 or 32 bits, the MSB is listed first.

(3) Notes on writing to I/O registers

When writing to an I/O register, the CPU starts executing the subsequent instruction before completing I/O register write. This may cause the subsequent instruction to be executed before the post-update I/O register value is reflected on the operation.
As described in the following examples, special care is required for the cases in which the subsequent instruction must be executed after the post-update I/O register value is actually reflected.

[Examples of cases requiring special care]

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERm of the ICU (interrupt request enable bit)*1 cleared to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

Note 1. See section 11.2.2, Interrupt Request Enable Register m (IERm) (m = 02h to 1Fh) in the User's manual: Hardware.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

Table 4.1 List of I/O Registers (Address Order) (13 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 C065h	PORT5	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C066h	PORT6	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C067h	PORT7	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C068h	PORT8	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C069h	PORT9	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C06Ah	PORTA	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C06Bh	PORTB	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C06Dh	PORTD	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C06Eh	PORTE	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C070h	PORTG	Input buffer control register	ICR*1	8	8	2, 3 PCLK*3
0008 C108h	IOPORT	Port function register 8	PF8IRQ	8	8	2, 3 PCLK*3
0008 C109h	IOPORT	Port function register 9	PF9IRQ	8	8	2, 3 PCLK*3
0008 C10Ah	IOPORT	Port function register A	PFAADC	8	8	2, 3 PCLK*3
0008 C10Ch	IOPORT	Port function register C	PFCMTU	8	8	2, 3 PCLK*3
0008 C10Dh	IOPORT	Port function register D	PFDGPT	8	8	2, 3 PCLK*3
0008 C10Fh	IOPORT	Port function register F	PFFSCI	8	8	2, 3 PCLK*3
0008 C110h	IOPORT	Port function register G	PFGSPI	8	8	2, 3 PCLK*3
0008 C111h	IOPORT	Port function register H	PFHSPI	8	8	2, 3 PCLK*3
0008 C113h	IOPORT	Port function register J	PFJCAN	8	8	2, 3 PCLK*3
0008 C114h	IOPORT	Port function register K	PFKLIN	8	8	2, 3 PCLK*3
0008 C116h	IOPORT	Port function register M	PFMPOE	8	8	2, 3 PCLK*3
0008 C117h	IOPORT	Port function register N	PFNPOE	8	8	2, 3 PCLK*3
0008 C280h	SYSTEM	Deep standby control register	DPSBYCR	8	8	4, 5 PCLK*3
0008 C281h	SYSTEM	Deep standby wait control register	DPSWCR	8	8	4, 5 PCLK*3
0008 C282h	SYSTEM	Deep standby interrupt enable register	DPSIER	8	8	4, 5 PCLK*3
0008 C283h	SYSTEM	Deep standby interrupt flag register	DPSIFR	8	8	4, 5 PCLK*3
0008 C284h	SYSTEM	Deep standby interrupt edge register	DPSIEGR	8	8	4, 5 PCLK*3
0008 C285h	SYSTEM	Reset status register	RSTSR	8	8	4, 5 PCLK*3
0008 C289h	FLASH	Flash write erase protection register	FWEPROR	8	8	4, 5 PCLK*3
0008 C28Ch	SYSTEM	Key code register for low-voltage detection control register	LVDKEYR	8	8	4, 5 PCLK*3
0008 C28Dh	SYSTEM	Voltage detection control register	LVDCR	8	8	4, 5 PCLK*3
0008 C290h	SYSTEM	Deep standby backup register 0	DPSBKR0	8	8	4, 5 PCLK*3
0008 C291h	SYSTEM	Deep standby backup register 1	DPSBKR1	8	8	4, 5 PCLK*3
0008 C292h	SYSTEM	Deep standby backup register 2	DPSBKR2	8	8	4, 5 PCLK*3
0008 C293h	SYSTEM	Deep standby backup register 3	DPSBKR3	8	8	4, 5 PCLK*3
0008 C294h	SYSTEM	Deep standby backup register 4	DPSBKR4	8	8	4, 5 PCLK*3
0008 C295h	SYSTEM	Deep standby backup register 5	DPSBKR5	8	8	4, 5 PCLK*3
0008 C296h	SYSTEM	Deep standby backup register 6	DPSBKR6	8	8	4, 5 PCLK*3
0008 C297h	SYSTEM	Deep standby backup register 7	DPSBKR7	8	8	4, 5 PCLK*3
0008 C298h	SYSTEM	Deep standby backup register 8	DPSBKR8	8	8	4, 5 PCLK*3
0008 C299h	SYSTEM	Deep standby backup register 9	DPSBKR9	8	8	4, 5 PCLK*3
0008 C29Ah	SYSTEM	Deep standby backup register 10	DPSBKR10	8	8	4, 5 PCLK*3
0008 C29Bh	SYSTEM	Deep standby backup register 11	DPSBKR11	8	8	4, 5 PCLK*3

Table 4.2 List of I/O Registers (Bit Order) (2 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
MPU	REPAGE0				REPN[27:0]				
					REPN[27:0]				
					REPN[27:0]				
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE1				RSPN[27:0]				
					RSPN[27:0]				
					RSPN[27:0]				
			RSPN[27:0]			—	—	—	—
MPU	REPAGE1				REPN[27:0]				
					REPN[27:0]				
					REPN[27:0]				
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE2				RSPN[27:0]				
					RSPN[27:0]				
					RSPN[27:0]				
			RSPN[27:0]			—	—	—	—
MPU	REPAGE2				REPN[27:0]				
					REPN[27:0]				
					REPN[27:0]				
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE3				RSPN[27:0]				
					RSPN[27:0]				
					RSPN[27:0]				
			RSPN[27:0]			—	—	—	—
MPU	REPAGE3				REPN[27:0]				
					REPN[27:0]				
					REPN[27:0]				
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE4				RSPN[27:0]				
					RSPN[27:0]				
					RSPN[27:0]				
			RSPN[27:0]			—	—	—	—
MPU	REPAGE4				REPN[27:0]				
					REPN[27:0]				
					REPN[27:0]				
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE5				RSPN[27:0]				
					RSPN[27:0]				
					RSPN[27:0]				
			RSPN[27:0]			—	—	—	—
MPU	REPAGE5				REPN[27:0]				
					REPN[27:0]				
					REPN[27:0]				
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE6				RSPN[27:0]				
					RSPN[27:0]				
					RSPN[27:0]				
			RSPN[27:0]			—	—	—	—
MPU	REPAGE6				REPN[27:0]				
					REPN[27:0]				
					REPN[27:0]				
			REPN[27:0]				UAC[2:0]		V

Table 4.2 List of I/O Registers (Bit Order) (13 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
S12AD0	ADRD*2	DIAGST[1:0]		—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD0	ADDR0A*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD0	ADDR1*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD0	ADDR2*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD0	ADDR3*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD0	ADDR0B*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD0	ADSSTR								
S12AD1	ADCSR	ADST	ADCS[1:0]		ADIE	CKS[1:0]		TRGE	EXTRG
S12AD1	ADANS	—	—	CH[1:0]		—	PG102SEL	PG101SEL	PG100SEL
		—	—	—	—	—	PG102EN	PG101EN	PG100EN
S12AD1	ADPG	—	—	—	—	PG102GAIN[3:0]			
		PG101GAIN[3:0]				PG100GAIN[3:0]			
S12AD1	ADCER	ADRFMT	—	ADIEW	ADIE2	DIAGM	DIAGLD	DIAGVAL[1:0]	
		—	—	ACE	—	—	ADPRC[1:0]		SHBYP
S12AD1	ADSTRGR	—	—	—	ADSTRS1[4:0]				
		—	—	—	ADSTRS0[4:0]				
S12AD1	ADRD*2	DIAGST[1:0]		—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD1	ADDR0A*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD1	ADDR1*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD1	ADDR2*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD1	ADDR3*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD1	ADDR0B*2	—	—	—	—	AD11	AD10	AD9	AD8
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
S12AD1	ADSSTR								
PORT1	DDR	—	—	—	—	—	—	B1	B0
PORT2	DDR	—	—	—	B4	B3	B2	B1	B0
PORT3	DDR	—	—	—	—	B3	B2	B1	B0
PORT7	DDR	—	B6	B5	B4	B3	B2	B1	B0
PORT8	DDR	—	—	—	—	—	B2	B1	B0
PORT9	DDR	—	B6	B5	B4	B3	B2	B1	B0
PORTA	DDR	—	—	B5	B4	B3	B2	B1	B0
PORTB	DDR	B7	B6	B5	B4	B3	B2	B1	B0
PORTD	DDR	B7	B6	B5	B4	B3	B2	B1	B0
PORTE	DDR	—	—	B5	B4	B3	—	B1	B0
PORTG	DDR	—	—	B5	B4	B3	B2	B1	B0
PORT1	DR	—	—	—	—	—	—	B1	B0
PORT2	DR	—	—	—	B4	B3	B2	B1	B0
PORT3	DR	—	—	—	—	B3	B2	B1	B0
PORT7	DR	—	B6	B5	B4	B3	B2	B1	B0

Table 4.2 List of I/O Registers (Bit Order) (16 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
POE	POECR2	—	—	—	—	—	MTU3BDZE	MTU4ACZE	MTU4BDZE
		—	—	—	—	—	MTU6BDZE	MTU7ACZE	MTU7BDZE
POE	POECR3	—	—	—	—	—	—	GPT3ABZE	GPT2ABZE
		—	—	—	—	—	—	GPT1ABZE	GPT0ABZE
POE	POECR4	—	—	IC5ADDMT67ZE	IC4ADDMT67ZE	IC3ADDMT67ZE	—	IC1ADDMT67ZE	CMADDMT67ZE
		—	—	IC5ADDMT34ZE	IC4ADDMT34ZE	IC3ADDMT34ZE	IC2ADDMT34ZE	—	CMADDMT34ZE
POE	POECR5	—	—	—	—	—	—	—	—
		—	—	IC5ADDMT0ZE	IC4ADDMT0ZE	—	IC2ADDMT0ZE	IC1ADDMT0ZE	CMADDMT0ZE
POE	POECR6	—	—	—	IC4ADDGPT23ZE	IC3ADDGPT23ZE	IC2ADDGPT23ZE	IC1ADDGPT23ZE	CMADDGPT23ZE
		—	—	IC5ADDGPT01ZE	—	IC3ADDGPT01ZE	IC2ADDGPT01ZE	IC1ADDGPT01ZE	CMADDGPT01ZE
POE	ICSR4	—	—	—	POE10F	—	—	POE10E	PIE4
		—	—	—	—	—	—	POE10M[1:0]	
POE	ALR1	—	—	—	—	—	—	—	—
		OLSEN	—	OLSG2B	OLSG2A	OLSG1B	OLSG1A	OLSG0B	OLSG0A
POE	ICSR5	—	—	—	POE11F	—	—	POE11E	PIE5
		—	—	—	—	—	—	POE11M[1:0]	
CAN0*3	MB.ID	IDE	RTR	—			SID[10:0]		
				SID[10:0]				EID[17:0]	
					EID[17:0]				
					EID[17:0]				
	MB.DLC	—	—	—	—	—	—	—	—
		—	—	—	—		DLC[3:0]		
	MB.DATA 0 to 7								
	MB.TS				TSH[7:0]				
					TSL[7:0]				
CAN0*3	MKR0	—	—	—			SID[10:0]		
				SID[10:0]				EID[17 0]	
					EID[17:0]				
					EID[17:0]				
CAN0*3	MKR1	—	—	—			SID[10:0]		
				SID[10:0]				EID[17 0]	
					EID[17:0]				
					EID[17:0]				
CAN0*3	MKR2	—	—	—			SID[10:0]		
				SID[10:0]				EID[17 0]	
					EID[17:0]				
					EID[17:0]				
CAN0*3	MKR3	—	—	—			SID[10:0]		
				SID[10:0]				EID[17 0]	
					EID[17:0]				
					EID[17:0]				
CAN0*3	MKR4	—	—	—			SID[10:0]		
				SID[10:0]				EID[17 0]	
					EID[17:0]				
					EID[17:0]				

Table 4.2 List of I/O Registers (Bit Order) (18 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
CAN0*3	AFSR	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
CAN0*3	TCR	—	—	—	—	—	TSTM[1:0]		TSTE
LIN0	LWBR	—	—	—	—	—	—	—	LWBR0
LIN0	LBRP0								
LIN0	LBRP1								
LIN0	LSTC								LSTM
LIN0	L0MD	—	—	—	—	LCKS[1:0]		—	—
LIN0	L0BRK	—	—	BDT[1:0]			BLT[3:0]		
LIN0	L0SPC	—	—	IBS[1:0]		—		IBSH[2:0]	
LIN0	L0WUP		WUTL[3:0]			—	—	—	—
LIN0	L0IE	—	—	—	—	—	ERRIE	FRCIE	FTCIE
LIN0	L0EDE	—	—	—	—	FERE	FTERE	PBERE	BERE
LIN0	L0C	—	—	—	—	—	—	OM1	OM0
LIN0	L0TC	—	—	—	—	—	—	RTS	FTS
LIN0	L0MST	—	—	—	—	—	—	OMM1	OMM0
LIN0	L0ST	HTRC	D1RC	—	—	ERR	—	FRC	FTC
LIN0	L0EST	—	—	CSER	—	FER	FTER	PBER	BER
LIN0	L0RFC	—	FSM	CSM	RFT		RFDL[3:0]		
LIN0	L0IDB	IDP				ID			
LIN0	L0CBR								
LIN0	L0DB1								
LIN0	L0DB2								
LIN0	L0DB3								
LIN0	L0DB4								
LIN0	L0DB5								
LIN0	L0DB6								
LIN0	L0DB7								
LIN0	L0DB8								
MTU3	TCR		CCLR[2:0]			CKEG[1:0]		TPSC[2:0]	
MTU4	TCR		CCLR[2:0]			CKEG[1:0]		TPSC[2:0]	
MTU3	TMDR1	—	—	BFB	BFA			MD[3:0]	
MTU4	TMDR1	—	—	BFB	BFA			MD[3:0]	
MTU3	TIORH		IOB[3:0]					IOA[3:0]	
MTU3	TIORL		IOD[3:0]					IOC[3:0]	
MTU4	TIORH		IOB[3:0]					IOA[3:0]	
MTU4	TIORL		IOD[3:0]					IOC[3:0]	
MTU3	TIER	TTGE	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA
MTU4	TIER	TTGE	TTGE2	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA
MTU	TOERA	—	—	OE4D	OE4C	OE3D	OE4B	OE4A	OE3B
MTU	TGCRA	—	BDC	N	P	FB	WF	VF	UF
MTU	TOCR1A	—	PSYE	—	—	TOCL	TOCS	OLSN	OLSP
MTU	TOCR2A	BF[1:0]		OLS3N	OLS3P	OLS2N	OLS2P	OLS1N	OLS1P
MTU3	TCNT								
MTU4	TCNT								
MTU	TCDRA								
MTU	TDDRA								

5.3.2 Control Signal Timing

Table 5.8 Control Signal Timing

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item	Symbol	Min.	Max.	Unit	Test Conditions
RES# pulse width (except for programming or erasure of the ROM or data-flash memory or blank checking of the data-flash memory*1)	t_{RESW}*2	20	-	t_{Icyc}*4	Figure 5.5
		1.5	-	µs	
Internal reset time*3	t_{RESW2}	35	-	µs	
NMI pulse width	t_{NMIW}	200	-	ns	Figure 5.6
IRQ pulse width	t_{IRQW}	200	-	ns	Figure 5.7

Note 1. For a reset by the signal on the RES# pin during programming or erasure of the ROM or data-flash memory or during blank checking of the data-flash memory, see section 31.12, Usage Notes in section 31, ROM (Flash Memory for Code Storage) in the User's manual: Hardware.
Note 2. Both the time and the number of cycles should satisfy the specifications.
Note 3. This is to specify the FCU reset.
Note 4. ICLK cycles.

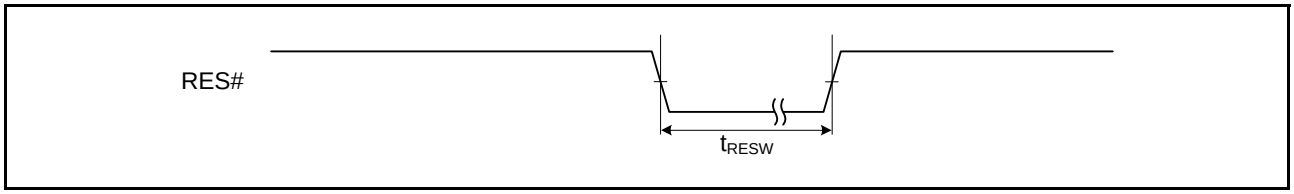


Figure 5.5 Reset Input Timing

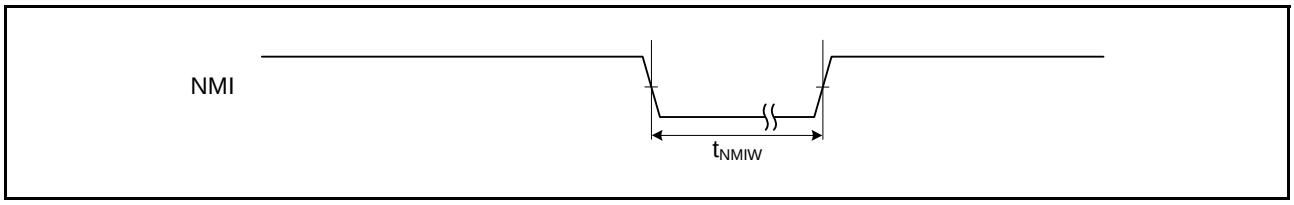


Figure 5.6 NMI Interrupt Input Timing

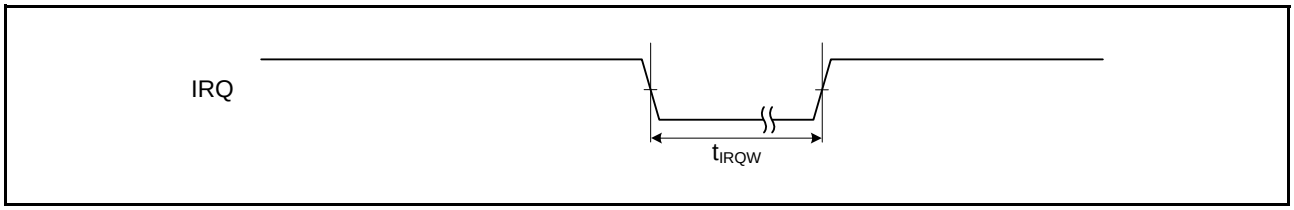


Figure 5.7 IRQ Interrupt Input Timing

Table 5.11 Timing of On-Chip Peripheral Modules (3)

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item			Symbol	Min.	Max.	Unit	Test Conditions
RSPI	RSPCK clock cycle	Master	t_{SPcyc}	4	4096	t_{Pcyc}	Figure 5.11
		Slave		8	4096		
	RSPCK clock high pulse width	Master	t_{SPCKWH}	(t_{Spcyc} - t_{SPCKR} - t_{SPCKF}) / 2-3	-	ns	
		Slave		(t_{Spcyc} - t_{SPCKR} - t_{SPCKF}) / 2	-		
	RSPCK clock low pulse width	Master	t_{SPCKWL}	(t_{Spcyc} - t_{SPCKR} - t_{SPCKF}) / 2-3	-	ns	
		Slave		(t_{Spcyc} - t_{SPCKR} - t_{SPCKF}) / 2	-		
	RSPCK clock rise/fall time	Output	t_{SPCKR} t_{SPCKF}	-	5	ns	
		Input		-	1	µs	
	Data input setup time	Master	t_{SU}	25	-	ns	Figure 5.12 to Figure 5.15
		Slave		0	-		
	Data input hold time	Master	t_H	0	-	ns	
		Slave		20+2×t_{Pcyc}	-		
	SSL setup time	Master	t_{LEAD}	1	8	t_{SPcyc}	
		Slave		4	-	t_{Pcyc}	
	SSL hold time	Master	t_{LAG}	1	8	t_{SPcyc}	
		Slave		4	-	t_{Pcyc}	
	Data output delay time	Master	t_{OD}	-	20	ns	
		Slave		-	3×t_{Pcyc} +40		
	Data output hold time	Master	t_{OH}	0	-	ns	
		Slave		0	-		
	Successive transmission delay time	Master	t_{TD}	t_{SPcyc}+2×t_{Pcyc}	8×t_{SPcyc} +2×t_{Pcyc}	ns	
		Slave		4×t_{Pcyc}	-		
	MOSI, MISO rise/fall time	Output	t_{DR} t_{DF}	-	15	ns	Figure 5.12 to Figure 5.15
		Input		-	1	µs	
	SSL rise/fall time	Output	t_{SSLR} t_{SSLF}	-	15	ns	
		Input		-	1	µs	
	Slave access time		t_{SA}	-	4	t_{Pcyc}	Figure 5.12 to Figure 5.15
	Slave output release time		t_{REL}	-	3	t_{Pcyc}	

Note: • Note 1: t_{Pcyc}: PCLK cycle

Table 5.17 Characteristics of the Programmable Gain Amplifier

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog input capacitance		Cin	-	-	6	pF	
Input offset voltage		Voff	-	-	8	mV	
Input voltage range (Vin)	Gain × 2.000	Vin	0.050 x AVcc	-	0.450 x AVcc	V	
	Gain × 2.500		0.047 x AVcc	-	0.360 x AVcc		
	Gain × 3.077		0.045 x AVcc	-	0.292 x AVcc		
	Gain × 3.636		0.042 x AVcc	-	0.247 x AVcc		
	Gain × 4.000		0.040 x AVcc	-	0.212 x AVcc		
	Gain × 4.444		0.036 x AVcc	-	0.191 x AVcc		
	Gain × 5.000		0.033 x AVcc	-	0.170 x AVcc		
	Gain × 5.714		0.031 x AVcc	-	0.148 x AVcc		
	Gain × 6.667		0.029 x AVcc	-	0.127 x AVcc		
	Gain × 10.000		0.025 x AVcc	-	0.08 x AVcc		
	Gain × 13.333		0.023 x AVcc	-	0.06 x AVcc		
Slew rate		SR	10	-	-	V/µs	
Gain error	Gain × 2.000	-	-	-	1	%	
	Gain × 2.500		-	-	1		
	Gain × 3.077		-	-	1		
	Gain × 3.636		-	-	1.5		
	Gain × 4.000		-	-	1.5		
	Gain × 4.444		-	-	2		
	Gain × 5.000		-	-	2		
	Gain × 5.714		-	-	2		
	Gain × 6.667		-	-	3		
	Gain × 10.000		-	-	4		
	Gain × 13.333		-	-	4		

5.5 Power-on Reset Circuit, Voltage Detection Circuit Characteristics

Table 5.19 Power-on Reset Circuit, Voltage Detection Circuit Characteristics

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 and 2.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	2.48	2.60	2.72	V	Figure 5.20
	Voltage detection circuit (LVD)	Vdet1	2.68	2.80	2.92		Figure 5.21
		Vdet2	2.98	3.10	3.22		Figure 5.22
Internal reset time		t_{POR}	20	35	50	ms	Figure 5.21 and Figure 5.22
Min. VCC down time*1		t_{VOFF}	200	-	-	us	Figure 5.20 to Figure 5.22
Reply delay time		tdet	-	-	200	us	

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	3.70	3.90	4.10	V	Figure 5.20
	Voltage detection circuit (LVD)	Vdet1	3.95	4.15	4.35		Figure 5.21
		Vdet2	4.40	4.60	4.80		Figure 5.22
Internal reset time		t_{POR}	20	35	50	ms	Figure 5.21 and Figure 5.22
Min. VCC down time*1		t_{VOFF}	200	-	-	us	Figure 5.20 to Figure 5.22
Reply delay time		tdet	-	-	200	us	

Note 1. The power-off time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det1}, and V_{det2} for the POR/ LVD.

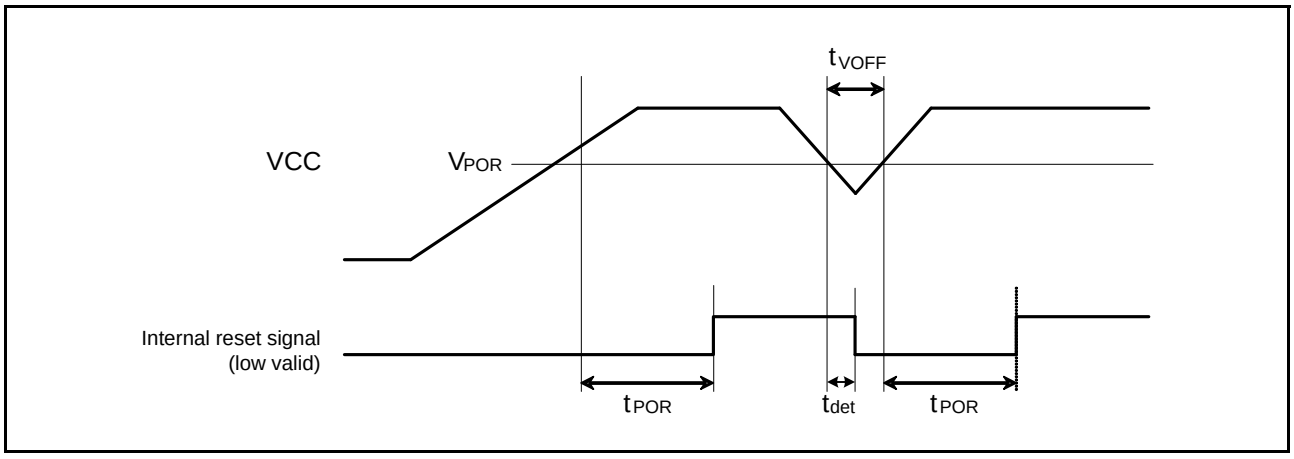


Figure 5.20 Power-on Reset Timing