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Details

Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I ² C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562t7bdfm-v1

Table 1.5 List of Pins and Pin Functions (100-Pin LQFP) (3 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi- cation	Interrupt	POE	Debugging
77		P60	AN0					
78		P55	AN11					
79		P54	AN10					
80		P53	AN9					
81		P52	AN8					
82		P51	AN7					
83		P50	AN6					
84		P47	AN103/ CVREFH					
85		P46	AN102					
86		P45	AN101					
87		P44	AN100					
88		P43	AN003/ CVREFL					
89		P42	AN002					
90		P41	AN001					
91		P40	AN000					
92	AVCC0							
93	VREFH0							
94	VREFL0							
95	AVSS0							
96		P82		MTIC5U	SCK2-B			
97		P81		MTIC5V	TXD2-B			
98		P80		MTIC5W	RXD2-B			
99		P11		MTCLKC-B		IRQ1-A		
100		P10		MTCLKD-B		IRQ0-A		

Table 1.7 List of Pins and Pin Functions (80-Pin LQFP: R5F562TxGDFF) (3 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communication	Interrupt	POE	Debugging
76	AVSS0							
77		P82		MTIC5U	SCK2-B			
78		P81		MTIC5V	TXD2-B			
79		P80		MTIC5W	RXD2-B			
80		P10		MTCLKD-B		IRQ0-A		

Table 1.9 Pin Functions (2 / 4)

Classifications	Pin Name	I/O	Description
Multi-function timer pulse unit 3 (MTU3)	MTIOC0A-A/MTIOC0A-B MTIOC0B-A/MTIOC0B-B MTIOC0C, MTIOC0D	I/O	The MTU0.TGRA to MTU0.TGRD input capture input/output compare output/PWM output pins.
	MTIOC1A, MTIOC1B	I/O	The MTU1.TGRA and MTU1.TGRB input capture input/output compare output/PWM output pins.
	MTIOC2A, MTIOC2B	I/O	The MTU2.TGRA and MTU2.TGRB input capture input/output compare output/PWM output pins.
	MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D	I/O	The MTU3.TGRA and MTU3.TGRD input capture input/output compare output/PWM output pins. Pins MTIOC3B and MTIOC3D can be used for large-current output.
	MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D	I/O	The MTU4.TGRA and MTU4.TGRD input capture input/output compare output/PWM output pins. These pins can be used for large-current output.
	MTIC5U, MTIC5V, MTIC5W	Input	The MTU5.TGRU, MTU5.TGRV, and MTU5.TGRW input capture input/dead time compensation input pins. Not included in the 80-/64-pin versions.
	MTIOC6A, MTIOC6B MTIOC6C, MTIOC6D	I/O	The MTU6.TGRA to MTU6.TGRD input capture input/output compare output/PWM output pins. Pins MTIOC6B and MTIOC6D can be used for large-current output. The MTIOC6A/MTIOC6C pin is not included in the 80-pin version. The MTIOC6A/MTIOC6B/MTIOC6C pin is not included in the 64-pin version.
	MTIOC7A, MTIOC7B MTIOC7C, MTIOC7D	I/O	The MTU7.TGRA to MTU7.TGRD input capture input/output compare output/PWM output pins. These pins can be used for large-current output. The MTIOC7D pin is not included in the 80-/64-pin versions.
General PWM timer (GPT)	MTCLKA-A/MTCLKA-B MTCLKB-A/MTCLKB-B MTCLKC-A/MTCLKC-B/ MTCLKC-C MTCLKD-A/MTCLKD-B/ MTCLKD-C	Input	Input pins for external clock signals. The MTCLKA-B/MTCLKB-B/MTCLKC-C/MTCLKD-C pin is not included in the 64-pin version.
	GTIOC0A-A/GTIOC0A-B GTIOC0B-A/GTIOC0B-B	I/O	The GPT0.GTCCRA and GPT0.GTCCRB CCRB input capture input/output compare output/PWM output pins. Pins GTIOC0A-A and GTIOC0B-A can be used for large-current output.
	GTIOC1A-A/GTIOC1A-B GTIOC1B-A/GTIOC1B-B	I/O	The GPT1.GTCCRA and GPT1.GTCCRB input capture input/output compare output/PWM output pins. Pins GTIOC1A-A and GTIOC1B-A can be used for large-current output.
	GTIOC2A-A/GTIOC2A-B GTIOC2B-A/GTIOC2B-B	I/O	The GPT2.GTCCRA and GPT2.GTCCRB input capture input/output compare output/PWM output pins. Pins GTIOC2A-A and GTIOC2B-A can be used for large-current output. The GTIOC2B-B pin is not included in the 80-pin version.
	GTIOC3A, GTIOC3B	I/O	The GPT3.GTCCRA and GPT3.GTCCRB input capture input/output compare output/PWM output pins. Not included in the 80-/64-pin versions.
Port output enable 3 (POE3)	GTETRG	Input	External trigger input pin for the GPT
	POE0#, POE4#, POE8# POE10#-A/POE10#-B POE11#	Input	Input pins for request signals to place the MTU3 and GPT large-current pins in the high impedance state. The POE4#/ POE10#-B/POE11# pin is not included in the 64-pin version.
Watchdog timer (WDT)	WDTOVF#	Output	Output pin for the counter-overflow signal in watchdog-timer mode. Not included in the 100-/80-/64-pin versions.

(9) Accumulator (ACC)

The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.

Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively.

Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

Table 4.1 List of I/O Registers (Address Order) (4 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 70BCh	ICU	Interrupt request register 188	IR188	8	8	2 ICLK
0008 70BDh	ICU	Interrupt request register 189	IR189	8	8	2 ICLK
0008 70BEh	ICU	Interrupt request register 190	IR190	8	8	2 ICLK
0008 70C0h	ICU	Interrupt request register 192	IR192	8	8	2 ICLK
0008 70C1h	ICU	Interrupt request register 193	IR193	8	8	2 ICLK
0008 70C2h	ICU	Interrupt request register 194	IR194	8	8	2 ICLK
0008 70C3h	ICU	Interrupt request register 195	IR195	8	8	2 ICLK
0008 70C4h	ICU	Interrupt request register 196	IR196	8	8	2 ICLK
0008 70D6h	ICU	Interrupt request register 214	IR214	8	8	2 ICLK
0008 70D7h	ICU	Interrupt request register 215	IR215	8	8	2 ICLK
0008 70D8h	ICU	Interrupt request register 216	IR216	8	8	2 ICLK
0008 70D9h	ICU	Interrupt request register 217	IR217	8	8	2 ICLK
0008 70DAh	ICU	Interrupt request register 218	IR218	8	8	2 ICLK
0008 70DBh	ICU	Interrupt request register 219	IR219	8	8	2 ICLK
0008 70DCh	ICU	Interrupt request register 220	IR220	8	8	2 ICLK
0008 70DDh	ICU	Interrupt request register 221	IR221	8	8	2 ICLK
0008 70DEh	ICU	Interrupt request register 222	IR222	8	8	2 ICLK
0008 70DFh	ICU	Interrupt request register 223	IR223	8	8	2 ICLK
0008 70E0h	ICU	Interrupt request register 224	IR224	8	8	2 ICLK
0008 70E1h	ICU	Interrupt request register 225	IR225	8	8	2 ICLK
0008 70F6h	ICU	Interrupt request register 246	IR246	8	8	2 ICLK
0008 70F7h	ICU	Interrupt request register 247	IR247	8	8	2 ICLK
0008 70F8h	ICU	Interrupt request register 248	IR248	8	8	2 ICLK
0008 70F9h	ICU	Interrupt request register 249	IR249	8	8	2 ICLK
0008 70FEh	ICU	Interrupt request register 254	IR254	8	8	2 ICLK
0008 711Bh	ICU	DTC activation enable register 027	DTCER027	8	8	2 ICLK
0008 711Ch	ICU	DTC activation enable register 028	DTCER028	8	8	2 ICLK
0008 711Dh	ICU	DTC activation enable register 029	DTCER029	8	8	2 ICLK
0008 711Eh	ICU	DTC activation enable register 030	DTCER030	8	8	2 ICLK
0008 711Fh	ICU	DTC activation enable register 031	DTCER031	8	8	2 ICLK
0008 712Dh	ICU	DTC activation enable register 045	DTCER045	8	8	2 ICLK
0008 712Eh	ICU	DTC activation enable register 046	DTCER046	8	8	2 ICLK
0008 7140h	ICU	DTC activation enable register 064	DTCER064	8	8	2 ICLK
0008 7141h	ICU	DTC activation enable register 065	DTCER065	8	8	2 ICLK
0008 7142h	ICU	DTC activation enable register 066	DTCER066	8	8	2 ICLK
0008 7143h	ICU	DTC activation enable register 067	DTCER067	8	8	2 ICLK
0008 7144h	ICU	DTC activation enable register 068	DTCER068	8	8	2 ICLK
0008 7145h	ICU	DTC activation enable register 069	DTCER069	8	8	2 ICLK
0008 7146h	ICU	DTC activation enable register 070	DTCER070	8	8	2 ICLK
0008 7147h	ICU	DTC activation enable register 071	DTCER071	8	8	2 ICLK
0008 7162h	ICU	DTC activation enable register 098	DTCER098	8	8	2 ICLK
0008 7166h	ICU	DTC activation enable register 102	DTCER102	8	8	2 ICLK
0008 7167h	ICU	DTC activation enable register 103	DTCER103	8	8	2 ICLK
0008 716Ah	ICU	DTC activation enable register 106	DTCER106	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (6 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 71BEh	ICU	DTC activation enable register 190	DTCER190	8	8	2 ICLK
0008 71C0h	ICU	DTC activation enable register 192	DTCER192	8	8	2 ICLK
0008 71C1h	ICU	DTC activation enable register 193	DTCER193	8	8	2 ICLK
0008 71C2h	ICU	DTC activation enable register 194	DTCER194	8	8	2 ICLK
0008 71C3h	ICU	DTC activation enable register 195	DTCER195	8	8	2 ICLK
0008 71C4h	ICU	DTC activation enable register 196	DTCER196	8	8	2 ICLK
0008 71D7h	ICU	DTC activation enable register 215	DTCER215	8	8	2 ICLK
0008 71D8h	ICU	DTC activation enable register 216	DTCER216	8	8	2 ICLK
0008 71DBh	ICU	DTC activation enable register 219	DTCER219	8	8	2 ICLK
0008 71DCh	ICU	DTC activation enable register 220	DTCER220	8	8	2 ICLK
0008 71DFh	ICU	DTC activation enable register 223	DTCER223	8	8	2 ICLK
0008 71E0h	ICU	DTC activation enable register 224	DTCER224	8	8	2 ICLK
0008 71F7h	ICU	DTC activation enable register 247	DTCER247	8	8	2 ICLK
0008 71F8h	ICU	DTC activation enable register 248	DTCER248	8	8	2 ICLK
0008 71FEh	ICU	DTC activation enable register 254	DTCER254	8	8	2 ICLK
0008 7202h	ICU	Interrupt request enable register 02	IER02	8	8	2 ICLK
0008 7203h	ICU	Interrupt request enable register 03	IER03	8	8	2 ICLK
0008 7205h	ICU	Interrupt request enable register 05	IER05	8	8	2 ICLK
0008 7207h	ICU	Interrupt request enable register 07	IER07	8	8	2 ICLK
0008 7208h	ICU	Interrupt request enable register 08	IER08	8	8	2 ICLK
0008 720Ch	ICU	Interrupt request enable register 0C	IER0C	8	8	2 ICLK
0008 720Dh	ICU	Interrupt request enable register 0D	IER0D	8	8	2 ICLK
0008 720Eh	ICU	Interrupt request enable register 0E	IER0E	8	8	2 ICLK
0008 720Fh	ICU	Interrupt request enable register 0F	IER0F	8	8	2 ICLK
0008 7210h	ICU	Interrupt request enable register 10	IER10	8	8	2 ICLK
0008 7211h	ICU	Interrupt request enable register 11	IER11	8	8	2 ICLK
0008 7212h	ICU	Interrupt request enable register 12	IER12	8	8	2 ICLK
0008 7213h	ICU	Interrupt request enable register 13	IER13	8	8	2 ICLK
0008 7215h	ICU	Interrupt request enable register 15	IER15	8	8	2 ICLK
0008 7216h	ICU	Interrupt request enable register 16	IER16	8	8	2 ICLK
0008 7217h	ICU	Interrupt request enable register 17	IER17	8	8	2 ICLK
0008 7218h	ICU	Interrupt request enable register 18	IER18	8	8	2 ICLK
0008 721Ah	ICU	Interrupt request enable register 1A	IER1A	8	8	2 ICLK
0008 721Bh	ICU	Interrupt request enable register 1B	IER1B	8	8	2 ICLK
0008 721Ch	ICU	Interrupt request enable register 1C	IER1C	8	8	2 ICLK
0008 721Eh	ICU	Interrupt request enable register 1E	IER1E	8	8	2 ICLK
0008 721Fh	ICU	Interrupt request enable register 1F	IER1F	8	8	2 ICLK
0008 72E0h	ICU	Software interrupt activation register	SWINTR	8	8	2 ICLK
0008 72F0h	ICU	Fast interrupt set register	FIR	16	16	2 ICLK
0008 7300h	ICU	Interrupt source priority register 00	IPR00	8	8	2 ICLK
0008 7301h	ICU	Interrupt source priority register 01	IPR01	8	8	2 ICLK
0008 7302h	ICU	Interrupt source priority register 02	IPR02	8	8	2 ICLK
0008 7303h	ICU	Interrupt source priority register 03	IPR03	8	8	2 ICLK
0008 7304h	ICU	Interrupt source priority register 04	IPR04	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (20 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000C 200Ah	GPT	General PWM timer hardware stop/clear source select register	GTHPSR	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 200Ch	GPT	General PWM timer write-protection register	GTWP	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 200Eh	GPT	General PWM timer sync register	GTSYNC	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2010h	GPT	General PWM timer external trigger input interrupt register	GTETINT	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2014h	GPT	General PWM timer buffer operation disable register	GTBDR	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2018h	GPT	General PWM timer start write protection register	GTSWP	16	16, 32	3 to 5 ICLK ^{*4}
000C 2080h	GPT	LOCO count control register	LCCR	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2082h	GPT	LOCO count status register	LCST	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2084h	GPT	LOCO count value register	LCNT	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2086h	GPT	LOCO count result average register	LCNTA	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2088h	GPT	LOCO count result register 0	LCNT00	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 208Ah	GPT	LOCO count result register 1	LCNT01	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 208Ch	GPT	LOCO count result register 2	LCNT02	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 208Eh	GPT	LOCO count result register 3	LCNT03	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2090h	GPT	LOCO count result register 4	LCNT04	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2092h	GPT	LOCO count result register 5	LCNT05	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2094h	GPT	LOCO count result register 6	LCNT06	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2096h	GPT	LOCO count result register 7	LCNT07	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2098h	GPT	LOCO count result register 8	LCNT08	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 209Ah	GPT	LOCO count result register 9	LCNT09	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 209Ch	GPT	LOCO count result register 10	LCNT10	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 209Eh	GPT	LOCO count result register 11	LCNT11	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 20A0h	GPT	LOCO count result register 12	LCNT12	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 20A2h	GPT	LOCO count result register 13	LCNT13	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 20A4h	GPT	LOCO count result register 14	LCNT14	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 20A6h	GPT	LOCO count result register 15	LCNT15	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 20A8h	GPT	LOCO count upper permissible deviation register	LCNTDU	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 20AAh	GPT	LOCO count lower permissible deviation register	LCNTDL	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2100h	GPT0	General PWM timer I/O control register	GTIOR	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2102h	GPT0	General PWM timer interrupt output setting register	GTINTAD	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2104h	GPT0	General PWM timer control register	GTCR	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2106h	GPT0	General PWM timer buffer enable register	GTBER	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2108h	GPT0	General PWM timer count direction register	GTUDC	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 210Ah	GPT0	General PWM timer interrupt and A/D converter start request skipping setting register	GTITC	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 210Ch	GPT0	General PWM timer status register	GTST	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 210Eh	GPT0	General PWM timer counter	GTCNT	16	16	3 to 5 ICLK ^{*4}
000C 2110h	GPT0	General PWM timer compare capture register A	GTCCRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 2112h	GPT0	General PWM timer compare capture register B	GTCCRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2114h	GPT0	General PWM timer compare capture register C	GTCCRC	16	16, 32	3 to 5 ICLK ^{*4}

Table 4.1 List of I/O Registers (Address Order) (22 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000C 21A0h	GPT1	General PWM timer cycle setting double-buffer register	GTPDBR	16	16, 32	3 to 5 ICLK ^{*4}
000C 21A4h	GPT1	A/D converter start request timing register A	GTADTRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 21A6h	GPT1	A/D converter start request timing buffer register A	GTADTBRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 21A8h	GPT1	A/D converter start request timing double-buffer register A	GTADTDBRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 21ACh	GPT1	A/D converter start request timing register B	GTADTRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 21AEh	GPT1	A/D converter start request timing buffer register B	GTADTBRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 21B0h	GPT1	A/D converter start request timing double-buffer register B	GTADTDBRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 21B4h	GPT1	General PWM timer output negate control register	GTONCR	16	16, 32	3 to 5 ICLK ^{*4}
000C 21B6h	GPT1	General PWM timer dead time control register	GTDTCR	16	16, 32	3 to 5 ICLK ^{*4}
000C 21B8h	GPT1	General PWM timer dead time value register	GTDVU	16	16, 32	3 to 5 ICLK ^{*4}
000C 21BAh	GPT1	General PWM timer dead time value register	GTDVD	16	16, 32	3 to 5 ICLK ^{*4}
000C 21BCh	GPT1	General PWM timer dead time buffer register	GTDBU	16	16, 32	3 to 5 ICLK ^{*4}
000C 21BEh	GPT1	General PWM timer dead time buffer register	GTDBD	16	16, 32	3 to 5 ICLK ^{*4}
000C 21C0h	GPT1	General PWM timer output protection function status register	GTSOS	16	16, 32	3 to 5 ICLK ^{*4}
000C 21C2h	GPT1	General PWM timer output protection temporary release register	GTSOTR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2200h	GPT2	General PWM timer I/O control register	GTIOR	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2202h	GPT2	General PWM timer interrupt output setting register	GTINTAD	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2204h	GPT2	General PWM timer control register	GTCR	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2206h	GPT2	General PWM timer buffer enable register	GTBER	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2208h	GPT2	General PWM timer count direction register	GTUDC	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 220Ah	GPT2	General PWM timer interrupt and A/D converter start request skipping setting register	GTITC	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 220Ch	GPT2	General PWM timer status register	GTST	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 220Eh	GPT2	General PWM timer counter	GTCNT	16	16	3 to 5 ICLK ^{*4}
000C 2210h	GPT2	General PWM timer compare capture register A	GTCCRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 2212h	GPT2	General PWM timer compare capture register B	GTCCRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2214h	GPT2	General PWM timer compare capture register C	GTCCRC	16	16, 32	3 to 5 ICLK ^{*4}
000C 2216h	GPT2	General PWM timer compare capture register D	GTCCRD	16	16, 32	3 to 5 ICLK ^{*4}
000C 2218h	GPT2	General PWM timer compare capture register E	GTCCRE	16	16, 32	3 to 5 ICLK ^{*4}
000C 221Ah	GPT2	General PWM timer compare capture register F	GTCCRF	16	16, 32	3 to 5 ICLK ^{*4}
000C 221Ch	GPT2	General PWM timer cycle setting register	GTPR	16	16, 32	3 to 5 ICLK ^{*4}
000C 221Eh	GPT2	General PWM timer cycle setting buffer register	GTPBR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2220h	GPT2	General PWM timer cycle setting double-buffer register	GTPDBR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2224h	GPT2	A/D converter start request timing register A	GTADTRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 2226h	GPT2	A/D converter start request timing buffer register A	GTADTBRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 2228h	GPT2	A/D converter start request timing double-buffer register A	GTADTDBRA	16	16, 32	3 to 5 ICLK ^{*4}

Table 4.1 List of I/O Registers (Address Order) (25 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
007F FFBAh	FLASH	FCU command register	FCMDR	16	16	2, 3 PCLK ^{*3}
007F FFC8h	FLASH	FCU processing switching register	FCPSR	16	16	2, 3 PCLK ^{*3}
007F FFCAh	FLASH	Data flash blank check control register	DFLBCCNT	16	16	2, 3 PCLK ^{*3}
007F FFCCh	FLASH	Flash P/E status register	FPESTAT	16	16	2, 3 PCLK ^{*3}
007F FFCEh	FLASH	Data flash blank check status register	DFLBCSTAT	16	16	2, 3 PCLK ^{*3}
007F FFE8h	FLASH	Peripheral clock notification register	PCKAR	16	16	2, 3 PCLK ^{*3}

Note 1. This register is not supported by the 100-pin LQFP version.

Note 2. This register is not supported by the product without the CAN function.

Note 3. The number of access states depends on the number of divided cycles for clock synchronization (0 to 1 PCLK).

Note 4. Reading the registers takes 3 cycles of ICLK and writing to the registers takes 5 cycles of ICLK.

Table 4.2 List of I/O Registers (Bit Order) (7 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
ICU	DTCER180	—	—	—	—	—	—	—	DTCE
ICU	DTCER181	—	—	—	—	—	—	—	DTCE
ICU	DTCER182	—	—	—	—	—	—	—	DTCE
ICU	DTCER183	—	—	—	—	—	—	—	DTCE
ICU	DTCER184	—	—	—	—	—	—	—	DTCE
ICU	DTCER186	—	—	—	—	—	—	—	DTCE
ICU	DTCER187	—	—	—	—	—	—	—	DTCE
ICU	DTCER188	—	—	—	—	—	—	—	DTCE
ICU	DTCER189	—	—	—	—	—	—	—	DTCE
ICU	DTCER190	—	—	—	—	—	—	—	DTCE
ICU	DTCER192	—	—	—	—	—	—	—	DTCE
ICU	DTCER193	—	—	—	—	—	—	—	DTCE
ICU	DTCER194	—	—	—	—	—	—	—	DTCE
ICU	DTCER195	—	—	—	—	—	—	—	DTCE
ICU	DTCER196	—	—	—	—	—	—	—	DTCE
ICU	DTCER215	—	—	—	—	—	—	—	DTCE
ICU	DTCER216	—	—	—	—	—	—	—	DTCE
ICU	DTCER219	—	—	—	—	—	—	—	DTCE
ICU	DTCER220	—	—	—	—	—	—	—	DTCE
ICU	DTCER223	—	—	—	—	—	—	—	DTCE
ICU	DTCER224	—	—	—	—	—	—	—	DTCE
ICU	DTCER247	—	—	—	—	—	—	—	DTCE
ICU	DTCER248	—	—	—	—	—	—	—	DTCE
ICU	DTCER254	—	—	—	—	—	—	—	DTCE
ICU	IER02	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER03	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER05	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER07	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER08	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER0C	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER0D	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER0E	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER0F	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER10	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER11	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER12	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER13	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER15	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER16	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER17	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER18	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER1A	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER1B	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER1C	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER1E	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER1F	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	SWINTR	—	—	—	—	—	—	—	SWINT
ICU	FIR	FIEN	—	—	—	—	—	—	—
FVCT[7:0]									
ICU	IPR00	—	—	—	—	—	—	IPR[3:0]	—
ICU	IPR01	—	—	—	—	—	—	IPR[3:0]	—
ICU	IPR02	—	—	—	—	—	—	IPR[3:0]	—

Table 4.2 List of I/O Registers (Bit Order) (12 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
RSPi0	SSLP	—	—	—	—	SSLP3	SSLP2	SSLP1	SSLP0
RSPi0	SPPCR	—	—	MOIFE	MOIFV	—	—	SPLP2	SPLP
RSPi0	SPSR	SPRF	—	SPTEF	—	PERF	MODF	IDLNF	OVRF
RSPi0	SPDR	H[15:0]							
		H[15:0]							
		L[15:0]							
		L[15:0]							
RSPi0	SPSCR	—	—	—	—	—	—	SPSLN[2:0]	—
RSPi0	SPSSR	—	—	SPECM[2:0]	—	—	—	SPCP[2:0]	—
RSPi0	SPBR	SPR7	SPR6	SPR5	SPR4	SPR3	SPR2	SPR1	SPR0
RSPi0	SPDCR	—	—	SPLW	SPRDTD	SLSEL[1:0]	—	SPFC[1:0]	—
RSPi0	SPCKD	—	—	—	—	—	—	SCKDL[2:0]	—
RSPi0	SSLND	—	—	—	—	—	—	SLNDL[2:0]	—
RSPi0	SPND	—	—	—	—	—	—	SPNDL[2:0]	—
RSPi0	SPCR2	—	—	—	—	PTE	SPIIE	SPOE	SPPE
RSPi0	SPCMD0	SCKDEN	SLNDEN	SPNDEN	LSBF	—	—	SPB[3:0]	—
		SSLKP	—	SSLA[2:0]	—	BRDV[1:0]	—	CPOL	CPHA
RSPi0	SPCMD1	SCKDEN	SLNDEN	SPNDEN	LSBF	—	—	SPB[3:0]	—
		SSLKP	—	SSLA[2:0]	—	BRDV[1:0]	—	CPOL	CPHA
RSPi0	SPCMD2	SCKDEN	SLNDEN	SPNDEN	LSBF	—	—	SPB[3:0]	—
		SSLKP	—	SSLA[2:0]	—	BRDV[1:0]	—	CPOL	CPHA
RSPi0	SPCMD3	SCKDEN	SLNDEN	SPNDEN	LSBF	—	—	SPB[3:0]	—
		SSLKP	—	SSLA[2:0]	—	BRDV[1:0]	—	CPOL	CPHA
RSPi0	SPCMD4	SCKDEN	SLNDEN	SPNDEN	LSBF	—	—	SPB[3:0]	—
		SSLKP	—	SSLA[2:0]	—	BRDV[1:0]	—	CPOL	CPHA
RSPi0	SPCMD5	SCKDEN	SLNDEN	SPNDEN	LSBF	—	—	SPB[3:0]	—
		SSLKP	—	SSLA[2:0]	—	BRDV[1:0]	—	CPOL	CPHA
RSPi0	SPCMD6	SCKDEN	SLNDEN	SPNDEN	LSBF	—	—	SPB[3:0]	—
		SSLKP	—	SSLA[2:0]	—	BRDV[1:0]	—	CPOL	CPHA
RSPi0	SPCMD7	SCKDEN	SLNDEN	SPNDEN	LSBF	—	—	SPB[3:0]	—
		SSLKP	—	SSLA[2:0]	—	BRDV[1:0]	—	CPOL	CPHA
S12AD0	ADCSR	ADST	ADCS[1:0]	—	ADIE	—	CKS[1:0]	TRGE	EXTRG
S12AD0	ADANS	—	—	CH[1:0]	—	—	PG002SEL	PG001SEL	PG000SEL
		—	—	—	—	—	PG002EN	PG001EN	PG000EN
S12AD0	ADPG	—	—	—	—	—	PG002GAIN[3:0]	PG001GAIN[3:0]	PG000GAIN[3:0]
		—	—	—	—	—	PG002GAIN[3:0]	PG001GAIN[3:0]	PG000GAIN[3:0]
S12AD0	ADCER	ADRFMT	—	ADIEW	ADIE2	DIAGM	DIAGLD	DIAGVAL[1:0]	—
		—	—	ACE	—	—	ADPRC[1:0]	SHBYP	—
S12AD0	ADSTRGR	—	—	—	—	—	ADSTRS1[4:0]	ADSTRS0[4:0]	—
		—	—	—	—	—	ADSTRS1[4:0]	ADSTRS0[4:0]	—
S12AD	ADCMPMD0	—	—	CEN102[1:0]	—	CEN101[1:0]	—	CEN100[1:0]	—
		—	—	CEN002[1:0]	—	CEN001[1:0]	—	CEN000[1:0]	—
S12AD	ADCMPMD1	—	VSELL1	VSELH1	CSEL1	—	VSELL0	VSELH0	CSEL0
		—	—	REFH[2:0]	—	—	—	REFL[2:0]	—
S12AD	ADCMPNR0	—	—	—	—	—	C002NR[3:0]	C001NR[3:0]	C000NR[3:0]
		—	—	—	—	—	C002NR[3:0]	C001NR[3:0]	C000NR[3:0]
S12AD	ADCMPNR1	—	—	—	—	—	C102NR[3:0]	C101NR[3:0]	C100NR[3:0]
		—	—	—	—	—	C102NR[3:0]	C101NR[3:0]	C100NR[3:0]
S12AD	ADCMPFR	—	—	C102FLAG	C101FLAG	C100FLAG	C002FLAG	C001FLAG	C000FLAG
S12AD	ADCMPSEL	—	—	—	—	—	—	POERQ	IE
		—	—	SEL102	SEL101	SEL100	SEL002	SEL001	SEL000

Table 4.2 List of I/O Registers (Bit Order) (17 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
CAN0*3	MKR5	—	—	—			SID[10:0]		
					SID[10:0]			EID[17:0]	
						EID[17:0]			
						EID[17:0]			
CAN0*3	MKR6	—	—	—			SID[10:0]		
					SID[10:0]			EID[17:0]	
						EID[17:0]			
						EID[17:0]			
CAN0*3	MKR7	—	—	—			SID[10:0]		
					SID[10:0]			EID[17:0]	
						EID[17:0]			
						EID[17:0]			
CAN0*3	FIDCR0	IDE	RTR	—			SID[10:0]		
					SID[10:0]			EID[17:0]	
						EID[17:0]			
						EID[17:0]			
CAN0*3	FIDCR1	IDE	RTR	—			SID[10:0]		
					SID[10:0]			EID[17:0]	
						EID[17:0]			
						EID[17:0]			
CAN0*3	MKIVLR								
CAN0*3	MIER	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
CAN0*3	MCTL.TX	TRMREQ	RECREQ	—	ONESHOT	—	TRMABT	TRMACTIVE	SENTDATA
	MCTL.RX	TRMREQ	RECREQ	—	ONESHOT	—	MSGLOST	INVALDATA	NEWDATA
CAN0*3	CTLR	—	—	RBOC	BOM[1:0]	—	SLPM	CANM[1:0]	—
		TSPS[1:0]	—	TSRC	TPM	MLM	IDFM[1:0]	—	MBM
CAN0*3	STR	—	RECST	TRMST	BOST	EPST	SLPST	HLTST	RSTST
		EST	TABST	FMLST	NMLST	TFST	RFST	SDST	NDST
CAN0*3	BCR		TSEG1[3:0]			—	—	BRP[9:0]	
CAN0*3	RFCR	RFEST	RFWST	RFFST	RFMLF		RFUST[2:0]		RFE
CAN0*3	RFPCR	—	—	—	—	—	—	—	—
CAN0*3	TFCR	TFEST	TFFST	—	—		TFUST[2:0]		TFE
CAN0*3	TFPCR	—	—	—	—	—	—	—	—
CAN0*3	EIER	BLIE	OLIE	ORIE	BORIE	BOEIE	EPIE	EWIE	BEIE
CAN0*3	EIFR	BLIF	OLIF	ORIF	BORIF	BOEIF	EPIF	EWIF	BEIF
CAN0*3	RECR	—	—	—	—	—	—	—	—
CAN0*3	TECR	—	—	—	—	—	—	—	—
CAN0*3	ECSR	EDPM	ADEF	BE0F	BE1F	CEF	AEF	FEF	SEF
CAN0*3	CSSR	—	—	—	—	—	—	—	—
CAN0*3	MSSR	SEST	—	—			MBNST[4:0]		
CAN0*3	MSMR	—	—	—	—	—	—	MBSM[1:0]	
CAN0*3	TSR	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—

Table 4.2 List of I/O Registers (Bit Order) (19 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
MTU3	TGRA								
MTU3	TGRB								
MTU4	TGRA								
MTU4	TGRB								
MTU	TCNTSA								
MTU	TCBRA								
MTU3	TGRC								
MTU3	TGRD								
MTU4	TGRC								
MTU4	TGRD								
MTU3	TSR	TCFD	—	—	TCFV	TGFD	TGFC	TGFB	TGFA
MTU4	TSR	TCFD	—	—	TCFV	TGFD	TGFC	TGFB	TGFA
MTU	TITCR1A	T3AEN		T3ACOR[2:0]		T4VEN		T4VCOR[2:0]	
MTU	TBTERA	—		T3ACOR[2:0]		—		T4VCNT[2:0]	
MTU	TBTERA	—	—	—	—	—	—	BTE[1:0]	
MTU	TDERA	—	—	—	—	—	—	—	TDER
MTU	TOLBRA	—	—	OLS3N	OLS3P	OLS2N	OLS2P	OLS1N	OLS1P
MTU3	TBTM	—	—	—	—	—	—	TTSB	TTSA
MTU4	TBTM	—	—	—	—	—	—	TTSB	TTSA
MTU	TITMRA	—	—	—	—	—	—	—	TITM
MTU	TITCR2A	—	—	—	—	—	—	TRG4COR[2:0]	
MTU	TITCNT2A	—	—	—	—	—	—	TRG4COR[2:0]	
MTU4	TADCR	BF[1:0]		—	—	—	—	—	—
		UT4AE	DT4AE	UT4BE	DT4BE	ITA3AE	ITA4VE	ITB3AE	ITB4VE
MTU4	TADCORA								
MTU4	TADCORB								
MTU4	TADCOBRA								
MTU4	TADCOBRB								
MTU	TWCRA	CCE	—	—	—	—	—	—	WRE
MTU	TMDR2A	—	—	—	—	—	—	—	DRS
MTU3	TGRE								
MTU4	TGRE								
MTU4	TGRF								
MTU	TSTRA	CST4	CST3	—	—	—	CST2	CST1	CST0
MTU	TSYRA	SYNC4	SYNC3	—	—	—	SYNC2	SYNC1	SYNC0
MTU	TCSYSTR	SCH0	SCH1	SCH2	SCH3	SCH4	—	SCH6	SCH7
MTU	TRWERA	—	—	—	—	—	—	—	RWE
MTU0	TCR		CCLR[2:0]		CKEG[1:0]			TPSC[2:0]	

Table 4.2 List of I/O Registers (Bit Order) (20 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
MTU0	TMDR1	—	BFE	BFB	BFA			MD[3:0]	
MTU0	TIORH			IOB[3:0]				IOA[3:0]	
MTU0	TIORL			IOD[3:0]				IOC[3:0]	
MTU0	TIER	TTEG	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA
MTU0	TSR	—	—	—	TCFV	TGFD	TGFC	TGFB	TGFA
MTU0	TCNT								
MTU0	TGRA								
MTU0	TGRB								
MTU0	TGRC								
MTU0	TGRD								
MTU0	TGRE								
MTU0	TGRF								
MTU0	TIER2	TTGE2	—	—	—	—	—	TGIEF	TGIEE
MTU0	TSR2	—	—	—	—	—	—	TGFF	TGFE
MTU0	TBTM	—	—	—	—	—	TTSE	TTSB	TTSA
MTU1	TCR	—	CCLR[1:0]		CKEG[1:0]			TPSC[2:0]	
MTU1	TMDR1	—	—	—	—			MD[3:0]	
MTU1	TIOR		IOB[3:0]					IOA[3:0]	
MTU1	TIER	TTEG	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA
MTU1	TSR	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA
MTU1	TCNT								
MTU1	TGRA								
MTU1	TGRB								
MTU1	TICCR	—	—	—	—	I2BE	I2AE	I1BE	I1AE
MTU2	TCR	—	CCLR[1:0]		CKEG[1:0]			TPSC[2:0]	
MTU2	TMDR1	—	—	—	—			MD[3:0]	
MTU2	TIOR		IOB[3:0]					IOA[3:0]	
MTU2	TIER	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA
MTU2	TSR	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA
MTU2	TCNT								
MTU2	TGRA								
MTU2	TGRB								
MTU6	TCR		CCLR[20]		CKEG[1:0]			TPSC[2:0]	
MTU7	TCR		CCLR[20]		CKEG[1:0]			TPSC[2:0]	
MTU6	TMDR1	—	—	BFB	BFA			MD[3:0]	
MTU7	TMDR1	—	—	BFB	BFA			MD[3:0]	
MTU6	TIORH		IOB[3:0]					IOA[3:0]	
MTU6	TIORL		IOD[3:0]					IOC[3:0]	
MTU7	TIORH		IOB[3:0]					IOA[3:0]	

Table 5.3 DC Characteristics (2)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Ta = Topr. Ta is the same under conditions 1 to 3.

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Supply current*1	In operation	Max.*2	I _{CC} *3	-	-	70	mA	ICLK = 100 MHz PCLK = 50 MHz
		Normal*4		-	35	-		
		Increased by BGO operation*5		-	15	-		
	Sleep				22	60		
	All-module-clock-stop mode*6				14	28		
	Standby mode	Software standby mode		-	0.10	3	mA	
		Deep software standby mode		-	20	60		
	Analog power supply current	During 12-bit A/D conversion (when a sample-and-hold circuit is in use; per unit)		AI _{CC0}	-	3	5	mA
During 12-bit A/D conversion (when a sample-and-hold circuit is not in use; per unit)		-	3		5			
Programmable gain amp (per channel)		-	1		2			
Window comparator (1 channel)			0.5		1			
Window comparator (6 channels)		-	1		2			
During 12-bit A/D conversion (per unit)		-	60		90	μA		
During 10-bit A/D conversion (per unit)		AI _{CC}	-	0.9	2	mA		
Waiting for 10-bit A/D conversion (all units)			-	0.3	3			μA
Reference power supply current	During 12-bit A/D conversion (per unit)		AI _{REFH0}	-	1.6	3	mA	
	Waiting for 12-bit A/D conversion (all units)			-	1.6	3		
	During 10-bit A/D conversion (per unit)		AI _{REF}	-	0.1	1	mA	
	Waiting for 10-bit A/D conversion (all units)			-	0.1	3		
VCC rising gradient			SV _{CC}	-	-	20	ms/V	

Note 1. Supply current values are with all output pins unloaded.

Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.

Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK: PCLK = 8:4)

$I_{CC} \text{ max.} = 0.54 \times f + 16 \text{ (max.)}$

$I_{CC} \text{ max.} = 0.3 \times f + 5 \text{ (normal operation)}$

$I_{CC} \text{ max.} = 0.44 \times f + 16 \text{ (sleep mode)}$

Note 4. Measured with clocks not supplied to the peripheral functions. This does not include the BGO operation.

Note 5. Incremented if data is written to or erased from the ROM or data flash for data storage during the program execution.

Note 6. The values are for reference.

5.3 AC Characteristics

Table 5.6 Operation Frequency Value

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit
Operating frequency	System clock (ICLK)	f	8	-	100	MHz
	Peripheral module clock (PCLK)		8	-	50	

5.3.1 Clock Timing

Table 5.7 Clock Timing

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC
Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item	Symbol	Min.	Max.	Unit	Test Conditions
Oscillation settling time after reset (crystal)	t _{OSC1}	10	-	ms	Figure 5.1
Oscillation settling time after leaving software standby mode (crystal)	t _{OSC2}	10	-	ms	Figure 5.2
Oscillation settling time after leaving deep software standby mode (crystal)	t _{OSC3}	10	-	ms	Figure 5.3
EXTAL external clock output delay settling time	t _{DEXT}	1	-	ms	Figure 5.1
EXTAL external clock input low pulse width	t _{EXL}	35	-	ns	Figure 5.4
EXTAL external clock input high pulse width	t _{EXH}	35	-	ns	
EXTAL external clock rising time	t _{EXr}	-	5	ns	
EXTAL external clock falling time	t _{EXf}	-	5	ns	
On-chip oscillator (IWDTCCLK) oscillation frequency	f _{IWDTCCLK}	62.5	187.5	kHz	

5.3.2 Control Signal Timing

Table 5.8 Control Signal Timing

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item	Symbol	Min.	Max.	Unit	Test Conditions
RES# pulse width (except for programming or erasure of the ROM or data-flash memory or blank checking of the data-flash memory*1)	t_{RESW}^{*2}	20	-	t_{cyc}^{*4}	Figure 5.5
		1.5	-	μs	
Internal reset time*3	t_{RESW2}	35	-	μs	
NMI pulse width	t_{NMIW}	200	-	ns	Figure 5.6
IRQ pulse width	t_{IRQW}	200	-	ns	Figure 5.7

Note 1. For a reset by the signal on the RES# pin during programming or erasure of the ROM or data-flash memory or during blank checking of the data-flash memory, see section 31.12, Usage Notes in section 31, ROM (Flash Memory for Code Storage) in the User's manual: Hardware.

Note 2. Both the time and the number of cycles should satisfy the specifications.

Note 3. This is to specify the FCU reset.

Note 4. ICLK cycles.

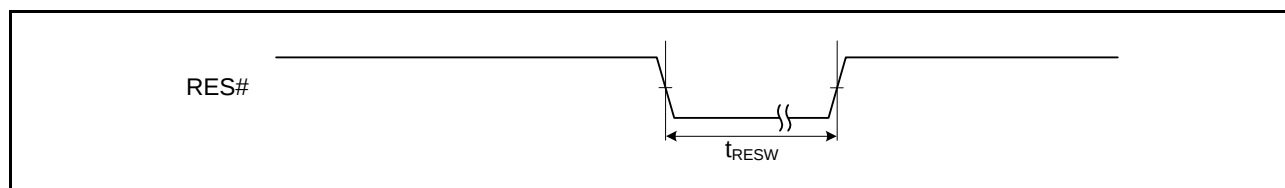


Figure 5.5 Reset Input Timing

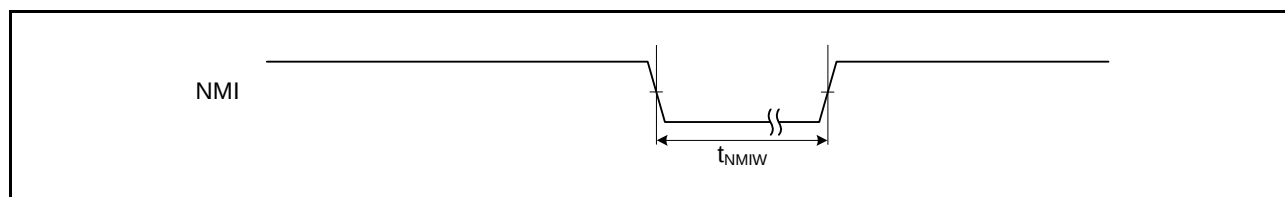


Figure 5.6 NMI Interrupt Input Timing

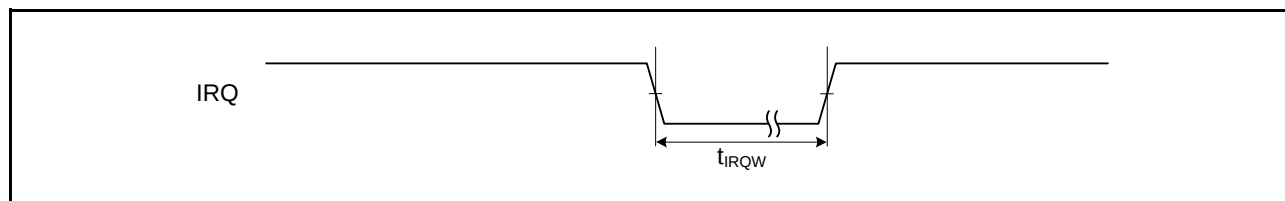


Figure 5.7 IRQ Interrupt Input Timing

5.8 Data Flash (Flash Memory for Data Storage) Characteristics

Table 5.23 Data Flash (Flash Memory for Data Storage) Characteristics (1)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Temperature range for the programming/erasure operation:
Ta = Topr. Ta is the same under conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Rewrite/erase cycle ^{*1}	N _{DPEC}	30000	—	—	Times	
Data hold time	t _{DDRP}	30 ^{*2}	—	—	Year	Ta = +85C°

Note 1. Definition of rewrite/erase cycle:

The rewrite/erase cycle is the number of erasing for each block. When the rewrite/erase cycle is n times (n = 30000), erasing can be performed n times for each block. For instance, when 128-byte writing is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the rewrite/erase cycle is counted as one. However, writing to the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. The value is obtained from the reliability test.

Table 5.24 Data Flash (Flash Memory for Data Storage) Characteristics (2)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Temperature range for the programming/erasure operation:
Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Programming time	8 bytes	t _{DP8}	—	0.4	2	ms	PCLK = 50 MHz
	128 bytes	t _{DP128}	—	1	5	ms	
Erase time	2 Kbytes	t _{DE2K}	—	70	250	ms	PCLK = 50 MHz
Blank check time	8 bytes	t _{DBC8}	—	—	30	μs	PCLK = 50 MHz
	2 Kbytes	t _{DBC2K}	—	—	0.7	ms	
Suspend delay time during writing		t _{DSPD}	—	—	120	μs	Figure 5.24 PCLK = 50 MHz
First suspend delay time during erasing (in suspend priority mode)		t _{DSESD1}	—	—	120	μs	
Second suspend delay time during erasing (in suspend priority mode)		t _{DSESD2}	—	—	1.7	ms	
Suspend delay time during erasing (in erasure priority mode)		t _{DSEED}	—	—	1.7	ms	

REVISION HISTORY	RX62T Group, RX62G Group Datasheet
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Rev.	Date	Description	
		Page	Summary
1.00	Apr 20, 2011	—	First edition issued
1.30	May 22, 2013	1	Features, Package lineup, added
		2	1. Overview
		3	Table 1.1 Outline of Specifications (1/5) Description of CPU, added
		6	Table 1.1 Outline of Specifications (2/5) Description of Programmable I/O ports, changed
		7	Table 1.1 Outline of Specifications (5/5), 64-pin packaged, added
		8	Table 1.2 Functions of RX62T Group Products, 64-pin package, and MTU3/GPT complementary PWM pins added
		9	Table 1.3 List of Products, 64-pin package part number, changed
		9	Figure 1.1 How to Read the Product Part No., 64-pin package part number, changed
		10	Figure 1.1 How to Read the Product Part No., 5-V version, two-motor control supported, added
		10	Figure 1.2 Block Diagram, changed
		14	Figure 1.6 Pin Assignment of the 80-Pin LQFP (Two-motor Control Supported), added
		15	Figure 1.7 Pin Assignment of the 64-Pin LQFP, Figure PLQP0064GA-A, added
		25 to 27	Table 1.7 List of Pins and Pin Functions (80-Pin LQFP: R5F562TxGDFF), added
		30 to 33	Table 1.9 Pin Functions, changed
		38 to 61	4. I/O Register
		47	Table 4.1 List of I/O Registers (Address Order), MPU, added
		57	Table 4.1 List of I/O Registers (Address Order) TMOCNTL, TMOCNTU register, added
		62	Table 4.1 List of I/O Registers (Address Order), GTSWP register, added
		62	5. Electrical Characteristics
		64	Table 5.1 Absolute Maximum Ratings, note changed
		66	Table 5.2 DC Characteristics (1) (2/3) Test Conditions of P90 to P95, changed
		67	Table 5.3 DC Characteristics (2), note changed
		72	Table 5.4 Permissible Output Currents, note changed
		73	Table 5.7 Control Signal Timing, notes changed
		73	Table 5.8 Timing of On-Chip Peripheral Modules (1), changed
		96	Appendix 1. Package Dimensions
		96	Figure E 64-Pin LQFP (PLQP0064GA-A), added
2.00	Jan 10, 2014	1	Features, changed
		2 to 6	1. Overview
		7, 8	Table 1.1 Outline of Specifications, changed; Note 1, added
		9, 10	Table 1.2 Functions of RX62T Group and RX62G Group Products, changed
		11	Table 1.3 List of Products, changed; Note 1, added
		15	Figure 1.1 How to Read the Product Part No., changed
		27 to 29	Figure 1.6 Pin Assignment of the 80-Pin LQFP (Two-Motor Control Supported Version), added
		27 to 29	Table 1.7 List of Pins and Pin Functions (80-Pin LQFP: R5F562TxGDFF), added
		43 to 67	4. I/O Registers
		68 to 97	Table 4.1 List of I/O Registers (Address Order), changed
		68 to 97	Table 4.2 List of I/O Registers (Bit Order), changed
		—	5. Electrical Characteristics
		—	Conditions in the table, change to Ta = -40 to +105°C from Ta = -40 to +85°C.

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