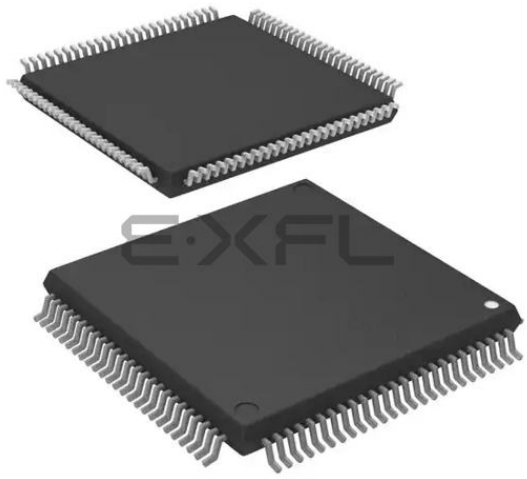

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 12x10b, 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562t7bdfp-v3

Table 1.1 Outline of Specifications (3 / 5)

Classification	Module/Function	Description
Timers	General PWM timer (GPT/GPTa)	• 16 bits x 4 channels • Counting up or down (saw-wave), counting up and down (triangle-wave) selectable for all channels • Clock sources independently selectable for all channels • 2 input/output pins per channel • 2 output compare/input capture registers per channel • For the 2 output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally asymmetrically PWM waveforms. • Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow) • Synchronizable operation of the several counters • Modes of synchronized operation (synchronized, or displaced by desired times for phase shifting) • Generation of dead times in PWM operation • Through combination of three counters, generation of automatic three-phase PWM waveforms incorporating dead times • Starting, clearing, and stopping counters in response to external or internal triggers • Internal trigger sources: output of the internal comparator detection, software, and compare-match • The frequency-divided system clock (ICLK) can be used as a counter clock for measuring timing of the edges of signals produced by frequency-dividing the low-speed on-chip oscillator clock signal dedicated to IWDT (to detect abnormal oscillation). • PWM delay generation can control the timing with which signals on the two PWM output pins for each channel rise and fall with an accuracy of up to 1/32 times the period of the system clock (ICLK) (only for GPTa).
	Compare match timer (CMT)	• (16 bits x 2 channels) x 2 units • Select from among four internal clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Watchdog timer (WDT)	• 8 bits x 1 channel • Select from among eight counter-input clock signals (PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192, PCLK/32768, PCLK/131072) • Switchable between watchdog timer mode and interval timer mode
	Independent watchdog timer (IWDT)	• 14 bits x 1 channel • Counter-input clock: low-speed on-chip oscillator dedicated to IWDT
Communications	Serial communications interface (SCIb)	• 3 channels • Serial communications modes: Asynchronous, clock synchronous, and smart-card interface • Multiprocessor communications • On-chip baud rate generator allows selection of the desired bit rate • Choice of LSB-first or MSB-first transfer • Noise cancellation (only available in asynchronous mode)
	I^2C bus interface (RIIC)	• 1 channel • Communications formats I^2C bus format/SMBus format Master/slave selectable

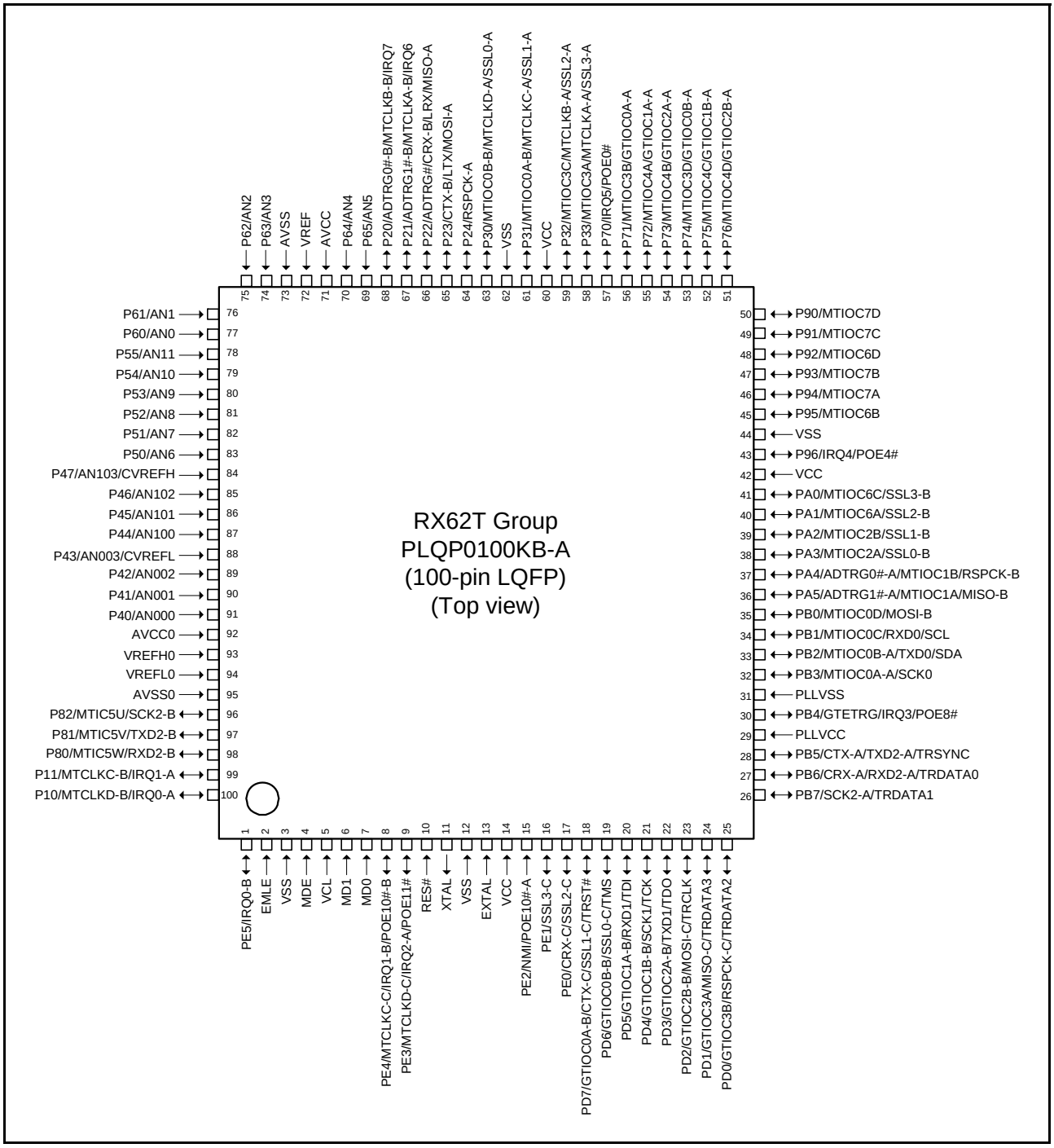


Figure 1.4 Pin Assignment of the 100-Pin LQFP

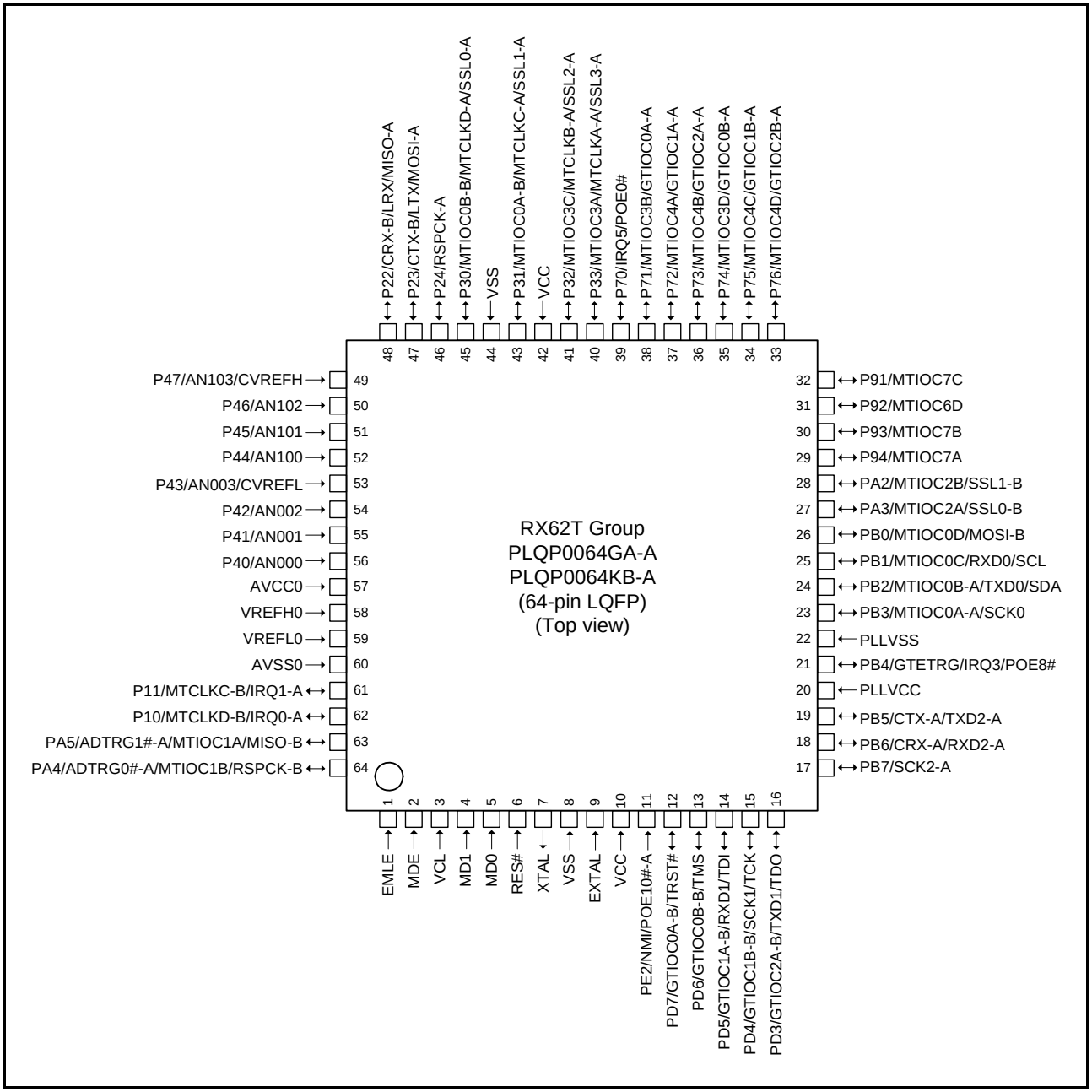


Figure 1.7 Pin Assignment of the 64-Pin LQFP

Table 1.8 List of Pins and Pin Functions (64-Pin LQFP) (2 / 2)

Pin No. (64-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi-cation	Interrupt	POE	Debuggi ng
40		P33		MTIOC3A/ MTCLKA-A	SSL3-A			
41		P32		MTIOC3C/ MTCLKB-A	SSL2-A			
42	VCC							
43		P31		MTIOC0A-B/ MTCLKC-A	SSL1-A			
44	VSS							
45		P30		MTIOC0B-B/ MTCLKD-A	SSL0-A			
46		P24			RSPCK-A			
47		P23			CTX-B/ LTX/ MOSI-A			
48		P22			CRX-B/ LRX/ MISO-A			
49		P47	AN103/ CVREFH					
50		P46	AN102					
51		P45	AN101					
52		P44	AN100					
53		P43	AN003/ CVREFL					
54		P42	AN002					
55		P41	AN001					
56		P40	AN000					
57	AVCC0							
58	VREFH0							
59	VREFL0							
60	AVSS0							
61		P11		MTCLKC-B		IRQ1-A		
62		P10		MTCLKD-B		IRQ0-A		
63		PA5	ADTRG1#-A	MTIOC1A	MISO-B			
64		PA4	ADTRG0#-A	MTIOC1B	RSPCK-B			

(9) Accumulator (ACC)

The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.

Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively.

Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

4. I/O Registers

This section gives information on the on-chip I/O register addresses and bit configurations. The information is given as shown below. Notes on writing to registers are also given at the end.

(1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to functional modules (abbreviations).
- The number of access cycles indicates the number of states based on the specified reference clock.
- Among the I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.
- A unit of access is specified for each register. Access other than in the specified unit is prohibited.

(2) I/O register bits

- Bit configurations of the registers are listed in the same order as the register addresses.
- Reserved bits are indicated by "—" in the bit name column.
- Space in the bit name field indicates that the entire register is allocated to either the counter or data.
- For the registers of 16 or 32 bits, the MSB is listed first.

(3) Notes on writing to I/O registers

When writing to an I/O register, the CPU starts executing the subsequent instruction before completing I/O register write. This may cause the subsequent instruction to be executed before the post-update I/O register value is reflected on the operation.
As described in the following examples, special care is required for the cases in which the subsequent instruction must be executed after the post-update I/O register value is actually reflected.

[Examples of cases requiring special care]

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERm of the ICU (interrupt request enable bit)*1 cleared to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

Note 1. See section 11.2.2, Interrupt Request Enable Register m (IERm) (m = 02h to 1Fh) in the User's manual: Hardware.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

Table 4.1 List of I/O Registers (Address Order) (3 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 707Dh	ICU	Interrupt request register 125	IR125	8	8	2 ICLK
0008 707Eh	ICU	Interrupt request register 126	IR126	8	8	2 ICLK
0008 707Fh	ICU	Interrupt request register 127	IR127	8	8	2 ICLK
0008 7080h	ICU	Interrupt request register 128	IR128	8	8	2 ICLK
0008 7081h	ICU	Interrupt request register 129	IR129	8	8	2 ICLK
0008 7082h	ICU	Interrupt request register 130	IR130	8	8	2 ICLK
0008 7083h	ICU	Interrupt request register 131	IR131	8	8	2 ICLK
0008 7084h	ICU	Interrupt request register 132	IR132	8	8	2 ICLK
0008 7085h	ICU	Interrupt request register 133	IR133	8	8	2 ICLK
0008 7086h	ICU	Interrupt request register 134	IR134	8	8	2 ICLK
0008 7087h	ICU	Interrupt request register 135	IR135	8	8	2 ICLK
0008 7088h	ICU	Interrupt request register 136	IR136	8	8	2 ICLK
0008 7089h	ICU	Interrupt request register 137	IR137	8	8	2 ICLK
0008 708Ah	ICU	Interrupt request register 138	IR138	8	8	2 ICLK
0008 708Bh	ICU	Interrupt request register 139	IR139	8	8	2 ICLK
0008 708Ch	ICU	Interrupt request register 140	IR140	8	8	2 ICLK
0008 708Dh	ICU	Interrupt request register 141	IR141	8	8	2 ICLK
0008 708Eh	ICU	Interrupt request register 142	IR142	8	8	2 ICLK
0008 708Fh	ICU	Interrupt request register 143	IR143	8	8	2 ICLK
0008 7090h	ICU	Interrupt request register 144	IR144	8	8	2 ICLK
0008 7091h	ICU	Interrupt request register 145	IR145	8	8	2 ICLK
0008 7092h	ICU	Interrupt request register 146	IR146	8	8	2 ICLK
0008 7095h	ICU	Interrupt request register 149	IR149	8	8	2 ICLK
0008 7096h	ICU	Interrupt request register 150	IR150	8	8	2 ICLK
0008 7097h	ICU	Interrupt request register 151	IR151	8	8	2 ICLK
0008 7098h	ICU	Interrupt request register 152	IR152	8	8	2 ICLK
0008 7099h	ICU	Interrupt request register 153	IR153	8	8	2 ICLK
0008 70AAh	ICU	Interrupt request register 170	IR170	8	8	2 ICLK
0008 70ABh	ICU	Interrupt request register 171	IR171	8	8	2 ICLK
0008 70ACh	ICU	Interrupt request register 172	IR172	8	8	2 ICLK
0008 70ADh	ICU	Interrupt request register 173	IR173	8	8	2 ICLK
0008 70AEh	ICU	Interrupt request register 174	IR174	8	8	2 ICLK
0008 70AFh	ICU	Interrupt request register 175	IR175	8	8	2 ICLK
0008 70B0h	ICU	Interrupt request register 176	IR176	8	8	2 ICLK
0008 70B1h	ICU	Interrupt request register 177	IR177	8	8	2 ICLK
0008 70B2h	ICU	Interrupt request register 178	IR178	8	8	2 ICLK
0008 70B3h	ICU	Interrupt request register 179	IR179	8	8	2 ICLK
0008 70B4h	ICU	Interrupt request register 180	IR180	8	8	2 ICLK
0008 70B5h	ICU	Interrupt request register 181	IR181	8	8	2 ICLK
0008 70B6h	ICU	Interrupt request register 182	IR182	8	8	2 ICLK
0008 70B7h	ICU	Interrupt request register 183	IR183	8	8	2 ICLK
0008 70B8h	ICU	Interrupt request register 184	IR184	8	8	2 ICLK
0008 70BAh	ICU	Interrupt request register 186	IR186	8	8	2 ICLK
0008 70BBh	ICU	Interrupt request register 187	IR187	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (14 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 C29Ch	SYSTEM	Deep standby backup register 12	DPSBKR12	8	8	4, 5 PCLK*3
0008 C29Dh	SYSTEM	Deep standby backup register 13	DPSBKR13	8	8	4, 5 PCLK*3
0008 C29Eh	SYSTEM	Deep standby backup register 14	DPSBKR14	8	8	4, 5 PCLK*3
0008 C29Fh	SYSTEM	Deep standby backup register 15	DPSBKR15	8	8	4, 5 PCLK*3
0008 C2A0h	SYSTEM	Deep standby backup register 16	DPSBKR16	8	8	4, 5 PCLK*3
0008 C2A1h	SYSTEM	Deep standby backup register 17	DPSBKR17	8	8	4, 5 PCLK*3
0008 C2A2h	SYSTEM	Deep standby backup register 18	DPSBKR18	8	8	4, 5 PCLK*3
0008 C2A3h	SYSTEM	Deep standby backup register 19	DPSBKR19	8	8	4, 5 PCLK*3
0008 C2A4h	SYSTEM	Deep standby backup register 20	DPSBKR20	8	8	4, 5 PCLK*3
0008 C2A5h	SYSTEM	Deep standby backup register 21	DPSBKR21	8	8	4, 5 PCLK*3
0008 C2A6h	SYSTEM	Deep standby backup register 22	DPSBKR22	8	8	4, 5 PCLK*3
0008 C2A7h	SYSTEM	Deep standby backup register 23	DPSBKR23	8	8	4, 5 PCLK*3
0008 C2A8h	SYSTEM	Deep standby backup register 24	DPSBKR24	8	8	4, 5 PCLK*3
0008 C2A9h	SYSTEM	Deep standby backup register 25	DPSBKR25	8	8	4, 5 PCLK*3
0008 C2AAh	SYSTEM	Deep standby backup register 26	DPSBKR26	8	8	4, 5 PCLK*3
0008 C2ABh	SYSTEM	Deep standby backup register 27	DPSBKR27	8	8	4, 5 PCLK*3
0008 C2ACh	SYSTEM	Deep standby backup register 28	DPSBKR28	8	8	4, 5 PCLK*3
0008 C2ADh	SYSTEM	Deep standby backup register 29	DPSBKR29	8	8	4, 5 PCLK*3
0008 C2AEh	SYSTEM	Deep standby backup register 30	DPSBKR30	8	8	4, 5 PCLK*3
0008 C2AFh	SYSTEM	Deep standby backup register 31	DPSBKR31	8	8	4, 5 PCLK*3
0008 C4C0h	POE	Input level control/status register 1	ICSR1	16	8, 16	2, 3 PCLK*3
0008 C4C2h	POE	Output level control/status register 1	OCSR1	16	8, 16	2, 3 PCLK*3
0008 C4C4h	POE	Input level control/status register 2	ICSR2	16	8, 16	2, 3 PCLK*3
0008 C4C6h	POE	Output level control/status register 2	OCSR2	16	8, 16	2, 3 PCLK*3
0008 C4C8h	POE	Input level control/status register 3	ICSR3	16	8, 16	2, 3 PCLK*3
0008 C4CAh	POE	Software port output enable register	SPOER	8	8	2, 3 PCLK*3
0008 C4CBh	POE	Port output enable control register 1	POECR1	8	8	2, 3 PCLK*3
0008 C4CCh	POE	Port output enable control register 2	POECR2	16	16	2, 3 PCLK*3
0008 C4CEh	POE	Port output enable control register 3	POECR3	16	16	2, 3 PCLK*3
0008 C4D0h	POE	Port output enable control register 4	POECR4	16	16	2, 3 PCLK*3
0008 C4D2h	POE	Port output enable control register 5	POECR5	16	16	2, 3 PCLK*3
0008 C4D4h	POE	Port output enable control register 6	POECR6	16	16	2, 3 PCLK*3
0008 C4D6h	POE	Input level control/status register 4	ICSR4	16	8, 16	2, 3 PCLK*3
0008 C4D8h	POE	Input level control/status register 5	ICSR5	16	8, 16	2, 3 PCLK*3
0008 C4DAh	POE	Active level setting register 1	ALR1	16	8, 16	2, 3 PCLK*3
0009 0200h to 0009 03FFh	CAN0*2	Mailbox registers 0 to 31	MB0 to MB 31	128	8, 16, 32	2, 3 PCLK*3
0009 0400h	CAN0*2	Mask register 0	MKR0	32	8, 16, 32	2, 3 PCLK*3
0009 0404h	CAN0*2	Mask register 1	MKR1	32	8, 16, 32	2, 3 PCLK*3
0009 0408h	CAN0*2	Mask register 2	MKR2	32	8, 16, 32	2, 3 PCLK*3
0009 040Ch	CAN0*2	Mask register 3	MKR3	32	8, 16, 32	2, 3 PCLK*3
0009 0410h	CAN0*2	Mask register 4	MKR4	32	8, 16, 32	2, 3 PCLK*3
0009 0414h	CAN0*2	Mask register 5	MKR5	32	8, 16, 32	2, 3 PCLK*3
0009 0418h	CAN0*2	Mask register 6	MKR6	32	8, 16, 32	2, 3 PCLK*3

Table 4.1 List of I/O Registers (Address Order) (22 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000C 21A0h	GPT1	General PWM timer cycle setting double-buffer register	GTPDBR	16	16, 32	3 to 5 ICLK*4
000C 21A4h	GPT1	A/D converter start request timing register A	GTADTRA	16	16, 32	3 to 5 ICLK*4
000C 21A6h	GPT1	A/D converter start request timing buffer register A	GTADTBRA	16	16, 32	3 to 5 ICLK*4
000C 21A8h	GPT1	A/D converter start request timing double-buffer register A	GTADTDBRA	16	16, 32	3 to 5 ICLK*4
000C 21ACh	GPT1	A/D converter start request timing register B	GTADTRB	16	16, 32	3 to 5 ICLK*4
000C 21AEh	GPT1	A/D converter start request timing buffer register B	GTADTBRB	16	16, 32	3 to 5 ICLK*4
000C 21B0h	GPT1	A/D converter start request timing double-buffer register B	GTADTDBRB	16	16, 32	3 to 5 ICLK*4
000C 21B4h	GPT1	General PWM timer output negate control register	GTONCR	16	16, 32	3 to 5 ICLK*4
000C 21B6h	GPT1	General PWM timer dead time control register	GTDTCR	16	16, 32	3 to 5 ICLK*4
000C 21B8h	GPT1	General PWM timer dead time value register	GTDVU	16	16, 32	3 to 5 ICLK*4
000C 21BAh	GPT1	General PWM timer dead time value register	GTDVD	16	16, 32	3 to 5 ICLK*4
000C 21BCh	GPT1	General PWM timer dead time buffer register	GTDBU	16	16, 32	3 to 5 ICLK*4
000C 21BEh	GPT1	General PWM timer dead time buffer register	GTDBD	16	16, 32	3 to 5 ICLK*4
000C 21C0h	GPT1	General PWM timer output protection function status register	GTSOS	16	16, 32	3 to 5 ICLK*4
000C 21C2h	GPT1	General PWM timer output protection temporary release register	GTSOTR	16	16, 32	3 to 5 ICLK*4
000C 2200h	GPT2	General PWM timer I/O control register	GTIOR	16	8, 16, 32	3 to 5 ICLK*4
000C 2202h	GPT2	General PWM timer interrupt output setting register	GTINTAD	16	8, 16, 32	3 to 5 ICLK*4
000C 2204h	GPT2	General PWM timer control register	GTCR	16	8, 16, 32	3 to 5 ICLK*4
000C 2206h	GPT2	General PWM timer buffer enable register	GTBER	16	8, 16, 32	3 to 5 ICLK*4
000C 2208h	GPT2	General PWM timer count direction register	GTUDC	16	8, 16, 32	3 to 5 ICLK*4
000C 220Ah	GPT2	General PWM timer interrupt and A/D converter start request skipping setting register	GTITC	16	8, 16, 32	3 to 5 ICLK*4
000C 220Ch	GPT2	General PWM timer status register	GTST	16	8, 16, 32	3 to 5 ICLK*4
000C 220Eh	GPT2	General PWM timer counter	GTCNT	16	16	3 to 5 ICLK*4
000C 2210h	GPT2	General PWM timer compare capture register A	GTCCRA	16	16, 32	3 to 5 ICLK*4
000C 2212h	GPT2	General PWM timer compare capture register B	GTCCRB	16	16, 32	3 to 5 ICLK*4
000C 2214h	GPT2	General PWM timer compare capture register C	GTCCRC	16	16, 32	3 to 5 ICLK*4
000C 2216h	GPT2	General PWM timer compare capture register D	GTCCRD	16	16, 32	3 to 5 ICLK*4
000C 2218h	GPT2	General PWM timer compare capture register E	GTCCRE	16	16, 32	3 to 5 ICLK*4
000C 221Ah	GPT2	General PWM timer compare capture register F	GTCCRF	16	16, 32	3 to 5 ICLK*4
000C 221Ch	GPT2	General PWM timer cycle setting register	GTPR	16	16, 32	3 to 5 ICLK*4
000C 221Eh	GPT2	General PWM timer cycle setting buffer register	GTPBR	16	16, 32	3 to 5 ICLK*4
000C 2220h	GPT2	General PWM timer cycle setting double-buffer register	GTPDBR	16	16, 32	3 to 5 ICLK*4
000C 2224h	GPT2	A/D converter start request timing register A	GTADTRA	16	16, 32	3 to 5 ICLK*4
000C 2226h	GPT2	A/D converter start request timing buffer register A	GTADTBRA	16	16, 32	3 to 5 ICLK*4
000C 2228h	GPT2	A/D converter start request timing double-buffer register A	GTADTDBRA	16	16, 32	3 to 5 ICLK*4

Table 4.2 List of I/O Registers (Bit Order) (7 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
ICU	DTCER180	—	—	—	—	—	—	—	DTCE
ICU	DTCER181	—	—	—	—	—	—	—	DTCE
ICU	DTCER182	—	—	—	—	—	—	—	DTCE
ICU	DTCER183	—	—	—	—	—	—	—	DTCE
ICU	DTCER184	—	—	—	—	—	—	—	DTCE
ICU	DTCER186	—	—	—	—	—	—	—	DTCE
ICU	DTCER187	—	—	—	—	—	—	—	DTCE
ICU	DTCER188	—	—	—	—	—	—	—	DTCE
ICU	DTCER189	—	—	—	—	—	—	—	DTCE
ICU	DTCER190	—	—	—	—	—	—	—	DTCE
ICU	DTCER192	—	—	—	—	—	—	—	DTCE
ICU	DTCER193	—	—	—	—	—	—	—	DTCE
ICU	DTCER194	—	—	—	—	—	—	—	DTCE
ICU	DTCER195	—	—	—	—	—	—	—	DTCE
ICU	DTCER196	—	—	—	—	—	—	—	DTCE
ICU	DTCER215	—	—	—	—	—	—	—	DTCE
ICU	DTCER216	—	—	—	—	—	—	—	DTCE
ICU	DTCER219	—	—	—	—	—	—	—	DTCE
ICU	DTCER220	—	—	—	—	—	—	—	DTCE
ICU	DTCER223	—	—	—	—	—	—	—	DTCE
ICU	DTCER224	—	—	—	—	—	—	—	DTCE
ICU	DTCER247	—	—	—	—	—	—	—	DTCE
ICU	DTCER248	—	—	—	—	—	—	—	DTCE
ICU	DTCER254	—	—	—	—	—	—	—	DTCE
ICU	IER02	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER03	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER05	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER07	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER08	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER0C	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER0D	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER0E	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER0F	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER10	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER11	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER12	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER13	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER15	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER16	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER17	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER18	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER1A	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER1B	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER1C	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER1E	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	IER1F	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
ICU	SWINTR	—	—	—	—	—	—	—	SWINT
ICU	FIR	FIEN	—	—	—	—	—	—	—
		FVCT[7:0]							
ICU	IPR00	—	—	—	—	IPR[3:0]			
ICU	IPR01	—	—	—	—	IPR[3:0]			
ICU	IPR02	—	—	—	—	IPR[3:0]			

Table 4.2 List of I/O Registers (Bit Order) (12 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
RSPI0	SSLP	—	—	—	—	SSLP3	SSLP2	SSLP1	SSLP0
RSPI0	SPPCR	—	—	MOIFE	MOIFV	—	—	SPLP2	SPLP
RSPI0	SPSR	SPRF	—	SPTEF	—	PERF	MODF	IDLNF	OVRF
RSPI0	SPDR	H[15:0]							
		H[15:0]							
		L[15:0]							
		L[15:0]							
RSPI0	SPSCR	—	—	—	—	—		SPSLN[2:0]	
RSPI0	SPSSR	—		SPECM[2:0]		—		SPCP[2:0]	
RSPI0	SPBR	SPR7	SPR6	SPR5	SPR4	SPR3	SPR2	SPR1	SPR0
RSPI0	SPDCR	—	—	SPLW	SPRDTD	SLSEL[1:0]		SPFC[1:0]	
RSPI0	SPCKD	—	—	—	—	—		SCKDL[2:0]	
RSPI0	SSLND	—	—	—	—	—		SLNDL[2:0]	
RSPI0	SPND	—	—	—	—	—		SPNDL[2:0]	
RSPI0	SPCR2	—	—	—	—	PTE	SPIIE	SPOE	SPPE
RSPI0	SPCMD0	SCKDEN	SLNDEN	SPNDEN	LSBF		SPB[3:0]		
		SSLKP		SSLA[2:0]		BRDV[1:0]		CPOL	CPHA
RSPI0	SPCMD1	SCKDEN	SLNDEN	SPNDEN	LSBF		SPB[3:0]		
		SSLKP		SSLA[2:0]		BRDV[1:0]		CPOL	CPHA
RSPI0	SPCMD2	SCKDEN	SLNDEN	SPNDEN	LSBF		SPB[3:0]		
		SSLKP		SSLA[2:0]		BRDV[1:0]		CPOL	CPHA
RSPI0	SPCMD3	SCKDEN	SLNDEN	SPNDEN	LSBF		SPB[3:0]		
		SSLKP		SSLA[2:0]		BRDV[1:0]		CPOL	CPHA
RSPI0	SPCMD4	SCKDEN	SLNDEN	SPNDEN	LSBF		SPB[3:0]		
		SSLKP		SSLA[2:0]		BRDV[1:0]		CPOL	CPHA
RSPI0	SPCMD5	SCKDEN	SLNDEN	SPNDEN	LSBF		SPB[3:0]		
		SSLKP		SSLA[2:0]		BRDV[1:0]		CPOL	CPHA
RSPI0	SPCMD6	SCKDEN	SLNDEN	SPNDEN	LSBF		SPB[3:0]		
		SSLKP		SSLA[2:0]		BRDV[1:0]		CPOL	CPHA
RSPI0	SPCMD7	SCKDEN	SLNDEN	SPNDEN	LSBF		SPB[3:0]		
		SSLKP		SSLA[2:0]		BRDV[1:0]		CPOL	CPHA
S12AD0	ADCSR	ADST	ADCS[1:0]		ADIE	CKS[1:0]		TRGE	EXTRG
S12AD0	ADANS	—	—	CH[1:0]		—	PG002SEL	PG001SEL	PG000SEL
		—	—	—	—	—	PG002EN	PG001EN	PG000EN
S12AD0	ADPG	—	—	—	—	PG002GAIN[3:0]			
		PG001GAIN[3:0]				PG000GAIN[3:0]			
S12AD0	ADCER	ADRFMT	—	ADIEW	ADIE2	DIAGM	DIAGLD	DIAGVAL[1:0]	
		—	—	ACE	—	—	ADPRC[1:0]		SHBYP
S12AD0	ADSTRGR	—	—	—	ADSTRS1[4:0]				
		—	—	—	ADSTRS0[4:0]				
S12AD	ADCMPMD0	—	—	CEN102[1:0]		CEN101[1:0]		CEN100[1:0]	
		—	—	CEN002[1:0]		CEN001[1:0]		CEN000[1:0]	
S12AD	ADCMPMD1	—	VSELL1	VSELH1	CSEL1	—	VSELL0	VSELH0	CSEL0
		—		REFH[2:0]		—		REFL[2:0]	
S12AD	ADCMPNR0	—	—	—	—	C002NR[3:0]			
		C001NR[3:0]				C000NR[3:0]			
S12AD	ADCMPNR1	—	—	—	—	C102NR[3:0]			
		C101NR[3:0]				C100NR[3:0]			
S12AD	ADCMPFR	—	—	C102FLAG	C101FLAG	C100FLAG	C002FLAG	C001FLAG	C000FLAG
S12AD	ADCMPSEL	—	—	—	—	—	—	POERQ	IE
		—	—	SEL102	SEL101	SEL100	SEL002	SEL001	SEL000

Table 4.2 List of I/O Registers (Bit Order) (16 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
POE	POECR2	—	—	—	—	—	MTU3BDZE	MTU4ACZE	MTU4BDZE
		—	—	—	—	—	MTU6BDZE	MTU7ACZE	MTU7BDZE
POE	POECR3	—	—	—	—	—	—	GPT3ABZE	GPT2ABZE
		—	—	—	—	—	—	GPT1ABZE	GPT0ABZE
POE	POECR4	—	—	IC5ADDMT67ZE	IC4ADDMT67ZE	IC3ADDMT67ZE	—	IC1ADDMT67ZE	CMADDMT67ZE
		—	—	IC5ADDMT34ZE	IC4ADDMT34ZE	IC3ADDMT34ZE	IC2ADDMT34ZE	—	CMADDMT34ZE
POE	POECR5	—	—	—	—	—	—	—	—
		—	—	IC5ADDMT0ZE	IC4ADDMT0ZE	—	IC2ADDMT0ZE	IC1ADDMT0ZE	CMADDMT0ZE
POE	POECR6	—	—	—	IC4ADDGPT23ZE	IC3ADDGPT23ZE	IC2ADDGPT23ZE	IC1ADDGPT23ZE	CMADDGPT23ZE
		—	—	IC5ADDGPT01ZE	—	IC3ADDGPT01ZE	IC2ADDGPT01ZE	IC1ADDGPT01ZE	CMADDGPT01ZE
POE	ICSR4	—	—	—	POE10F	—	—	POE10E	PIE4
		—	—	—	—	—	—	POE10M[1:0]	
POE	ALR1	—	—	—	—	—	—	—	—
		OLSEN	—	OLSG2B	OLSG2A	OLSG1B	OLSG1A	OLSG0B	OLSG0A
POE	ICSR5	—	—	—	POE11F	—	—	POE11E	PIE5
		—	—	—	—	—	—	POE11M[1:0]	
CAN0*3	MB.ID	IDE	RTR	—			SID[10:0]		
				SID[10:0]				EID[17:0]	
					EID[17:0]				
					EID[17:0]				
	MB.DLC	—	—	—	—	—	—	—	—
		—	—	—	—		DLC[3:0]		
	MB.DATA 0 to 7								
	MB.TS				TSH[7:0]				
					TSL[7:0]				
CAN0*3	MKR0	—	—	—			SID[10:0]		
				SID[10:0]				EID[17 0]	
					EID[17:0]				
					EID[17:0]				
CAN0*3	MKR1	—	—	—			SID[10:0]		
				SID[10:0]				EID[17 0]	
					EID[17:0]				
					EID[17:0]				
CAN0*3	MKR2	—	—	—			SID[10:0]		
				SID[10:0]				EID[17 0]	
					EID[17:0]				
					EID[17:0]				
CAN0*3	MKR3	—	—	—			SID[10:0]		
				SID[10:0]				EID[17 0]	
					EID[17:0]				
					EID[17:0]				
CAN0*3	MKR4	—	—	—			SID[10:0]		
				SID[10:0]				EID[17 0]	
					EID[17:0]				
					EID[17:0]				

Table 4.2 List of I/O Registers (Bit Order) (20 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
MTU0	TMDR1	—	BFE	BFB	BFA			MD[3:0]	
MTU0	TIORH		IOB[3:0]					IOA[3:0]	
MTU0	TIORL		IOD[3:0]					IOC[3:0]	
MTU0	TIER	TTEG	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA
MTU0	TSR	—	—	—	TCFV	TGFD	TGFC	TGFB	TGFA
MTU0	TCNT								
MTU0	TGRA								
MTU0	TGRB								
MTU0	TGRC								
MTU0	TGRD								
MTU0	TGRE								
MTU0	TGRF								
MTU0	TIER2	TTGE2	—	—	—	—	—	TGIEF	TGIEE
MTU0	TSR2	—	—	—	—	—	—	TGFF	TGFE
MTU0	TBTM	—	—	—	—	—	TTSE	TTSB	TTSA
MTU1	TCR	—	CCLR[1:0]		CKEG[1:0]			TPSC[2:0]	
MTU1	TMDR1	—	—	—	—			MD[3:0]	
MTU1	TIOR		IOB[3:0]					IOA[3:0]	
MTU1	TIER	TTEG	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA
MTU1	TSR	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA
MTU1	TCNT								
MTU1	TGRA								
MTU1	TGRB								
MTU1	TICCR	—	—	—	—	I2BE	I2AE	I1BE	I1AE
MTU2	TCR	—	CCLR[1:0]		CKEG[1:0]			TPSC[2:0]	
MTU2	TMDR1	—	—	—	—			MD[3:0]	
MTU2	TIOR		IOB[3:0]					IOA[3:0]	
MTU2	TIER	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA
MTU2	TSR	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA
MTU2	TCNT								
MTU2	TGRA								
MTU2	TGRB								
MTU6	TCR		CCLR[20]		CKEG[1:0]			TPSC[2:0]	
MTU7	TCR		CCLR[20]		CKEG[1:0]			TPSC[2:0]	
MTU6	TMDR1	—	—	BFB	BFA			MD[3:0]	
MTU7	TMDR1	—	—	BFB	BFA			MD[3:0]	
MTU6	TIORH		IOB[3:0]					IOA[3:0]	
MTU6	TIORL		IOD[3:0]					IOC[3:0]	
MTU7	TIORH		IOB[3:0]					IOA[3:0]	

Table 4.2 List of I/O Registers (Bit Order) (28 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
GPT3	GTCCRB								
GPT3	GTCCRC								
GPT3	GTCCRD								
GPT3	GTCCRE								
GPT3	GTCCRF								
GPT3	GTPR								
GPT3	GTPBR								
GPT3	GTPDBR								
GPT3	GTADTRA								
GPT3	GTADTBRA								
GPT3	GTADTDBRA								
GPT3	GTADTRB								
GPT3	GTADTBRB								
GPT3	GTADTDBRB								
GPT3	GTONCR	OBE	OAE	—	SWN	—	—	—	NFV
				NFS[3:0]		NVB	NVA	NEB	NEA
GPT3	GTDTCR	—	—	—	—	—	—	—	TDFER
		—	—	TDBDE	TDBUE	—	—	—	TDE
GPT3	GTDVU								
GPT3	GTDVD								
GPT3	GTDBU								
GPT3	GTDBD	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	SOS[1:0]	
GPT3	GTSOS	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	SOS[1:0]	
GPT3	GTSOTR	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	SOTR
GPT0	GTDLYCR	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLYEN	DLYRST	DLLEN
GPT1	GTDLYCR	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLYEN	DLYRST	DLLEN

Table 5.2 DC Characteristics (1) (2 / 3)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	All output pins (except for P71 to P76 and P90 to P95)	V_{OH}	VCC-0.5	-	-	V	I_{OH} = -1 mA
	P71 to P76		VCC-0.5	-	-		I_{OH} = -1mA 64-pin LQFP Condition 3
			VCC-1.0	-	-		I_{OH} = -5mA 64-pin LQFP Other than condition 3
	P90 to P95		VCC-0.5	-	-		I_{OH} = -1mA 80-pin LQFP or 64-pin LQFP
			VCC-1.0	-	-		I_{OH} = -5 mA 112-pin LQFP or 100-pin LQFP
Output low voltage	All output pins (except for P71 to P76, P90 to P95, and RIIC)	V_{OL}	-	-	0.5	V	I_{OL} = 1.0 mA
	P71 to P76		-	-	0.5		I_{OL} = 1.0 mA 64-pin LQFP Other than condition 3
			-	-	1.1		I_{OL} = 15 mA Conditions 1 and 2
			-	-	1.4		I_{OL} = 15 mA Other than 64-pin LQFP Condition 3
	P90 to P95		-	-	0.5		I_{OL} = 1.0 mA 80-pin LQFP or 64-pin LQFP
			-	-	1.1		I_{OL} = 15 mA 112-pin LQFP or 100-pin LQFP Conditions 1 and 2
			-	-	1.4		I_{OL} = 1 mA 112-pin LQFP or 100-pin LQFP Condition 3
	RIIC pin		-	-	0.4		I_{OL} = 3 mA
			-	-	0.6		I_{OL} = 6 mA
Input leakage current	RES#, MD pin, EMLE	$\lvert I_{in} \rvert$	-	-	1.0	µA	V_{in} = 0 V, V_{in} = VCC
Three-state leakage current (off state)	Ports 1 to A, PB0, PB3 to PB7, D, E, G	$\lvert I_{TSI} \rvert$	-	-	1.0	µA	V_{in} = 0 V, V_{in} = VCC
	Ports PB1 and PB2		-	-	5.0		

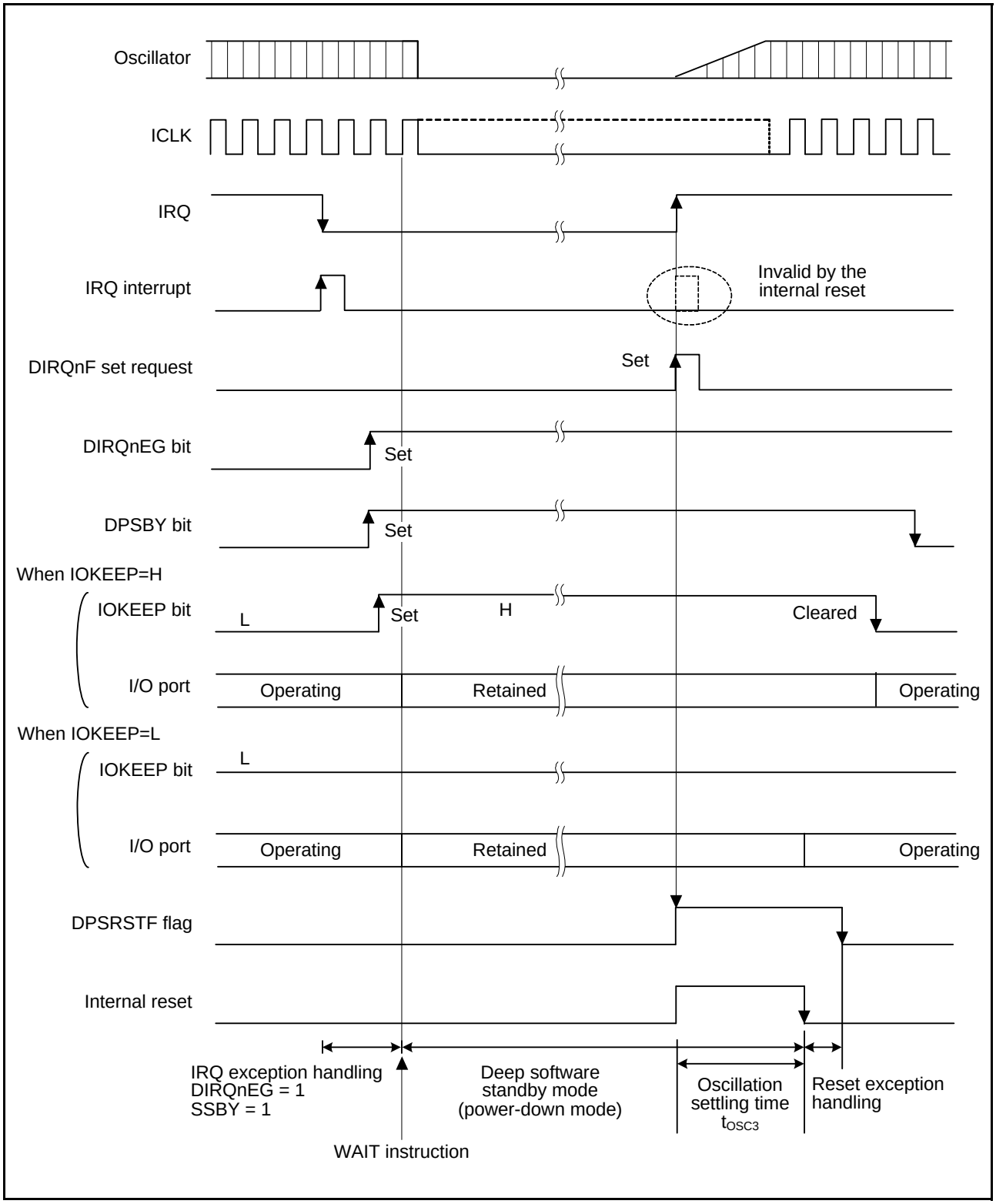


Figure 5.3 Oscillation Settling Timing after Deep Software Standby Mode

Table 5.12 Timing of On-Chip Peripheral Modules (4)

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Max.	Unit	Test Conditions
MTU3	Input capture input pulse width (single-edge setting)	t_{TICW}	3.0	-	t_{Icyc}	Figure 5.16
	Input capture input pulse width (both-edge setting)	t_{TICW}	5.0	-	t_{Icyc}	
	Timer clock pulse width (single-edge setting)	$t_{TCKWH/L}$	3.0	-	t_{Icyc}	Figure 5.17
	Timer clock pulse width (both-edge setting)	$t_{TCKWH/L}$	5.0	-	t_{Icyc}	
	Timer clock pulse width (phase coefficient mode)	$t_{TCKWH/L}$	5.0	-	t_{Icyc}	
GPT	Input capture input pulse width (single-edge setting)	t_{GTICW}	3.0	-	t_{Icyc}	Figure 5.18
	Input capture input pulse width (both-edge setting)	t_{GTICW}	5.0	-	t_{Icyc}	

Note: • t_{Icyc}: ICLK cycle

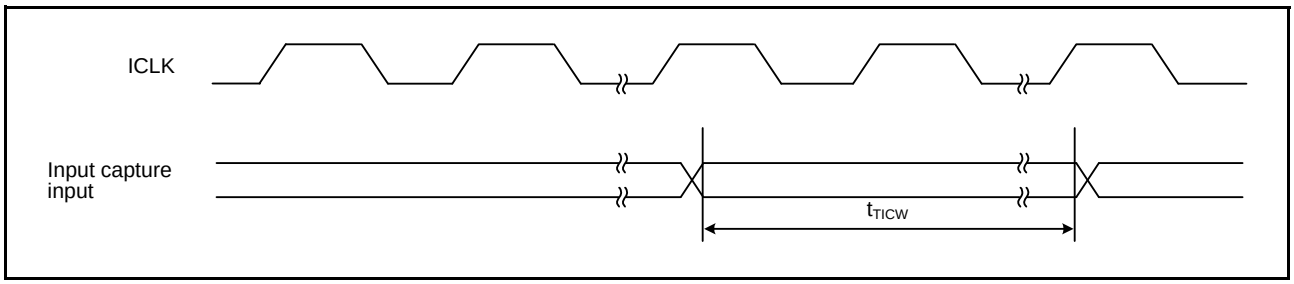


Figure 5.16 MTU3 Input/Output Timing

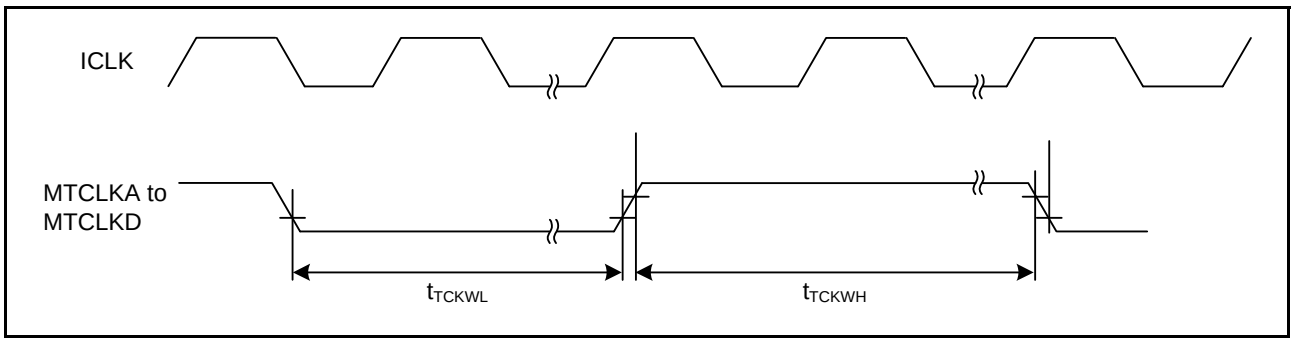


Figure 5.17 MTU3 Clock Input Timing

Table 5.17 Characteristics of the Programmable Gain Amplifier

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

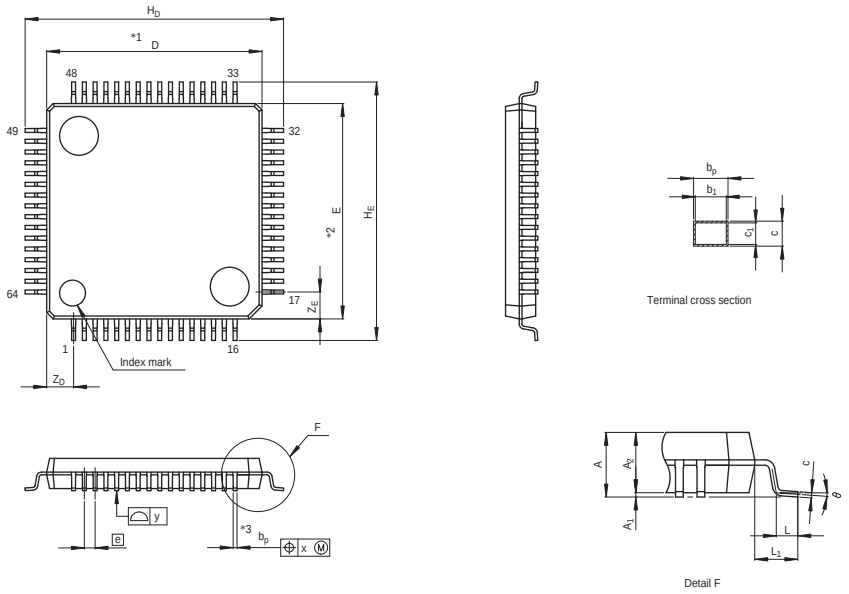
Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog input capacitance		Cin	-	-	6	pF	
Input offset voltage		Voff	-	-	8	mV	
Input voltage range (Vin)	Gain × 2.000	Vin	0.050 x AVcc	-	0.450 x AVcc	V	
	Gain × 2.500		0.047 x AVcc	-	0.360 x AVcc		
	Gain × 3.077		0.045 x AVcc	-	0.292 x AVcc		
	Gain × 3.636		0.042 x AVcc	-	0.247 x AVcc		
	Gain × 4.000		0.040 x AVcc	-	0.212 x AVcc		
	Gain × 4.444		0.036 x AVcc	-	0.191 x AVcc		
	Gain × 5.000		0.033 x AVcc	-	0.170 x AVcc		
	Gain × 5.714		0.031 x AVcc	-	0.148 x AVcc		
	Gain × 6.667		0.029 x AVcc	-	0.127 x AVcc		
	Gain × 10.000		0.025 x AVcc	-	0.08 x AVcc		
	Gain × 13.333		0.023 x AVcc	-	0.06 x AVcc		
Slew rate		SR	10	-	-	V/µs	
Gain error	Gain × 2.000	-	-	-	1	%	
	Gain × 2.500		-	-	1		
	Gain × 3.077		-	-	1		
	Gain × 3.636		-	-	1.5		
	Gain × 4.000		-	-	1.5		
	Gain × 4.444		-	-	2		
	Gain × 5.000		-	-	2		
	Gain × 5.714		-	-	2		
	Gain × 6.667		-	-	3		
	Gain × 10.000		-	-	4		
	Gain × 13.333		-	-	4		

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure D 64-Pin LQFP (PLQP0064KB-A) Package Dimensions

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.