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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	44
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 4x10b, 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562t7ddff-v3

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and Table 1.2 lists the functions of products.

Table 1.1 Outline of Specifications (1 / 5)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 100MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4-Gbyte linear • Register set of the CPU • General purpose: Sixteen 32-bit registers • Control: Nine 32-bit registers • Accumulator: One 64-bit register • Basic instructions: 73 • Floating-point instructions: 8 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement • Instructions: Little endian • Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 x 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Memory-protection unit (MPU)
	FPU	• Single precision (32-bit) floating point • Data types and floating-point exceptions in conformance with the IEEE754 standard
Memory	ROM	• ROM capacity: 256 Kbytes (max.) • Two on-board programming modes • Boot mode (The user MAT is programmable via the SCI) • User program mode • Off-board programming • A PROM programmer can be used to program the user mat.
	RAM	• RAM capacity: 16 Kbytes (max.)
	Data flash	• Data flash capacity: 32 Kbytes (max.) • Supports background operations (BGO)
MCU operating mode		• Single-chip mode
Clock	Clock generation circuit	• One circuit: Main clock oscillator • Internal oscillator: Low-speed on-chip oscillator dedicated to IWDT • Structure of a PLL frequency synthesizer and frequency divider for selectable operating frequency • Oscillation stoppage detection • Independent frequency-division and multiplication settings for the system clock (ICLK) and peripheral module clock (PCLK) • The CPU and system sections such as other bus masters, MTU3, and GPT run in synchronization with the system clock (ICLK): 8 to 100 MHz. • Peripheral modules run in synchronization with the peripheral module clock (PCLK): 8 to 50 MHz
Reset		Pin reset, power-on reset (automatic power-on reset when the power is turned on), voltage-monitoring reset, watchdog timer reset, independent watchdog timer reset, and deep software standby reset
Voltage detection circuit (LVD)		When the voltage on VCC falls below the voltage detection level (Vdet), an internal reset or internal interrupt is generated.
Low power consumption	Low power consumption facilities	• Module stop function • Four low power consumption modes • Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode

Table 1.1 Outline of Specifications (4 / 5)

Classification	Module/Function	Description
Communications	CAN module (CAN) (as an optional function)	• 1 channel • 32 mailboxes
	Serial peripheral interface (RSPI)	• 1 unit • RSPI transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPI clock (RSPCK) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) Capable of handling serial transfer as a master or slave • Data formats Switching between MSB first and LSB first The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Buffered structure • Double buffers for both transmission and reception
	LIN module (LIN)	• 1 channel (LIN master) • Supports revisions 1.3, 2.0, and 2.1 of the LIN protocol
A/D converter	12-bit A/D converter (S12ADA)	• 12 bits (2 units x 4 channels) • 12-bit resolution • Conversion time: 1.0 μs per channel (in operation with A/D conversion clock ADCLK at 50 MHz) for AVCC = 4.0 to 5.5 V 2.0 μs per channel (in operation with A/D conversion clock ADCLK at 25 MHz) for AVCC0 = 3.0 to 3.6 V • Two basic operating modes Single mode and scan mode • Scan mode One-cycle scan mode Continuous scan mode 2-channel scan mode (Input ports of the A/D unit are divided into two groups in this mode, and the activation sources are separately selectable for each group.) • Sample-and-hold function A common sample-and-hold circuit for both units is included. Additionally, sample-and-hold circuit for each unit is included. (three channels per unit) • A/D-conversion register settings for each input pin. • Two registers for the result of conversion are provided for a single analog input pin of each unit (AN000 and AN100). • Three ways to start A/D conversion Conversion can be started by software, a conversion start trigger from a timer (MTU3 or GPT), or an external trigger signal. • Functionality for 8- or 10-bit precision output Right-shifting of the results of conversion for output by two or four bits is selectable. • Self-diagnostic function The self-diagnostic function internally generates three analog input voltages (VREFL0, VREFH0 x 1/2, VREFH0). • Amplification of input signals by a programmable gain amplifier (three channels per unit) Amplification rate: 2.0-, 2.5-, 3.077-, 3.636-, 4.0-, 4.444-, 5.0-, 5.714-, 6.667-, 10.0-, or 13.333-times amplification (a total of 11 steps) • Window comparators (three channels per unit)

Table 1.2 Functions of RX62T Group and RX62G Group Products (2 / 2)

Functions	RX62G Group		RX62T Group				
Pin number	**112 Pins**	**100 Pins**	**112 Pins**	**100 Pins**	**80 Pins (R5F562T xGDFF)**	**80 Pins**	**64 Pins**
Package	LQFP2020 (0.65-mm pitch)	LQFP1414 (0.5-mm pitch)	LQFP2020 (0.65-mm pitch)	LQFP1414 (0.5-mm pitch)	LQFP1414 (0.65-mm pitch)	LQFP1414 (0.65-mm pitch)	LQFP1010 (0.5-mm pitch) LQFP1414 (0.8-mm pitch)

O: Supported, —: Not supported

Note 1. For the MTU and GPT, the number of pins will differ with the package. See the list of pins and pin functions for details. In addition, the CAN module is an optional function. See Table 1.3 for details.

1.4 Pin Assignments

Figure 1.3 to Figure 1.7 show the pins assignments. Table 1.4 to Table 1.8 show the list of pins and pin functions.

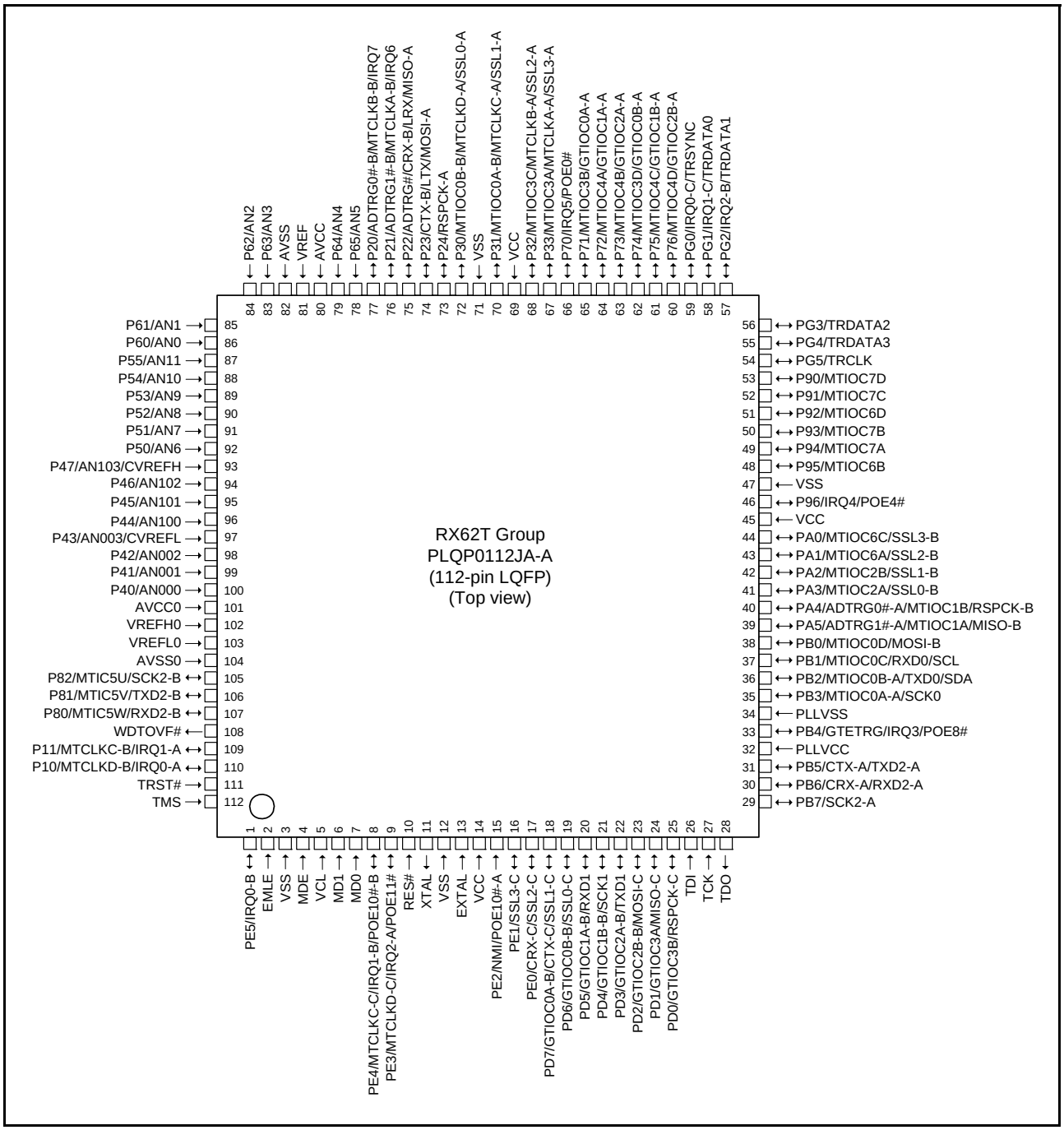


Figure 1.3 Pin Assignment of the 112-Pin LQFP

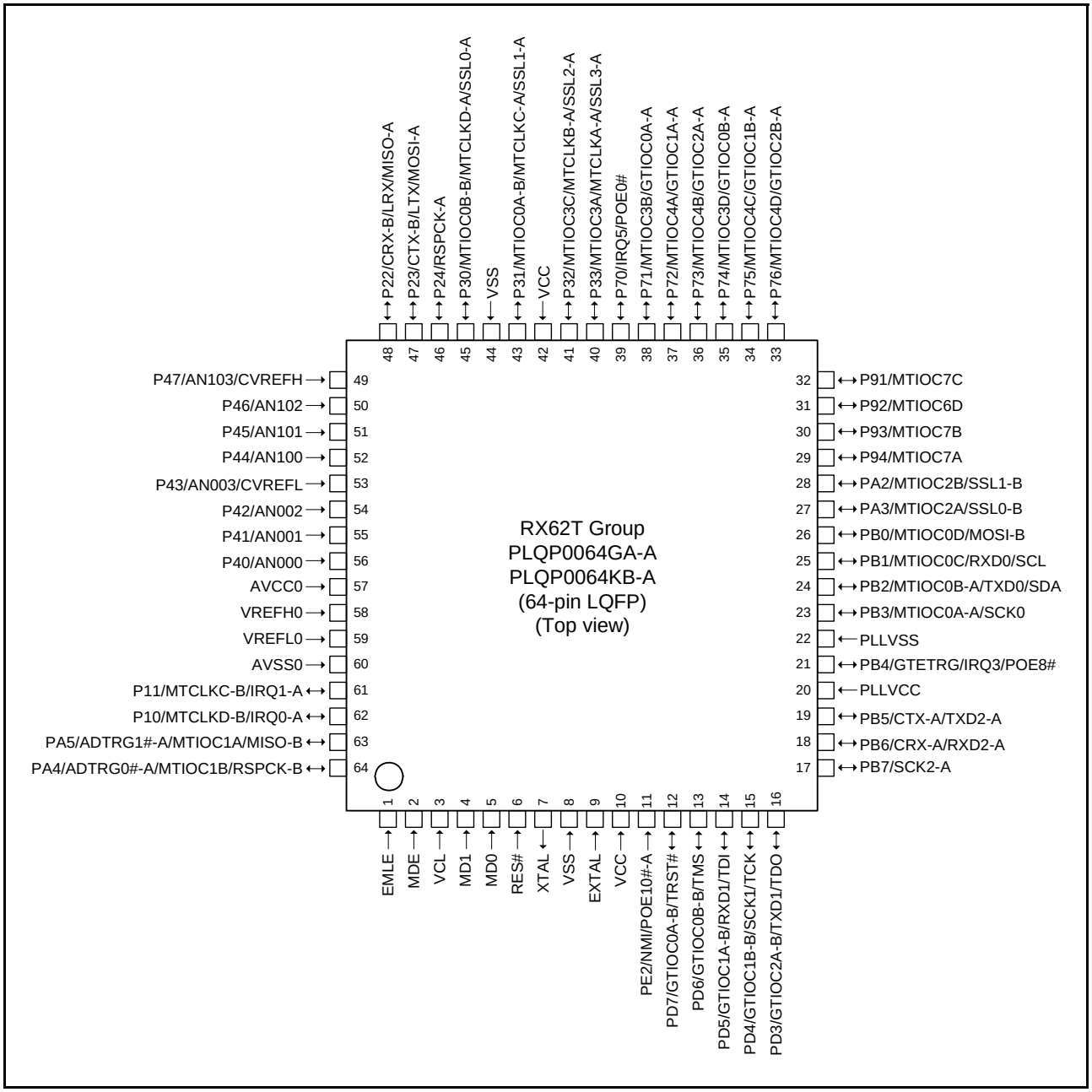


Figure 1.7 Pin Assignment of the 64-Pin LQFP

Table 1.4 List of Pins and Pin Functions (112-Pin LQFP) (3 / 3)

Pin No. (112-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi-cation	Interrupt	POE	Debugging
80	AVCC							
81	VREF							
82	AVSS							
83		P63	AN3					
84		P62	AN2					
85		P61	AN1					
86		P60	AN0					
87		P55	AN11					
88		P54	AN10					
89		P53	AN9					
90		P52	AN8					
91		P51	AN7					
92		P50	AN6					
93		P47	AN103/ CVREFH					
94		P46	AN102					
95		P45	AN101					
96		P44	AN100					
97		P43	AN003/ CVREFL					
98		P42	AN002					
99		P41	AN001					
100		P40	AN000					
101	AVCC0							
102	VREFH0							
103	VREFL0							
104	AVSS0							
105		P82		MTIC5U	SCK2-B			
106		P81		MTIC5V	TXD2-B			
107		P80		MTIC5W	RXD2-B			
108				WDTOVF#				
109		P11		MTCLKC-B		IRQ1-A		
110		P10		MTCLKD-B		IRQ0-A		
111								TRST#
112								TMS

Table 1.5 List of Pins and Pin Functions (100-Pin LQFP) (3 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi-cation	Interrupt	POE	Debugging
77		P60	AN0					
78		P55	AN11					
79		P54	AN10					
80		P53	AN9					
81		P52	AN8					
82		P51	AN7					
83		P50	AN6					
84		P47	AN103/ CVREFH					
85		P46	AN102					
86		P45	AN101					
87		P44	AN100					
88		P43	AN003/ CVREFL					
89		P42	AN002					
90		P41	AN001					
91		P40	AN000					
92	AVCC0							
93	VREFH0							
94	VREFL0							
95	AVSS0							
96		P82		MTIC5U	SCK2-B			
97		P81		MTIC5V	TXD2-B			
98		P80		MTIC5W	RXD2-B			
99		P11		MTCLKC-B		IRQ1-A		
100		P10		MTCLKD-B		IRQ0-A		

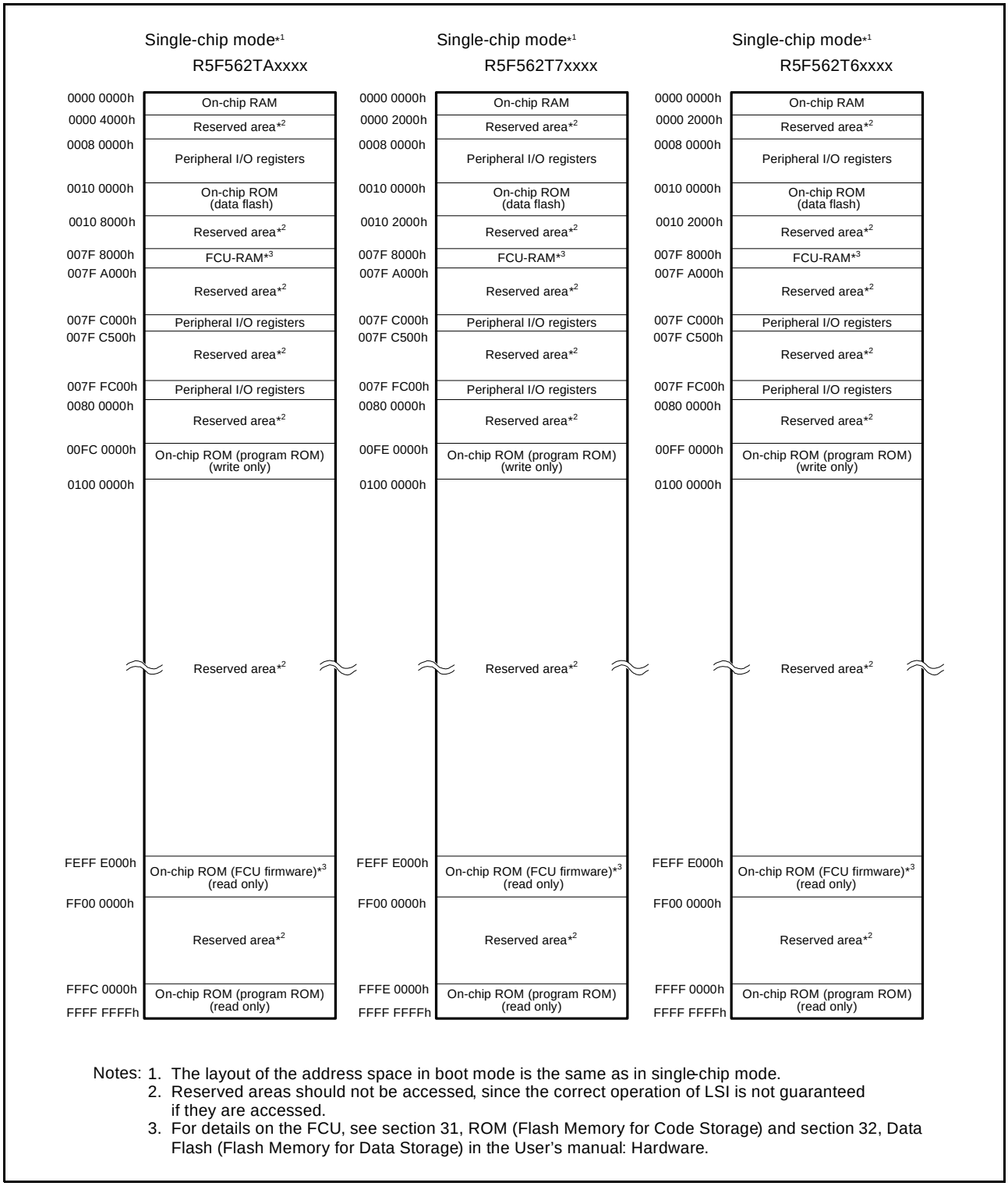
Table 1.9 Pin Functions (3 / 4)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCIb)	TXD0, TXD1, TXD2-A/TXD2-B	Output	Output pins for data transmission. The TXD2-B pin is not included in the 80-/64-pin versions.
	RXD0, RXD1, RXD2-A/ RXD2-B	Input	Input pins for data reception. The RXD2-B pin is not included in the 80-/64-pin versions.
	SCK0, SCK1, SCK2-A/ SCK2-B	I/O	Input/output pins for clock signals. The SCK2-B pin is not included in the 80-/64-pin versions.
I^2C bus interface (RIIC)	SCL	I/O	Input/output pin for I^2C bus interface clocks. Bus can be directly driven by the NMOS open drain output.
	SDA	I/O	Input/output pin for I^2C bus interface data. Bus can be directly driven by the NMOS open drain output.
CAN module (CAN) (as an optional function)	CRX-A/CRX-B/CRX-C	Input	Input pin for the CAN. The CRX-C pin is not included in the 64-pin version.
	CTX-A/CTX-B/CTX-C	Output	Output pin for the CAN. The CTX-C pin is not included in the 64-pin version.
LIN module (LIN)	LRX	Input	Input pin for the LIN.
	LTX	Output	Output pin for the LIN.
Serial peripheral interface (RSPI)	RSPCK-A/RSPCK-B/ RSPCK-C	I/O	Clock input/output pin for the RSPI. The RSPCK-C pin is not included in the 80-/64-pin versions.
	MOSI-A/MOSI-B/MOSI-C	I/O	Inputs or outputs data output from the master for the RSPI. The MOSI-C pin is not included in the 80-/64-pin versions.
	MISO-A/MISO-B/MISO-C	I/O	Inputs or outputs data output from the slave for the RSPI. The MISO-C pin is not included in the 80-/64-pin versions.
	SSL0-A/SSL0-B/SSL0-C	I/O	Select the slave for the RSPI. The SSL0-C/SSL1-C/SSL2-C/ SSL3-C pin is not included in the 80-/64-pin versions.
	SSL1-A/SSL1-B/SSL1-C SSL2-A/SSL2-B/SSL2-C SSL3-A/SSL3-B/SSL3-C	Output	
A/D converter	AN000 to AN003 AN100 to AN103	Input	Input pins for the analog signals to be processed by the 12-bit A/D converter.
	AN0 to AN11	Input	Input pins for the analog signals to be processed by the 10-bit A/D converter. The AN4 to AN11 pins are not included in the 80-pin version. Not included in the 64-pin version.
	ADTRG0#-A/ADTRG0#-B ADTRG1#-A/ADTRG1#-B ADTRG#	Input	Input pins for the external trigger signals that start the A/D conversion. The ADTRG0#-B/ADTRG1#-B/ADTRG# pin is not included in the 64-pin version.
	CVREFH	Input	Input pin for the high-level reference voltage to the comparator
	CVREFL	Input	Input pin for the low-level reference voltage to the comparator
Analog power supply	AVCC0	Input	Analog power supply pin for the 12-bit A/D converter. When the A/D converter is not in use, connect this pin to the system power supply.
	AVSS0	Input	Ground pin for the 12-bit A/D converter. Connect this pin to the system power supply (0 V).
	VREFH0	Input	Reference power supply pin for the 12-bit A/D converter. When the 12-bit A/D converter is not in use, connect this pin to the system power supply.
	VREFL0	Input	Ground pin of the reference power supply pin for the 12-bit A/D converter. When the 12-bit A/D converter is not in use, connect this pin to the system power supply (0 V).
	AVCC	Input	Analog power supply pin for the 10-bit A/D converter. When the A/D converter is not in use, connect this pin to the system power supply. Not included in the 64-pin version.
	AVSS	Input	Ground pin for the 10-bit A/D converter. Connect this pin to the system power supply (0 V). Not included in the 64-pin version.
	VREF	Input	Reference power supply pin for the 10-bit A/D converter. When the 10-bit A/D converter is not in use, connect this pin to the system power supply. Not included in the 80-/64-pin versions.

3. Address Space

3.1 Address Space

This LSI has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas. Figure 3.1 shows the memory maps.



Notes: 1. The layout of the address space in boot mode is the same as in single-chip mode.
2. Reserved areas should not be accessed, since the correct operation of LSI is not guaranteed if they are accessed.
3. For details on the FCU, see section 31, ROM (Flash Memory for Code Storage) and section 32, Data Flash (Flash Memory for Data Storage) in the User's manual: Hardware.

Figure 3.1 Memory Map (RX62T Group)

Table 4.1 List of I/O Registers (Address Order) (8 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 7382h	ICU	Interrupt source priority register 82	IPR82	8	8	2 ICLK
0008 7388h	ICU	Interrupt source priority register 88	IPR88	8	8	2 ICLK
0008 7389h	ICU	Interrupt source priority register 89	IPR89	8	8	2 ICLK
0008 738Ah	ICU	Interrupt source priority register 8A	IPR8A	8	8	2 ICLK
0008 738Bh	ICU	Interrupt source priority register 8B	IPR8B	8	8	2 ICLK
0008 7390h	ICU	Interrupt source priority register 90	IPR90	8	8	2 ICLK
0008 7500h	ICU	IRQ control register 0	IRQCR0	8	8	2 ICLK
0008 7501h	ICU	IRQ control register 1	IRQCR1	8	8	2 ICLK
0008 7502h	ICU	IRQ control register 2	IRQCR2	8	8	2 ICLK
0008 7503h	ICU	IRQ control register 3	IRQCR3	8	8	2 ICLK
0008 7504h	ICU	IRQ control register 4	IRQCR4	8	8	2 ICLK
0008 7505h	ICU	IRQ control register 5	IRQCR5	8	8	2 ICLK
0008 7506h	ICU	IRQ control register 6	IRQCR6	8	8	2 ICLK
0008 7507h	ICU	IRQ control register 7	IRQCR7	8	8	2 ICLK
0008 7580h	ICU	Non-maskable interrupt status register	NMISR	8	8	2 ICLK
0008 7581h	ICU	Non-maskable interrupt enable register	NMIER	8	8	2 ICLK
0008 7582h	ICU	Non-maskable interrupt clear register	NMICLR	8	8	2 ICLK
0008 7583h	ICU	NMI pin interrupt control register	NMICR	8	8	2 ICLK
0008 8000h	CMT	Compare match timer start register 0	CMSTR0	16	16	2, 3 PCLK*3
0008 8002h	CMT0	Compare match timer control register	CMCR	16	16	2, 3 PCLK*3
0008 8004h	CMT0	Compare match timer counter	CMCNT	16	16	2, 3 PCLK*3
0008 8006h	CMT0	Compare match timer constant register	CMCOR	16	16	2, 3 PCLK*3
0008 8008h	CMT1	Compare match timer control register	CMCR	16	16	2, 3 PCLK*3
0008 800Ah	CMT1	Compare match timer counter	CMCNT	16	16	2, 3 PCLK*3
0008 800Ch	CMT1	Compare match timer constant register	CMCOR	16	16	2, 3 PCLK*3
0008 8010h	CMT	Compare match timer start register 1	CMSTR1	16	16	2, 3 PCLK*3
0008 8012h	CMT2	Compare match timer control register	CMCR	16	16	2, 3 PCLK*3
0008 8014h	CMT2	Compare match timer counter	CMCNT	16	16	2, 3 PCLK*3
0008 8016h	CMT2	Compare match timer constant register	CMCOR	16	16	2, 3 PCLK*3
0008 8018h	CMT3	Compare match timer control register	CMCR	16	16	2, 3 PCLK*3
0008 801Ah	CMT3	Compare match timer counter	CMCNT	16	16	2, 3 PCLK*3
0008 801Ch	CMT3	Compare match timer constant register	CMCOR	16	16	2, 3 PCLK*3
0008 8028h	WDT	Timer control/status register	TCSR	8	8	2, 3 PCLK*3
0008 8028h	WDT	Write window A register	WINA	16	16	2, 3 PCLK*3
0008 8029h	WDT	Timer counter	TCNT	8	8	2, 3 PCLK*3
0008 802Ah	WDT	Write window B register	WINB	16	16	2, 3 PCLK*3
0008 802Bh	WDT	Reset control/status register	RSTCSR	8	8	2, 3 PCLK*3
0008 8030h	IWDT	IWDT refresh register	IWDTRR	8	8	2, 3 PCLK*3
0008 8032h	IWDT	IWDT control register	IWDTCR	16	16	2, 3 PCLK*3
0008 8034h	IWDT	IWDT status register	IWDTSR	16	16	2, 3 PCLK*3
0008 8040h	ADA	A/D data register A	ADDRA	16	16	2, 3 PCLK*3
0008 8042h	ADA	A/D data register B	ADDRB	16	16	2, 3 PCLK*3
0008 8044h	ADA	A/D data register C	ADDRC	16	16	2, 3 PCLK*3
0008 8046h	ADA	A/D data register D	ADDRD	16	16	2, 3 PCLK*3

Table 4.1 List of I/O Registers (Address Order) (12 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 90A4h	S12AD1	A/D data register 2	ADDR2	16	16	2, 3 PCLK*3
0008 90A6h	S12AD1	A/D data register 3	ADDR3	16	16	2, 3 PCLK*3
0008 90B0h	S12AD1	A/D data register 0B	ADDR0B	16	16	2, 3 PCLK*3
0008 90E0h	S12AD1	A/D sampling state register	ADSSTR	8	8	2, 3 PCLK*3
0008 C001h	PORT1	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C002h	PORT2	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C003h	PORT3	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C007h	PORT7	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C008h	PORT8	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C009h	PORT9	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C00Ah	PORTA	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C00Bh	PORTB	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C00Dh	PORTD	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C00Eh	PORTE	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C010h	PORTG	Data direction register	DDR*1	8	8	2, 3 PCLK*3
0008 C021h	PORT1	Data register	DR	8	8	2, 3 PCLK*3
0008 C022h	PORT2	Data register	DR	8	8	2, 3 PCLK*3
0008 C023h	PORT3	Data register	DR	8	8	2, 3 PCLK*3
0008 C027h	PORT7	Data register	DR	8	8	2, 3 PCLK*3
0008 C028h	PORT8	Data register	DR	8	8	2, 3 PCLK*3
0008 C029h	PORT9	Data register	DR	8	8	2, 3 PCLK*3
0008 C02Ah	PORTA	Data register	DR	8	8	2, 3 PCLK*3
0008 C02Bh	PORTB	Data register	DR	8	8	2, 3 PCLK*3
0008 C02Dh	PORTD	Data register	DR	8	8	2, 3 PCLK*3
0008 C02Eh	PORTE	Data register	DR	8	8	2, 3 PCLK*3
0008 C030h	PORTG	Data register	DR*1	8	8	2, 3 PCLK*3
0008 C041h	PORT1	Data register	PORT	8	8	2, 3 PCLK*3
0008 C042h	PORT2	Data register	PORT	8	8	2, 3 PCLK*3
0008 C043h	PORT3	Data register	PORT	8	8	2, 3 PCLK*3
0008 C044h	PORT4	Data register	PORT	8	8	2, 3 PCLK*3
0008 C045h	PORT5	Data register	PORT	8	8	2, 3 PCLK*3
0008 C046h	PORT6	Data register	PORT	8	8	2, 3 PCLK*3
0008 C047h	PORT7	Data register	PORT	8	8	2, 3 PCLK*3
0008 C048h	PORT8	Data register	PORT	8	8	2, 3 PCLK*3
0008 C049h	PORT9	Data register	PORT	8	8	2, 3 PCLK*3
0008 C04Ah	PORTA	Data register	PORT	8	8	2, 3 PCLK*3
0008 C04Bh	PORTB	Data register	PORT	8	8	2, 3 PCLK*3
0008 C04Dh	PORTD	Data register	PORT	8	8	2, 3 PCLK*3
0008 C04Eh	PORTE	Data register	PORT	8	8	2, 3 PCLK*3
0008 C050h	PORTG	Port register	PORT*1	8	8	2, 3 PCLK*3
0008 C061h	PORT1	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C062h	PORT2	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C063h	PORT3	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C064h	PORT4	Input buffer control register	ICR	8	8	2, 3 PCLK*3

Table 4.1 List of I/O Registers (Address Order) (25 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
007F FFBAh	FLASH	FCU command register	FCMDR	16	16	2, 3 PCLK*3
007F FFC8h	FLASH	FCU processing switching register	FCPSR	16	16	2, 3 PCLK*3
007F FFCAh	FLASH	Data flash blank check control register	DFLBCCNT	16	16	2, 3 PCLK*3
007F FFCCh	FLASH	Flash P/E status register	FPESTAT	16	16	2, 3 PCLK*3
007F FFCEh	FLASH	Data flash blank check status register	DFLBCSTAT	16	16	2, 3 PCLK*3
007F FFE8h	FLASH	Peripheral clock notification register	PCKAR	16	16	2, 3 PCLK*3

Note 1. This register is not supported by the 100-pin LQFP version.
Note 2. This register is not supported by the product without the CAN function.
Note 3. The number of access states depends on the number of divided cycles for clock synchronization (0 to 1 PCLK).
Note 4. Reading the registers takes 3 cycles of ICLK and writing to the registers takes 5 cycles of ICLK.

Table 4.2 List of I/O Registers (Bit Order) (2 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
MPU	REPAGE0				REPN[27:0]				
					REPN[27:0]				
					REPN[27:0]				
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE1				RSPN[27:0]				
					RSPN[27:0]				
					RSPN[27:0]				
			RSPN[27:0]			—	—	—	—
MPU	REPAGE1				REPN[27:0]				
					REPN[27:0]				
					REPN[27:0]				
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE2				RSPN[27:0]				
					RSPN[27:0]				
					RSPN[27:0]				
			RSPN[27:0]			—	—	—	—
MPU	REPAGE2				REPN[27:0]				
					REPN[27:0]				
					REPN[27:0]				
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE3				RSPN[27:0]				
					RSPN[27:0]				
					RSPN[27:0]				
			RSPN[27:0]			—	—	—	—
MPU	REPAGE3				REPN[27:0]				
					REPN[27:0]				
					REPN[27:0]				
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE4				RSPN[27:0]				
					RSPN[27:0]				
					RSPN[27:0]				
			RSPN[27:0]			—	—	—	—
MPU	REPAGE4				REPN[27:0]				
					REPN[27:0]				
					REPN[27:0]				
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE5				RSPN[27:0]				
					RSPN[27:0]				
					RSPN[27:0]				
			RSPN[27:0]			—	—	—	—
MPU	REPAGE5				REPN[27:0]				
					REPN[27:0]				
					REPN[27:0]				
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE6				RSPN[27:0]				
					RSPN[27:0]				
					RSPN[27:0]				
			RSPN[27:0]			—	—	—	—
MPU	REPAGE6				REPN[27:0]				
					REPN[27:0]				
					REPN[27:0]				
			REPN[27:0]				UAC[2:0]		V

Table 4.2 List of I/O Registers (Bit Order) (14 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
PORT8	DR	—	—	—	—	—	B2	B1	B0
PORT9	DR	—	B6	B5	B4	B3	B2	B1	B0
PORTA	DR	—	—	B5	B4	B3	B2	B1	B0
PORTB	DR	B7	B6	B5	B4	B3	B2	B1	B0
PORTD	DR	B7	B6	B5	B4	B3	B2	B1	B0
PORTE	DR	—	—	B5	B4	B3	—	B1	B0
PORTG	DR	—	—	B5	B4	B3	B2	B1	B0
PORT1	PORT	—	—	—	—	—	—	B1	B0
PORT2	PORT	—	—	—	B4	B3	B2	B1	B0
PORT3	PORT	—	—	—	—	B3	B2	B1	B0
PORT4	PORT	B7	B6	B5	B4	B3	B2	B1	B0
PORT5	PORT	—	—	B5	B4	B3	B2	B1	B0
PORT6	PORT	—	—	B5	B4	B3	B2	B1	B0
PORT7	PORT	—	B6	B5	B4	B3	B2	B1	B0
PORT8	PORT	—	—	—	—	—	B2	B1	B0
PORT9	PORT	—	B6	B5	B4	B3	B2	B1	B0
PORTA	PORT	—	—	B5	B4	B3	B2	B1	B0
PORTB	PORT	B7	B6	B5	B4	B3	B2	B1	B0
PORTD	PORT	B7	B6	B5	B4	B3	B2	B1	B0
PORTE	PORT	—	—	B5	B4	B3	B2	B1	B0
PORTG	PORT	—	—	B5	B4	B3	B2	B1	B0
PORT1	ICR	—	—	—	—	—	—	B1	B0
PORT2	ICR	—	—	—	B4	B3	B2	B1	B0
PORT3	ICR	—	—	—	—	B3	B2	B1	B0
PORT4	ICR	B7	B6	B5	B4	B3	B2	B1	B0
PORT5	ICR	—	—	B5	B4	B3	B2	B1	B0
PORT6	ICR	—	—	B5	B4	B3	B2	B1	B0
PORT7	ICR	—	B6	B5	B4	B3	B2	B1	B0
PORT8	ICR	—	—	—	—	—	B2	B1	B0
PORT9	ICR	—	B6	B5	B4	B3	B2	B1	B0
PORTA	ICR	—	—	B5	B4	B3	B2	B1	B0
PORTB	ICR	B7	B6	B5	B4	B3	B2	B1	B0
PORTD	ICR	B7	B6	B5	B4	B3	B2	B1	B0
PORTE	ICR	—	—	B5	B4	B3	—	B1	B0
PORTG	ICR	—	—	B5	B4	B3	B2	B1	B0
IOPORT	PF8IRQ	—	—	—	—	ITS1[1:0]		ITS0[1:0]	
IOPORT	PF9IRQ	—	—	—	—	—	ITS2	—	—
IOPORT	PFAADC	—	—	—	—	—	—	ADTRG1S	ADTRG0S
IOPORT	PFCMTU	TCLKS[1:0]		—	—	—	—	MTUS1	MTUS0
IOPORT	PFDGPT	—	—	—	—	—	—	—	GPTS
IOPORT	PFFSCI	—	—	—	—	—	SCI2S	—	—
IOPORT	PFGSPI	SSL3E	SSL2E	SSL1E	SSL0E	MISOE	MOSIE	RSPCKE	—
IOPORT	PFHSPI	—	—	—	—	—	—	RSPIS[1:0]	
IOPORT	PFJCAN	CANS[1:0]		—	—	—	—	—	CANE
IOPORT	PFKLIN	—	—	—	—	—	—	—	LINE
IOPORT	PFMPOE	—	—	—	POE11E	POE10E	POE8E	POE4E	POE0E
IOPORT	PFNPOE	POE10S	—	—	—	—	—	—	—
SYSTEM	DPSBYCR	DPSBY	IOKEEP	—	—	—	—	—	—
SYSTEM	DPSWCR	—	—	WTSTS[5:0]					
SYSTEM	DPSIER	DNMIE	—	—	DLVDE	—	—	DIRQ1E	DIRQ0E

Table 4.2 List of I/O Registers (Bit Order) (29 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
GPT2	GTDLYCR	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLYEN	DLYRST	DLLEN
GPT3	GTDLYCR	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLYEN	DLYRST	DLLEN
GPT0	GTDLYRA	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT0	GTDLYRB	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT1	GTDLYRA	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT1	GTDLYRB	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT2	GTDLYRA	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT2	GTDLYRB	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT3	GTDLYRA	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT3	GTDLYRB	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT0	GTDLYFA	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT0	GTDLYFB	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT1	GTDLYFA	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT1	GTDLYFB	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT2	GTDLYRA	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT2	GTDLYFB	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT3	GTDLYFA	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
GPT3	GTDLYFB	—	—	—	—	—	—	—	—
		—	—	—			DLY[4:0]		
FLASH	FMODR	—	—	—	FRDMD		—	—	—
FLASH	FASTAT	ROMAE	—	—	CMDLK	DFLAE	—	DFLRPE	DFLWPE
FLASH	FAEINT	ROMAEIE	—	—	CMDLKIE	DFLAEIE	—	DFLRPEIE	DFLWPEIE
FLASH	FRDYIE	—	—	—	—	—	—	—	FRDYIE
FLASH	DFLRE0				KEY[7:0]				
		DBRE07	DBRE06	DBRE05	DBRE04	DBRE03	DBRE02	DBRE01	DBRE00
FLASH	DFLRE1				KEY[7:0]				
		DBRE15	DBRE14	DBRE13	DBRE12	DBRE11	DBRE10	DBRE09	DBRE08
FLASH	DFLWE0				KEY[7:0]				
		DBWE07	DBWE06	DBWE05	DBWE04	DBWE03	DBWE02	DBWE01	DBWE00
FLASH	DFLWE1				KEY[7:0]				
		DBWE15	DBWE14	DBWE13	DBWE12	DBWE11	DBWE10	DBWE09	DBWE08
FLASH	FCURAME				KEY[7:0]				
		—	—	—	—	—	—	—	FCRME

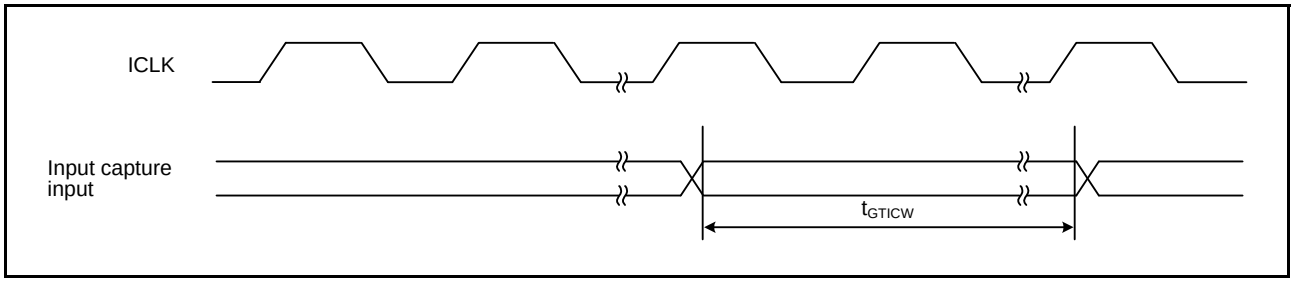


Figure 5.18 GPT Input/Output Timing

Table 5.13 Timing of On-Chip Peripheral Modules (5)

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Max.	Unit	Test Conditions
POE3	POE# input pulse width	t_{POEW}	1.5	-	t_{Pcyc}	Figure 5.19

Note: • t_{Pcyc}: PCLK cycle

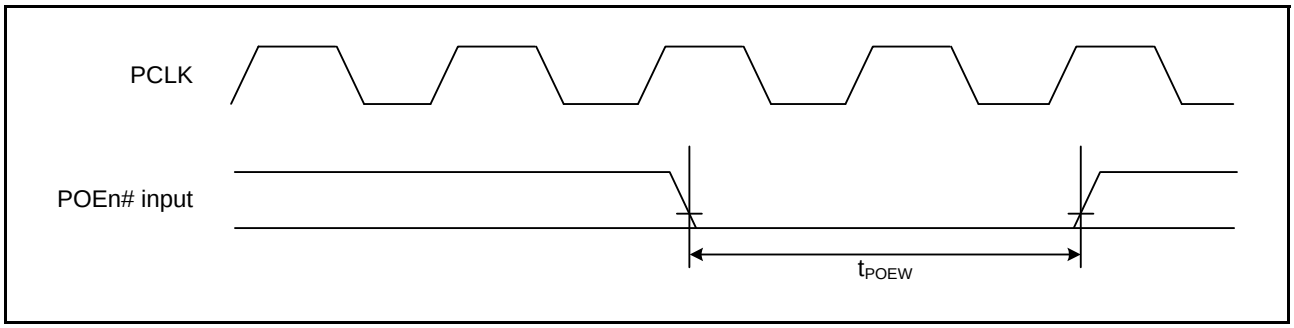


Figure 5.19 POE3# Clock Timing

5.3.4 Timing of PWM Delay Generation Circuit

Table 5.14 Timing of the PWM Delay Generation Circuit

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS = VREL0 = 0 V
AVCC = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr.

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Resolution	—	312.5	—	ps	ICLK = 100 MHz
DNL*1	—	±2.0	—	LSB	

Note 1. This value is correct when the difference between each code and the next is a resolution of one bit (1 LSB).

5.4 A/D Conversion Characteristics

Table 5.15 10-Bit A/D Conversion Characteristics

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC
Ta = Topr

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	10	10	10	Bit	
Conversion time*1 (AD clock = 25-MHz operation)	2.0	-	-	μs	Sampling 25 states
Analog input capacitance	-	-	4	pF	
Integral nonlinearity error	-	-	±3.0	LSB	
Offset error	-	-	±3.0	LSB	
Full-scale error	-	-	±3.0	LSB	
Quantization error	-	±0.5	-	LSB	
Absolute accuracy	-	-	±4.0	LSB	
Permissible signal source impedance	-	-	1.0	kΩ	

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 2 and 3.

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	10	10	10	Bit	
Conversion time*1 (AD clock = 50-MHz operation)	1.0	-	-	μs	Sampling 25 states
Analog input capacitance	-	-	4	pF	
Integral nonlinearity error	-	-	±3.0	LSB	
Offset error	-	-	±3.0	LSB	
Full-scale error	-	-	±3.0	LSB	
Quantization error	-	±0.5	-	LSB	
Absolute accuracy	-	-	±4.0	LSB	
Permissible signal source impedance	-	-	1.0	kΩ	

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 5.17 Characteristics of the Programmable Gain Amplifier

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog input capacitance		Cin	-	-	6	pF	
Input offset voltage		Voff	-	-	8	mV	
Input voltage range (Vin)	Gain × 2.000	Vin	0.050 x AVcc	-	0.450 x AVcc	V	
	Gain × 2.500		0.047 x AVcc	-	0.360 x AVcc		
	Gain × 3.077		0.045 x AVcc	-	0.292 x AVcc		
	Gain × 3.636		0.042 x AVcc	-	0.247 x AVcc		
	Gain × 4.000		0.040 x AVcc	-	0.212 x AVcc		
	Gain × 4.444		0.036 x AVcc	-	0.191 x AVcc		
	Gain × 5.000		0.033 x AVcc	-	0.170 x AVcc		
	Gain × 5.714		0.031 x AVcc	-	0.148 x AVcc		
	Gain × 6.667		0.029 x AVcc	-	0.127 x AVcc		
	Gain × 10.000		0.025 x AVcc	-	0.08 x AVcc		
	Gain × 13.333		0.023 x AVcc	-	0.06 x AVcc		
Slew rate		SR	10	-	-	V/µs	
Gain error	Gain × 2.000	-	-	-	1	%	
	Gain × 2.500		-	-	1		
	Gain × 3.077		-	-	1		
	Gain × 3.636		-	-	1.5		
	Gain × 4.000		-	-	1.5		
	Gain × 4.444		-	-	2		
	Gain × 5.000		-	-	2		
	Gain × 5.714		-	-	2		
	Gain × 6.667		-	-	3		
	Gain × 10.000		-	-	4		
	Gain × 13.333		-	-	4		

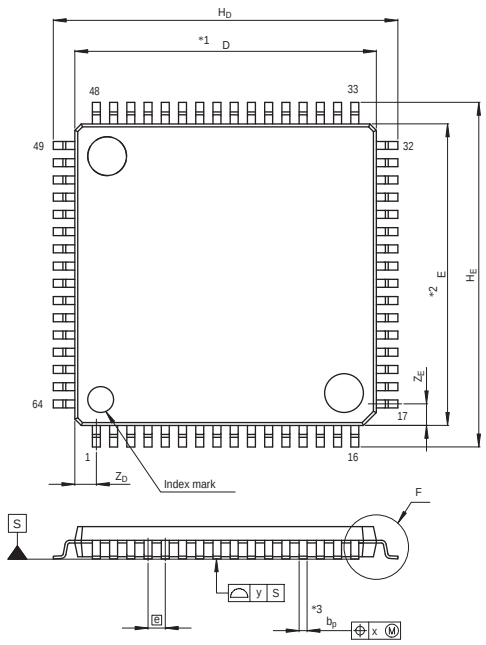
Table 5.18 Comparator Characteristics

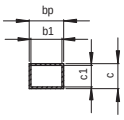
Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC
Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

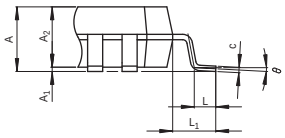
Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog input capacitance	Cin	-	-	6	pF	
REFH pin offset voltage	Voff	-	-	5	mV	
REFL pin offset voltage		-	-	5	mV	
REFH input voltage range	Vin	1.7	-	AVcc – 0.3	V	
REFL input voltage range		0.3	-	AVcc – 1.7	V	
REFH reply time	tCR	-	-	1	µs	
REFL reply time	tCF	-	-	1	µs	

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-14x14-0.80	PLQP0064GA-A	64P6U-A/ —	0.7g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.3	0.5	0.7
L_1	—	1.0	—

Figure E 64-Pin LQFP (PLQP0064GA-A) Package Dimensions