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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I ² C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	61
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 12x10b, 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562t7ddfh-v1

1.4 Pin Assignments

Figure 1.3 to Figure 1.7 show the pins assignments. Table 1.4 to Table 1.8 show the list of pins and pin functions.

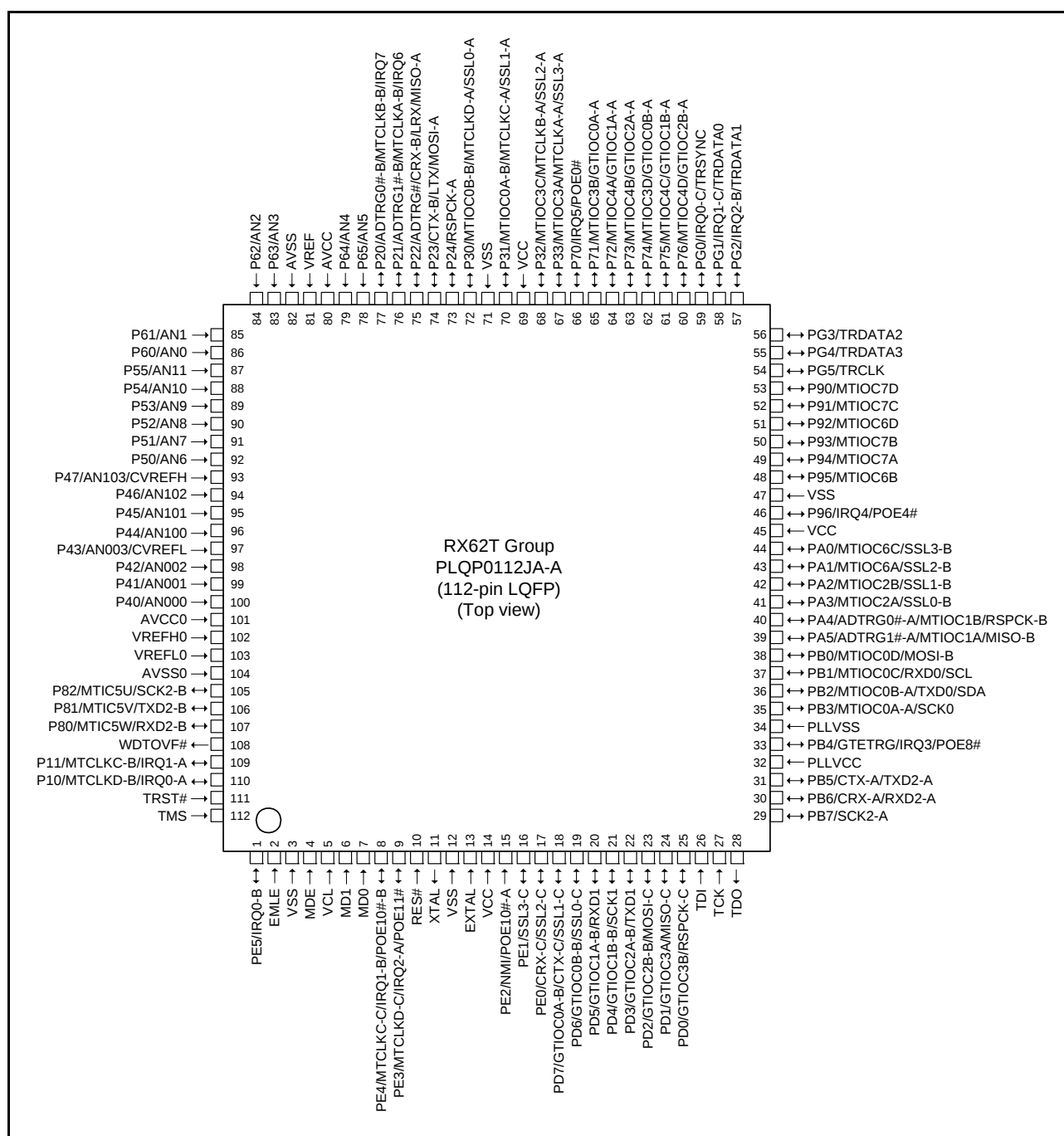


Figure 1.3 Pin Assignment of the 112-Pin LQFP

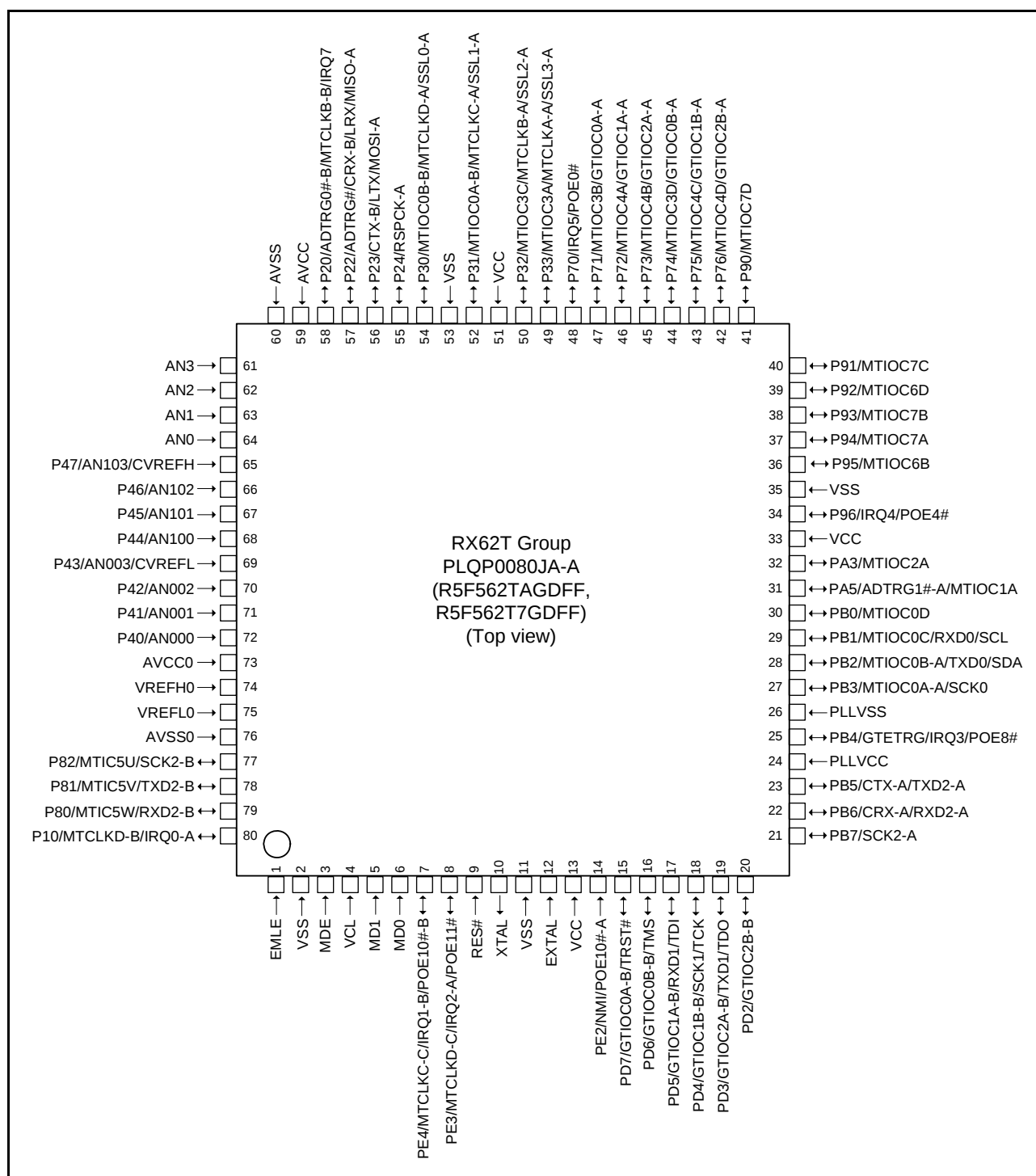


Figure 1.6 Pin Assignment of the 80-Pin LQFP (Two-Motor Control Supported Version)

Table 1.6 List of Pins and Pin Functions (80-Pin LQFP) (3 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi- cation	Interrupt	POE	Debugging
76	AVSS0							
77		P11		MTCLKC-B		IRQ1-A		
78		P10		MTCLKD-B		IRQ0-A		
79		PA5	ADTRG1#-A	MTIOC1A	MISO-B			
80		PA4	ADTRG0#-A	MTIOC1B	RSPCK-B			

Table 1.7 List of Pins and Pin Functions (80-Pin LQFP: R5F562TxGDFF) (3 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communication	Interrupt	POE	Debugging
76	AVSS0							
77		P82		MTIC5U	SCK2-B			
78		P81		MTIC5V	TXD2-B			
79		P80		MTIC5W	RXD2-B			
80		P10		MTCLKD-B		IRQ0-A		

Table 4.1 List of I/O Registers (Address Order) (6 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 71BEh	ICU	DTC activation enable register 190	DTCER190	8	8	2 ICLK
0008 71C0h	ICU	DTC activation enable register 192	DTCER192	8	8	2 ICLK
0008 71C1h	ICU	DTC activation enable register 193	DTCER193	8	8	2 ICLK
0008 71C2h	ICU	DTC activation enable register 194	DTCER194	8	8	2 ICLK
0008 71C3h	ICU	DTC activation enable register 195	DTCER195	8	8	2 ICLK
0008 71C4h	ICU	DTC activation enable register 196	DTCER196	8	8	2 ICLK
0008 71D7h	ICU	DTC activation enable register 215	DTCER215	8	8	2 ICLK
0008 71D8h	ICU	DTC activation enable register 216	DTCER216	8	8	2 ICLK
0008 71DBh	ICU	DTC activation enable register 219	DTCER219	8	8	2 ICLK
0008 71DCh	ICU	DTC activation enable register 220	DTCER220	8	8	2 ICLK
0008 71DFh	ICU	DTC activation enable register 223	DTCER223	8	8	2 ICLK
0008 71E0h	ICU	DTC activation enable register 224	DTCER224	8	8	2 ICLK
0008 71F7h	ICU	DTC activation enable register 247	DTCER247	8	8	2 ICLK
0008 71F8h	ICU	DTC activation enable register 248	DTCER248	8	8	2 ICLK
0008 71FEh	ICU	DTC activation enable register 254	DTCER254	8	8	2 ICLK
0008 7202h	ICU	Interrupt request enable register 02	IER02	8	8	2 ICLK
0008 7203h	ICU	Interrupt request enable register 03	IER03	8	8	2 ICLK
0008 7205h	ICU	Interrupt request enable register 05	IER05	8	8	2 ICLK
0008 7207h	ICU	Interrupt request enable register 07	IER07	8	8	2 ICLK
0008 7208h	ICU	Interrupt request enable register 08	IER08	8	8	2 ICLK
0008 720Ch	ICU	Interrupt request enable register 0C	IER0C	8	8	2 ICLK
0008 720Dh	ICU	Interrupt request enable register 0D	IER0D	8	8	2 ICLK
0008 720Eh	ICU	Interrupt request enable register 0E	IER0E	8	8	2 ICLK
0008 720Fh	ICU	Interrupt request enable register 0F	IER0F	8	8	2 ICLK
0008 7210h	ICU	Interrupt request enable register 10	IER10	8	8	2 ICLK
0008 7211h	ICU	Interrupt request enable register 11	IER11	8	8	2 ICLK
0008 7212h	ICU	Interrupt request enable register 12	IER12	8	8	2 ICLK
0008 7213h	ICU	Interrupt request enable register 13	IER13	8	8	2 ICLK
0008 7215h	ICU	Interrupt request enable register 15	IER15	8	8	2 ICLK
0008 7216h	ICU	Interrupt request enable register 16	IER16	8	8	2 ICLK
0008 7217h	ICU	Interrupt request enable register 17	IER17	8	8	2 ICLK
0008 7218h	ICU	Interrupt request enable register 18	IER18	8	8	2 ICLK
0008 721Ah	ICU	Interrupt request enable register 1A	IER1A	8	8	2 ICLK
0008 721Bh	ICU	Interrupt request enable register 1B	IER1B	8	8	2 ICLK
0008 721Ch	ICU	Interrupt request enable register 1C	IER1C	8	8	2 ICLK
0008 721Eh	ICU	Interrupt request enable register 1E	IER1E	8	8	2 ICLK
0008 721Fh	ICU	Interrupt request enable register 1F	IER1F	8	8	2 ICLK
0008 72E0h	ICU	Software interrupt activation register	SWINTR	8	8	2 ICLK
0008 72F0h	ICU	Fast interrupt set register	FIR	16	16	2 ICLK
0008 7300h	ICU	Interrupt source priority register 00	IPR00	8	8	2 ICLK
0008 7301h	ICU	Interrupt source priority register 01	IPR01	8	8	2 ICLK
0008 7302h	ICU	Interrupt source priority register 02	IPR02	8	8	2 ICLK
0008 7303h	ICU	Interrupt source priority register 03	IPR03	8	8	2 ICLK
0008 7304h	ICU	Interrupt source priority register 04	IPR04	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (25 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
007F FFBAh	FLASH	FCU command register	FCMDR	16	16	2, 3 PCLK ^{*3}
007F FFC8h	FLASH	FCU processing switching register	FCPSR	16	16	2, 3 PCLK ^{*3}
007F FFCAh	FLASH	Data flash blank check control register	DFLBCCNT	16	16	2, 3 PCLK ^{*3}
007F FFCCh	FLASH	Flash P/E status register	FPESTAT	16	16	2, 3 PCLK ^{*3}
007F FFCEh	FLASH	Data flash blank check status register	DFLBCSTAT	16	16	2, 3 PCLK ^{*3}
007F FFE8h	FLASH	Peripheral clock notification register	PCKAR	16	16	2, 3 PCLK ^{*3}

Note 1. This register is not supported by the 100-pin LQFP version.

Note 2. This register is not supported by the product without the CAN function.

Note 3. The number of access states depends on the number of divided cycles for clock synchronization (0 to 1 PCLK).

Note 4. Reading the registers takes 3 cycles of ICLK and writing to the registers takes 5 cycles of ICLK.

Table 4.2 List of I/O Registers (Bit Order) (2 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
MPU	REPAGE0					REPN[27:0]			
						REPN[27:0]			
						REPN[27:0]			
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE1					RSPN[27:0]			
						RSPN[27:0]			
						RSPN[27:0]			
			RSPN[27:0]			—	—	—	—
MPU	REPAGE1					REPN[27:0]			
						REPN[27:0]			
						REPN[27:0]			
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE2					RSPN[27:0]			
						RSPN[27:0]			
						RSPN[27:0]			
			RSPN[27:0]			—	—	—	—
MPU	REPAGE2					REPN[27:0]			
						REPN[27:0]			
						REPN[27:0]			
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE3					RSPN[27:0]			
						RSPN[27:0]			
						RSPN[27:0]			
			RSPN[27:0]			—	—	—	—
MPU	REPAGE3					REPN[27:0]			
						REPN[27:0]			
						REPN[27:0]			
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE4					RSPN[27:0]			
						RSPN[27:0]			
						RSPN[27:0]			
			RSPN[27:0]			—	—	—	—
MPU	REPAGE4					REPN[27:0]			
						REPN[27:0]			
						REPN[27:0]			
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE5					RSPN[27:0]			
						RSPN[27:0]			
						RSPN[27:0]			
			RSPN[27:0]			—	—	—	—
MPU	REPAGE5					REPN[27:0]			
						REPN[27:0]			
						REPN[27:0]			
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE6					RSPN[27:0]			
						RSPN[27:0]			
						RSPN[27:0]			
			RSPN[27:0]			—	—	—	—
MPU	REPAGE6					REPN[27:0]			
						REPN[27:0]			
						REPN[27:0]			
			REPN[27:0]				UAC[2:0]		V

Table 4.2 List of I/O Registers (Bit Order) (6 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
ICU	DTCER029	—	—	—	—	—	—	—	DTCE
ICU	DTCER030	—	—	—	—	—	—	—	DTCE
ICU	DTCER031	—	—	—	—	—	—	—	DTCE
ICU	DTCER045	—	—	—	—	—	—	—	DTCE
ICU	DTCER046	—	—	—	—	—	—	—	DTCE
ICU	DTCER064	—	—	—	—	—	—	—	DTCE
ICU	DTCER065	—	—	—	—	—	—	—	DTCE
ICU	DTCER066	—	—	—	—	—	—	—	DTCE
ICU	DTCER067	—	—	—	—	—	—	—	DTCE
ICU	DTCER068	—	—	—	—	—	—	—	DTCE
ICU	DTCER069	—	—	—	—	—	—	—	DTCE
ICU	DTCER070	—	—	—	—	—	—	—	DTCE
ICU	DTCER071	—	—	—	—	—	—	—	DTCE
ICU	DTCER098	—	—	—	—	—	—	—	DTCE
ICU	DTCER102	—	—	—	—	—	—	—	DTCE
ICU	DTCER103	—	—	—	—	—	—	—	DTCE
ICU	DTCER106	—	—	—	—	—	—	—	DTCE
ICU	DTCER114	—	—	—	—	—	—	—	DTCE
ICU	DTCER115	—	—	—	—	—	—	—	DTCE
ICU	DTCER116	—	—	—	—	—	—	—	DTCE
ICU	DTCER117	—	—	—	—	—	—	—	DTCE
ICU	DTCER121	—	—	—	—	—	—	—	DTCE
ICU	DTCER122	—	—	—	—	—	—	—	DTCE
ICU	DTCER125	—	—	—	—	—	—	—	DTCE
ICU	DTCER126	—	—	—	—	—	—	—	DTCE
ICU	DTCER129	—	—	—	—	—	—	—	DTCE
ICU	DTCER130	—	—	—	—	—	—	—	DTCE
ICU	DTCER131	—	—	—	—	—	—	—	DTCE
ICU	DTCER132	—	—	—	—	—	—	—	DTCE
ICU	DTCER134	—	—	—	—	—	—	—	DTCE
ICU	DTCER135	—	—	—	—	—	—	—	DTCE
ICU	DTCER136	—	—	—	—	—	—	—	DTCE
ICU	DTCER137	—	—	—	—	—	—	—	DTCE
ICU	DTCER138	—	—	—	—	—	—	—	DTCE
ICU	DTCER139	—	—	—	—	—	—	—	DTCE
ICU	DTCER140	—	—	—	—	—	—	—	DTCE
ICU	DTCER141	—	—	—	—	—	—	—	DTCE
ICU	DTCER142	—	—	—	—	—	—	—	DTCE
ICU	DTCER143	—	—	—	—	—	—	—	DTCE
ICU	DTCER144	—	—	—	—	—	—	—	DTCE
ICU	DTCER145	—	—	—	—	—	—	—	DTCE
ICU	DTCER149	—	—	—	—	—	—	—	DTCE
ICU	DTCER150	—	—	—	—	—	—	—	DTCE
ICU	DTCER151	—	—	—	—	—	—	—	DTCE
ICU	DTCER152	—	—	—	—	—	—	—	DTCE
ICU	DTCER153	—	—	—	—	—	—	—	DTCE
ICU	DTCER174	—	—	—	—	—	—	—	DTCE
ICU	DTCER175	—	—	—	—	—	—	—	DTCE
ICU	DTCER176	—	—	—	—	—	—	—	DTCE
ICU	DTCER177	—	—	—	—	—	—	—	DTCE
ICU	DTCER178	—	—	—	—	—	—	—	DTCE
ICU	DTCER179	—	—	—	—	—	—	—	DTCE

Table 4.2 List of I/O Registers (Bit Order) (8 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
ICU	IPR03	—	—	—	—			IPR[3:0]	
ICU	IPR04	—	—	—	—			IPR[3:0]	
ICU	IPR05	—	—	—	—			IPR[3:0]	
ICU	IPR06	—	—	—	—			IPR[3:0]	
ICU	IPR07	—	—	—	—			IPR[3:0]	
ICU	IPR14	—	—	—	—			IPR[3:0]	
ICU	IPR18	—	—	—	—			IPR[3:0]	
ICU	IPR20	—	—	—	—			IPR[3:0]	
ICU	IPR21	—	—	—	—			IPR[3:0]	
ICU	IPR22	—	—	—	—			IPR[3:0]	
ICU	IPR23	—	—	—	—			IPR[3:0]	
ICU	IPR24	—	—	—	—			IPR[3:0]	
ICU	IPR25	—	—	—	—			IPR[3:0]	
ICU	IPR26	—	—	—	—			IPR[3:0]	
ICU	IPR27	—	—	—	—			IPR[3:0]	
ICU	IPR40	—	—	—	—			IPR[3:0]	
ICU	IPR44	—	—	—	—			IPR[3:0]	
ICU	IPR48	—	—	—	—			IPR[3:0]	
ICU	IPR49	—	—	—	—			IPR[3:0]	
ICU	IPR51	—	—	—	—			IPR[3:0]	
ICU	IPR52	—	—	—	—			IPR[3:0]	
ICU	IPR53	—	—	—	—			IPR[3:0]	
ICU	IPR54	—	—	—	—			IPR[3:0]	
ICU	IPR55	—	—	—	—			IPR[3:0]	
ICU	IPR56	—	—	—	—			IPR[3:0]	
ICU	IPR57	—	—	—	—			IPR[3:0]	
ICU	IPR58	—	—	—	—			IPR[3:0]	
ICU	IPR59	—	—	—	—			IPR[3:0]	
ICU	IPR5A	—	—	—	—			IPR[3:0]	
ICU	IPR5B	—	—	—	—			IPR[3:0]	
ICU	IPR5C	—	—	—	—			IPR[3:0]	
ICU	IPR5D	—	—	—	—			IPR[3:0]	
ICU	IPR5E	—	—	—	—			IPR[3:0]	
ICU	IPR5F	—	—	—	—			IPR[3:0]	
ICU	IPR60	—	—	—	—			IPR[3:0]	
ICU	IPR67	—	—	—	—			IPR[3:0]	
ICU	IPR68	—	—	—	—			IPR[3:0]	
ICU	IPR69	—	—	—	—			IPR[3:0]	
ICU	IPR6A	—	—	—	—			IPR[3:0]	
ICU	IPR6B	—	—	—	—			IPR[3:0]	
ICU	IPR6C	—	—	—	—			IPR[3:0]	
ICU	IPR6D	—	—	—	—			IPR[3:0]	
ICU	IPR6E	—	—	—	—			IPR[3:0]	
ICU	IPR6F	—	—	—	—			IPR[3:0]	
ICU	IPR80	—	—	—	—			IPR[3:0]	
ICU	IPR81	—	—	—	—			IPR[3:0]	
ICU	IPR82	—	—	—	—			IPR[3:0]	
ICU	IPR88	—	—	—	—			IPR[3:0]	
ICU	IPR89	—	—	—	—			IPR[3:0]	
ICU	IPR8A	—	—	—	—			IPR[3:0]	
ICU	IPR8B	—	—	—	—			IPR[3:0]	
ICU	IPR90	—	—	—	—			IPR[3:0]	

Table 4.2 **List of I/O Registers (Bit Order) (9 / 30)**

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
ICU	IRQCR0	—	—	—	—		IRQMD[1:0]	—	—
ICU	IRQCR1	—	—	—	—		IRQMD[1:0]	—	—
ICU	IRQCR2	—	—	—	—		IRQMD[1:0]	—	—
ICU	IRQCR3	—	—	—	—		IRQMD[1:0]	—	—
ICU	IRQCR4	—	—	—	—		IRQMD[1:0]	—	—
ICU	IRQCR5	—	—	—	—		IRQMD[1:0]	—	—
ICU	IRQCR6	—	—	—	—		IRQMD[1:0]	—	—
ICU	IRQCR7	—	—	—	—		IRQMD[1:0]	—	—
ICU	NMISR	—	—	—	—	—	OSTST	LVDST	NMIST
ICU	NMIER	—	—	—	—	—	OSTEN	LVDEN	NMIEN
ICU	NMICLR	—	—	—	—	—	OSTCLR	—	NMICLR
ICU	NMICR	—	—	—	—	NMIMD	—	—	—
CMT	CMSTR0	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	STR1	STR0
CMT0	CMCR	—	—	—	—	—	—	—	—
		—	CMIE	—	—	—	—	CKS[1:0]	
CMT0	CMCNT								
CMT0	CMCOR								
CMT1	CMCR	—	—	—	—	—	—	—	—
		—	CMIE	—	—	—	—	CKS[1:0]	
CMT1	CMCNT								
CMT1	CMCOR								
CMT	CMSTR1	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	STR3	STR2
CMT2	CMCR	—	—	—	—	—	—	—	—
		—	CMIE	—	—	—	—	CKS[1:0]	
CMT2	CMCNT								
CMT2	CMCOR								
CMT3	CMCR	—	—	—	—	—	—	—	—
		—	CMIE	—	—	—	—	CKS[1:0]	
CMT3	CMCNT								
CMT3	CMCOR								
WDT	TCSR	—	TMS	TME	—	—		CKS[2:0]	
WDT	WINA								
WDT	TCNT								
WDT	WINB								
WDT	RSTCSR	WOVF	RSTE	—	—	—	—	—	—
IWDT	IWDTCR	—	—	—	—	—	—	—	—
			CKS[3:0]			—	—	TOPS[1:0]	
IWDT	IWDTSR	—	UNDF			CNTVAL[13:0]			
						CNTVAL[13:0]			
AD0	ADDRA ^{*1}	—	—	—	—	—	—		

Table 4.2 List of I/O Registers (Bit Order) (10 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
AD0	ADDRB ^{*1}	—	—	—	—	—	—		
AD0	ADDRC ^{*1}	—	—	—	—	—	—		
AD0	ADDRD ^{*1}	—	—	—	—	—	—		
AD0	ADDRE ^{*1}	—	—	—	—	—	—		
AD0	ADDRF ^{*1}	—	—	—	—	—	—		
AD0	ADDRG ^{*1}	—	—	—	—	—	—		
AD0	ADDRH ^{*1}	—	—	—	—	—	—		
AD0	ADCSR	—	ADIE	ADST	—		CH[3:0]		
AD0	ADCR	—	—	—	—	CKS[1:0]		MODE[1:0]	
AD0	ADSSSTR								
AD0	ADDIAGR	—	—	—	—	—	—	DIAG[1:0]	
AD0	ADDRI ^{*1}	—	—	—	—	—	—		
AD0	ADDRJ ^{*1}	—	—	—	—	—	—		
AD0	ADDRK ^{*1}	—	—	—	—	—	—		
AD0	ADDRL ^{*1}	—	—	—	—	—	—		
AD0	ADSTRGR	—	—	—		ADSTRS[4:0]			
AD0	ADDP	DPSEL	—	—	—	—	—	—	DPPRC
SCI0	SMR	CM	CHR	PE	PM	STOP	MP	CKS[1:0]	
SCI0	BRR								
SCI0	SCR	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
SCI0	TDR								
SCI0	SSR	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
SCI0	RDR								
SCI0	SCMR	BCP2	—	—	—	SDIR	SINV	—	SMIF
SCI0	SEMR	—	—	NFEN	ABCS	—	—	—	—
SMCI0	SMR	GM	BLK	PE	PM	(BCP[1:0])		CKS[1:0]	
SMCI0	BRR								
SMCI0	SCR	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
SMCI0	TDR								
SMCI0	SSR	TDRE	RDRF	ORER	ERS	PER	TEND	MPB	MPBT
SMCI0	RDR								
SMCI0	SCMR	BCP2	—	—	—	SDIR	SINV	—	SMIF
SCI1	SMR	CM	CHR	PE	PM	STOP	MP	CKS[1:0]	
SCI1	BRR								
SCI1	SCR	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
SCI1	TDR								
SCI1	SSR	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
SCI1	RDR								
SCI1	SCMR	BCP2	—	—	—	SDIR	SINV	—	SMIF

Table 4.2 List of I/O Registers (Bit Order) (14 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
PORT8	DR	—	—	—	—	—	B2	B1	B0
PORT9	DR	—	B6	B5	B4	B3	B2	B1	B0
PORTA	DR	—	—	B5	B4	B3	B2	B1	B0
PORTB	DR	B7	B6	B5	B4	B3	B2	B1	B0
PORTD	DR	B7	B6	B5	B4	B3	B2	B1	B0
PORTE	DR	—	—	B5	B4	B3	—	B1	B0
PORTG	DR	—	—	B5	B4	B3	B2	B1	B0
PORT1	PORT	—	—	—	—	—	—	B1	B0
PORT2	PORT	—	—	—	B4	B3	B2	B1	B0
PORT3	PORT	—	—	—	—	B3	B2	B1	B0
PORT4	PORT	B7	B6	B5	B4	B3	B2	B1	B0
PORT5	PORT	—	—	B5	B4	B3	B2	B1	B0
PORT6	PORT	—	—	B5	B4	B3	B2	B1	B0
PORT7	PORT	—	B6	B5	B4	B3	B2	B1	B0
PORT8	PORT	—	—	—	—	—	B2	B1	B0
PORT9	PORT	—	B6	B5	B4	B3	B2	B1	B0
PORTA	PORT	—	—	B5	B4	B3	B2	B1	B0
PORTB	PORT	B7	B6	B5	B4	B3	B2	B1	B0
PORTD	PORT	B7	B6	B5	B4	B3	B2	B1	B0
PORTE	PORT	—	—	B5	B4	B3	B2	B1	B0
PORTG	PORT	—	—	B5	B4	B3	B2	B1	B0
PORT1	ICR	—	—	—	—	—	—	B1	B0
PORT2	ICR	—	—	—	B4	B3	B2	B1	B0
PORT3	ICR	—	—	—	—	B3	B2	B1	B0
PORT4	ICR	B7	B6	B5	B4	B3	B2	B1	B0
PORT5	ICR	—	—	B5	B4	B3	B2	B1	B0
PORT6	ICR	—	—	B5	B4	B3	B2	B1	B0
PORT7	ICR	—	B6	B5	B4	B3	B2	B1	B0
PORT8	ICR	—	—	—	—	—	B2	B1	B0
PORT9	ICR	—	B6	B5	B4	B3	B2	B1	B0
PORTA	ICR	—	—	B5	B4	B3	B2	B1	B0
PORTB	ICR	B7	B6	B5	B4	B3	B2	B1	B0
PORTD	ICR	B7	B6	B5	B4	B3	B2	B1	B0
PORTE	ICR	—	—	B5	B4	B3	—	B1	B0
PORTG	ICR	—	—	B5	B4	B3	B2	B1	B0
IOPORT	PF8IRQ	—	—	—	—	ITS1[1:0]		ITS0[1:0]	
IOPORT	PF9IRQ	—	—	—	—	—	ITS2	—	—
IOPORT	PFAADC	—	—	—	—	—	—	ADTRG1S	ADTRG0S
IOPORT	PFCMTU	TCLKS[1:0]		—	—	—	—	MTUS1	MTUS0
IOPORT	PFDGPT	—	—	—	—	—	—	—	GPTS
IOPORT	PPFSCI	—	—	—	—	—	SCI2S	—	—
IOPORT	PFGSPI	SSL3E	SSL2E	SSL1E	SSL0E	MISOE	MOSIE	RSPCKE	—
IOPORT	PFHSPI	—	—	—	—	—	—	RSPIS[1:0]	
IOPORT	PFJCAN	CANS[1:0]		—	—	—	—	—	CANE
IOPORT	PFKLIN	—	—	—	—	—	—	—	LINE
IOPORT	PFMPOE	—	—	—	POE11E	POE10E	POE8E	POE4E	POE0E
IOPORT	PFNPOE	POE10S	—	—	—	—	—	—	—
SYSTEM	DPSBYCR	DPSBY	IOKEEP	—	—	—	—	—	—
SYSTEM	DPSWCR	—	—	—	—	WTSTS[5:0]			
SYSTEM	DPSIER	DNMIE	—	—	DLVDE	—	—	DIRQ1E	DIRQ0E

Table 4.2 List of I/O Registers (Bit Order) (27 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
GPT2	GTPBR								
GPT2	GTPDBR								
GPT2	GTADTRA								
GPT2	GTADTBRA								
GPT2	GTADTDBRA								
GPT2	GTADTRB								
GPT2	GTADTBRB								
GPT2	GTADTDBRB								
GPT2	GTONCR	OBE	OAE	—	SWN	—	—	—	NFV
					NFS[3:0]	NVB	NVA	NEB	NEA
GPT2	GTDTCR	—	—	—	—	—	—	—	TDFER
		—	—	TDBDE	TDBUE	—	—	—	TDE
GPT2	GTDVU								
GPT2	GTDVD								
GPT2	GTDBU								
GPT2	GTDBD								
GPT2	GTSOS	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	SOS[1:0]	—
GPT2	GTSOTR	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	SOTR
GPT3	GTIOR	OBHLD	OBDFLT				GTIOB[5:0]		
		OAHL	OADFLT				GTIOA[5:0]		
GPT3	GTINTAD	ADTRBDEN	ADTRBUEN	ADTRADEN	ADTRAUEN	EINT	—	—	—
			GTINTPR[1:0]	GTINTF	GTINTE	GTINTD	GTINTC	GTINTB	GTINTA
GPT3	GTCR	—	—		CCLR[1:0]	—	—	—	—
		—	—	—	—	—	—	—	—
GPT3	GTBER	—	ADTDB	ADTTB[1:0]	—	ADTDA	ADTTA[1:0]		
		—	CCRSWT	PR[1:0]		CCRB[1:0]	CCRA[1:0]		
GPT3	GTUDC	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	UDF	UD
GPT3	GTITC	—	ADTBL	—	ADTAL	—		IVTT[2:0]	
			IVTC[1:0]	ITLF	ITLE	ITLD	ITLC	ITLB	ITLA
GPT3	GTST	TUCF	—	—	—	DTEF		ITCNT[2:0]	
		TCFPU	TCFPO	TCFF	TCFE	TCFD	TCFC	TCFB	TCFA
GPT3	GCNT								
GPT3	GTCCRA								

Table 4.2 List of I/O Registers (Bit Order) (28 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
GPT3	GTCCRB								
GPT3	GTCCRC								
GPT3	GTCCRD								
GPT3	GTCCRE								
GPT3	GTCCRF								
GPT3	GTPR								
GPT3	GTPBR								
GPT3	GTPDBR								
GPT3	GTADTRA								
GPT3	GTADTBRA								
GPT3	GTADTDBRA								
GPT3	GTADTRB								
GPT3	GTADTBRB								
GPT3	GTADTDBRB								
GPT3	GTONCR	OBE	OAE	—	SWN	—	—	—	NFV
			NFS[3:0]			NVB	NVA	NEB	NEA
GPT3	GTDTCR	—	—	—	—	—	—	—	TDFER
		—	—	TDBDE	TDBUE	—	—	—	TDE
GPT3	GTDVU								
GPT3	GTDVD								
GPT3	GTDBU								
GPT3	GTDBD	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	SOS[1:0]	—
GPT3	GTSOS	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	SOS[1:0]	—
GPT3	GTSOTR	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	SOTR
GPT0	GTDLYCR	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLYEN	DLYRST	DLLEN
GPT1	GTDLYCR	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLYEN	DLYRST	DLLEN

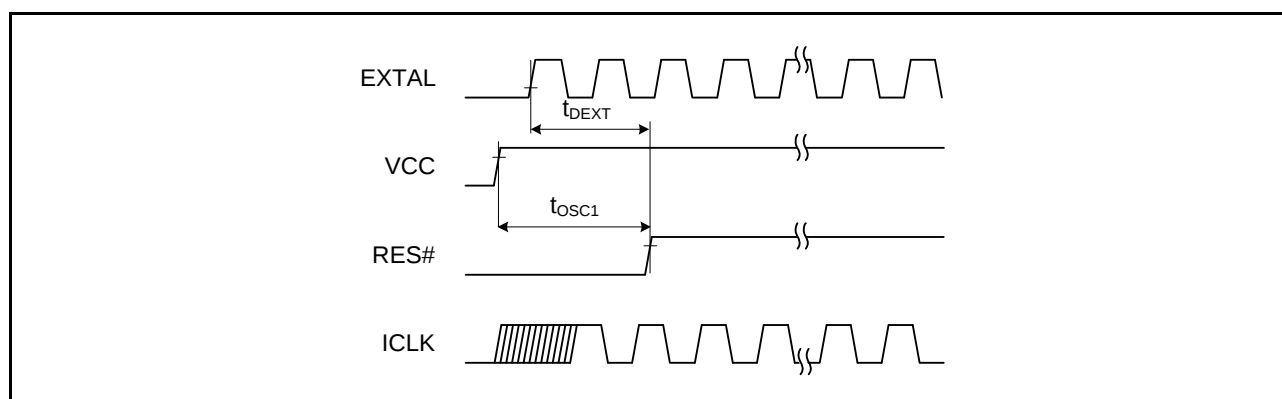


Figure 5.1 Oscillation Settling Timing

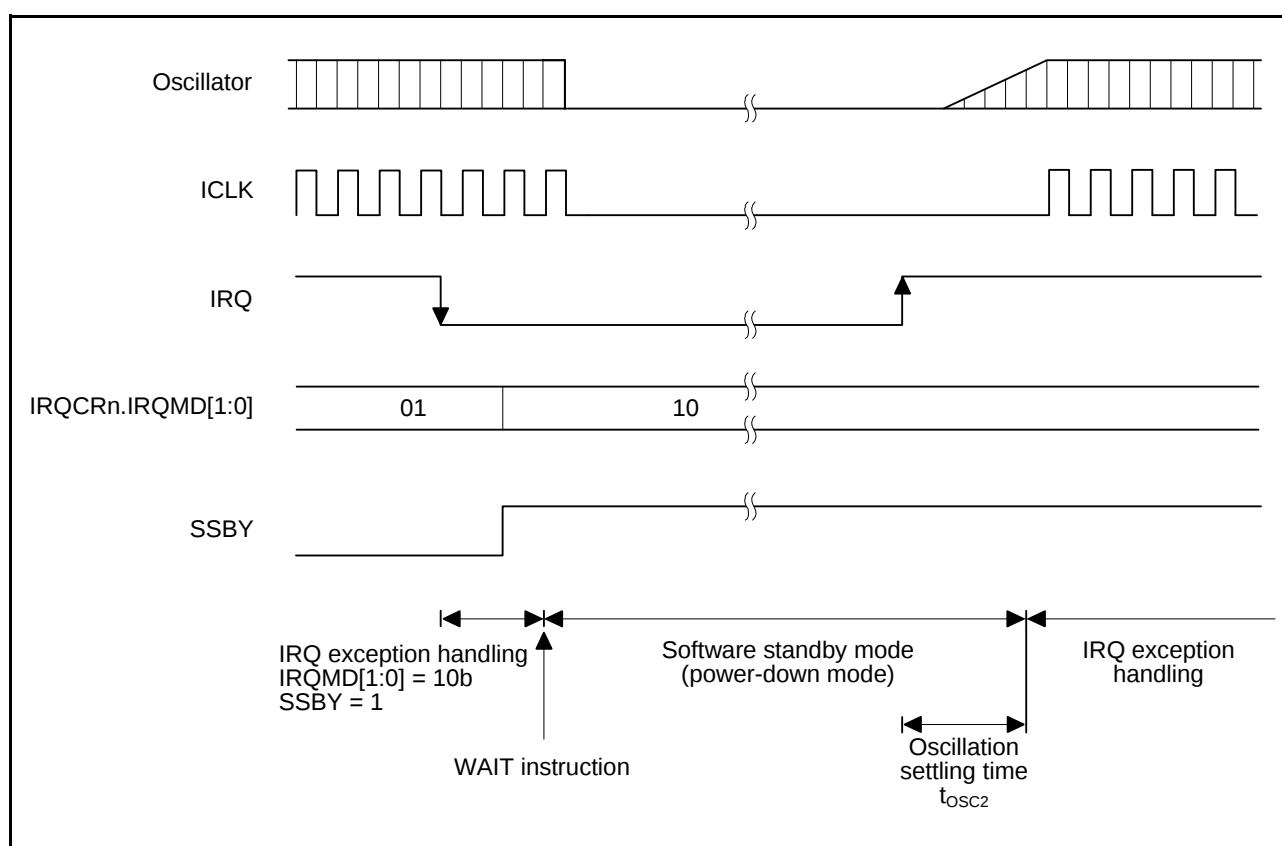


Figure 5.2 Oscillation Settling Timing after Software Standby Mode

5.3.2 Control Signal Timing

Table 5.8 Control Signal Timing

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item	Symbol	Min.	Max.	Unit	Test Conditions
RES# pulse width (except for programming or erasure of the ROM or data-flash memory or blank checking of the data-flash memory*1)	t_{RESW}^{*2}	20	-	t_{cyc}^{*4}	Figure 5.5
		1.5	-	μs	
Internal reset time*3	t_{RESW2}	35	-	μs	
NMI pulse width	t_{NMIW}	200	-	ns	Figure 5.6
IRQ pulse width	t_{IRQW}	200	-	ns	Figure 5.7

Note 1. For a reset by the signal on the RES# pin during programming or erasure of the ROM or data-flash memory or during blank checking of the data-flash memory, see section 31.12, Usage Notes in section 31, ROM (Flash Memory for Code Storage) in the User's manual: Hardware.

Note 2. Both the time and the number of cycles should satisfy the specifications.

Note 3. This is to specify the FCU reset.

Note 4. ICLK cycles.

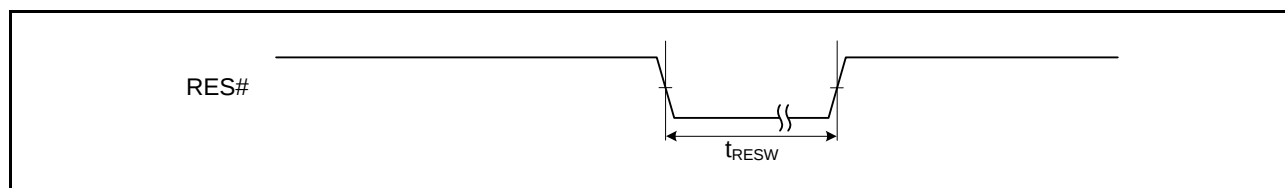


Figure 5.5 Reset Input Timing

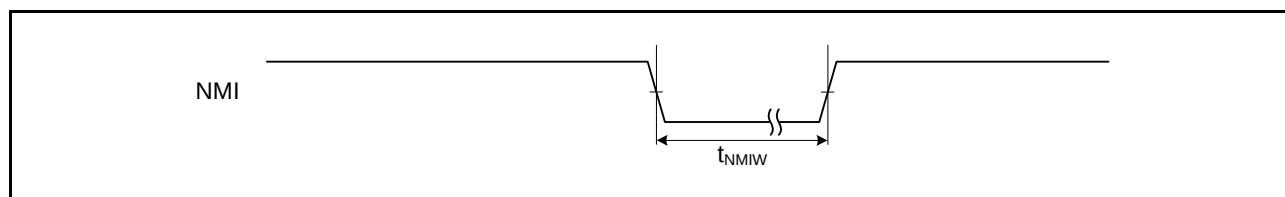


Figure 5.6 NMI Interrupt Input Timing

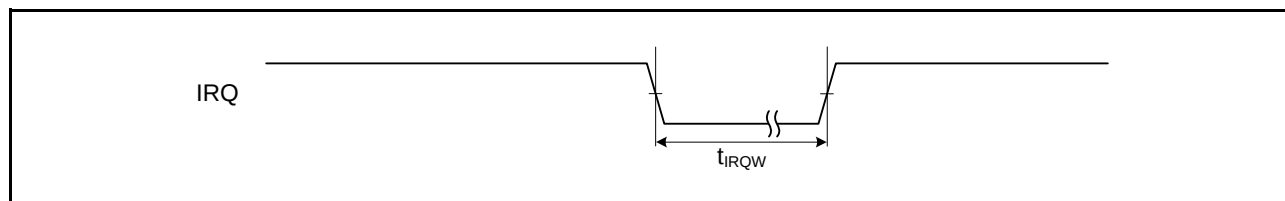


Figure 5.7 IRQ Interrupt Input Timing

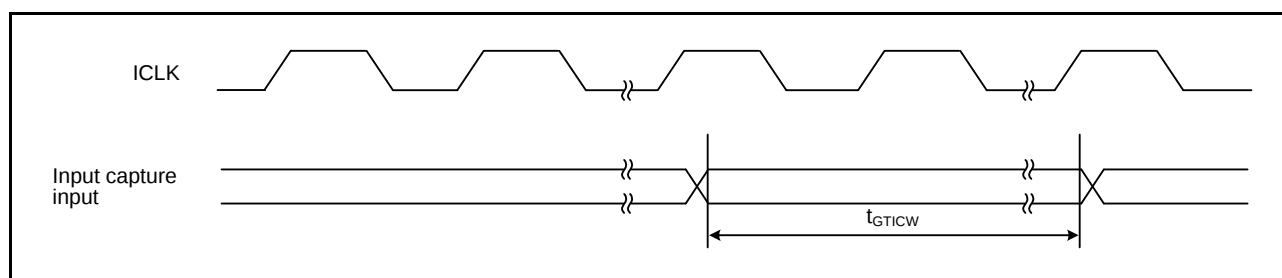


Figure 5.18 GPT Input/Output Timing

Table 5.13 Timing of On-Chip Peripheral Modules (5)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Max.	Unit	Test Conditions
POE3	POE# input pulse width	t _{POEW}	1.5	-	t _{Pcyc}	Figure 5.19

Note: • t_{Pcyc}: PCLK cycle

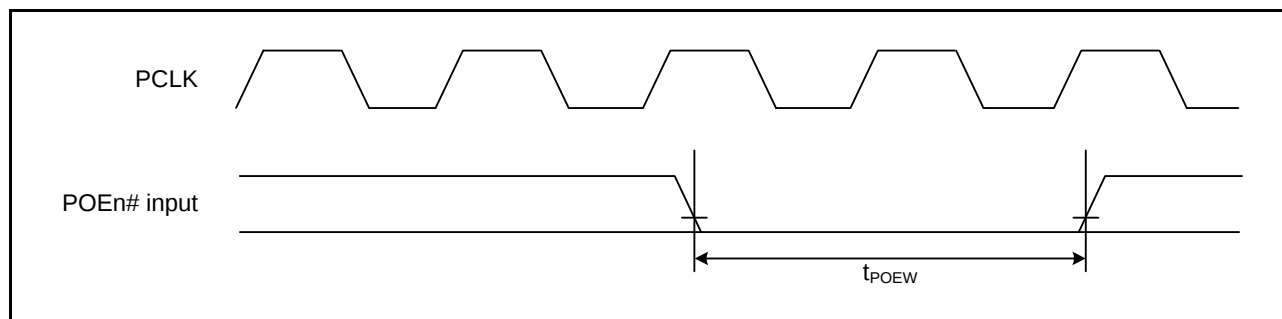


Figure 5.19 POE3# Clock Timing

5.3.4 Timing of PWM Delay Generation Circuit

Table 5.14 Timing of the PWM Delay Generation Circuit

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS = VREL0 = 0 V

AVCC = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Ta = Topr.

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Resolution	—	312.5	—	ps	ICLK = 100 MHz
DNL *1	—	±2.0	—	LSB	

Note 1. This value is correct when the difference between each code and the next is a resolution of one bit (1 LSB).

Table 5.18 Comparator Characteristics

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Ta = Topr. Ta is the same under conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog input capacitance	Cin	-	-	6	pF	
REFH pin offset voltage	Voff	-	-	5	mV	
REFL pin offset voltage		-	-	5	mV	
REFH input voltage range	Vin	1.7	-	AVcc – 0.3	V	
REFL input voltage range		0.3	-	AVcc – 1.7	V	
REFH reply time	tCR	-	-	1	μs	
REFL reply time	tCF	-	-	1	μs	

5.5 Power-on Reset Circuit, Voltage Detection Circuit Characteristics

Table 5.19 Power-on Reset Circuit, Voltage Detection Circuit Characteristics

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

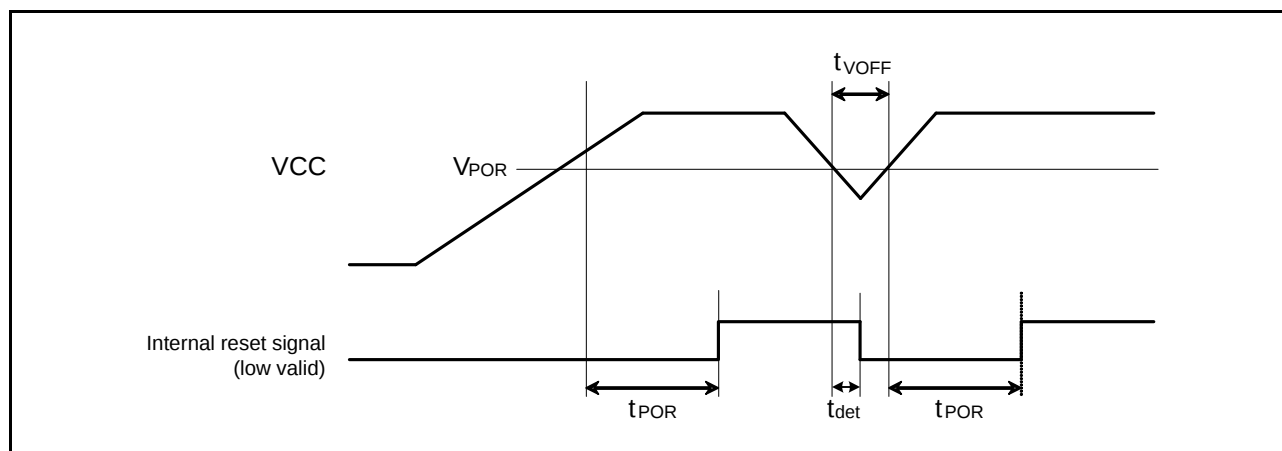
Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 and 2.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V _{POR}	2.48	2.60	2.72	V	Figure 5.20
	Voltage detection circuit (LVD)	V _{det1}	2.68	2.80	2.92		Figure 5.21
		V _{det2}	2.98	3.10	3.22		Figure 5.22
Internal reset time		t _{POR}	20	35	50	ms	Figure 5.21 and Figure 5.22
Min. VCC down time ^{*1}		t _{VOFF}	200	-	-	us	Figure 5.20 to Figure 5.22
Reply delay time		t _{det}	-	-	200	us	

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V _{POR}	3.70	3.90	4.10	V	Figure 5.20
	Voltage detection circuit (LVD)	V _{det1}	3.95	4.15	4.35		Figure 5.21
		V _{det2}	4.40	4.60	4.80		Figure 5.22
Internal reset time		t _{POR}	20	35	50	ms	Figure 5.21 and Figure 5.22
Min. VCC down time*1		t _{VOFF}	200	-	-	us	Figure 5.20 to Figure 5.22
Reply delay time		t _{det}	-	-	200	us	

Note 1. The power-off time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det1}, and V_{det2} for the POR/ LVD.


Figure 5.20 Power-on Reset Timing

Rev.	Date	Description	
		Page	Summary
2.00	Jan 10, 2014	98	Table 5.1 Absolute Maximum Ratings, changed
		102	Table 5.3 DC Characteristics (2): Note 3, changed
		103	Table 5.5 Permissible Power Consumption, added
		117	5.3.4 Timing of PWM Delay Generation Circuit, added
		117	Table 5.14 Timing of the PWM Delay Generation Circuit, added
		120	Table 5.17 Characteristics of the Programmable Gain Amplifier, changed
		125	Table 5.21 ROM (Flash Memory for Code Storage) Characteristics (1), changed
		125	Table 5.22 ROM (Flash Memory for Code Storage) Characteristics (2), added
		126	Table 5.23 Data Flash (Flash Memory for Data Storage) Characteristics (1), changed
		126	Table 5.24 Data Flash (Flash Memory for Data Storage) Characteristics (2), added

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