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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	l²C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	61
Program Memory Size	128KB (128K × 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 12x10b, 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562t7ddfh-v3

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Classification	Module/Function	Description				
Communications	CAN module (CAN) (as an optional function)	 1 channel 32 mailboxes				
	Serial peripheral interface (RSPI)	 1 unit RSPI transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPI clock (RSPCK) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) Capable of handling serial transfer as a master or slave Data formats Switching between MSB first and LSB first The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) Buffered structure Double buffers for both transmission and reception 				
	LIN module (LIN)	 1 channel (LIN master) Supports revisions 1.3, 2.0, and 2.1 of the LIN protocol 				
A/D converter	12-bit A/D converter (S12ADA)	 12 bits (2 units x 4 channels) 12-bit resolution Conversion time: 0 µs per channel (in operation with A/D conversion clock ADCLK at 50 MHz) for AVCC 4.0 to 5.5 V 0 µs per channel (in operation with A/D conversion clock ADCLK at 25 MHz) for AVCC0 = 3.0 to 3.6 V Two basic operating modes Single mode and scan mode Scan mode One-cycle scan mode Continuous scan mode Control to the activation sources are separately selectable for each group.) Sample-and-hold circuit for both units is included. Additionally, sample-and-hold circuit for each unit is includ				

 Table 1.1
 Outline of Specifications (4 / 5)



Classification	Module/Function	Description					
A/D converter 10-bit A/D converter (ADA)		 10 bits (1 unit x 12 channels) 10-bit resolution Conversion time: 0 µs per channel (in operation with A/D conversion clock ADCLK at 50 MHz) for AVCC0 = 4.0 to 5.5 V 0 µs per channel (in operation with A/D conversion clock ADCLK at 25 MHz) for AVC = 3.0 to 3.6 V Two basic operating modes Single mode and scan mode Scan mode One-cycle scan mode Sample-and-hold function A common sample-and-hold circuit for both units is included. A/D-conversion register settings for each input pin Three ways to start A/D conversion Conversion can be started by software, a conversion start trigger from a timer (MTU3 of GPT), or an external trigger signal. Functionality for 8-bit precision output Right-shifting the results of conversion for output by two bits is selectable. Self-diagnostic function 					
CRC calculator (C	RC)	 CRC code generation for arbitrary amounts of data in 8-bit units Select any of three generating polynomials: X⁸ + X² + X + 1, X¹⁶ + X¹⁵ + X² + 1, or X¹⁶ + X¹² + X⁵ + 1. Generation of CRC codes for use with LSB-first or MSB-first communications is selectable. 					
Operating frequent	су	ICLK: 8 to 100 MHz PCLK: 8 to 50 MHz					
Power supply volta	ige	 3-V version VCC = PLLVCC = 2.7 to 3.6V AVCC0 = AVCC = 3.0 to 3.6V, or 4.0 to 5.5V VREFH0 = 3.0 to AVCC0, or 4.0 to AVCC0 VREF = 3.0 to AVCC, or 4.0 to AVCC 5-V version VCC = PLLVCC = 4.0 to 5.5V AVCC0 = AVCC = 4.0 to 5.5V VREFH0 = 4.0 to AVCC0 VREF = 4.0 to AVCC 					
Operating tempera	ture	D version: -40 to +85°C, G version: -40 to +105°C*1					
Packages		112-pin LQFP (PLQP0112JA-A, 20x20-0.65-mm pitch) 100-pin LQFP (PLQP0100KB-A, 14x14-0.5-mm pitch) 80-pin LQFP (PLQP0080JA-A, 14x14-0.65-mm pitch) 64-pin LQFP (PLQP0064KB-A, 10x10-0.5-mm pitch) 64-pin LQFP (PLQP0064GA-A, 14x14-0.8mm pitch)					

 Table 1.1
 Outline of Specifications (5 / 5)

Note 1. Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.



Table 1.3List of Products (2 / 2)

Group	Part No.	Order Part No.	Package	ROM Capacity	RAM Capacity	Data Flash Capacity	Power Supply Voltage	CAN	Operating Temp. Range
RX62T	R5F562T7EDFH	R5F562T7EDFH#V3	PLQP0112JA-A	128	8	8	2.7 to 3.6 V	Not	-40 to +85°C
	R5F562T7EDFP	R5F562T7EDFP#V3	PLQP0100KB-A	Kbytes	Kbytes	es Kbytes		Support- ed	(D version)
	R5F562T7EDFF	R5F562T7EDFF#V3	PLQP0080JA-A						
	R5F562T7EDFM	R5F562T7EDFM#V3	PLQP0064KB-A						
	R5F562T7EDFK	R5F562T7EDFK#V3	PLQP0064GA-A						
	R5F562T6EDFF	R5F562T6EDFF#V3	PLQP0080JA-A	64	8				
	R5F562T6EDFM	R5F562T6EDFM#V3	PLQP0064KB-A	Kbytes	Kbytes				
	R5F562T6EDFK	R5F562T6EDFK#V3	PLQP0064GA-A						
	R5F562TAAGFH	R5F562TAAGFH#V3	PLQP0112JA-A	256	16	32	VCC/PLLVCC	Support-	-40 to +105°C
	R5F562TAAGFP	R5F562TAAGFP#V3	PLQP0100KB-A	Kbytes	Kbytes	Kbytes	4.0 to 5.5 V AVCC/AVCC0	ed	(G version) *1
	R5F562TAAGFF	R5F562TAAGFF#V3	PLQP0080JA-A				4.0 to 5.5 V		
	R5F562TAGGFF	R5F562TAGGFF#V3	PLQP0080JA-A						
	R5F562TAAGFM	R5F562TAAGFM#V3	PLQP0064KB-A						
	R5F562TAAGFK	R5F562TAAGFK#V3	PLQP0064GA-A						
	R5F562T7AGFH	R5F562T7AGFH#V3	PLQP0112JA-A	128	8	8			
	R5F562T7AGFP	R5F562T7AGFP#V3	PLQP0100KB-A	Kbytes	Kbytes	Kbytes			
	R5F562T7AGFF	R5F562T7AGFF#V3	PLQP0080JA-A						
	R5F562T7GGFF	R5F562T7GGFF#V3	PLQP0080JA-A						
	R5F562T7AGFM	R5F562T7AGFM#V3	PLQP0064KB-A						
	R5F562T7AGFK	R5F562T7AGFK#V3	PLQP0064GA-A						
	R5F562T6AGFF	R5F562T6AGFF#V3	PLQP0080JA-A	64	8				
	R5F562T6AGFM	R5F562T6AGFM#V3	PLQP0064KB-A	Kbytes	Kbytes				
	R5F562T6AGFK	R5F562T6AGFK#V3	PLQP0064GA-A						
	R5F562TABGFH	R5F562TABGFH#V3	PLQP0112JA-A	256	16	32	Provide VCC/PLLVCC 2.7 to 3.6 V AVCC/AVCC0 3.0 to 3.6 V or 4.0 to 5.5 V V	CC V CO V V	
	R5F562TABGFP	R5F562TABGFP#V3	PLQP0100KB-A	Kbytes	Kbytes	Kbytes			
	R5F562TABGFF	R5F562TABGFF#V3	PLQP0080JA-A						
	R5F562TABGFM	R5F562TABGFM#V3	PLQP0064KB-A						
	R5F562TABGFK	R5F562TABGFK#V3	PLQP0064GA-A						
	R5F562T7BGFH	R5F562T7BGFH#V3	PLQP0112JA-A	128	8 Khutaa	8			
	R5F562T7BGFP	R5F562T7BGFP#V3	PLQP0100KB-A	Kbytes	KDytes	KDytes			
	R5F562T7BGFF	R5F562T7BGFF#V3	PLQP0080JA-A						
	R5F562T7BGFM	R5F562T7BGFM#V3	PLQP0064KB-A						
	R5F562T7BGFK	R5F562T7BGFK#V3	PLQP0064GA-A						
	R5F562T6BGFF	R5F562T6BGFF#V3	PLQP0080JA-A	64 Khutoo	8 Khutoo				
	R5F562T6BGFM	R5F562T6BGFM#V3	PLQP0064KB-A	KDytes	KDytes				
	R5F562T6BGFK	R5F562T6BGFK#V3	PLQP0064GA-A						
RX62G	R5F562GAADFH	R5F562GAADFH#V3	PLQP0112JA-A	256	16 Khutee	32 Khutaa	VCC/PLLVCC	Support-	-40 to +85°C
	R5F562GAADFP	R5F562GAADFP#V3	PLQP0100KB-A	Kbyles	KDytes	KDytes	AVCC/AVCC0	eu	(D version)
	R5F562G7ADFH	R5F562G7ADFH#V3	PLQP0112JA-A	128 Khutos	8 Khutos	8 Khutos	4.0 to 5.5 V		
	R5F562G7ADFP	R5F562G7ADFP#V3	PLQP0100KB-A	KDytes	Kbytes	KDytes			
	R5F562GADDFH	R5F562GADDFH#V3	PLQP0112JA-A	256 Khytes	16 Kbytes	32 Khytes		Not Support-	
	R5F562GADDFP	R5F562GADDFP#V3	PLQP0100KB-A	Ruytes	Ruytes	Ruytes		ed	
	R5F562G7DDFH	R5F562G7DDFH#V3	PLQP0112JA-A	128 Khutos	8 Khutos	8 Khutos			
	R5F562G7DDFP	R5F562G7DDFP#V3	PLQP0100KB-A	NUYIES	NUYIES	Ruytes			
	R5F562GAAGFH	R5F562GAAGFH#V3	PLQP0112JA-A	256 Khytos	16 Khytee	32 Khytos	VCC/PLLVCC	Support-	-40 to +105°C
	R5F562GAAGFP	R5F562GAAGFP#V3	PLQP0100KB-A	NUYIES	NUYIES	Ruytes	AVCC/AVCC0	eu	(0 versio) *1
	R5F562G7AGFH	R5F562G7AGFH#V3	PLQP0112JA-A	128 Khutos	8 Khutoc	8 Khutos	4.0 to 5.5 V		
	R5F562G7AGFP	R5F562G7AGFP#V3	PLQP0100KB-A	NUYIES	ruytes	NUYIES			

Note 1. Please contact us if you are using a G version.



1.3 Block Diagram

Figure 1.2 shows a block diagram.





1.4 Pin Assignments

Figure 1.3 to Figure 1.7 show the pins assignments. Table 1.4 to Table 1.8 show the list of pins and pin functions.





Pin Assignment of the 112-Pin LQFP







Pin No. (80-Pin	Power Supply Clock				Communi-			
LQFP)	System Control	I/O Port	Analog	Timer	cation	Interrupt	POE	Debugging
1	EMLE							
2	VSS							
3	MDE							
4	VCL							
5	MD1							
6	MD0							
7		PE4		MTCLKC-C		IRQ1-B	POE10#-B	
8		PE3		MTCLKD-C		IRQ2-A	POE11#	
9	RES#							
10	XTAL							
11	VSS							
12	EXTAL							
13	VCC							
14		PE2				NMI	POE10#-A	
15		PE0			CRX-C			
16		PD7		GTIOC0A-B	CTX-C			TRST#
17		PD6		GTIOC0B-B				TMS
18		PD5		GTIOC1A-B	RXD1			TDI
19		PD4		GTIOC1B-B	SCK1			тск
20		PD3		GTIOC2A-B	TXD1			TDO
21		PB7			SCK2-A			
22		PB6			CRX-A/ RXD2-A			
23		PB5			CTX-A/ TXD2-A			
24	PLLVCC							
25		PB4		GTETRG		IRQ3	POE8#	
26	PLLVSS							
27		PB3		MTIOC0A-A	SCK0			
28		PB2		MTIOC0B-A	TXD0/SDA			
29		PB1		MTIOC0C	RXD0/SCL			
30		PB0		MTIOC0D	MOSI-B			
31		PA3		MTIOC2A	SSL0-B			
32		PA2		MTIOC2B	SSL1-B			
33	VCC							
34		P96				IRQ4	POE4#	
35	VSS							
36		P95		MTIOC6B				
37		P94		MTIOC7A				
38		P93		MTIOC7B				
39		P92		MTIOC6D				
40		P91		MTIOC7C				
41		P76		MTIOC4D/ GTIOC2B-A				

Table 1.6 List of Pins and Pin Functions (80-Pin LQFP) (1 / 3)



Pin No. (80-Pin	Power Supply Clock				Communi-			
LQFP)	System Control	I/O Port	Analog	Timer	cation	Interrupt	POE	Debugging
42		P75		MTIOC4C/ GTIOC1B-A				
43		P74		MTIOC3D/ GTIOC0B-A				
44		P73		MTIOC4B/ GTIOC2A-A				
45		P72		MTIOC4A/ GTIOC1A-A				
46		P71		MTIOC3B/ GTIOC0A-A				
47		P70				IRQ5	POE0#	
48		P33		MTIOC3A/ MTCLKA-A	SSL3-A			
49		P32		MTIOC3C/ MTCLKB-A	SSL2-A			
50	VCC							
51		P31		MTIOC0A-B/ MTCLKC-A	SSL1-A			
52	VSS							
53		P30		MTIOC0B-B/ MTCLKD-A	SSL0-A			
54		P24			RSPCK-A			
55		P23			CTX-B/ LTX/ MOSI-A			
56		P22	ADTRG#		CRX-B/ LRX/ MISO-A			
57		P21	ADTRG1#-B	MTCLKA-B		IRQ6		
58		P20	ADTRG0#-B	MTCLKB-B		IRQ7		
59	AVCC							
60	AVSS							
61		P63	AN3					
62		P62	AN2					
63		P61	AN1					
64		P60	AN0					
65		P47	AN103/ CVREFH					
66		P46	AN102					
67		P45	AN101					
68		P44	AN100					
69		P43	AN003/ CVREFL					
70		P42	AN002					
71		P41	AN001					
72		P40	AN000					
73	AVCC0							
74	VREFH0							
75	VREFL0							

Table 1.6	List of Pins and Pin Functions (80-Pin LQFP) (2 / 3)



Table 1.9 Pin Fund	ctions (3 / 4)		
Classifications	Pin Name	I/O	Description
Serial communications interface (SCIb)	TXD0, TXD1, TXD2-A/TXD2- B	Output	Output pins for data transmission. The TXD2-B pin is not included in the 80-/64-pin versions.
	RXD0, RXD1, RXD2-A/ RXD2-B	Input	Input pins for data reception. The RXD2-B pin is not included in the 80-/64-pin versions.
	SCK0, SCK1, SCK2-A/ SCK2-B	I/O	Input/output pins for clock signals. The SCK2-B pin is not included in the 80-/64-pin versions.
I ² C bus interface (RIIC)	SCL	I/O	Input/output pin for I ² C bus interface clocks. Bus can be directly driven by the NMOS open drain output.
	SDA	I/O	Input/output pin for I ² C bus interface data. Bus can be directly driven by the NMOS open drain output.
CAN module (CAN) (as an optional function)	CRX-A/CRX-B/CRX-C	Input	Input pin for the CAN. The CRX-C pin is not included in the 64- pin version.
	CTX-A/CTX-B/CTX-C	Output	Output pin for the CAN. The CTX-C pin is not included in the 64-pin version.
LIN module (LIN)	LRX	Input	Input pin for the LIN.
	LTX	Output	Output pin for the LIN.
Serial peripheral interface (RSPI)	RSPCK-A/RSPCK-B/ RSPCK-C	I/O	Clock input/output pin for the RSPI. The RSPCK-C pin is not included in the 80-/64-pin versions.
	MOSI-A/MOSI-B/MOSI-C	I/O	Inputs or outputs data output from the master for the RSPI. The MOSI-C pin is not included in the 80-/64-pin versions.
	MISO-A/MISO-B/MISO-C	I/O	Inputs or outputs data output from the slave for the RSPI. The MISO-C pin is not included in the 80-/64-pin versions.
	SSL0-A/SSL0-B/SSL0-C	I/O	Select the slave for the RSPI. The SSL0-C/SSL1-C/SSL2-C/
	SSL1-A/SSL1-B/SSL1-C SSL2-A/SSL2-B/SSL2-C SSL3-A/SSL3-B/SSL3-C	Output	SSL3-C pin is not included in the 80-/64-pin versions.
A/D converter	AN000 to AN003 AN100 to AN103	Input	Input pins for the analog signals to be processed by the 12-bit A/D converter.
	AN0 to AN11	Input	Input pins for the analog signals to be processed by the 10-bit A/D converter. The AN4 to AN11 pins are not included in the 80-pin version. Not included in the 64-pin version.
	ADTRG0#-A/ADTRG0#-B ADTRG1#-A/ADTRG1#-B ADTRG#	Input	Input pins for the external trigger signals that start the A/D conversion. The ADTRG0#-B/ADTRG1#-B/ADTRG# pin is not included in the 64-pin version.
	CVREFH	Input	Input pin for the high-level reference voltage to the comparator
	CVREFL	Input	Input pin for the low-level reference voltage to the comparator
Analog power supply	AVCC0	Input	Analog power supply pin for the 12-bit A/D converter. When the A/D converter is not in use, connect this pin to the system power supply.
	AVSS0	Input	Ground pin for the 12-bit A/D converter. Connect this pin to the system power supply (0 V).
	VREFH0	Input	Reference power supply pin for the 12-bit A/D converter. When the 12-bit A/D converter is not in use, connect this pin to the system power supply.
	VREFL0	Input	Ground pin of the reference power supply pin for the 12-bit A/D converter. When the 12-bit A/D converter is not in use, connect this pin to the system power supply (0 V).
	AVCC	Input	Analog power supply pin for the 10-bit A/D converter. When the A/D converter is not in use, connect this pin to the system power supply. Not included in the 64-pin version.
	AVSS	Input	Ground pin for the 10-bit A/D converter. Connect this pin to the system power supply (0 V). Not included in the 64-pin version.
	VREF	Input	Reference power supply pin for the 10-bit A/D converter. When the 10-bit A/D converter is not in use, connect this pin to the system power supply. Not included in the 80-/64-pin versions.

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2. CPU

2. CPU

The RX CPU has sixteen general-purpose registers, nine control registers, and one accumulator used for DSP instructions.

	b31
	R0 (SP) *
	R1
	R2
	R3
	R4
	R5
	R6
	R7
	R8
	R9
	R10
	R12
	R13
	R14
	R15
	USP (User stack pointer)
	INTB (Interrupt table register)
	PC (Program counter)
	PSW/ (Processor status word)
	BPC (Backup PC)
	BPC (Backup PC) BPSW (Backup PSW)
	BPC (Backup PC) BPSW (Backup PSW) FINTV (Fast interrupt vector register)
	BPC (Backup PC) BPSW (Backup PSW) FINTV (Fast interrupt vector register) FPSW (Floating-point status word)
SP instruction register	BPC (Backup PC) BPSW (Backup PSW) FINTV (Fast interrupt vector register) FPSW (Floating-point status word)
SP instruction register	BPC (Backup PC) BPSW (Backup PSW) FINTV (Fast interrupt vector register) FPSW (Floating-point status word)

Figure 2.1 Register Set of the CPU

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
MTU7	TIORL		IOI	D[3:0]			100	C[3:0]	
MTU6	TIER	TTEG	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA
MTU7	TIER	TTEG	TTEG2	_	TCIEV	TGIED	TGIEC	TGIEB	TGIEA
MTU	TOERB	_	—	OE7D	OE7C	OE6D	OE7B	OE7A	OE6B
MTU	TOCR1B	_	PSYE		_	TOCL	TOCS	OLSN	OLSP
MTU6	TCNT								
MTU7	TCNT								
MTU	TCDRB								
MTU	TDDRB								
MTU6	TGRA								
MTU6	TGRB								
MTU7	TGRA								
MTU7	TGRB								
MTU	TCNTSB								
MTU	TCBRB								
MTU6	TGRC								
MTU6	TGRD								
MTU7	TGRC								
MTU7	TGRD								
MTU6	TSR	TCFD	_	_	TCFV	TGFD	TGFC	TGFB	TGFA
MTU7	TSR	TCFD	_	_	TCFV	TGFD	TGFC	TGFB	TGFA
MTU	TITCR1B	T6AEN		T6ACOR[2:0]		T7VEN		T7VCOR[2:0]	
MTU	TITCNT1B	_		T6ACNT[2:0]		_		T7VCNT[2:0]	
MTU	TBTERB	_	_	_	_	_	_	BTE[1:0]	
MTU	TDERB	_	_	_	_	_	_	_	TDER
MTU	TOLBRB	_	_	OLS3N	OLS3P	OLS2N	OLS2P	OLS1N	OLS1P
MTU6	ТВТМ	_	_	_	_	_	_	TTSB	TTSA
MTU7	TBTM	_	_	_	_	_	_	TTSB	TTSA
MTU	TITMRB	_	_	_	_	_	_	_	TITM
MTU	TITCR2B	—	—	—	—	—		TRGCOR[2:0]	
MTU	TITCNT2B	_	_	_	_	_		TRG7CNT[2:0]	
MTU7	TADCR	BF UT7AE	[1:0]	UT7BE	DT7BE	ITA6AE	ITA7VE	ITB6AE	ITB7VE
MTU7	TADCORA		/ 12						
MTU7	TADCORB								
MTU7	TADCOBRA								

Table 4.2 List of I/O Registers (Bit Order) (21 / 30)



5.3 AC Characteristics

Table 5.6 Operation Frequency Value

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Тур.	Max.	Unit
Operating	System clock (ICLK)	f	8	-	100	MHz
frequency	Peripheral module clock (PCLK)		8	-	50	

5.3.1 Clock Timing

Table 5.7Clock Timing

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC Condition 3: VCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC Ta = Topr. Ta is the same under conditions 1 to 3.

ltem	Symbol	Min.	Max.	Unit	Test Conditions
Oscillation settling time after reset (crystal)	t _{OSC1}	10	-	ms	Figure 5.1
Oscillation settling time after leaving software standby mode (crystal)	t _{OSC2}	10	-	ms	Figure 5.2
Oscillation settling time after leaving deep software standby mode (crystal)	t _{OSC3}	10	-	ms	Figure 5.3
EXTAL external clock output delay settling time	t _{DEXT}	1	-	ms	Figure 5.1
EXTAL external clock input low pulse width	t _{EXL}	35	-	ns	Figure 5.4
EXTAL external clock input high pulse width	t _{EXH}	35	-	ns	
EXTAL external clock rising time	t _{EXr}	-	5	ns	
EXTAL external clock falling time	t _{EXf}	-	5	ns	
On-chip oscillator (IWDTCLK) oscillation frequency	f _{IWDTCLK}	62.5	187.5	kHz	





Figure 5.10 I2C Bus Interface Input/Output Timing



5.4 A/D Conversion Characteristics

Table 5.15 10-Bit A/D Conversion Characteristics

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Ta = Topr

Item	Min.	Тур.	Max.	Unit	Test Conditions
Resolution	10	10	10	Bit	
Conversion time*1 (AD clock = 25-MHz operation)	2.0	-	-	μs	Sampling 25 states
Analog input capacitance	-	-	4	pF	
Integral nonlinearity error	-	-	±3.0	LSB	
Offset error	-	-	±3.0	LSB	
Full-scale error	-	-	±3.0	LSB	
Quantization error	-	±0.5	-	LSB	
Absolute accuracy	-	-	±4.0	LSB	
Permissible signal source impedance	-	-	1.0	kΩ	

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC Ta = Topr. Ta is the same under conditions 2 and 3.

Item	Min.	Тур.	Max.	Unit	Test Conditions	
Resolution	10	10	10	Bit		
Conversion time*1 (AD clock = 50-MHz operation)	1.0	-	-	μs	Sampling 25 states	
Analog input capacitance	-	-	4	pF		
Integral nonlinearity error	-	-	±3.0	LSB		
Offset error	-	-	±3.0	LSB		
Full-scale error	-	-	±3.0	LSB		
Quantization error	-	±0.5	-	LSB		
Absolute accuracy	-	-	±4.0	LSB		
Permissible signal source impedance	-	-	1.0	kΩ		

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.



Table 5.17 Characteristics of the Programmable Gain Amplifier

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

 $\begin{array}{l} \mbox{Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V \\ \mbox{AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC} \end{array}$

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V AVCC0 = AVCC = 4.0 to 5.5V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC Ta = Topr. Ta is the same under conditions 1 to 3.

ltem		Symbol	Min.	Тур.	Max.	Unit	Test Conditions
Analog input capacitance		Cin	-	-	6	pF	
Input offset voltage		Voff	-	-	8	mV	
Input voltage range (Vin)	Gain × 2.000	Vin	0.050 x AVcc	-	0.450 x AVcc	V	
	Gain × 2.500		0.047 x AVcc	-	0.360 x AVcc		
	Gain × 3.077		0.045 x AVcc	-	0.292 x AVcc		
	Gain × 3.636		0.042 x AVcc	-	0.247 x AVcc		
	Gain × 4.000		0.040 x AVcc	-	0.212 x AVcc		
	Gain × 4.444		0.036 x AVcc	-	0.191 x AVcc		
	Gain × 5.000		0.033 x AVcc	-	0.170 x AVcc		
	Gain × 5.714		0.031 x AVcc	-	0.148 x AVcc		
	Gain × 6.667		0.029 x AVcc	-	0.127 x AVcc		
	Gain × 10.000		0.025 x AVcc	-	0.08 x AVcc		
	Gain × 13.333		0.023 x AVcc	-	0.06 x AVcc		
Slew rate		SR	10	-	-	V/µs	
Gain error	Gain × 2.000	-	-	-	1	%	
	Gain × 2.500		-	-	1		
	Gain × 3.077		-	-	1		
	Gain × 3.636		-	-	1.5		
	Gain × 4.000		-	-	1.5		
	Gain × 4.444		-	-	2		
	Gain × 5.000		-	-	2		
	Gain × 5.714		-	-	2		
	Gain × 6.667		-	-	3		
	Gain × 10.000		-	-	4		
	Gain × 13.333		-	-	4		





Figure 5.21 Voltage Detection Circuit Timing (Vdet1)



Figure 5.22 Voltage Detection Circuit Timing (Vdet2)



Appendix 1. Package Dimensions



Figure A 112-Pin LQFP (PLQP0112JA-A) Package Dimensions





Figure D 64-Pin LQFP (PLQP0064KB-A) Package Dimensions



REVISION HISTORY

RX62T Group, RX62G Group Datasheet

		Description					
Rev.	Date	Page	Summary				
1.00	Apr 20, 2011	—	First edition issued				
1.30	May 22, 2013	1	Features, Package lineup, added				
			1. Overview				
		2	Table 1.1 Outline of Specifications (1/5) Description of CPU, added				
		3	Table 1.1 Outline of Specifications (2/5) Description of Programmable I/O ports, changed				
		6	Table 1.1 Outline of Specifications (5/5), 64-pin packaged, added				
		7	Table 1.2 Functions of RX62T Group Products, 64-pin package, and MTU3/GPT completary PWM pins added				
		8	Table 1.3 List of Products, 64-pin package part number, changed				
		9	Figure 1.1 How to Read the Product Part No., 64-pin package part number, changed				
		9	Figure 1.1 How to Read the Product Part No., 5-V version, two-motor control supported, added				
		10	Figure 1.2 Block Diagram, changed				
		14	Figure 1.6 Pin Assignment of the 80-Pin LQFP (Two-motor Control Supported), added				
		15	Figure 1.7 Pin Assignment of the 64-Pin LQFP, Figure PLQP0064GA-A, added				
		25 to 27	Table 1.7 List of Pins and Pin Functions (80-Pin LQFP: R5F562TxGDFF) , added				
		30 to 33	Table 1.9 Pin Functions, changed				
			4. I/ORegister				
		38to 61	Table 4.1 List of I/O Registers (Address Order), MPU, added				
		47	Table 4.1 List of I/O Registers (Address Order) TMOCNTL, TMOCNTU register, added				
		57	Table 4.1 List of I/O Registers (Address Order), GTSWP register, added				
			5. Electrical Characteristics				
		62	Table 5.1 Absolute Maximum Ratings, note changed				
		64	Table 5.2 DC Characteristics (1) (2/3) Test Conditions of P90 to P95, changed				
		66	Table 5.3 DC Characteristics (2), note changed				
		67	Table 5.4 Permissible Output Currents, note changed				
		72	Table 5.7 Control Signal Timing, notes changed				
		73	Table 5.8 Timing of On-Chip Peripheral Modules (1), changed				
			Appendix 1.Package Dimensions				
		96	Figure E 64-Pin LQFP (PLQP0064GA-A), added				
2.00	Jan 10, 2014	1	Features, changed				
			1. Overview				
		2 to 6	Table 1.1 Outline of Specifications, changed; Note 1, added				
		7, 8	Table 1.2 Functions of RX62T Group and RX62G Group Products, changed				
		9, 10	Table 1.3 List of Products, changed; Note 1, added				
		11	Figure 1.1 How to Read the Product Part No., changed				
		15	Figure 1.6 Pin Assignment of the 80-Pin LQFP (Two-Motor Control Supported Version), added				
		27 to 29	Table 1.7 List of Pins and Pin Functions (80-Pin LQFP: R5F562TxGDFF), added				
			4. I/O Registers				
		43 to 67	Table 4.1 List of I/O Registers (Address Order), changed				
		68 to 97	Table 4.2 List of I/O Registers (Bit Order), changed				
			5. Electrical Characteristics				
		_	Conditions in the table, change to Ta = -40 to +105°C from Ta = -40 to +85°C.				



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