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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I ² C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562t7ddfk-v1

Table 1.1 Outline of Specifications (5 / 5)

Classification	Module/Function	Description
A/D converter	10-bit A/D converter (ADA)	• 10 bits (1 unit x 12 channels) • 10-bit resolution • Conversion time: 1.0 μs per channel (in operation with A/D conversion clock ADCLK at 50 MHz) for AVCC0 = 4.0 to 5.5 V 2.0 μs per channel (in operation with A/D conversion clock ADCLK at 25 MHz) for AVCC = 3.0 to 3.6 V • Two basic operating modes - Single mode and scan mode • Scan mode - One-cycle scan mode - Continuous scan mode • Sample-and-hold function - A common sample-and-hold circuit for both units is included. • A/D-conversion register settings for each input pin • Three ways to start A/D conversion - Conversion can be started by software, a conversion start trigger from a timer (MTU3 or GPT), or an external trigger signal. • Functionality for 8-bit precision output - Right-shifting the results of conversion for output by two bits is selectable. • Self-diagnostic function - The self-diagnostic function internally generates three analog input voltages (AVSS, VREF x 1/2, VREF).
CRC calculator (CRC)		• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$. • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.
Operating frequency		ICLK: 8 to 100 MHz PCLK: 8 to 50 MHz
Power supply voltage		• 3-V version - VCC = PLLVCC = 2.7 to 3.6V - AVCC0 = AVCC = 3.0 to 3.6V, or 4.0 to 5.5V - VREFH0 = 3.0 to AVCC0, or 4.0 to AVCC0 - VREF = 3.0 to AVCC, or 4.0 to AVCC • 5-V version - VCC = PLLVCC = 4.0 to 5.5V - AVCC0 = AVCC = 4.0 to 5.5V - VREFH0 = 4.0 to AVCC0 - VREF = 4.0 to AVCC
Operating temperature		D version: -40 to +85°C, G version: -40 to +105°C*1
Packages		112-pin LQFP (PLQP0112JA-A, 20x20-0.65-mm pitch) 100-pin LQFP (PLQP0100KB-A, 14x14-0.5-mm pitch) 80-pin LQFP (PLQP0080JA-A, 14x14-0.65-mm pitch) 64-pin LQFP (PLQP0064KB-A, 10x10-0.5-mm pitch) 64-pin LQFP (PLQP0064GA-A, 14x14-0.8mm pitch)

Note 1. Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

1.3 Block Diagram

Figure 1.2 shows a block diagram.

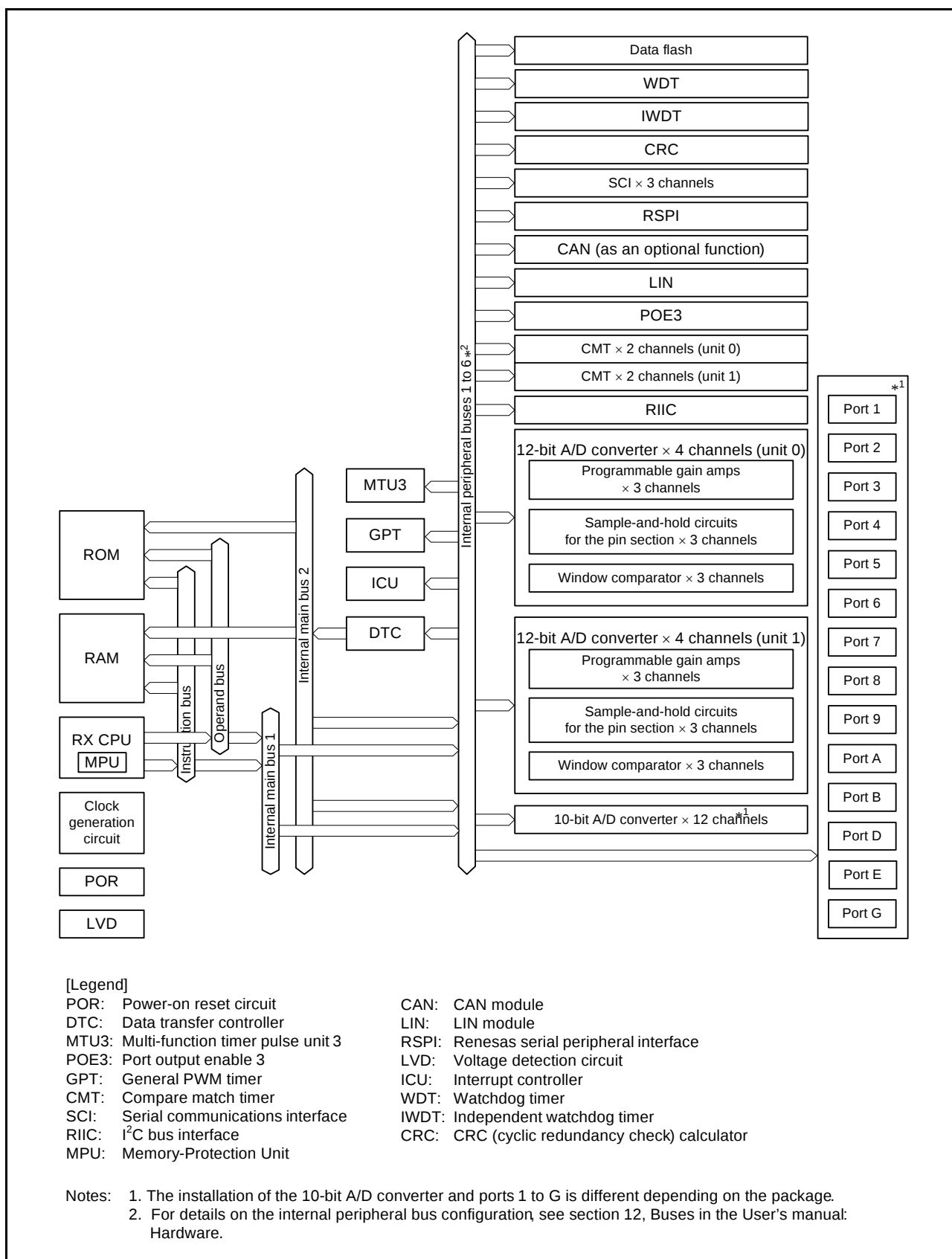


Figure 1.2 Block Diagram

1.4 Pin Assignments

Figure 1.3 to Figure 1.7 show the pins assignments. Table 1.4 to Table 1.8 show the list of pins and pin functions.

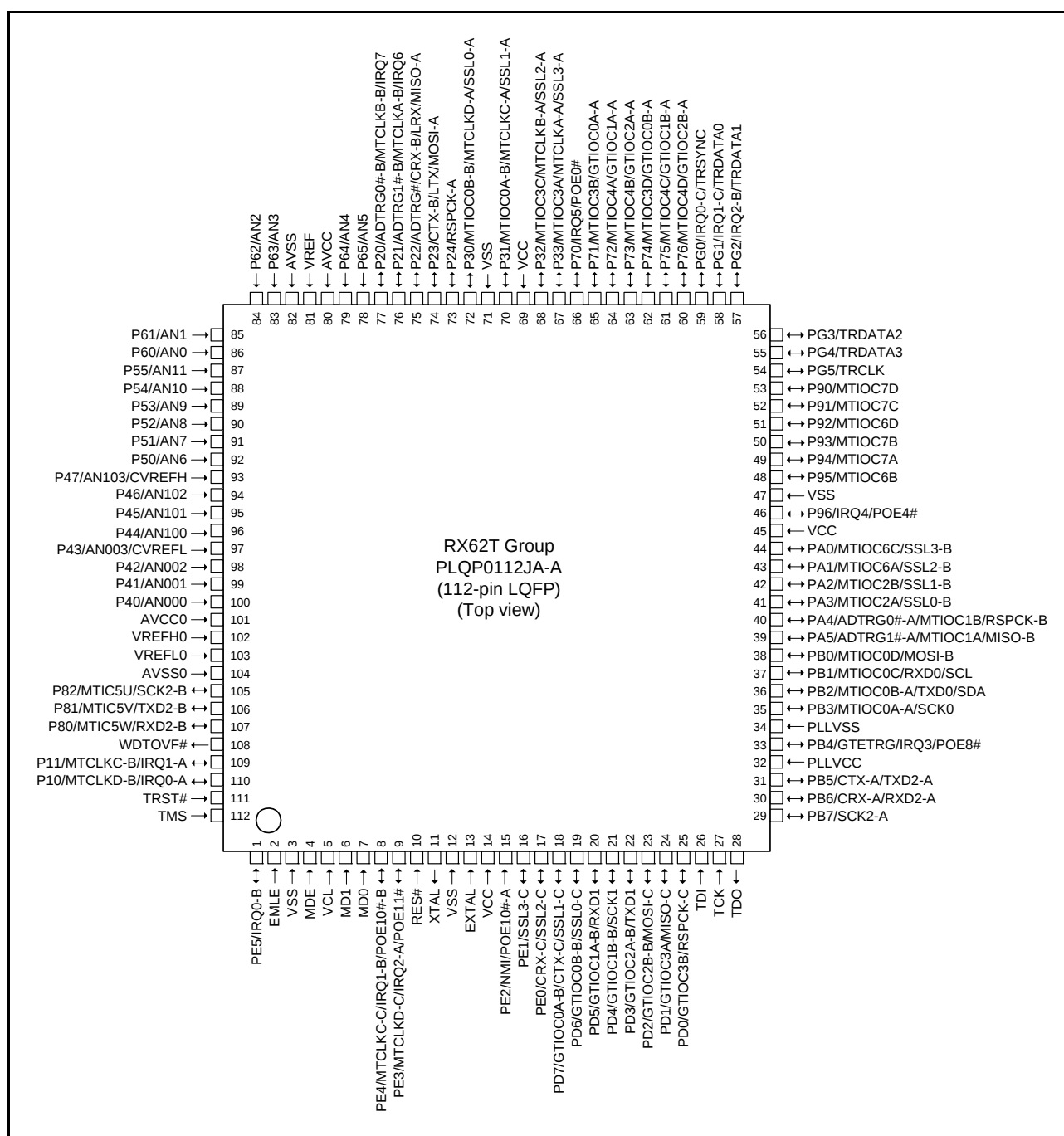


Figure 1.3 Pin Assignment of the 112-Pin LQFP

Table 1.4 List of Pins and Pin Functions (112-Pin LQFP) (2 / 3)

Pin No. (112-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi- cation	Interrupt	POE	Debugging
44		PA0		MTIOC6C	SSL3-B			
45	VCC							
46		P96				IRQ4	POE4#	
47	VSS							
48		P95		MTIOC6B				
49		P94		MTIOC7A				
50		P93		MTIOC7B				
51		P92		MTIOC6D				
52		P91		MTIOC7C				
53		P90		MTIOC7D				
54		PG5						TRCLK
55		PG4						TRDATA3
56		PG3						TRDATA2
57		PG2				IRQ2-B		TRDATA1
58		PG1				IRQ1-C		TRDATA0
59		PG0				IRQ0-C		TRSYNC
60		P76		MTIOC4D/ GTIOC2B-A				
61		P75		MTIOC4C/ GTIOC1B-A				
62		P74		MTIOC3D/ GTIOC0B-A				
63		P73		MTIOC4B/ GTIOC2A-A				
64		P72		MTIOC4A/ GTIOC1A-A				
65		P71		MTIOC3B/ GTIOC0A-A				
66		P70				IRQ5	POE0#	
67		P33		MTIOC3A/ MTCLKA-A	SSL3-A			
68		P32		MTIOC3C/ MTCLKB-A	SSL2-A			
69	VCC							
70		P31		MTIOC0A-B/ MTCLKC-A	SSL1-A			
71	VSS							
72		P30		MTIOC0B-B/ MTCLKD-A	SSL0-A			
73		P24			RSPCK-A			
74		P23			CTX-B/ LTX/ MOSI-A			
75		P22	ADTRG#		CRX-B/ LRX/ MISO-A			
76		P21	ADTRG1#-B	MTCLKA-B		IRQ6		
77		P20	ADTRG0#-B	MTCLKB-B		IRQ7		
78		P65	AN5					
79		P64	AN4					

Table 1.9 Pin Functions (3 / 4)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCIb)	TXD0, TXD1, TXD2-A/TXD2-B	Output	Output pins for data transmission. The TXD2-B pin is not included in the 80-/64-pin versions.
	RXD0, RXD1, RXD2-A/RXD2-B	Input	Input pins for data reception. The RXD2-B pin is not included in the 80-/64-pin versions.
	SCK0, SCK1, SCK2-A/SCK2-B	I/O	Input/output pins for clock signals. The SCK2-B pin is not included in the 80-/64-pin versions.
I ² C bus interface (RIIC)	SCL	I/O	Input/output pin for I ² C bus interface clocks. Bus can be directly driven by the NMOS open drain output.
	SDA	I/O	Input/output pin for I ² C bus interface data. Bus can be directly driven by the NMOS open drain output.
CAN module (CAN) (as an optional function)	CRX-A/CRX-B/CRX-C	Input	Input pin for the CAN. The CRX-C pin is not included in the 64-pin version.
	CTX-A/CTX-B/CTX-C	Output	Output pin for the CAN. The CTX-C pin is not included in the 64-pin version.
LIN module (LIN)	LRX	Input	Input pin for the LIN.
	LTX	Output	Output pin for the LIN.
Serial peripheral interface (RSPI)	RSPCK-A/RSPCK-B/RSPCK-C	I/O	Clock input/output pin for the RSPI. The RSPCK-C pin is not included in the 80-/64-pin versions.
	MOSI-A/MOSI-B/MOSI-C	I/O	Inputs or outputs data output from the master for the RSPI. The MOSI-C pin is not included in the 80-/64-pin versions.
	MISO-A/MISO-B/MISO-C	I/O	Inputs or outputs data output from the slave for the RSPI. The MISO-C pin is not included in the 80-/64-pin versions.
	SSL0-A/SSL0-B/SSL0-C	I/O	Select the slave for the RSPI. The SSL0-C/SSL1-C/SSL2-C/SSL3-C pin is not included in the 80-/64-pin versions.
	SSL1-A/SSL1-B/SSL1-C SSL2-A/SSL2-B/SSL2-C SSL3-A/SSL3-B/SSL3-C	Output	
A/D converter	AN000 to AN003 AN100 to AN103	Input	Input pins for the analog signals to be processed by the 12-bit A/D converter.
	AN0 to AN11	Input	Input pins for the analog signals to be processed by the 10-bit A/D converter. The AN4 to AN11 pins are not included in the 80-pin version. Not included in the 64-pin version.
	ADTRG0#-A/ADTRG0#-B ADTRG1#-A/ADTRG1#-B ADTRG#	Input	Input pins for the external trigger signals that start the A/D conversion. The ADTRG0#-B/ADTRG1#-B/ADTRG# pin is not included in the 64-pin version.
	CVREFH	Input	Input pin for the high-level reference voltage to the comparator
	CVREFL	Input	Input pin for the low-level reference voltage to the comparator
Analog power supply	AVCC0	Input	Analog power supply pin for the 12-bit A/D converter. When the A/D converter is not in use, connect this pin to the system power supply.
	AVSS0	Input	Ground pin for the 12-bit A/D converter. Connect this pin to the system power supply (0 V).
	VREFH0	Input	Reference power supply pin for the 12-bit A/D converter. When the 12-bit A/D converter is not in use, connect this pin to the system power supply.
	VREFL0	Input	Ground pin of the reference power supply pin for the 12-bit A/D converter. When the 12-bit A/D converter is not in use, connect this pin to the system power supply (0 V).
	AVCC	Input	Analog power supply pin for the 10-bit A/D converter. When the A/D converter is not in use, connect this pin to the system power supply. Not included in the 64-pin version.
	AVSS	Input	Ground pin for the 10-bit A/D converter. Connect this pin to the system power supply (0 V). Not included in the 64-pin version.
	VREF	Input	Reference power supply pin for the 10-bit A/D converter. When the 10-bit A/D converter is not in use, connect this pin to the system power supply. Not included in the 80-/64-pin versions.

4. I/O Registers

This section gives information on the on-chip I/O register addresses and bit configurations. The information is given as shown below. Notes on writing to registers are also given at the end.

(1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to functional modules (abbreviations).
- The number of access cycles indicates the number of states based on the specified reference clock.
- Among the I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.
- A unit of access is specified for each register. Access other than in the specified unit is prohibited.

(2) I/O register bits

- Bit configurations of the registers are listed in the same order as the register addresses.
- Reserved bits are indicated by "-" in the bit name column.
- Space in the bit name field indicates that the entire register is allocated to either the counter or data.
- For the registers of 16 or 32 bits, the MSB is listed first.

(3) Notes on writing to I/O registers

When writing to an I/O register, the CPU starts executing the subsequent instruction before completing I/O register write. This may cause the subsequent instruction to be executed before the post-update I/O register value is reflected on the operation.

As described in the following examples, special care is required for the cases in which the subsequent instruction must be executed after the post-update I/O register value is actually reflected.

[Examples of cases requiring special care]

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERm of the ICU (interrupt request enable bit)*1 cleared to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

Note 1. See section 11.2.2, Interrupt Request Enable Register m (IERm) (m = 02h to 1Fh) in the User's manual: Hardware.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

Table 4.1 List of I/O Registers (Address Order) (4 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 70BCh	ICU	Interrupt request register 188	IR188	8	8	2 ICLK
0008 70BDh	ICU	Interrupt request register 189	IR189	8	8	2 ICLK
0008 70BEh	ICU	Interrupt request register 190	IR190	8	8	2 ICLK
0008 70C0h	ICU	Interrupt request register 192	IR192	8	8	2 ICLK
0008 70C1h	ICU	Interrupt request register 193	IR193	8	8	2 ICLK
0008 70C2h	ICU	Interrupt request register 194	IR194	8	8	2 ICLK
0008 70C3h	ICU	Interrupt request register 195	IR195	8	8	2 ICLK
0008 70C4h	ICU	Interrupt request register 196	IR196	8	8	2 ICLK
0008 70D6h	ICU	Interrupt request register 214	IR214	8	8	2 ICLK
0008 70D7h	ICU	Interrupt request register 215	IR215	8	8	2 ICLK
0008 70D8h	ICU	Interrupt request register 216	IR216	8	8	2 ICLK
0008 70D9h	ICU	Interrupt request register 217	IR217	8	8	2 ICLK
0008 70DAh	ICU	Interrupt request register 218	IR218	8	8	2 ICLK
0008 70DBh	ICU	Interrupt request register 219	IR219	8	8	2 ICLK
0008 70DCh	ICU	Interrupt request register 220	IR220	8	8	2 ICLK
0008 70DDh	ICU	Interrupt request register 221	IR221	8	8	2 ICLK
0008 70DEh	ICU	Interrupt request register 222	IR222	8	8	2 ICLK
0008 70DFh	ICU	Interrupt request register 223	IR223	8	8	2 ICLK
0008 70E0h	ICU	Interrupt request register 224	IR224	8	8	2 ICLK
0008 70E1h	ICU	Interrupt request register 225	IR225	8	8	2 ICLK
0008 70F6h	ICU	Interrupt request register 246	IR246	8	8	2 ICLK
0008 70F7h	ICU	Interrupt request register 247	IR247	8	8	2 ICLK
0008 70F8h	ICU	Interrupt request register 248	IR248	8	8	2 ICLK
0008 70F9h	ICU	Interrupt request register 249	IR249	8	8	2 ICLK
0008 70FEh	ICU	Interrupt request register 254	IR254	8	8	2 ICLK
0008 711Bh	ICU	DTC activation enable register 027	DTCER027	8	8	2 ICLK
0008 711Ch	ICU	DTC activation enable register 028	DTCER028	8	8	2 ICLK
0008 711Dh	ICU	DTC activation enable register 029	DTCER029	8	8	2 ICLK
0008 711Eh	ICU	DTC activation enable register 030	DTCER030	8	8	2 ICLK
0008 711Fh	ICU	DTC activation enable register 031	DTCER031	8	8	2 ICLK
0008 712Dh	ICU	DTC activation enable register 045	DTCER045	8	8	2 ICLK
0008 712Eh	ICU	DTC activation enable register 046	DTCER046	8	8	2 ICLK
0008 7140h	ICU	DTC activation enable register 064	DTCER064	8	8	2 ICLK
0008 7141h	ICU	DTC activation enable register 065	DTCER065	8	8	2 ICLK
0008 7142h	ICU	DTC activation enable register 066	DTCER066	8	8	2 ICLK
0008 7143h	ICU	DTC activation enable register 067	DTCER067	8	8	2 ICLK
0008 7144h	ICU	DTC activation enable register 068	DTCER068	8	8	2 ICLK
0008 7145h	ICU	DTC activation enable register 069	DTCER069	8	8	2 ICLK
0008 7146h	ICU	DTC activation enable register 070	DTCER070	8	8	2 ICLK
0008 7147h	ICU	DTC activation enable register 071	DTCER071	8	8	2 ICLK
0008 7162h	ICU	DTC activation enable register 098	DTCER098	8	8	2 ICLK
0008 7166h	ICU	DTC activation enable register 102	DTCER102	8	8	2 ICLK
0008 7167h	ICU	DTC activation enable register 103	DTCER103	8	8	2 ICLK
0008 716Ah	ICU	DTC activation enable register 106	DTCER106	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (13 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 C065h	PORT5	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C066h	PORT6	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C067h	PORT7	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C068h	PORT8	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C069h	PORT9	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C06Ah	PORTA	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C06Bh	PORTB	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C06Dh	PORTD	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C06Eh	PORTE	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C070h	PORTG	Input buffer control register	ICR*1	8	8	2, 3 PCLK*3
0008 C108h	IOPORT	Port function register 8	PF8IRQ	8	8	2, 3 PCLK*3
0008 C109h	IOPORT	Port function register 9	PF9IRQ	8	8	2, 3 PCLK*3
0008 C10Ah	IOPORT	Port function register A	PFAADC	8	8	2, 3 PCLK*3
0008 C10Ch	IOPORT	Port function register C	PFCMTU	8	8	2, 3 PCLK*3
0008 C10Dh	IOPORT	Port function register D	PFDGPT	8	8	2, 3 PCLK*3
0008 C10Fh	IOPORT	Port function register F	PFFSCI	8	8	2, 3 PCLK*3
0008 C110h	IOPORT	Port function register G	PFGSPI	8	8	2, 3 PCLK*3
0008 C111h	IOPORT	Port function register H	PFHSPI	8	8	2, 3 PCLK*3
0008 C113h	IOPORT	Port function register J	PFJCAN	8	8	2, 3 PCLK*3
0008 C114h	IOPORT	Port function register K	PFKLIN	8	8	2, 3 PCLK*3
0008 C116h	IOPORT	Port function register M	PFMPOE	8	8	2, 3 PCLK*3
0008 C117h	IOPORT	Port function register N	PFNPOE	8	8	2, 3 PCLK*3
0008 C280h	SYSTEM	Deep standby control register	DPSBYCR	8	8	4, 5 PCLK*3
0008 C281h	SYSTEM	Deep standby wait control register	DPSWCR	8	8	4, 5 PCLK*3
0008 C282h	SYSTEM	Deep standby interrupt enable register	DPSIER	8	8	4, 5 PCLK*3
0008 C283h	SYSTEM	Deep standby interrupt flag register	DPSIFR	8	8	4, 5 PCLK*3
0008 C284h	SYSTEM	Deep standby interrupt edge register	DPSIEGR	8	8	4, 5 PCLK*3
0008 C285h	SYSTEM	Reset status register	RSTSR	8	8	4, 5 PCLK*3
0008 C289h	FLASH	Flash write erase protection register	FWEPROR	8	8	4, 5 PCLK*3
0008 C28Ch	SYSTEM	Key code register for low-voltage detection control register	LVDKEYR	8	8	4, 5 PCLK*3
0008 C28Dh	SYSTEM	Voltage detection control register	LVDCR	8	8	4, 5 PCLK*3
0008 C290h	SYSTEM	Deep standby backup register 0	DPSBKR0	8	8	4, 5 PCLK*3
0008 C291h	SYSTEM	Deep standby backup register 1	DPSBKR1	8	8	4, 5 PCLK*3
0008 C292h	SYSTEM	Deep standby backup register 2	DPSBKR2	8	8	4, 5 PCLK*3
0008 C293h	SYSTEM	Deep standby backup register 3	DPSBKR3	8	8	4, 5 PCLK*3
0008 C294h	SYSTEM	Deep standby backup register 4	DPSBKR4	8	8	4, 5 PCLK*3
0008 C295h	SYSTEM	Deep standby backup register 5	DPSBKR5	8	8	4, 5 PCLK*3
0008 C296h	SYSTEM	Deep standby backup register 6	DPSBKR6	8	8	4, 5 PCLK*3
0008 C297h	SYSTEM	Deep standby backup register 7	DPSBKR7	8	8	4, 5 PCLK*3
0008 C298h	SYSTEM	Deep standby backup register 8	DPSBKR8	8	8	4, 5 PCLK*3
0008 C299h	SYSTEM	Deep standby backup register 9	DPSBKR9	8	8	4, 5 PCLK*3
0008 C29Ah	SYSTEM	Deep standby backup register 10	DPSBKR10	8	8	4, 5 PCLK*3
0008 C29Bh	SYSTEM	Deep standby backup register 11	DPSBKR11	8	8	4, 5 PCLK*3

Table 4.1 List of I/O Registers (Address Order) (14 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 C29Ch	SYSTEM	Deep standby backup register 12	DPSBKR12	8	8	4, 5 PCLK ^{*3}
0008 C29Dh	SYSTEM	Deep standby backup register 13	DPSBKR13	8	8	4, 5 PCLK ^{*3}
0008 C29Eh	SYSTEM	Deep standby backup register 14	DPSBKR14	8	8	4, 5 PCLK ^{*3}
0008 C29Fh	SYSTEM	Deep standby backup register 15	DPSBKR15	8	8	4, 5 PCLK ^{*3}
0008 C2A0h	SYSTEM	Deep standby backup register 16	DPSBKR16	8	8	4, 5 PCLK ^{*3}
0008 C2A1h	SYSTEM	Deep standby backup register 17	DPSBKR17	8	8	4, 5 PCLK ^{*3}
0008 C2A2h	SYSTEM	Deep standby backup register 18	DPSBKR18	8	8	4, 5 PCLK ^{*3}
0008 C2A3h	SYSTEM	Deep standby backup register 19	DPSBKR19	8	8	4, 5 PCLK ^{*3}
0008 C2A4h	SYSTEM	Deep standby backup register 20	DPSBKR20	8	8	4, 5 PCLK ^{*3}
0008 C2A5h	SYSTEM	Deep standby backup register 21	DPSBKR21	8	8	4, 5 PCLK ^{*3}
0008 C2A6h	SYSTEM	Deep standby backup register 22	DPSBKR22	8	8	4, 5 PCLK ^{*3}
0008 C2A7h	SYSTEM	Deep standby backup register 23	DPSBKR23	8	8	4, 5 PCLK ^{*3}
0008 C2A8h	SYSTEM	Deep standby backup register 24	DPSBKR24	8	8	4, 5 PCLK ^{*3}
0008 C2A9h	SYSTEM	Deep standby backup register 25	DPSBKR25	8	8	4, 5 PCLK ^{*3}
0008 C2AAh	SYSTEM	Deep standby backup register 26	DPSBKR26	8	8	4, 5 PCLK ^{*3}
0008 C2ABh	SYSTEM	Deep standby backup register 27	DPSBKR27	8	8	4, 5 PCLK ^{*3}
0008 C2ACh	SYSTEM	Deep standby backup register 28	DPSBKR28	8	8	4, 5 PCLK ^{*3}
0008 C2ADh	SYSTEM	Deep standby backup register 29	DPSBKR29	8	8	4, 5 PCLK ^{*3}
0008 C2AEh	SYSTEM	Deep standby backup register 30	DPSBKR30	8	8	4, 5 PCLK ^{*3}
0008 C2AFh	SYSTEM	Deep standby backup register 31	DPSBKR31	8	8	4, 5 PCLK ^{*3}
0008 C4C0h	POE	Input level control/status register 1	ICSR1	16	8, 16	2, 3 PCLK ^{*3}
0008 C4C2h	POE	Output level control/status register 1	OCSR1	16	8, 16	2, 3 PCLK ^{*3}
0008 C4C4h	POE	Input level control/status register 2	ICSR2	16	8, 16	2, 3 PCLK ^{*3}
0008 C4C6h	POE	Output level control/status register 2	OCSR2	16	8, 16	2, 3 PCLK ^{*3}
0008 C4C8h	POE	Input level control/status register 3	ICSR3	16	8, 16	2, 3 PCLK ^{*3}
0008 C4CAh	POE	Software port output enable register	SPOER	8	8	2, 3 PCLK ^{*3}
0008 C4CBh	POE	Port output enable control register 1	POECR1	8	8	2, 3 PCLK ^{*3}
0008 C4CCh	POE	Port output enable control register 2	POECR2	16	16	2, 3 PCLK ^{*3}
0008 C4CEh	POE	Port output enable control register 3	POECR3	16	16	2, 3 PCLK ^{*3}
0008 C4D0h	POE	Port output enable control register 4	POECR4	16	16	2, 3 PCLK ^{*3}
0008 C4D2h	POE	Port output enable control register 5	POECR5	16	16	2, 3 PCLK ^{*3}
0008 C4D4h	POE	Port output enable control register 6	POECR6	16	16	2, 3 PCLK ^{*3}
0008 C4D6h	POE	Input level control/status register 4	ICSR4	16	8, 16	2, 3 PCLK ^{*3}
0008 C4D8h	POE	Input level control/status register 5	ICSR5	16	8, 16	2, 3 PCLK ^{*3}
0008 C4DAh	POE	Active level setting register 1	ALR1	16	8, 16	2, 3 PCLK ^{*3}
0009 0200h to 0009 03FFh	CAN0 ^{*2}	Mailbox registers 0 to 31	MB0 to MB 31	128	8, 16, 32	2, 3 PCLK ^{*3}
0009 0400h	CAN0 ^{*2}	Mask register 0	MKR0	32	8, 16, 32	2, 3 PCLK ^{*3}
0009 0404h	CAN0 ^{*2}	Mask register 1	MKR1	32	8, 16, 32	2, 3 PCLK ^{*3}
0009 0408h	CAN0 ^{*2}	Mask register 2	MKR2	32	8, 16, 32	2, 3 PCLK ^{*3}
0009 040Ch	CAN0 ^{*2}	Mask register 3	MKR3	32	8, 16, 32	2, 3 PCLK ^{*3}
0009 0410h	CAN0 ^{*2}	Mask register 4	MKR4	32	8, 16, 32	2, 3 PCLK ^{*3}
0009 0414h	CAN0 ^{*2}	Mask register 5	MKR5	32	8, 16, 32	2, 3 PCLK ^{*3}
0009 0418h	CAN0 ^{*2}	Mask register 6	MKR6	32	8, 16, 32	2, 3 PCLK ^{*3}

Table 4.1 List of I/O Registers (Address Order) (15 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0009 041Ch	CAN0*2	Mask register 7	MKR7	32	8, 16, 32	2, 3 PCLK*3
0009 0420h	CAN0*2	FIFO received ID compare register 0	FIDCR0	32	8, 16, 32	2, 3 PCLK*3
0009 0424h	CAN0*2	FIFO received ID compare register 1	FIDCR1	32	8, 16, 32	2, 3 PCLK*3
0009 0428h	CAN0*2	Mask invalid register	MKIVLR	32	8, 16, 32	2, 3 PCLK*3
0009 042Ch	CAN0*2	Mailbox interrupt enable register	MIER	32	8, 16, 32	2, 3 PCLK*3
0009 0820h to 0009 083Fh	CAN0*2	Message control registers 0 to 31	MCTL0 to MCTL31	8	8	2, 3 PCLK*3
0009 0840h	CAN0*2	Control register	CTLR	16	8, 16	2, 3 PCLK*3
0009 0842h	CAN0*2	Status register	STR	16	8, 16	2, 3 PCLK*3
0009 0844h	CAN0*2	Bit configuration register	BCR	32	8, 16, 32	2, 3 PCLK*3
0009 0848h	CAN0*2	Receive FIFO control register	RFCR	8	8	2, 3 PCLK*3
0009 0849h	CAN0*2	Receive FIFO pointer control register	RFPCR	8	8	2, 3 PCLK*3
0009 084Ah	CAN0*2	Transmit FIFO control register	TFCR	8	8	2, 3 PCLK*3
0009 084Bh	CAN0*2	Transmit FIFO pointer control register	TFPCR	8	8	2, 3 PCLK*3
0009 084Ch	CAN0*2	Error interrupt enable register	EIER	8	8	2, 3 PCLK*3
0009 084Dh	CAN0*2	Error interrupt factor judge register	EIFR	8	8	2, 3 PCLK*3
0009 084Eh	CAN0*2	Receive error count register	RECR	8	8	2, 3 PCLK*3
0009 084Fh	CAN0*2	Transmit error count register	TECR	8	8	2, 3 PCLK*3
0009 0850h	CAN0*2	Error code store register	ECSR	8	8	2, 3 PCLK*3
0009 0851h	CAN0*2	Channel search support register	CSSR	8	8	2, 3 PCLK*3
0009 0852h	CAN0*2	Mailbox search status register	MSSR	8	8	2, 3 PCLK*3
0009 0853h	CAN0*2	Mailbox search mode register	MSMR	8	8	2, 3 PCLK*3
0009 0854h	CAN0*2	Time stamp register	TSR	16	8, 16	2, 3 PCLK*3
0009 0856h	CAN0*2	Acceptance filter support register	AFSR	16	8, 16	2, 3 PCLK*3
0009 0858h	CAN0*2	Test control register	TCR	8	8	2, 3 PCLK*3
0009 4001h	LIN0	LIN wake-up baud rate select register	LWBR	8	8	2, 3 PCLK*3
0009 4002h	LIN0	LIN baud rate prescaler 0 register	LBRP0	8	8, 16	2, 3 PCLK*3
0009 4003h	LIN0	LIN baud rate prescaler 1 register	LBRP1	8	8, 16	2, 3 PCLK*3
0009 4004h	LIN0	LIN self-test control register	LSTC	8	8	2, 3 PCLK*3
0009 4008h	LIN0	Mode register	L0MD	8	8, 16, 32	2, 3 PCLK*3
0009 4009h	LIN0	Break field setting register	L0BRK	8	8, 16, 32	2, 3 PCLK*3
0009 400Ah	LIN0	Space setting register	L0SPC	8	8, 16, 32	2, 3 PCLK*3
0009 400Bh	LIN0	Wake-up setting register	L0WUP	8	8, 16, 32	2, 3 PCLK*3
0009 400Ch	LIN0	Interrupt enable register	L0IE	8	8, 16	2, 3 PCLK*3
0009 400Dh	LIN0	Error detection enable register	L0EDE	8	8, 16	2, 3 PCLK*3
0009 400Eh	LIN0	Control register	L0C	8	8	2, 3 PCLK*3
0009 4010h	LIN0	Transmission control register	L0TC	8	8, 16, 32	2, 3 PCLK*3
0009 4011h	LIN0	Mode status register	L0MST	8	8, 16, 32	2, 3 PCLK*3
0009 4012h	LIN0	Status register	L0ST	8	8, 16, 32	2, 3 PCLK*3
0009 4013h	LIN0	Error status register	L0EST	8	8, 16, 32	2, 3 PCLK*3
0009 4014h	LIN0	Response field set register	L0RFC	8	8, 16	2, 3 PCLK*3
0009 4015h	LIN0	Buffer register	L0IDB	8	8, 16	2, 3 PCLK*3
0009 4016h	LIN0	Check sum buffer register	L0CBR	8	8	2, 3 PCLK*3
0009 4018h	LIN0	Data 1 buffer register	L0DB1	8	8, 16, 32	2, 3 PCLK*3

Table 4.1 List of I/O Registers (Address Order) (17 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000C 123Ah	MTU	Timer interrupt skipping mode register A	TITMRA	8	8	5 ICLK
000C 123Bh	MTU	Timer interrupt skipping set register 2A	TITCR2A	8	8	5 ICLK
000C 123Ch	MTU	Timer interrupt skipping counter 2A	TITCNT2A	8	8	5 ICLK
000C 1240h	MTU4	Timer A/D converter start request control register	TADCR	16	16	5 ICLK
000C 1244h	MTU4	Timer A/D converter start request cycle set register A	TADCORA	16	16, 32	5 ICLK
000C 1246h	MTU4	Timer A/D converter start request cycle set register B	TADCORB	16	16	5 ICLK
000C 1248h	MTU4	Timer A/D converter start request cycle set buffer register A	TADCOBRA	16	16, 32	5 ICLK
000C 124Ah	MTU4	Timer A/D converter start request cycle set buffer register B	TADCOBRB	16	16	5 ICLK
000C 1260h	MTU	Timer waveform control register A	TWCRA	8	8	5 ICLK
000C 1270h	MTU3	Timer mode register 2A	TMDR2A	8	8	5 ICLK
000C 1272h	MTU3	Timer general register E	TGRE	16	16	5 ICLK
000C 1274h	MTU4	Timer general register E	TGRE	16	16	5 ICLK
000C 1276h	MTU4	Timer general register F	TGRF	16	16	5 ICLK
000C 1280h	MTU	Timer start register A	TSTRA	8	8, 16	5 ICLK
000C 1281h	MTU	Timer synchronous register A	TSYRA	8	8	5 ICLK
000C 1282h	MTU	Timer counter synchronous start register	TCSYSTR	8	8	5 ICLK
000C 1284h	MTU	Timer read/write enable register A	TRWERA	8	8	5 ICLK
000C 1300h	MTU0	Timer control register	TCR	8	8, 16, 32	5 ICLK
000C 1301h	MTU0	Timer mode register 1	TMDR1	8	8	5 ICLK
000C 1302h	MTU0	Timer I/O control register H	TIORH	8	8, 16	5 ICLK
000C 1303h	MTU0	Timer I/O control register L	TIORL	8	8	5 ICLK
000C 1304h	MTU0	Timer interrupt enable register	TIER	8	8, 16, 32	5 ICLK
000C 1305h	MTU0	Timer status register	TSR	8	8	5 ICLK
000C 1306h	MTU0	Timer counter	TCNT	16	16	5 ICLK
000C 1308h	MTU0	Timer general register A	TGRA	16	16, 32	5 ICLK
000C 130Ah	MTU0	Timer general register B	TGRB	16	16	5 ICLK
000C 130Ch	MTU0	Timer general register C	TGRC	16	16, 32	5 ICLK
000C 130Eh	MTU0	Timer general register D	TGRD	16	16	5 ICLK
000C 1320h	MTU0	Timer general register E	TGRE	16	16, 32	5 ICLK
000C 1322h	MTU0	Timer general register F	TGRF	16	16	5 ICLK
000C 1324h	MTU0	Timer interrupt enable register 2	TIER2	8	8, 16	5 ICLK
000C 1325h	MTU0	Timer status register 2	TSR2	8	8	5 ICLK
000C 1326h	MTU0	Timer buffer operation transfer mode register	TBTM	8	8	5 ICLK
000C 1380h	MTU1	Timer control register	TCR	8	8, 16	5 ICLK
000C 1381h	MTU1	Timer mode register 1	TMDR1	8	8	5 ICLK
000C 1382h	MTU1	Timer I/O control register	TIOR	8	8	5 ICLK
000C 1384h	MTU1	Timer interrupt enable register	TIER	8	8, 16, 32	5 ICLK
000C 1385h	MTU1	Timer status register	TSR	8	8	5 ICLK
000C 1386h	MTU1	Timer counter	TCNT	16	16	5 ICLK
000C 1388h	MTU1	Timer general register A	TGRA	16	16, 32	5 ICLK
000C 138Ah	MTU1	Timer general register B	TGRB	16	16	5 ICLK

Table 4.1 List of I/O Registers (Address Order) (21 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000C 2116h	GPT0	General PWM timer compare capture register D	GTCCRD	16	16, 32	3 to 5 ICLK ^{*4}
000C 2118h	GPT0	General PWM timer compare capture register E	GTCCRE	16	16, 32	3 to 5 ICLK ^{*4}
000C 211Ah	GPT0	General PWM timer compare capture register F	GTCCRF	16	16, 32	3 to 5 ICLK ^{*4}
000C 211Ch	GPT0	General PWM timer cycle setting register	GTPR	16	16, 32	3 to 5 ICLK ^{*4}
000C 211Eh	GPT0	General PWM timer cycle setting buffer register	GTPBR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2120h	GPT0	General PWM timer cycle setting double-buffer register	GTPDBR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2124h	GPT0	A/D converter start request timing register A	GTADTRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 2126h	GPT0	A/D converter start request timing buffer register A	GTADTBRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 2128h	GPT0	A/D converter start request timing double-buffer register A	GTADTBRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 212Ch	GPT0	A/D converter start request timing register B	GTADTRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 212Eh	GPT0	A/D converter start request timing buffer register B	GTADTRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2130h	GPT0	A/D converter start request timing double-buffer register B	GTADTRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2134h	GPT0	General PWM timer output negate control register	GTONCR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2136h	GPT0	General PWM timer dead time control register	GTDTCR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2138h	GPT0	General PWM timer dead time value register	GTDVU	16	16, 32	3 to 5 ICLK ^{*4}
000C 213Ah	GPT0	General PWM timer dead time value register	GTDVD	16	16, 32	3 to 5 ICLK ^{*4}
000C 213Ch	GPT0	General PWM timer dead time buffer register	GTDBU	16	16, 32	3 to 5 ICLK ^{*4}
000C 213Eh	GPT0	General PWM timer dead time buffer register	GTDBD	16	16, 32	3 to 5 ICLK ^{*4}
000C 2140h	GPT0	General PWM timer output protection function status register	GTSOS	16	16, 32	3 to 5 ICLK ^{*4}
000C 2142h	GPT0	General PWM timer output protection function temporary release register	GTSOTR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2180h	GPT1	General PWM timer I/O control register	GTIOR	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2182h	GPT1	General PWM timer interrupt output setting register	GTINTAD	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2184h	GPT1	General PWM timer control register	GTCR	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2186h	GPT1	General PWM timer buffer enable register	GTBER	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2188h	GPT1	General PWM timer count direction register	GTUDC	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 218Ah	GPT1	General PWM timer interrupt and A/D converter start request skipping setting register	GTITC	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 218Ch	GPT1	General PWM timer status register	GTST	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 218Eh	GPT1	General PWM timer counter	GTCNT	16	16	3 to 5 ICLK ^{*4}
000C 2190h	GPT1	General PWM timer compare capture register A	GTCCRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 2192h	GPT1	General PWM timer compare capture register B	GTCCRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2194h	GPT1	General PWM timer compare capture register C	GTCCRC	16	16, 32	3 to 5 ICLK ^{*4}
000C 2196h	GPT1	General PWM timer compare capture register D	GTCCRD	16	16, 32	3 to 5 ICLK ^{*4}
000C 2198h	GPT1	General PWM timer compare capture register E	GTCCRE	16	16, 32	3 to 5 ICLK ^{*4}
000C 219Ah	GPT1	General PWM timer compare capture register F	GTCCRF	16	16, 32	3 to 5 ICLK ^{*4}
000C 219Ch	GPT1	General PWM timer cycle setting register	GTPR	16	16, 32	3 to 5 ICLK ^{*4}
000C 219Eh	GPT1	General PWM timer cycle setting buffer register	GTPBR	16	16, 32	3 to 5 ICLK ^{*4}

Table 4.2 **List of I/O Registers (Bit Order) (9 / 30)**

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
ICU	IRQCR0	—	—	—	—		IRQMD[1:0]	—	—
ICU	IRQCR1	—	—	—	—		IRQMD[1:0]	—	—
ICU	IRQCR2	—	—	—	—		IRQMD[1:0]	—	—
ICU	IRQCR3	—	—	—	—		IRQMD[1:0]	—	—
ICU	IRQCR4	—	—	—	—		IRQMD[1:0]	—	—
ICU	IRQCR5	—	—	—	—		IRQMD[1:0]	—	—
ICU	IRQCR6	—	—	—	—		IRQMD[1:0]	—	—
ICU	IRQCR7	—	—	—	—		IRQMD[1:0]	—	—
ICU	NMISR	—	—	—	—	—	OSTST	LVDST	NMIST
ICU	NMIER	—	—	—	—	—	OSTEN	LVDEN	NMIEN
ICU	NMICLR	—	—	—	—	—	OSTCLR	—	NMICLR
ICU	NMICR	—	—	—	—	NMIMD	—	—	—
CMT	CMSTR0	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	STR1	STR0
CMT0	CMCR	—	—	—	—	—	—	—	—
		—	CMIE	—	—	—	—	CKS[1:0]	
CMT0	CMCNT								
CMT0	CMCOR								
CMT1	CMCR	—	—	—	—	—	—	—	—
		—	CMIE	—	—	—	—	CKS[1:0]	
CMT1	CMCNT								
CMT1	CMCOR								
CMT	CMSTR1	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	STR3	STR2
CMT2	CMCR	—	—	—	—	—	—	—	—
		—	CMIE	—	—	—	—	CKS[1:0]	
CMT2	CMCNT								
CMT2	CMCOR								
CMT3	CMCR	—	—	—	—	—	—	—	—
		—	CMIE	—	—	—	—	CKS[1:0]	
CMT3	CMCNT								
CMT3	CMCOR								
WDT	TCSR	—	TMS	TME	—	—		CKS[2:0]	
WDT	WINA								
WDT	TCNT								
WDT	WINB								
WDT	RSTCSR	WOVF	RSTE	—	—	—	—	—	—
IWD	IWDTCR	—	—	—	—	—	—	—	—
			CKS[3:0]			—	—	TOPS[1:0]	
IWD	IWDTSR	—	UNDF			CNTVAL[13:0]			
						CNTVAL[13:0]			
AD0	ADDR ^{A1}	—	—	—	—	—	—		

Table 4.2 List of I/O Registers (Bit Order) (12 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
RSPi0	SSLP	—	—	—	—	SSLP3	SSLP2	SSLP1	SSLP0
RSPi0	SPPCR	—	—	MOIFE	MOIFV	—	—	SPLP2	SPLP
RSPi0	SPSR	SPRF	—	SPTEF	—	PERF	MODF	IDLNF	OVRF
RSPi0	SPDR	H[15:0]							
		H[15:0]							
		L[15:0]							
		L[15:0]							
RSPi0	SPSCR	—	—	—	—	—	—	SPSLN[2:0]	—
RSPi0	SPSSR	—	—	SPECM[2:0]	—	—	—	SPCP[2:0]	—
RSPi0	SPBR	SPR7	SPR6	SPR5	SPR4	SPR3	SPR2	SPR1	SPR0
RSPi0	SPDCR	—	—	SPLW	SPRDTD	SLSEL[1:0]	—	SPFC[1:0]	—
RSPi0	SPCKD	—	—	—	—	—	—	SCKDL[2:0]	—
RSPi0	SSLND	—	—	—	—	—	—	SLNDL[2:0]	—
RSPi0	SPND	—	—	—	—	—	—	SPNDL[2:0]	—
RSPi0	SPCR2	—	—	—	—	PTE	SPIIE	SPOE	SPPE
RSPi0	SPCMD0	SCKDEN	SLNDEN	SPNDEN	LSBF	—	—	SPB[3:0]	—
		SSLKP	—	SSLA[2:0]	—	BRDV[1:0]	—	CPOL	CPHA
RSPi0	SPCMD1	SCKDEN	SLNDEN	SPNDEN	LSBF	—	—	SPB[3:0]	—
		SSLKP	—	SSLA[2:0]	—	BRDV[1:0]	—	CPOL	CPHA
RSPi0	SPCMD2	SCKDEN	SLNDEN	SPNDEN	LSBF	—	—	SPB[3:0]	—
		SSLKP	—	SSLA[2:0]	—	BRDV[1:0]	—	CPOL	CPHA
RSPi0	SPCMD3	SCKDEN	SLNDEN	SPNDEN	LSBF	—	—	SPB[3:0]	—
		SSLKP	—	SSLA[2:0]	—	BRDV[1:0]	—	CPOL	CPHA
RSPi0	SPCMD4	SCKDEN	SLNDEN	SPNDEN	LSBF	—	—	SPB[3:0]	—
		SSLKP	—	SSLA[2:0]	—	BRDV[1:0]	—	CPOL	CPHA
RSPi0	SPCMD5	SCKDEN	SLNDEN	SPNDEN	LSBF	—	—	SPB[3:0]	—
		SSLKP	—	SSLA[2:0]	—	BRDV[1:0]	—	CPOL	CPHA
RSPi0	SPCMD6	SCKDEN	SLNDEN	SPNDEN	LSBF	—	—	SPB[3:0]	—
		SSLKP	—	SSLA[2:0]	—	BRDV[1:0]	—	CPOL	CPHA
RSPi0	SPCMD7	SCKDEN	SLNDEN	SPNDEN	LSBF	—	—	SPB[3:0]	—
		SSLKP	—	SSLA[2:0]	—	BRDV[1:0]	—	CPOL	CPHA
S12AD0	ADCSR	ADST	ADCS[1:0]	—	ADIE	—	CKS[1:0]	TRGE	EXTRG
S12AD0	ADANS	—	—	CH[1:0]	—	—	PG002SEL	PG001SEL	PG000SEL
		—	—	—	—	—	PG002EN	PG001EN	PG000EN
S12AD0	ADPG	—	—	—	—	—	PG002GAIN[3:0]	—	—
		—	—	—	—	—	PG000GAIN[3:0]	—	—
S12AD0	ADCER	ADRFMT	—	ADIEW	ADIE2	DIAGM	DIAGLD	DIAGVAL[1:0]	—
		—	—	ACE	—	—	ADPRC[1:0]	—	SHBYP
S12AD0	ADSTRGR	—	—	—	—	—	ADSTRS1[4:0]	—	—
		—	—	—	—	—	ADSTRS0[4:0]	—	—
S12AD	ADCMPMD0	—	—	CEN102[1:0]	—	CEN101[1:0]	—	CEN100[1:0]	—
		—	—	CEN002[1:0]	—	CEN001[1:0]	—	CEN000[1:0]	—
S12AD	ADCMPMD1	—	VSELL1	VSELH1	CSEL1	—	VSELL0	VSELH0	CSEL0
		—	—	REFH[2:0]	—	—	—	REFL[2:0]	—
S12AD	ADCMPNR0	—	—	—	—	—	C002NR[3:0]	—	—
		—	—	—	—	—	C001NR[3:0]	—	—
S12AD	ADCMPNR1	—	—	—	—	—	C102NR[3:0]	—	—
		—	—	—	—	—	C101NR[3:0]	—	—
S12AD	ADCMPFR	—	—	C102FLAG	C101FLAG	C100FLAG	C002FLAG	C001FLAG	C000FLAG
S12AD	ADCMPSEL	—	—	—	—	—	—	POERQ	IE
		—	—	SEL102	SEL101	SEL100	SEL002	SEL001	SEL000

Table 4.2 List of I/O Registers (Bit Order) (17 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
CAN0*3	MKR5	—	—	—			SID[10:0]		
					SID[10:0]			EID[17:0]	
						EID[17:0]			
						EID[17:0]			
CAN0*3	MKR6	—	—	—			SID[10:0]		
					SID[10:0]			EID[17:0]	
						EID[17:0]			
						EID[17:0]			
CAN0*3	MKR7	—	—	—			SID[10:0]		
					SID[10:0]			EID[17:0]	
						EID[17:0]			
						EID[17:0]			
CAN0*3	FIDCR0	IDE	RTR	—			SID[10:0]		
					SID[10:0]			EID[17:0]	
						EID[17:0]			
						EID[17:0]			
CAN0*3	FIDCR1	IDE	RTR	—			SID[10:0]		
					SID[10:0]			EID[17:0]	
						EID[17:0]			
						EID[17:0]			
CAN0*3	MKIVLR								
CAN0*3	MIER	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
CAN0*3	MCTL.TX	TRMREQ	RECREQ	—	ONESHOT	—	TRMABT	TRMACTIVE	SENTDATA
	MCTL.RX	TRMREQ	RECREQ	—	ONESHOT	—	MSGLOST	INVALDATA	NEWDATA
CAN0*3	CTLR	—	—	RBOC	BOM[1:0]		SLPM	CANM[1:0]	
			TSPS[1:0]	TSRC	TPM	MLM	IDFM[1:0]		MBM
CAN0*3	STR	—	RECST	TRMST	BOST	EPST	SLPST	HLTST	RSTST
		EST	TABST	FMLST	NMLST	TFST	RFST	SDST	NDST
CAN0*3	BCR		TSEG1[3:0]			—	—	BRP[9:0]	
CAN0*3	RFCR	RFEST	RFWST	RFFST	RFMLF		RFUST[2:0]		RFE
CAN0*3	RFPCR	—	—	—	—	—	—	—	—
CAN0*3	TFCR	TFEST	TFFST	—	—		TFUST[2:0]		TFE
CAN0*3	TFPCR	—	—	—	—	—	—	—	—
CAN0*3	EIER	BLIE	OLIE	ORIE	BORIE	BOEIE	EPIE	EWIE	BEIE
CAN0*3	EIFR	BLIF	OLIF	ORIF	BORIF	BOEIF	EPIF	EWIF	BEIF
CAN0*3	RECR	—	—	—	—	—	—	—	—
CAN0*3	TECR	—	—	—	—	—	—	—	—
CAN0*3	ECSR	EDPM	ADEF	BE0F	BE1F	CEF	AEF	FEF	SEF
CAN0*3	CSSR	—	—	—	—	—	—	—	—
CAN0*3	MSSR	SEST	—	—			MBNST[4:0]		
CAN0*3	MSMR	—	—	—	—	—	—	MBSM[1:0]	
CAN0*3	TSR	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—

Table 4.2 List of I/O Registers (Bit Order) (22 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
MTU7	TADCOBRB								
MTU	TSYCR	CE0A	CE0D	CE0C	CE0D	CE1A	CE1B	CE2A	CE2B
MTU	TWCRB	CCE	—	—	—	—	—	SCC	WRE
MTU	TMDR2B	—	—	—	—	—	—	—	DRS
MTU6	TGRE								
MTU7	TGRE								
MTU7	TGRF								
MTU	TSTRB	CST7	CST6	—	—	—	—	—	—
MTU	TSYRB	SYNC7	SYNC6	—	—	—	—	—	—
MTU	TRWERB	—	—	—	—	—	—	—	RWE
MTU5	TCNTU								
MTU5	TGRU								
MTU5	TCRU	—	—	—	—	—	—	TPSC[1:0]	
MTU5	TIORU	—	—	—			IOC[4:0]		
MTU5	TCNTV								
MTU5	TGRV								
MTU5	TCRV	—	—	—	—	—	—	TPSC[1:0]	
MTU5	TIORV	—	—	—			IOC[4:0]		
MTU5	TCNTW								
MTU5	TGRW								
MTU5	TCRW	—	—	—	—	—	—	TPSC[1:0]	
MTU5	TIORW	—	—	—			IOC[4:0]		
MTU5	TSR	—	—	—	—	—	CMFU5	CMFV5	CMFW5
MTU5	TIER	—	—	—	—	—	TGIE5U	TGIE5V	TGIE5W
MTU5	TSTR	—	—	—	—	—	CSTU5	CSTV5	CSTW5
MTU5	TCNTCMPCLR	—	—	—	—	—	CMPCLR5U	CMPCLR5V	CMPCLR5W
GPT	GTSTR	—	—	—	—	—	—	—	—
		—	—	—	—	CST3	CST2	CST1	CST0
GPT	GTHSCR	CPHW3[1:0]		CPHW2[1:0]		CPHW1[1:0]		CPHW0[1:0]	
		CSHW3[1:0]		CSHW2[1:0]		CSHW1[1:0]		CSHW0[1:0]	
GPT	GTHCCR	—	—	—	—	CCSW3	CCSW2	CCSW1	CCSW0
		CCHW3[1:0]		CCHW2[1:0]		CCHW1[1:0]		CCHW0[1:0]	
GPT	GTHSSR		CSHSL3[3:0]				CSHSL2[3:0]		
			CSHSL1[3:0]				CSHSL0[3:0]		
GPT	GTHPSR		CSHPL3[3:0]				CSHPL2[3:0]		
			CSHPL1[3:0]				CSHPL0[3:0]		
GPT	GTWP	—	—	—	—	—	—	—	—
		—	—	—	—	WP3	WP2	WP1	WP0
GPT	GTSYNC	—	—	SYNC3[1:0]		—	—	SYNC2[1:0]	
		—	—	SYNC1[1:0]		—	—	SYNC0[1:0]	
GPT	GTETINT	—	—	—	—	—	—	ETINF	ETIPF
		—	—	—	—	—	—	ETINEN	ETIPEN

5.3.3 Timing of On-Chip Peripheral Modules

Table 5.9 Timing of On-Chip Peripheral Modules (1)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

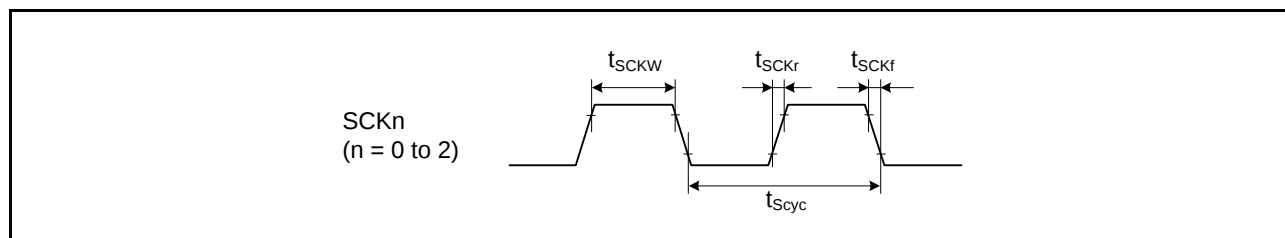
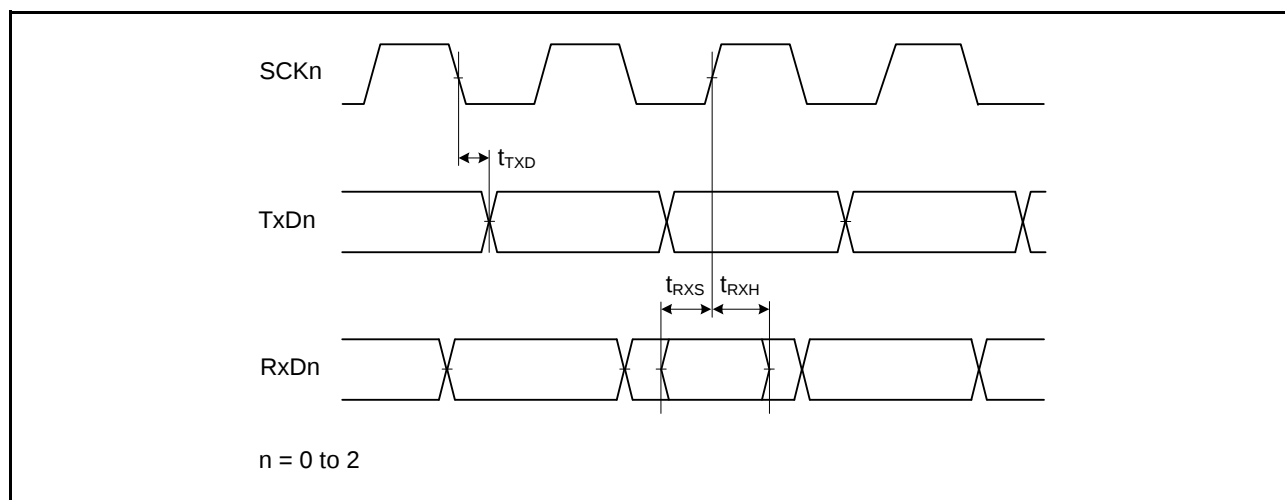
Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item			Symbol	Min.	Typ.	Max.	Unit
SCI	Input clock cycle	Asynchronous	t_{Scyc}	$4 \times t_{\text{Pcyc}}$	-	ns	Figure 5.8
		Clock synchronous		$6 \times t_{\text{Pcyc}}$	-		
	Input clock pulse width		t_{SCKW}	$0.4 \times t_{\text{Pcyc}}$	$0.6 \times t_{\text{Scyc}}$	ns	
	Input clock rise time		t_{SCKr}	-	20	ns	
	Input clock fall time		t_{SCKf}	-	20	ns	
	Output clock cycle	Asynchronous	t_{Scyc}	$16 \times t_{\text{Pcyc}}$	-	ns	
		Clock synchronous		$6 \times t_{\text{Pcyc}}$	-	ns	
	Output clock pulse width		t_{SCKW}	$0.4 \times t_{\text{Scyc}}$	$0.6 \times t_{\text{Scyc}}$	ns	
	Output clock rise time		t_{SCKr}	-	20	ns	
	Output clock fall time		t_{SCKf}	-	20	ns	
	Transmit data delay time (clock synchronous)		t_{TXD}	-	40	ns	Figure 5.9
	Receive data setup time (clock synchronous)		t_{RXS}	40	-	ns	
	Receive data hold time (clock synchronous)		t_{RXH}	40	-	ns	

Note: • t_{Pcyc} : PCLK cycle


Figure 5.8 SCK Clock Input Timing

Figure 5.9 SCI Input/Output Timing: Clock Synchronous Mode

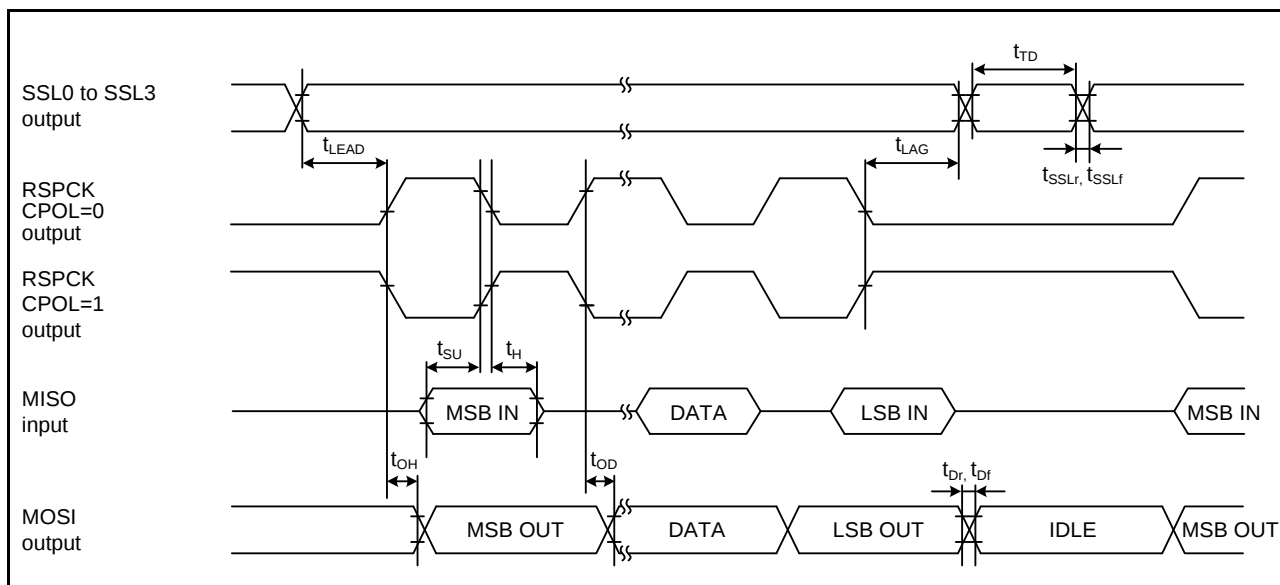


Figure 5.13 RSPI Timing (Master, CPHA = 1)

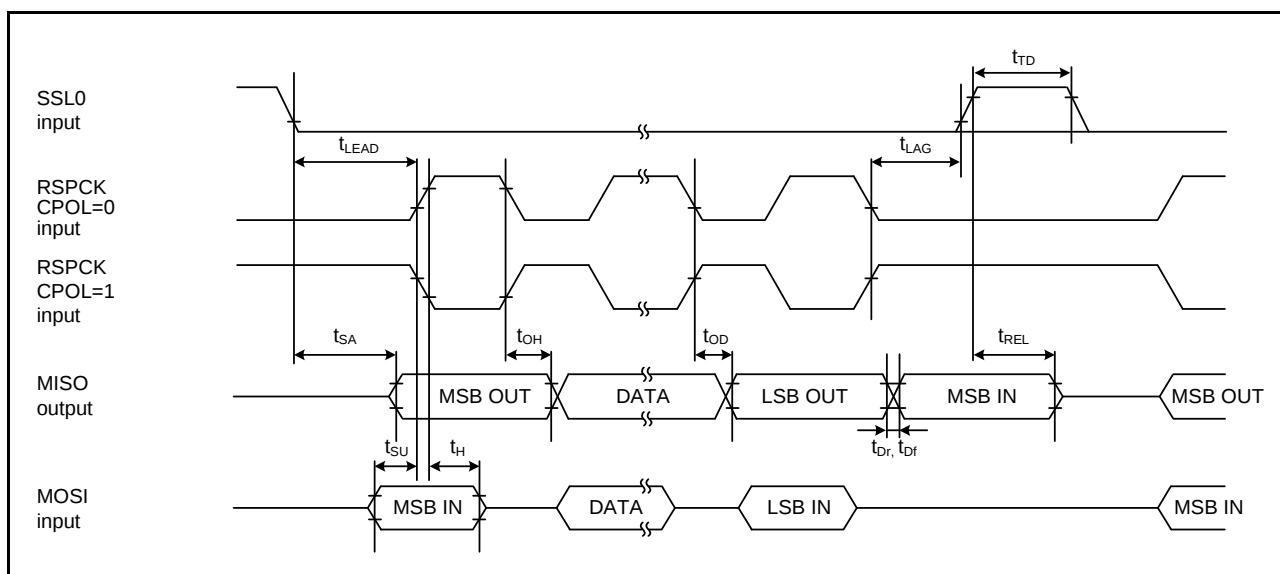


Figure 5.14 RSPI Timing (Slave, CPHA = 0)

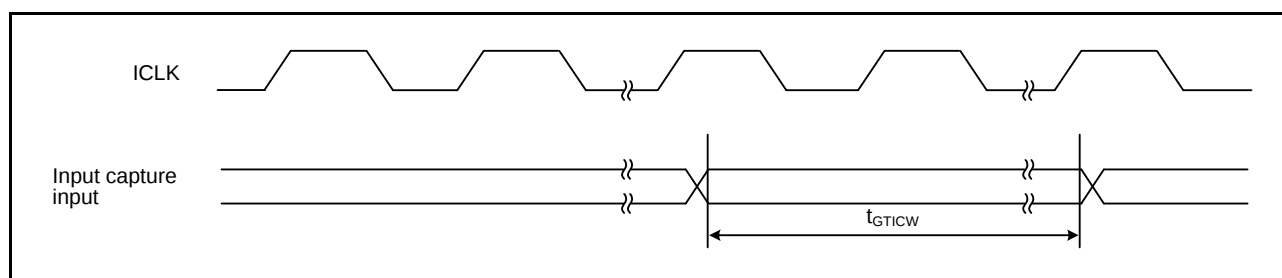


Figure 5.18 GPT Input/Output Timing

Table 5.13 Timing of On-Chip Peripheral Modules (5)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Max.	Unit	Test Conditions
POE3	POE# input pulse width	t _{POEW}	1.5	-	t _{Pcyc}	Figure 5.19

Note: • t_{Pcyc}: PCLK cycle

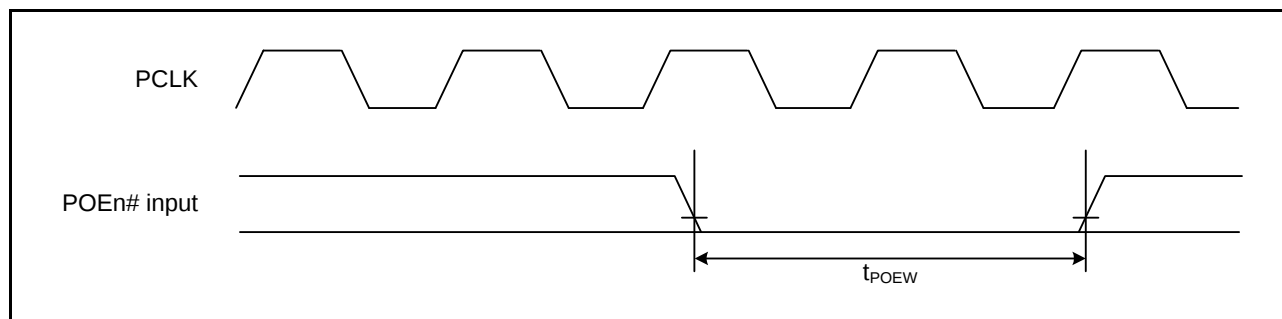


Figure 5.19 POE3# Clock Timing

5.3.4 Timing of PWM Delay Generation Circuit

Table 5.14 Timing of the PWM Delay Generation Circuit

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS = VREL0 = 0 V

AVCC = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Ta = Topr.

Item	Symbol	Typ.	Max.	Unit	Test Conditions
Resolution	—	312.5	—	ps	ICLK = 100 MHz
DNL *1	—	±2.0	—	LSB	

Note 1. This value is correct when the difference between each code and the next is a resolution of one bit (1 LSB).

Table 5.17 Characteristics of the Programmable Gain Amplifier

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog input capacitance		Cin	-	-	6	pF	
Input offset voltage		Voff	-	-	8	mV	
Input voltage range (Vin)	Gain × 2.000	Vin	0.050 × AVcc	-	0.450 × AVcc	V	
	Gain × 2.500		0.047 × AVcc	-	0.360 × AVcc		
	Gain × 3.077		0.045 × AVcc	-	0.292 × AVcc		
	Gain × 3.636		0.042 × AVcc	-	0.247 × AVcc		
	Gain × 4.000		0.040 × AVcc	-	0.212 × AVcc		
	Gain × 4.444		0.036 × AVcc	-	0.191 × AVcc		
	Gain × 5.000		0.033 × AVcc	-	0.170 × AVcc		
	Gain × 5.714		0.031 × AVcc	-	0.148 × AVcc		
	Gain × 6.667		0.029 × AVcc	-	0.127 × AVcc		
	Gain × 10.000		0.025 × AVcc	-	0.08 × AVcc		
	Gain × 13.333		0.023 × AVcc	-	0.06 × AVcc		
Slew rate		SR	10	-	-	V/μs	
Gain error	Gain × 2.000	-	-	-	1	%	
	Gain × 2.500		-	-	1		
	Gain × 3.077		-	-	1		
	Gain × 3.636		-	-	1.5		
	Gain × 4.000		-	-	1.5		
	Gain × 4.444		-	-	2		
	Gain × 5.000		-	-	2		
	Gain × 5.714		-	-	2		
	Gain × 6.667		-	-	3		
	Gain × 10.000		-	-	4		
	Gain × 13.333		-	-	4		