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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I ² C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 12x10b, 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562t7edfp-v3

Table 1.2 Functions of RX62T Group and RX62G Group Products (1 / 2)

Functions		RX62G Group		RX62T Group					
Pin number		112 Pins	100 Pins	112 Pins	100 Pins	80 Pins (R5F562T xGDFF)	80 Pins	64 Pins	
Data transfer	Data transfer controller (DTC)	√							
Interrupt controller (ICU)	Input on the NMI pin	√							
	Input on the IRQ pins	√ (8)						√ (4)	
Timers	Multi-function timer pulse unit 3 (MTU3)	√				√*1			
	General PWM timer (GPT)	—		√		√*1			
	General PWM timer (GPTa)	√		—					
	MTU3/GPT complementary PWM pin	12					6		
	Port output enable 3 (POE3)	√ (POE pins: 5)						√ (POE pins: 3)	
	Compare match timer (CMT)	√							
	Watchdog timer (WDT)	√							
	Independent watchdog timer (IWDT)	√							
Communication function	Serial communications interface (SCI)	√							
	I ² C bus interface (RIIC)	√							
	CAN module (CAN) (as an optional function)	√							
	LIN module (LIN)	√							
	Serial peripheral interface (RSPI)	√							
12-bit A/D converter (S12ADA)		√ (4 ch. x 2 units)							
	Simultaneous sampling on three channels	√ (2 units)							
	Programmable gain amplifier	√ (3 ch. x 2 units)							
	Window comparator	√ (3 ch. x 2 units)							
10-bit A/D converter (ADA)		√ (12 ch.)				√ (4 ch.)		—	
CRC calculator (CRC)		√							
I/O ports	I/O pins	61	55	61	55	44	44	37	
	Input pins	21	21	21	21	13	13	9	

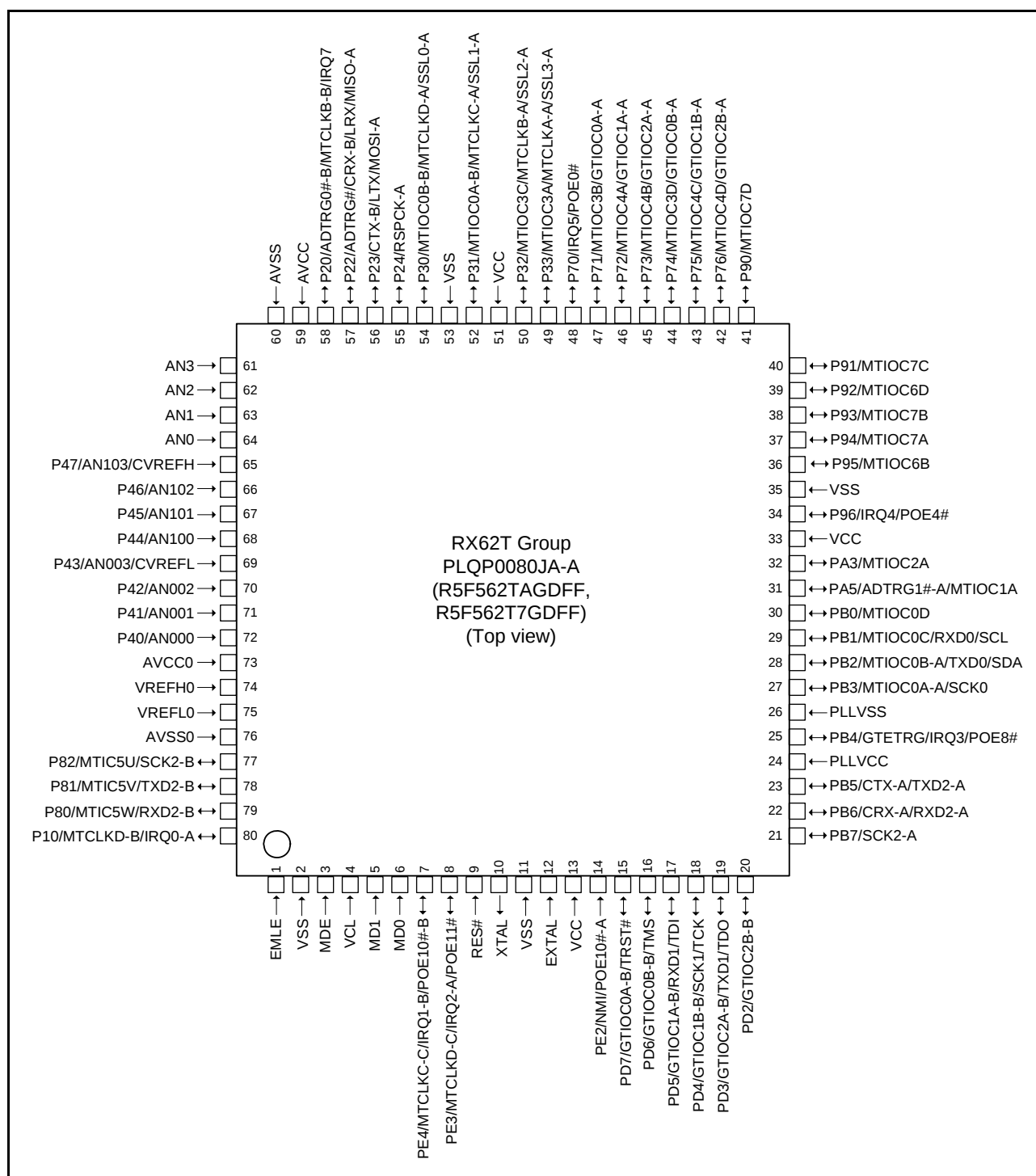


Figure 1.6 Pin Assignment of the 80-Pin LQFP (Two-Motor Control Supported Version)

Table 1.6 List of Pins and Pin Functions (80-Pin LQFP) (3 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi- cation	Interrupt	POE	Debugging
76	AVSS0							
77		P11		MTCLKC-B		IRQ1-A		
78		P10		MTCLKD-B		IRQ0-A		
79		PA5	ADTRG1#-A	MTIOC1A	MISO-B			
80		PA4	ADTRG0#-A	MTIOC1B	RSPCK-B			

Table 1.7 List of Pins and Pin Functions (80-Pin LQFP: R5F562TxGDFF) (3 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communication	Interrupt	POE	Debugging
76	AVSS0							
77		P82		MTIC5U	SCK2-B			
78		P81		MTIC5V	TXD2-B			
79		P80		MTIC5W	RXD2-B			
80		P10		MTCLKD-B		IRQ0-A		

Table 1.8 List of Pins and Pin Functions (64-Pin LQFP) (1 / 2)

Pin No. (64-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi- cation	Interrupt	POE	Debuggi ng
1	EMLE							
2	MDE							
3	VCL							
4	MD1							
5	MD0							
6	RES#							
7	XTAL							
8	VSS							
9	EXTAL							
10	VCC							
11		PE2				NMI	POE10#-A	
12		PD7		GTIOC0A-B				TRST#
13		PD6		GTIOC0B-B				TMS
14		PD5		GTIOC1A-B	RXD1			TDI
15		PD4		GTIOC1B-B	SCK1			TCK
16		PD3		GTIOC2A-B	TXD1			TDO
17		PB7			SCK2-A			
18		PB6			CRX-A/ RXD2-A			
19		PB5			CTX-A/ TXD2-A			
20	PLLVC							
21		PB4		GTETR		IRQ3	POE8#	
22	PLLVSS							
23		PB3		MTIOC0A-A	SCK0			
24		PB2		MTIOC0B-A	TXD0/SDA			
25		PB1		MTIOC0C	RXD0/SCL			
26		PB0		MTIOC0D	MOSI-B			
27		PA3		MTIOC2A	SSL0-B			
28		PA2		MTIOC2B	SSL1-B			
29		P94		MTIOC7A				
30		P93		MTIOC7B				
31		P92		MTIOC6D				
32		P91		MTIOC7C				
33		P76		MTIOC4D/ GTIOC2B-A				
34		P75		MTIOC4C/ GTIOC1B-A				
35		P74		MTIOC3D/ GTIOC0B-A				
36		P73		MTIOC4B/ GTIOC2A-A				
37		P72		MTIOC4A/ GTIOC1A-A				
38		P71		MTIOC3B/ GTIOC0A-A				
39		P70				IRQ5	POE0#	

Table 1.9 Pin Functions (2 / 4)

Classifications	Pin Name	I/O	Description
Multi-function timer pulse unit 3 (MTU3)	MTIOC0A-A/MTIOC0A-B MTIOC0B-A/MTIOC0B-B MTIOC0C, MTIOC0D	I/O	The MTU0.TGRA to MTU0.TGRD input capture input/output compare output/PWM output pins.
	MTIOC1A, MTIOC1B	I/O	The MTU1.TGRA and MTU1.TGRB input capture input/output compare output/PWM output pins.
	MTIOC2A, MTIOC2B	I/O	The MTU2.TGRA and MTU2.TGRB input capture input/output compare output/PWM output pins.
	MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D	I/O	The MTU3.TGRA and MTU3.TGRD input capture input/output compare output/PWM output pins. Pins MTIOC3B and MTIOC3D can be used for large-current output.
	MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D	I/O	The MTU4.TGRA and MTU4.TGRD input capture input/output compare output/PWM output pins. These pins can be used for large-current output.
	MTIC5U, MTIC5V, MTIC5W	Input	The MTU5.TGRU, MTU5.TGRV, and MTU5.TGRW input capture input/dead time compensation input pins. Not included in the 80-/64-pin versions.
	MTIOC6A, MTIOC6B MTIOC6C, MTIOC6D	I/O	The MTU6.TGRA to MTU6.TGRD input capture input/output compare output/PWM output pins. Pins MTIOC6B and MTIOC6D can be used for large-current output. The MTIOC6A/MTIOC6C pin is not included in the 80-pin version. The MTIOC6A/MTIOC6B/MTIOC6C pin is not included in the 64-pin version.
	MTIOC7A, MTIOC7B MTIOC7C, MTIOC7D	I/O	The MTU7.TGRA to MTU7.TGRD input capture input/output compare output/PWM output pins. These pins can be used for large-current output. The MTIOC7D pin is not included in the 80-/64-pin versions.
General PWM timer (GPT)	MTCLKA-A/MTCLKA-B MTCLKB-A/MTCLKB-B MTCLKC-A/MTCLKC-B/ MTCLKC-C MTCLKD-A/MTCLKD-B/ MTCLKD-C	Input	Input pins for external clock signals. The MTCLKA-B/MTCLKB-B/MTCLKC-C/MTCLKD-C pin is not included in the 64-pin version.
	GTIOC0A-A/GTIOC0A-B GTIOC0B-A/GTIOC0B-B	I/O	The GPT0.GTCCRA and GPT0.GTCCRB CCRB input capture input/output compare output/PWM output pins. Pins GTIOC0A-A and GTIOC0B-A can be used for large-current output.
	GTIOC1A-A/GTIOC1A-B GTIOC1B-A/GTIOC1B-B	I/O	The GPT1.GTCCRA and GPT1.GTCCRB input capture input/output compare output/PWM output pins. Pins GTIOC1A-A and GTIOC1B-A can be used for large-current output.
	GTIOC2A-A/GTIOC2A-B GTIOC2B-A/GTIOC2B-B	I/O	The GPT2.GTCCRA and GPT2.GTCCRB input capture input/output compare output/PWM output pins. Pins GTIOC2A-A and GTIOC2B-A can be used for large-current output. The GTIOC2B-B pin is not included in the 80-pin version.
	GTIOC3A, GTIOC3B	I/O	The GPT3.GTCCRA and GPT3.GTCCRB input capture input/output compare output/PWM output pins. Not included in the 80-/64-pin versions.
Port output enable 3 (POE3)	GTETRG	Input	External trigger input pin for the GPT
	POE0#, POE4#, POE8# POE10#-A/POE10#-B POE11#	Input	Input pins for request signals to place the MTU3 and GPT large-current pins in the high impedance state. The POE4#/ POE10#-B/POE11# pin is not included in the 64-pin version.
Watchdog timer (WDT)	WDTOVF#	Output	Output pin for the counter-overflow signal in watchdog-timer mode. Not included in the 100-/80-/64-pin versions.

Table 1.9 Pin Functions (3 / 4)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCIb)	TXD0, TXD1, TXD2-A/TXD2-B	Output	Output pins for data transmission. The TXD2-B pin is not included in the 80-/64-pin versions.
	RXD0, RXD1, RXD2-A/RXD2-B	Input	Input pins for data reception. The RXD2-B pin is not included in the 80-/64-pin versions.
	SCK0, SCK1, SCK2-A/SCK2-B	I/O	Input/output pins for clock signals. The SCK2-B pin is not included in the 80-/64-pin versions.
I ² C bus interface (RIIC)	SCL	I/O	Input/output pin for I ² C bus interface clocks. Bus can be directly driven by the NMOS open drain output.
	SDA	I/O	Input/output pin for I ² C bus interface data. Bus can be directly driven by the NMOS open drain output.
CAN module (CAN) (as an optional function)	CRX-A/CRX-B/CRX-C	Input	Input pin for the CAN. The CRX-C pin is not included in the 64-pin version.
	CTX-A/CTX-B/CTX-C	Output	Output pin for the CAN. The CTX-C pin is not included in the 64-pin version.
LIN module (LIN)	LRX	Input	Input pin for the LIN.
	LTX	Output	Output pin for the LIN.
Serial peripheral interface (RSPI)	RSPCK-A/RSPCK-B/RSPCK-C	I/O	Clock input/output pin for the RSPI. The RSPCK-C pin is not included in the 80-/64-pin versions.
	MOSI-A/MOSI-B/MOSI-C	I/O	Inputs or outputs data output from the master for the RSPI. The MOSI-C pin is not included in the 80-/64-pin versions.
	MISO-A/MISO-B/MISO-C	I/O	Inputs or outputs data output from the slave for the RSPI. The MISO-C pin is not included in the 80-/64-pin versions.
	SSL0-A/SSL0-B/SSL0-C	I/O	Select the slave for the RSPI. The SSL0-C/SSL1-C/SSL2-C/SSL3-C pin is not included in the 80-/64-pin versions.
	SSL1-A/SSL1-B/SSL1-C SSL2-A/SSL2-B/SSL2-C SSL3-A/SSL3-B/SSL3-C	Output	
A/D converter	AN000 to AN003 AN100 to AN103	Input	Input pins for the analog signals to be processed by the 12-bit A/D converter.
	AN0 to AN11	Input	Input pins for the analog signals to be processed by the 10-bit A/D converter. The AN4 to AN11 pins are not included in the 80-pin version. Not included in the 64-pin version.
	ADTRG0#-A/ADTRG0#-B ADTRG1#-A/ADTRG1#-B ADTRG#	Input	Input pins for the external trigger signals that start the A/D conversion. The ADTRG0#-B/ADTRG1#-B/ADTRG# pin is not included in the 64-pin version.
	CVREFH	Input	Input pin for the high-level reference voltage to the comparator
	CVREFL	Input	Input pin for the low-level reference voltage to the comparator
Analog power supply	AVCC0	Input	Analog power supply pin for the 12-bit A/D converter. When the A/D converter is not in use, connect this pin to the system power supply.
	AVSS0	Input	Ground pin for the 12-bit A/D converter. Connect this pin to the system power supply (0 V).
	VREFH0	Input	Reference power supply pin for the 12-bit A/D converter. When the 12-bit A/D converter is not in use, connect this pin to the system power supply.
	VREFL0	Input	Ground pin of the reference power supply pin for the 12-bit A/D converter. When the 12-bit A/D converter is not in use, connect this pin to the system power supply (0 V).
	AVCC	Input	Analog power supply pin for the 10-bit A/D converter. When the A/D converter is not in use, connect this pin to the system power supply. Not included in the 64-pin version.
	AVSS	Input	Ground pin for the 10-bit A/D converter. Connect this pin to the system power supply (0 V). Not included in the 64-pin version.
	VREF	Input	Reference power supply pin for the 10-bit A/D converter. When the 10-bit A/D converter is not in use, connect this pin to the system power supply. Not included in the 80-/64-pin versions.

Table 4.1 List of I/O Registers (Address Order) (7 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 7305h	ICU	Interrupt source priority register 05	IPR05	8	8	2 ICLK
0008 7306h	ICU	Interrupt source priority register 06	IPR06	8	8	2 ICLK
0008 7307h	ICU	Interrupt source priority register 07	IPR07	8	8	2 ICLK
0008 7314h	ICU	Interrupt source priority register 14	IPR14	8	8	2 ICLK
0008 7318h	ICU	Interrupt source priority register 18	IPR18	8	8	2 ICLK
0008 7320h	ICU	Interrupt source priority register 20	IPR20	8	8	2 ICLK
0008 7321h	ICU	Interrupt source priority register 21	IPR21	8	8	2 ICLK
0008 7322h	ICU	Interrupt source priority register 22	IPR22	8	8	2 ICLK
0008 7323h	ICU	Interrupt source priority register 23	IPR23	8	8	2 ICLK
0008 7324h	ICU	Interrupt source priority register 24	IPR24	8	8	2 ICLK
0008 7325h	ICU	Interrupt source priority register 25	IPR25	8	8	2 ICLK
0008 7326h	ICU	Interrupt source priority register 26	IPR26	8	8	2 ICLK
0008 7327h	ICU	Interrupt source priority register 27	IPR27	8	8	2 ICLK
0008 7340h	ICU	Interrupt source priority register 40	IPR40	8	8	2 ICLK
0008 7344h	ICU	Interrupt source priority register 44	IPR44	8	8	2 ICLK
0008 7348h	ICU	Interrupt source priority register 48	IPR48	8	8	2 ICLK
0008 7349h	ICU	Interrupt source priority register 49	IPR49	8	8	2 ICLK
0008 7351h	ICU	Interrupt source priority register 51	IPR51	8	8	2 ICLK
0008 7352h	ICU	Interrupt source priority register 52	IPR52	8	8	2 ICLK
0008 7353h	ICU	Interrupt source priority register 53	IPR53	8	8	2 ICLK
0008 7354h	ICU	Interrupt source priority register 54	IPR54	8	8	2 ICLK
0008 7355h	ICU	Interrupt source priority register 55	IPR55	8	8	2 ICLK
0008 7356h	ICU	Interrupt source priority register 56	IPR56	8	8	2 ICLK
0008 7357h	ICU	Interrupt source priority register 57	IPR57	8	8	2 ICLK
0008 7358h	ICU	Interrupt source priority register 58	IPR58	8	8	2 ICLK
0008 7359h	ICU	Interrupt source priority register 59	IPR59	8	8	2 ICLK
0008 735Ah	ICU	Interrupt source priority register 5A	IPR5A	8	8	2 ICLK
0008 735Bh	ICU	Interrupt source priority register 5B	IPR5B	8	8	2 ICLK
0008 735Ch	ICU	Interrupt source priority register 5C	IPR5C	8	8	2 ICLK
0008 735Dh	ICU	Interrupt source priority register 5D	IPR5D	8	8	2 ICLK
0008 735Eh	ICU	Interrupt source priority register 5E	IPR5E	8	8	2 ICLK
0008 735Fh	ICU	Interrupt source priority register 5F	IPR5F	8	8	2 ICLK
0008 7360h	ICU	Interrupt source priority register 60	IPR60	8	8	2 ICLK
0008 7367h	ICU	Interrupt source priority register 67	IPR67	8	8	2 ICLK
0008 7368h	ICU	Interrupt source priority register 68	IPR68	8	8	2 ICLK
0008 7369h	ICU	Interrupt source priority register 69	IPR69	8	8	2 ICLK
0008 736Ah	ICU	Interrupt source priority register 6A	IPR6A	8	8	2 ICLK
0008 736Bh	ICU	Interrupt source priority register 6B	IPR6B	8	8	2 ICLK
0008 736Ch	ICU	Interrupt source priority register 6C	IPR6C	8	8	2 ICLK
0008 736Dh	ICU	Interrupt source priority register 6D	IPR6D	8	8	2 ICLK
0008 736Eh	ICU	Interrupt source priority register 6E	IPR6E	8	8	2 ICLK
0008 736Fh	ICU	Interrupt source priority register 6F	IPR6F	8	8	2 ICLK
0008 7380h	ICU	Interrupt source priority register 80	IPR80	8	8	2 ICLK
0008 7381h	ICU	Interrupt source priority register 81	IPR81	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (10 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 8250h	SCI2	Serial mode register	SMR ^{*1}	8	8	2, 3 PCLK ^{*3}
0008 8251h	SCI2	Bit rate register	BRR	8	8	2, 3 PCLK ^{*3}
0008 8252h	SCI2	Serial control register	SCR ^{*1}	8	8	2, 3 PCLK ^{*3}
0008 8253h	SCI2	Transmit data register	TDR	8	8	2, 3 PCLK ^{*3}
0008 8254h	SCI2	Serial status register	SSR ^{*1}	8	8	2, 3 PCLK ^{*3}
0008 8255h	SCI2	Receive data register	RDR	8	8	2, 3 PCLK ^{*3}
0008 8256h	SCI2	Smart card mode register	SCMR	8	8	2, 3 PCLK ^{*3}
0008 8257h	SCI2	Serial extended mode register	SEMR	8	8	2, 3 PCLK ^{*3}
0008 8250h	SMCI2	Serial mode register	SMR ^{*1}	8	8	2, 3 PCLK ^{*3}
0008 8251h	SMCI2	Bit rate register	BRR	8	8	2, 3 PCLK ^{*3}
0008 8252h	SMCI2	Serial control register	SCR ^{*1}	8	8	2, 3 PCLK ^{*3}
0008 8253h	SMCI2	Transmit data register	TDR	8	8	2, 3 PCLK ^{*3}
0008 8254h	SMCI2	Serial status register	SSR ^{*1}	8	8	2, 3 PCLK ^{*3}
0008 8255h	SMCI2	Receive data register	RDR	8	8	2, 3 PCLK ^{*3}
0008 8256h	SMCI2	Smart card mode register	SCMR	8	8	2, 3 PCLK ^{*3}
0008 8280h	CRC	CRC control register	CRCCR	8	8	2, 3 PCLK ^{*3}
0008 8281h	CRC	CRC data input register	CRCDIR	8	8	2, 3 PCLK ^{*3}
0008 8282h	CRC	CRC data output register	CRCDOR	16	16	2, 3 PCLK ^{*3}
0008 8300h	RIIC	I ² C bus control register 1	ICCR1	8	8	2, 3 PCLK ^{*3}
0008 8301h	RIIC	I ² C bus control register 2	ICCR2	8	8	2, 3 PCLK ^{*3}
0008 8302h	RIIC	I ² C bus mode register 1	ICMR1	8	8	2, 3 PCLK ^{*3}
0008 8303h	RIIC	I ² C bus mode register 2	ICMR2	8	8	2, 3 PCLK ^{*3}
0008 8304h	RIIC	I ² C bus mode register 3	ICMR3	8	8	2, 3 PCLK ^{*3}
0008 8305h	RIIC	I ² C bus function enable register	ICFER	8	8	2, 3 PCLK ^{*3}
0008 8306h	RIIC	I ² C bus status enable register	ICSER	8	8	2, 3 PCLK ^{*3}
0008 8307h	RIIC	I ² C bus interrupt enable register	ICIER	8	8	2, 3 PCLK ^{*3}
0008 8308h	RIIC	I ² C bus status register 1	ICSR1	8	8	2, 3 PCLK ^{*3}
0008 8309h	RIIC	I ² C bus status register 2	ICSR2	8	8	2, 3 PCLK ^{*3}
0008 830Ah	RIIC	Slave address register L0	SARL0	8	8	2, 3 PCLK ^{*3}
0008 830Ah	RIIC	Internal counter L for timeout	TMOCNTL	8	8	2, 3 PCLK ^{*3}
0008 830Bh	RIIC	Slave address register U0	SARU0	8	8	2, 3 PCLK ^{*3}
0008 830Bh	RIIC	Internal counter U for timeout	TMOCNTU	8	8	2, 3 PCLK ^{*3}
0008 830Bh	RIIC	Slave address register U0	SARU0	8	8	2, 3 PCLK ^{*3}
0008 830Ch	RIIC	Slave address register L1	SARL1	8	8	2, 3 PCLK ^{*3}
0008 830Dh	RIIC	Slave address register U1	SARU1	8	8	2, 3 PCLK ^{*3}
0008 830Eh	RIIC	Slave address register L2	SARL2	8	8	2, 3 PCLK ^{*3}
0008 830Fh	RIIC	Slave address register U2	SARU2	8	8	2, 3 PCLK ^{*3}
0008 8310h	RIIC	I ² C bus bit rate low-level register	ICBRL	8	8	2, 3 PCLK ^{*3}
0008 8311h	RIIC	I ² C bus bit rate high-level register	ICBRH	8	8	2, 3 PCLK ^{*3}
0008 8312h	RIIC	I ² C bus transmit data register	ICDRT	8	8	2, 3 PCLK ^{*3}
0008 8313h	RIIC	I ² C bus receive data register	ICDRR	8	8	2, 3 PCLK ^{*3}
0008 8380h	RSPI	RSPI control register	SPCR	8	8	2, 3 PCLK ^{*3}
0008 8381h	RSPI	RSPI slave select polarity register	SSLP	8	8	2, 3 PCLK ^{*3}
0008 8382h	RSPI	RSPI pin control register	SPPCR	8	8	2, 3 PCLK ^{*3}

Table 4.1 List of I/O Registers (Address Order) (12 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 90A4h	S12AD1	A/D data register 2	ADDR2	16	16	2, 3 PCLK* ³
0008 90A6h	S12AD1	A/D data register 3	ADDR3	16	16	2, 3 PCLK* ³
0008 90B0h	S12AD1	A/D data register 0B	ADDR0B	16	16	2, 3 PCLK* ³
0008 90E0h	S12AD1	A/D sampling state register	ADSSTR	8	8	2, 3 PCLK* ³
0008 C001h	PORT1	Data direction register	DDR	8	8	2, 3 PCLK* ³
0008 C002h	PORT2	Data direction register	DDR	8	8	2, 3 PCLK* ³
0008 C003h	PORT3	Data direction register	DDR	8	8	2, 3 PCLK* ³
0008 C007h	PORT7	Data direction register	DDR	8	8	2, 3 PCLK* ³
0008 C008h	PORT8	Data direction register	DDR	8	8	2, 3 PCLK* ³
0008 C009h	PORT9	Data direction register	DDR	8	8	2, 3 PCLK* ³
0008 C00Ah	PORTA	Data direction register	DDR	8	8	2, 3 PCLK* ³
0008 C00Bh	PORTB	Data direction register	DDR	8	8	2, 3 PCLK* ³
0008 C00Dh	PORTD	Data direction register	DDR	8	8	2, 3 PCLK* ³
0008 C00Eh	PORTE	Data direction register	DDR	8	8	2, 3 PCLK* ³
0008 C010h	PORTG	Data direction register	DDR* ¹	8	8	2, 3 PCLK* ³
0008 C021h	PORT1	Data register	DR	8	8	2, 3 PCLK* ³
0008 C022h	PORT2	Data register	DR	8	8	2, 3 PCLK* ³
0008 C023h	PORT3	Data register	DR	8	8	2, 3 PCLK* ³
0008 C027h	PORT7	Data register	DR	8	8	2, 3 PCLK* ³
0008 C028h	PORT8	Data register	DR	8	8	2, 3 PCLK* ³
0008 C029h	PORT9	Data register	DR	8	8	2, 3 PCLK* ³
0008 C02Ah	PORTA	Data register	DR	8	8	2, 3 PCLK* ³
0008 C02Bh	PORTB	Data register	DR	8	8	2, 3 PCLK* ³
0008 C02Dh	PORTD	Data register	DR	8	8	2, 3 PCLK* ³
0008 C02Eh	PORTE	Data register	DR	8	8	2, 3 PCLK* ³
0008 C030h	PORTG	Data register	DR* ¹	8	8	2, 3 PCLK* ³
0008 C041h	PORT1	Data register	PORT	8	8	2, 3 PCLK* ³
0008 C042h	PORT2	Data register	PORT	8	8	2, 3 PCLK* ³
0008 C043h	PORT3	Data register	PORT	8	8	2, 3 PCLK* ³
0008 C044h	PORT4	Data register	PORT	8	8	2, 3 PCLK* ³
0008 C045h	PORT5	Data register	PORT	8	8	2, 3 PCLK* ³
0008 C046h	PORT6	Data register	PORT	8	8	2, 3 PCLK* ³
0008 C047h	PORT7	Data register	PORT	8	8	2, 3 PCLK* ³
0008 C048h	PORT8	Data register	PORT	8	8	2, 3 PCLK* ³
0008 C049h	PORT9	Data register	PORT	8	8	2, 3 PCLK* ³
0008 C04Ah	PORTA	Data register	PORT	8	8	2, 3 PCLK* ³
0008 C04Bh	PORTB	Data register	PORT	8	8	2, 3 PCLK* ³
0008 C04Dh	PORTD	Data register	PORT	8	8	2, 3 PCLK* ³
0008 C04Eh	PORTE	Data register	PORT	8	8	2, 3 PCLK* ³
0008 C050h	PORTG	Port register	PORT* ¹	8	8	2, 3 PCLK* ³
0008 C061h	PORT1	Input buffer control register	ICR	8	8	2, 3 PCLK* ³
0008 C062h	PORT2	Input buffer control register	ICR	8	8	2, 3 PCLK* ³
0008 C063h	PORT3	Input buffer control register	ICR	8	8	2, 3 PCLK* ³
0008 C064h	PORT4	Input buffer control register	ICR	8	8	2, 3 PCLK* ³

Table 4.1 List of I/O Registers (Address Order) (18 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000C 1390h	MTU1	Timer input capture control register	TICCR	8	8	5 ICLK
000C 1400h	MTU2	Timer control register	TCR	8	8, 16	5 ICLK
000C 1401h	MTU2	Timer mode register 1	TMDR1	8	8	5 ICLK
000C 1402h	MTU2	Timer I/O control register	TIOR	8	8	5 ICLK
000C 1404h	MTU2	Timer interrupt enable register	TIER	8	8, 16, 32	5 ICLK
000C 1405h	MTU2	Timer status register	TSR	8	8	5 ICLK
000C 1406h	MTU2	Timer counter	TCNT	16	16	5 ICLK
000C 1408h	MTU2	Timer general register A	TGRA	16	16, 32	5 ICLK
000C 140Ah	MTU2	Timer general register B	TGRB	16	16	5 ICLK
000C 1A00h	MTU6	Timer control register	TCR	8	8, 16, 32	5 ICLK
000C 1A01h	MTU7	Timer control register	TCR	8	8	5 ICLK
000C 1A02h	MTU6	Timer mode register 1	TMDR1	8	8, 16	5 ICLK
000C 1A03h	MTU7	Timer mode register 1	TMDR1	8	8	5 ICLK
000C 1A04h	MTU6	Timer I/O control register H	TIORH	8	8, 16, 32	5 ICLK
000C 1A05h	MTU6	Timer I/O control register L	TIORL	8	8	5 ICLK
000C 1A06h	MTU7	Timer I/O control register H	TIORH	8	8, 16	5 ICLK
000C 1A07h	MTU7	Timer I/O control register L	TIORL	8	8	5 ICLK
000C 1A08h	MTU6	Timer interrupt enable register	TIER	8	8, 16	5 ICLK
000C 1A09h	MTU7	Timer interrupt enable register	TIER	8	8	5 ICLK
000C 1A0Ah	MTU	Timer output master enable register B	TOERB	8	8	5 ICLK
000C 1A0Eh	MTU	Timer output control register 1B	TOCR1B	8	8, 16	5 ICLK
000C 1A0Fh	MTU	Timer output control register 2B	TOCR2B	8	8	5 ICLK
000C 1A10h	MTU6	Timer counter	TCNT	16	16, 32	5 ICLK
000C 1A12h	MTU7	Timer counter	TCNT	16	16	5 ICLK
000C 1A14h	MTU	Timer cycle data register B	TCDRB	16	16, 32	5 ICLK
000C 1A16h	MTU	Timer dead time data register B	TDDRB	16	16	5 ICLK
000C 1A18h	MTU6	Timer general register A	TGRA	16	16, 32	5 ICLK
000C 1A1Ah	MTU6	Timer general register B	TGRB	16	16	5 ICLK
000C 1A1Ch	MTU7	Timer general register A	TGRA	16	16, 32	5 ICLK
000C 1A1Eh	MTU7	Timer general register B	TGRB	16	16	5 ICLK
000C 1A20h	MTU	Timer subcounter B	TCNTSB	16	16, 32	5 ICLK
000C 1A22h	MTU	Timer cycle buffer register B	TCBRB	16	16	5 ICLK
000C 1A24h	MTU6	Timer general register C	TGRC	16	16, 32	5 ICLK
000C 1A26h	MTU6	Timer general register D	TGRD	16	16	5 ICLK
000C 1A28h	MTU7	Timer general register C	TGRC	16	16, 32	5 ICLK
000C 1A2Ah	MTU7	Timer general register D	TGRD	16	16	5 ICLK
000C 1A2Ch	MTU6	Timer status register	TSR	8	8, 16	5 ICLK
000C 1A2Dh	MTU7	Timer status register	TSR	8	8	5 ICLK
000C 1A30h	MTU	Timer interrupt skipping set register 1B	TITCR1B	8	8, 16	5 ICLK
000C 1A31h	MTU	Timer interrupt skipping counter 1B	TITCNT1B	8	8	5 ICLK
000C 1A32h	MTU	Timer buffer transfer set register B	TBTERB	8	8	5 ICLK
000C 1A34h	MTU	Timer dead time enable register B	TDERB	8	8	5 ICLK
000C 1A36h	MTU	Timer output level buffer register B	TOLBRB	8	8	5 ICLK
000C 1A38h	MTU6	Timer buffer operation transfer mode register	TBTM	8	8, 16	5 ICLK

Table 4.1 List of I/O Registers (Address Order) (20 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000C 200Ah	GPT	General PWM timer hardware stop/clear source select register	GTHPSR	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 200Ch	GPT	General PWM timer write-protection register	GTWP	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 200Eh	GPT	General PWM timer sync register	GTSYNC	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2010h	GPT	General PWM timer external trigger input interrupt register	GTETINT	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2014h	GPT	General PWM timer buffer operation disable register	GTBDR	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2018h	GPT	General PWM timer start write protection register	GTSWP	16	16, 32	3 to 5 ICLK ^{*4}
000C 2080h	GPT	LOCO count control register	LCCR	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2082h	GPT	LOCO count status register	LCST	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2084h	GPT	LOCO count value register	LCNT	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2086h	GPT	LOCO count result average register	LCNTA	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2088h	GPT	LOCO count result register 0	LCNT00	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 208Ah	GPT	LOCO count result register 1	LCNT01	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 208Ch	GPT	LOCO count result register 2	LCNT02	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 208Eh	GPT	LOCO count result register 3	LCNT03	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2090h	GPT	LOCO count result register 4	LCNT04	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2092h	GPT	LOCO count result register 5	LCNT05	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2094h	GPT	LOCO count result register 6	LCNT06	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2096h	GPT	LOCO count result register 7	LCNT07	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2098h	GPT	LOCO count result register 8	LCNT08	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 209Ah	GPT	LOCO count result register 9	LCNT09	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 209Ch	GPT	LOCO count result register 10	LCNT10	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 209Eh	GPT	LOCO count result register 11	LCNT11	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 20A0h	GPT	LOCO count result register 12	LCNT12	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 20A2h	GPT	LOCO count result register 13	LCNT13	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 20A4h	GPT	LOCO count result register 14	LCNT14	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 20A6h	GPT	LOCO count result register 15	LCNT15	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 20A8h	GPT	LOCO count upper permissible deviation register	LCNTDU	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 20AAh	GPT	LOCO count lower permissible deviation register	LCNTDL	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2100h	GPT0	General PWM timer I/O control register	GTIOR	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2102h	GPT0	General PWM timer interrupt output setting register	GTINTAD	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2104h	GPT0	General PWM timer control register	GTCR	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2106h	GPT0	General PWM timer buffer enable register	GTBER	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 2108h	GPT0	General PWM timer count direction register	GTUDC	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 210Ah	GPT0	General PWM timer interrupt and A/D converter start request skipping setting register	GTITC	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 210Ch	GPT0	General PWM timer status register	GTST	16	8, 16, 32	3 to 5 ICLK ^{*4}
000C 210Eh	GPT0	General PWM timer counter	GTCNT	16	16	3 to 5 ICLK ^{*4}
000C 2110h	GPT0	General PWM timer compare capture register A	GTCCRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 2112h	GPT0	General PWM timer compare capture register B	GTCCRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2114h	GPT0	General PWM timer compare capture register C	GTCCRC	16	16, 32	3 to 5 ICLK ^{*4}

Table 4.1 List of I/O Registers (Address Order) (24 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000C 22B6h	GPT3	General PWM timer dead time control register	GTDTCCR	16	16, 32	3 to 5 ICLK ^{*4}
000C 22B8h	GPT3	General PWM timer dead time value register	GTDVU	16	16, 32	3 to 5 ICLK ^{*4}
000C 22BAh	GPT3	General PWM timer dead time value register	GTDVD	16	16, 32	3 to 5 ICLK ^{*4}
000C 22BCh	GPT3	General PWM timer dead time buffer register	GTDBU	16	16, 32	3 to 5 ICLK ^{*4}
000C 22BEh	GPT3	General PWM timer dead time buffer register	GTDBD	16	16, 32	3 to 5 ICLK ^{*4}
000C 22C0h	GPT3	General PWM timer output protection function status register	GTSOS	16	16, 32	3 to 5 ICLK ^{*4}
000C 22C2h	GPT3	General PWM timer output protection temporary release register	GTSOTR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2300h	GPT0	PWM output delay control register	GTDLYCR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2302h	GPT1	PWM output delay control register	GTDLYCR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2304h	GPT2	PWM output delay control register	GTDLYCR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2306h	GPT3	PWM output delay control register	GTDLYCR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2318h	GPT0	GTIOCA rising output delay register	GTDLYRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 231Ah	GPT0	GTIOCB rising output delay register	GTDLYRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 231Ch	GPT1	GTIOCA rising output delay register	GTDLYRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 231Eh	GPT1	GTIOCB rising output delay register	GTDLYRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2320h	GPT2	GTIOCA rising output delay register	GTDLYRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 2322h	GPT2	GTIOCB rising output delay register	GTDLYRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2324h	GPT3	GTIOCA falling output delay register	GTDLYRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 2326h	GPT3	GTIOCB falling output delay register	GTDLYRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2328h	GPT0	GTIOCA falling output delay register	GTDLYFA	16	16, 32	3 to 5 ICLK ^{*4}
000C 232Ah	GPT0	GTIOCB falling output delay register	GTDLYFB	16	16, 32	3 to 5 ICLK ^{*4}
000C 232Ch	GPT1	GTIOCA falling output delay register	GTDLYFA	16	16, 32	3 to 5 ICLK ^{*4}
000C 232Eh	GPT1	GTIOCB falling output delay register	GTDLYFB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2330h	GPT2	GTIOCA falling output delay register	GTDLYFA	16	16, 32	3 to 5 ICLK ^{*4}
000C 2332h	GPT2	GTIOCB falling output delay register	GTDLYFB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2334h	GPT3	GTIOCA falling output delay register	GTDLYFA	16	16, 32	3 to 5 ICLK ^{*4}
000C 2336h	GPT3	GTIOCB falling output delay register	GTDLYFB	16	16, 32	3 to 5 ICLK ^{*4}
007F C402h	FLASH	Flash mode register	FMODR	8	8	2, 3 PCLK ^{*3}
007F C410h	FLASH	Flash access status register	FASTAT	8	8	2, 3 PCLK ^{*3}
007F C411h	FLASH	Flash access error interrupt enable register	FAEINT	8	8	2, 3 PCLK ^{*3}
007F C412h	FLASH	Flash ready interrupt enable register	FRDYIE	8	8	2, 3 PCLK ^{*3}
007F C440h	FLASH	Data flash read enable register 0	DFLRE0	16	16	2, 3 PCLK ^{*3}
007F C442h	FLASH	Data flash read enable register 1	DFLRE1	16	16	2, 3 PCLK ^{*3}
007F C450h	FLASH	Data flash programming/erasure enable register 0	DFLWE0	16	16	2, 3 PCLK ^{*3}
007F C452h	FLASH	Data flash programming/erasure enable register 1	DFLWE1	16	16	2, 3 PCLK ^{*3}
007F C454h	FLASH	FCU RAM enable register	FCURAME	16	16	2, 3 PCLK ^{*3}
007F FFB0h	FLASH	Flash status register 0	FSTATR0	8	8	2, 3 PCLK ^{*3}
007F FFB1h	FLASH	Flash status register 1	FSTATR1	8	8	2, 3 PCLK ^{*3}
007F FFB2h	FLASH	Flash P/E mode entry register	FENTRYR	16	16	2, 3 PCLK ^{*3}
007F FFB4h	FLASH	Flash protect register	FPROTR	16	16	2, 3 PCLK ^{*3}
007F FFB6h	FLASH	Flash reset register	FRESETR	16	16	2, 3 PCLK ^{*3}

Table 4.2 List of I/O Registers (Bit Order) (23 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
GPT	GTBDR	BD33	BD32	BD31	BD30	BD23	BD22	BD21	BD20
		BD13	BD12	BD11	BD10	BD03	BD02	BD01	BD00
GPT	GTSWP	—	—	—	—	—	—	—	—
		—	—	—	—	SWP3	SWP2	SWP1	SWP0
GPT	LCCR	LPSC[1:0]		TPSC[1:0]		LCNTAT		LCTQ[2:0]	
		—	LCINTO	LCINTD	LCINTC	—	LCNTS	LCNTCR	LCNTE
GPT	LCST	—	—	—	—	—	—	—	—
		—	—	—	—	—	LISO	LISD	LISC
GPT	LCNTA								
GPT	LCNT00								
GPT	LCNT01								
GPT	LCNT02								
GPT	LCNT03								
GPT	LCNT04								
GPT	LCNT05								
GPT	LCNT06								
GPT	LCNT07								
GPT	LCNT08								
GPT	LCNT09								
GPT	LCNT10								
GPT	LCNT11								
GPT	LCNT12								
GPT	LCNT13								
GPT	LCNT14								
GPT	LCNT15								
GPT	LCNTDU								
GPT	LCNTDL								
GPT0	GTIOR	OBHLD	OBDFLT			GTIOB[5:0]			
		OAHL	OADFLT			GTIOA[5:0]			
GPT0	GTINTAD	ADTRBDEN	ADTRBUEN	ADTRADEN	ADTRAUEN	EINT	—	—	—
		GTINTPR[1:0]		GTINTF	GTINTE	GTINTD	GTINTC	GTINTB	GTINTA

Table 4.2 List of I/O Registers (Bit Order) (29 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
GPT2	GTDLYCR	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLYEN	DLYRST	DLEN
GPT3	GTDLYCR	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLYEN	DLYRST	DLEN
GPT0	GTDLYRA	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT0	GTDLYRB	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT1	GTDLYRA	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT1	GTDLYRB	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT2	GTDLYRA	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT2	GTDLYRB	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT3	GTDLYRA	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT3	GTDLYRB	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT0	GTDLYFA	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT0	GTDLYFB	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT1	GTDLYFA	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT1	GTDLYFB	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT2	GTDLYRA	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT2	GTDLYFB	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT3	GTDLYFA	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
GPT3	GTDLYFB	—	—	—	—	—	—	—	—
		—	—	—	—	—	DLY[4:0]	—	—
FLASH	FMODR	—	—	—	FRDMD	—	—	—	—
FLASH	FASTAT	ROMAE	—	—	CMDLK	DFLAE	—	DFLRPE	DFLWPE
FLASH	FAEINT	ROMAEIE	—	—	CMDLKIE	DFLAEIE	—	DFLRPEIE	DFLWPEIE
FLASH	FRDYIE	—	—	—	—	—	—	—	FRDYIE
FLASH	DFLRE0	KEY[7:0]							
		DBRE07	DBRE06	DBRE05	DBRE04	DBRE03	DBRE02	DBRE01	DBRE00
FLASH	DFLRE1	KEY[7:0]							
		DBRE15	DBRE14	DBRE13	DBRE12	DBRE11	DBRE10	DBRE09	DBRE08
FLASH	DFLWE0	KEY[7:0]							
		DBWE07	DBWE06	DBWE05	DBWE04	DBWE03	DBWE02	DBWE01	DBWE00
FLASH	DFLWE1	KEY[7:0]							
		DBWE15	DBWE14	DBWE13	DBWE12	DBWE11	DBWE10	DBWE09	DBWE08
FLASH	FCURAME	KEY[7:0]							
		—	—	—	—	—	—	—	FCRME

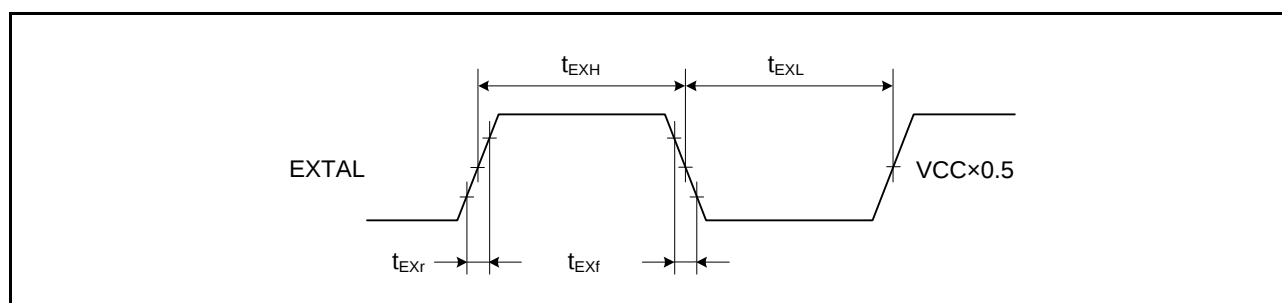


Figure 5.4 EXTAL External Input Clock Timing

5.4 A/D Conversion Characteristics

Table 5.15 10-Bit A/D Conversion Characteristics

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Ta = Topr

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	10	10	10	Bit	
Conversion time*1 (AD clock = 25-MHz operation)	2.0	-	-	μs	Sampling 25 states
Analog input capacitance	-	-	4	pF	
Integral nonlinearity error	-	-	±3.0	LSB	
Offset error	-	-	±3.0	LSB	
Full-scale error	-	-	±3.0	LSB	
Quantization error	-	±0.5	-	LSB	
Absolute accuracy	-	-	±4.0	LSB	
Permissible signal source impedance	-	-	1.0	kΩ	

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V

AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Ta = Topr. Ta is the same under conditions 2 and 3.

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	10	10	10	Bit	
Conversion time*1 (AD clock = 50-MHz operation)	1.0	-	-	μs	Sampling 25 states
Analog input capacitance	-	-	4	pF	
Integral nonlinearity error	-	-	±3.0	LSB	
Offset error	-	-	±3.0	LSB	
Full-scale error	-	-	±3.0	LSB	
Quantization error	-	±0.5	-	LSB	
Absolute accuracy	-	-	±4.0	LSB	
Permissible signal source impedance	-	-	1.0	kΩ	

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

5.5 Power-on Reset Circuit, Voltage Detection Circuit Characteristics

Table 5.19 Power-on Reset Circuit, Voltage Detection Circuit Characteristics

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: $V_{CC} = PLLVCC = 2.7$ to 3.6 V, $V_{SS} = PLLVSS = AVSS0 = AVSS = VREFL0 = 0$ V
 $AVCC0 = AVCC = 3.0$ to 3.6 V, $VREFH0 = 3.0$ V to $AVCC0$, $VREF = 3.0$ V to $AVCC$

Condition 2: $V_{CC} = PLLVCC = 2.7$ to 3.6 V, $V_{SS} = PLLVSS = AVSS0 = AVSS = VREFL0 = 0$ V
 $AVCC0 = AVCC = 4.0$ to 5.5 V, $VREFH0 = 4.0$ V to $AVCC0$, $VREF = 4.0$ V to $AVCC$

$T_a = T_{opr}$. T_a is the same under conditions 1 and 2.

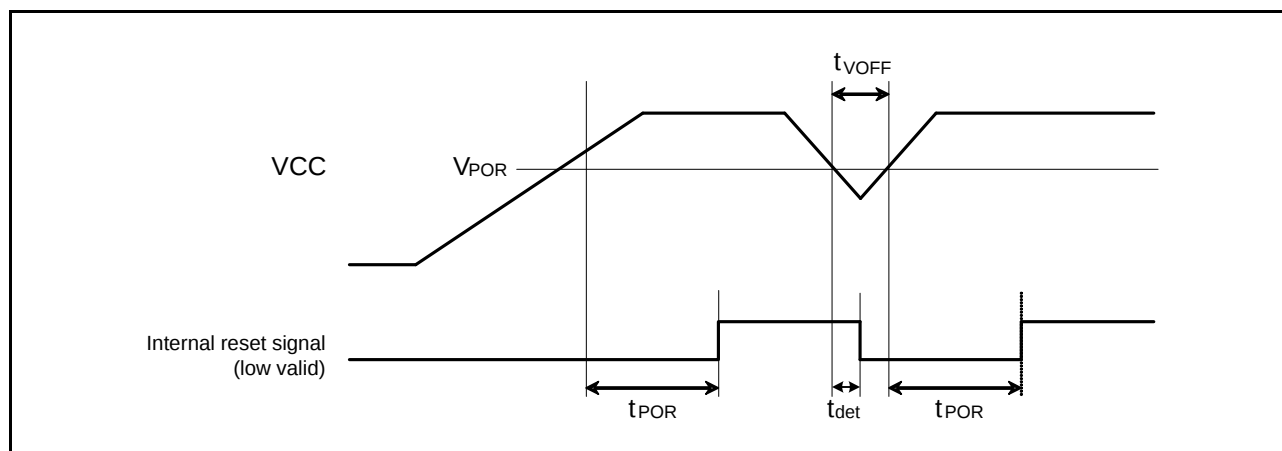
Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V _{POR}	2.48	2.60	2.72	V	Figure 5.20
	Voltage detection circuit (LVD)	V _{det1}	2.68	2.80	2.92		Figure 5.21
		V _{det2}	2.98	3.10	3.22		Figure 5.22
Internal reset time		t _{POR}	20	35	50	ms	Figure 5.21 and Figure 5.22
Min. VCC down time* ¹		t _{VOFF}	200	-	-	us	Figure 5.20 to Figure 5.22
Reply delay time		t _{det}	-	-	200	us	

Condition 3: $V_{CC} = PLLVCC = 4.0$ to 5.5 V, $V_{SS} = PLLVSS = AVSS0 = AVSS = VREFL0 = 0$ V
 $AVCC0 = AVCC = 4.0$ to 5.5 V, $VREFH0 = 4.0$ V to $AVCC0$, $VREF = 4.0$ V to $AVCC$

$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V _{POR}	3.70	3.90	4.10	V	Figure 5.20
	Voltage detection circuit (LVD)	V _{det1}	3.95	4.15	4.35		Figure 5.21
		V _{det2}	4.40	4.60	4.80		Figure 5.22
Internal reset time		t _{POR}	20	35	50	ms	Figure 5.21 and Figure 5.22
Min. VCC down time*1		t _{VOFF}	200	-	-	us	Figure 5.20 to Figure 5.22
Reply delay time		t _{det}	-	-	200	us	

Note 1. The power-off time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR} , V_{det1} , and V_{det2} for the POR/ LVD.


Figure 5.20 Power-on Reset Timing

5.6 Oscillation Stop Detection Timing

Table 5.20 Oscillation Stop Detection Circuit Characteristics

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t _{dr}	-	-	1.0	ms	Figure 5.23
Internal oscillation frequency when oscillation stop is detected	f _{MAIN}	0.5	-	7.0	MHz	

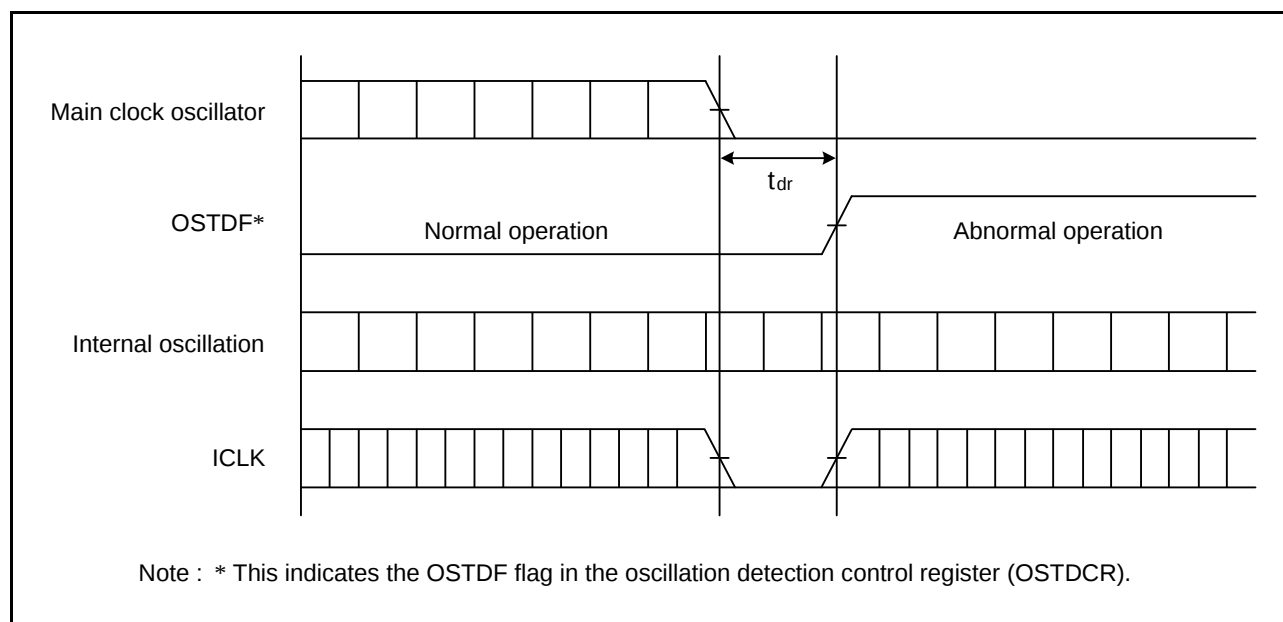


Figure 5.23 Oscillation Stop Detection Timing

5.8 Data Flash (Flash Memory for Data Storage) Characteristics

Table 5.23 Data Flash (Flash Memory for Data Storage) Characteristics (1)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Temperature range for the programming/erasure operation:
Ta = Topr. Ta is the same under conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Rewrite/erase cycle*1	N _{DPEC}	30000	—	—	Times	
Data hold time	t _{DDRP}	30*2	—	—	Year	Ta = +85C°

Note 1. Definition of rewrite/erase cycle:

The rewrite/erase cycle is the number of erasing for each block. When the rewrite/erase cycle is n times (n = 30000), erasing can be performed n times for each block. For instance, when 128-byte writing is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the rewrite/erase cycle is counted as one. However, writing to the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. The value is obtained from the reliability test.

Table 5.24 Data Flash (Flash Memory for Data Storage) Characteristics (2)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Temperature range for the programming/erasure operation:
Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Programming time	8 bytes	t _{DP8}	—	0.4	2	ms	PCLK = 50 MHz
	128 bytes	t _{DP128}	—	1	5	ms	
Erase time	2 Kbytes	t _{DE2K}	—	70	250	ms	PCLK = 50 MHz
Blank check time	8 bytes	t _{DBC8}	—	—	30	μs	PCLK = 50 MHz
	2 Kbytes	t _{DBC2K}	—	—	0.7	ms	
Suspend delay time during writing		t _{DSPD}	—	—	120	μs	Figure 5.24 PCLK = 50 MHz
First suspend delay time during erasing (in suspend priority mode)		t _{DSESD1}	—	—	120	μs	
Second suspend delay time during erasing (in suspend priority mode)		t _{DSESD2}	—	—	1.7	ms	
Suspend delay time during erasing (in erasure priority mode)		t _{DSEED}	—	—	1.7	ms	