Renesas Electronics America Inc - R5F562TAADFM#V3 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I²C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562taadfm-v3

Table 1.1 Outline of Specifications (5 / 5)

Classification	Module/Function	Description
A/D converter	10-bit A/D converter (ADA)	• 10 bits (1 unit x 12 channels) • 10-bit resolution • Conversion time: 1.0 μs per channel (in operation with A/D conversion clock ADCLK at 50 MHz) for AVCC0 = 4.0 to 5.5 V 2.0 μs per channel (in operation with A/D conversion clock ADCLK at 25 MHz) for AVCC = 3.0 to 3.6 V • Two basic operating modes Single mode and scan mode • Scan mode One-cycle scan mode Continuous scan mode • Sample-and-hold function A common sample-and-hold circuit for both units is included. • A/D-conversion register settings for each input pin • Three ways to start A/D conversion Conversion can be started by software, a conversion start trigger from a timer (MTU3 or GPT), or an external trigger signal. • Functionality for 8-bit precision output Right-shifting the results of conversion for output by two bits is selectable. • Self-diagnostic function The self-diagnostic function internally generates three analog input voltages (AVSS, VREF x 1/2, VREF).
CRC calculator (CRC)		• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$. • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.
Operating frequency		ICLK: 8 to 100 MHz PCLK: 8 to 50 MHz
Power supply voltage		• 3-V version VCC = PLLVCC = 2.7 to 3.6V AVCC0 = AVCC = 3.0 to 3.6V, or 4.0 to 5.5V VREFH0 = 3.0 to AVCC0, or 4.0 to AVCC0 VREF = 3.0 to AVCC, or 4.0 to AVCC • 5-V version VCC = PLLVCC = 4.0 to 5.5V AVCC0 = AVCC = 4.0 to 5.5V VREFH0 = 4.0 to AVCC0 VREF = 4.0 to AVCC
Operating temperature		D version: -40 to +85°C, G version: -40 to +105°C*1
Packages		112-pin LQFP (PLQP0112JA-A, 20x20-0.65-mm pitch) 100-pin LQFP (PLQP0100KB-A, 14x14-0.5-mm pitch) 80-pin LQFP (PLQP0080JA-A, 14x14-0.65-mm pitch) 64-pin LQFP (PLQP0064KB-A, 10x10-0.5-mm pitch) 64-pin LQFP (PLQP0064GA-A, 14x14-0.8mm pitch)

Note 1. Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

Table 1.3 List of Products (2 / 2)

Group	Part No.	Order Part No.	Package	ROM Capacity	RAM Capacity	Data Flash Capacity	Power Supply Voltage	CAN	Operating Temp. Range
RX62T	R5F562T7EDFH	R5F562T7EDFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes	2.7 to 3.6 V	Not Support-ed	-40 to +85°C (D version)
	R5F562T7EDFP	R5F562T7EDFP#V3	PLQP0100KB-A						
	R5F562T7EDFF	R5F562T7EDFF#V3	PLQP0080JA-A						
	R5F562T7EDFM	R5F562T7EDFM#V3	PLQP0064KB-A						
	R5F562T7EDFK	R5F562T7EDFK#V3	PLQP0064GA-A						
	R5F562T6EDFF	R5F562T6EDFF#V3	PLQP0080JA-A	64 Kbytes	8 Kbytes				
	R5F562T6EDFM	R5F562T6EDFM#V3	PLQP0064KB-A						
	R5F562T6EDFK	R5F562T6EDFK#V3	PLQP0064GA-A						
	R5F562TAAGFH	R5F562TAAGFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes	VCC/PLLVCC 4.0 to 5.5 V AVCC/AVCC0 4.0 to 5.5 V	Support-ed	-40 to +105°C (G version) *1
	R5F562TAAGFP	R5F562TAAGFP#V3	PLQP0100KB-A						
	R5F562TAAGFF	R5F562TAAGFF#V3	PLQP0080JA-A						
	R5F562TAGGFF	R5F562TAGGFF#V3	PLQP0080JA-A						
	R5F562TAAGFM	R5F562TAAGFM#V3	PLQP0064KB-A						
	R5F562TAAGFK	R5F562TAAGFK#V3	PLQP0064GA-A						
	R5F562T7AGFH	R5F562T7AGFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes			
	R5F562T7AGFP	R5F562T7AGFP#V3	PLQP0100KB-A						
	R5F562T7AGFF	R5F562T7AGFF#V3	PLQP0080JA-A						
	R5F562T7GGFF	R5F562T7GGFF#V3	PLQP0080JA-A						
	R5F562T7AGFM	R5F562T7AGFM#V3	PLQP0064KB-A						
	R5F562T7AGFK	R5F562T7AGFK#V3	PLQP0064GA-A						
	R5F562T6AGFF	R5F562T6AGFF#V3	PLQP0080JA-A	64 Kbytes	8 Kbytes				
	R5F562T6AGFM	R5F562T6AGFM#V3	PLQP0064KB-A						
	R5F562T6AGFK	R5F562T6AGFK#V3	PLQP0064GA-A						
	R5F562TABGFH	R5F562TABGFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes	VCC/PLLVCC 2.7 to 3.6 V AVCC/AVCC0 3.0 to 3.6 V or 4.0 to 5.5 V		
	R5F562TABGFP	R5F562TABGFP#V3	PLQP0100KB-A						
	R5F562TABGFF	R5F562TABGFF#V3	PLQP0080JA-A						
	R5F562TABGFM	R5F562TABGFM#V3	PLQP0064KB-A						
	R5F562TABGFK	R5F562TABGFK#V3	PLQP0064GA-A						
	R5F562T7BGFH	R5F562T7BGFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes			
	R5F562T7BGFP	R5F562T7BGFP#V3	PLQP0100KB-A						
	R5F562T7BGFF	R5F562T7BGFF#V3	PLQP0080JA-A						
	R5F562T7BGFM	R5F562T7BGFM#V3	PLQP0064KB-A						
	R5F562T7BGFK	R5F562T7BGFK#V3	PLQP0064GA-A						
	R5F562T6BGFF	R5F562T6BGFF#V3	PLQP0080JA-A	64 Kbytes	8 Kbytes				
	R5F562T6BGFM	R5F562T6BGFM#V3	PLQP0064KB-A						
	R5F562T6BGFK	R5F562T6BGFK#V3	PLQP0064GA-A						
RX62G	R5F562GAADFH	R5F562GAADFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes	VCC/PLLVCC 4.0 to 5.5 V AVCC/AVCC0 4.0 to 5.5 V	Support-ed	-40 to +85°C (D version)
	R5F562GAADFP	R5F562GAADFP#V3	PLQP0100KB-A						
	R5F562G7ADFH	R5F562G7ADFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes			
	R5F562G7ADFP	R5F562G7ADFP#V3	PLQP0100KB-A						
	R5F562GADDFH	R5F562GADDFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes		Not Support-ed	
	R5F562GADDFP	R5F562GADDFP#V3	PLQP0100KB-A						
	R5F562G7DDFH	R5F562G7DDFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes			
	R5F562G7DDFP	R5F562G7DDFP#V3	PLQP0100KB-A						
	R5F562GAAGFH	R5F562GAAGFH#V3	PLQP0112JA-A	256 Kbytes	16 Kbytes	32 Kbytes	VCC/PLLVCC 4.0 to 5.5 V AVCC/AVCC0 4.0 to 5.5 V	Support-ed	-40 to +105°C (G versio) *1
	R5F562GAAGFP	R5F562GAAGFP#V3	PLQP0100KB-A						
	R5F562G7AGFH	R5F562G7AGFH#V3	PLQP0112JA-A	128 Kbytes	8 Kbytes	8 Kbytes			
	R5F562G7AGFP	R5F562G7AGFP#V3	PLQP0100KB-A						

Note 1. Please contact us if you are using a G version.

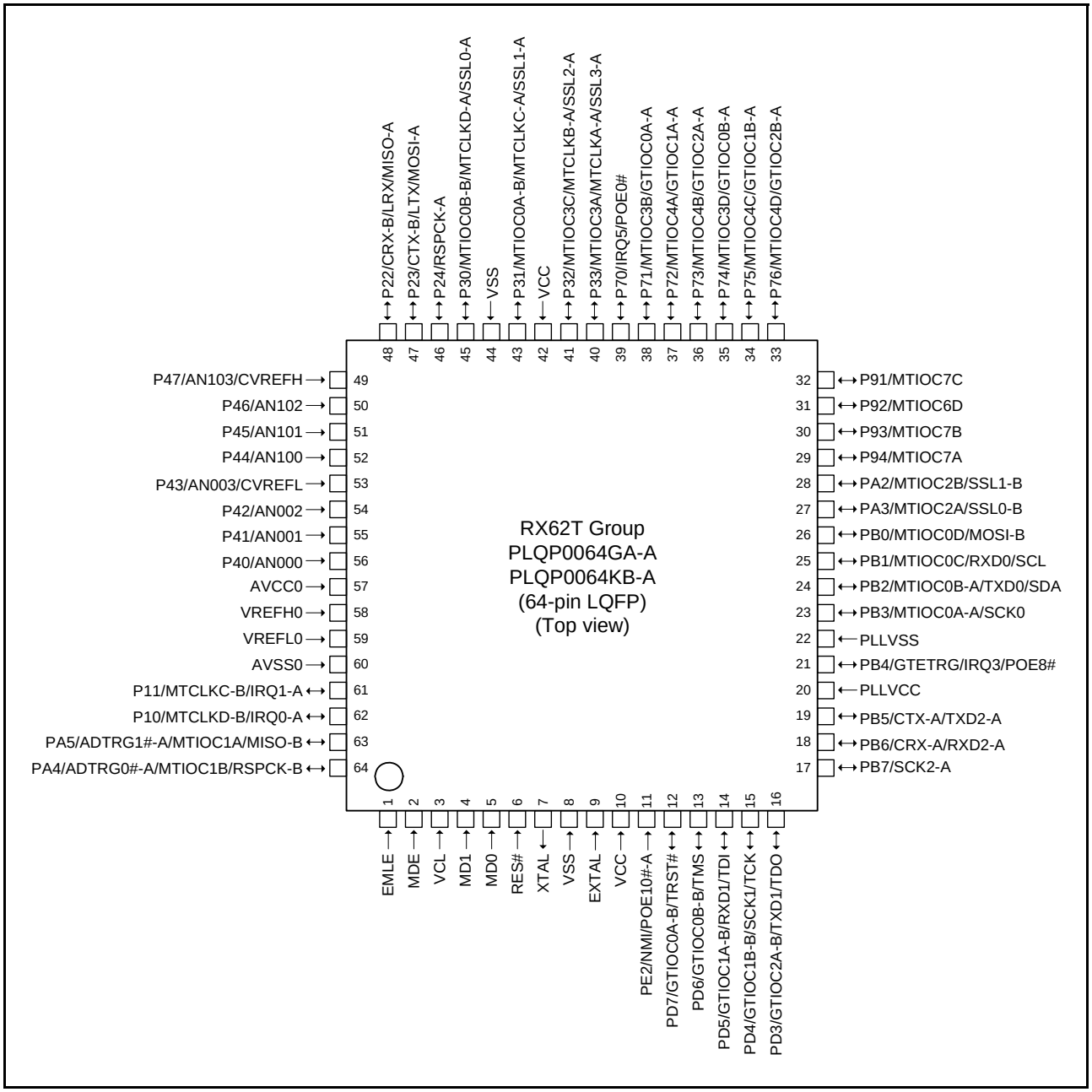


Figure 1.7 Pin Assignment of the 64-Pin LQFP

Table 1.6 List of Pins and Pin Functions (80-Pin LQFP) (2 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi-cation	Interrupt	POE	Debugging
42		P75		MTIOC4C/ GTIOC1B-A				
43		P74		MTIOC3D/ GTIOC0B-A				
44		P73		MTIOC4B/ GTIOC2A-A				
45		P72		MTIOC4A/ GTIOC1A-A				
46		P71		MTIOC3B/ GTIOC0A-A				
47		P70				IRQ5	POE0#	
48		P33		MTIOC3A/ MTCLKA-A	SSL3-A			
49		P32		MTIOC3C/ MTCLKB-A	SSL2-A			
50	VCC							
51		P31		MTIOC0A-B/ MTCLKC-A	SSL1-A			
52	VSS							
53		P30		MTIOC0B-B/ MTCLKD-A	SSL0-A			
54		P24			RSPCK-A			
55		P23			CTX-B/ LTX/ MOSI-A			
56		P22	ADTRG#		CRX-B/ LRX/ MISO-A			
57		P21	ADTRG1#-B	MTCLKA-B		IRQ6		
58		P20	ADTRG0#-B	MTCLKB-B		IRQ7		
59	AVCC							
60	AVSS							
61		P63	AN3					
62		P62	AN2					
63		P61	AN1					
64		P60	AN0					
65		P47	AN103/ CVREFH					
66		P46	AN102					
67		P45	AN101					
68		P44	AN100					
69		P43	AN003/ CVREFL					
70		P42	AN002					
71		P41	AN001					
72		P40	AN000					
73	AVCC0							
74	VREFH0							
75	VREFL0							

Table 1.8 List of Pins and Pin Functions (64-Pin LQFP) (1 / 2)

Pin No. (64-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi-cation	Interrupt	POE	Debugging
1	EMLE							
2	MDE							
3	VCL							
4	MD1							
5	MD0							
6	RES#							
7	XTAL							
8	VSS							
9	EXTAL							
10	VCC							
11		PE2				NMI	POE10#-A	
12		PD7		GTIOC0A-B				TRST#
13		PD6		GTIOC0B-B				TMS
14		PD5		GTIOC1A-B	RXD1			TDI
15		PD4		GTIOC1B-B	SCK1			TCK
16		PD3		GTIOC2A-B	TXD1			TDO
17		PB7			SCK2-A			
18		PB6			CRX-A/ RXD2-A			
19		PB5			CTX-A/ TXD2-A			
20	PLLVCC							
21		PB4		GTETRG		IRQ3	POE8#	
22	PLLVSS							
23		PB3		MTIOC0A-A	SCK0			
24		PB2		MTIOC0B-A	TXD0/SDA			
25		PB1		MTIOC0C	RXD0/SCL			
26		PB0		MTIOC0D	MOSI-B			
27		PA3		MTIOC2A	SSL0-B			
28		PA2		MTIOC2B	SSL1-B			
29		P94		MTIOC7A				
30		P93		MTIOC7B				
31		P92		MTIOC6D				
32		P91		MTIOC7C				
33		P76		MTIOC4D/ GTIOC2B-A				
34		P75		MTIOC4C/ GTIOC1B-A				
35		P74		MTIOC3D/ GTIOC0B-A				
36		P73		MTIOC4B/ GTIOC2A-A				
37		P72		MTIOC4A/ GTIOC1A-A				
38		P71		MTIOC3B/ GTIOC0A-A				
39		P70				IRQ5	POE0#	

4. I/O Registers

This section gives information on the on-chip I/O register addresses and bit configurations. The information is given as shown below. Notes on writing to registers are also given at the end.

(1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to functional modules (abbreviations).
- The number of access cycles indicates the number of states based on the specified reference clock.
- Among the I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.
- A unit of access is specified for each register. Access other than in the specified unit is prohibited.

(2) I/O register bits

- Bit configurations of the registers are listed in the same order as the register addresses.
- Reserved bits are indicated by "—" in the bit name column.
- Space in the bit name field indicates that the entire register is allocated to either the counter or data.
- For the registers of 16 or 32 bits, the MSB is listed first.

(3) Notes on writing to I/O registers

When writing to an I/O register, the CPU starts executing the subsequent instruction before completing I/O register write. This may cause the subsequent instruction to be executed before the post-update I/O register value is reflected on the operation.
As described in the following examples, special care is required for the cases in which the subsequent instruction must be executed after the post-update I/O register value is actually reflected.

[Examples of cases requiring special care]

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERm of the ICU (interrupt request enable bit)*1 cleared to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

Note 1. See section 11.2.2, Interrupt Request Enable Register m (IERm) (m = 02h to 1Fh) in the User's manual: Hardware.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

Table 4.1 List of I/O Registers (Address Order) (5 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 7172h	ICU	DTC activation enable register 114	DTCER114	8	8	2 ICLK
0008 7173h	ICU	DTC activation enable register 115	DTCER115	8	8	2 ICLK
0008 7174h	ICU	DTC activation enable register 116	DTCER116	8	8	2 ICLK
0008 7175h	ICU	DTC activation enable register 117	DTCER117	8	8	2 ICLK
0008 7179h	ICU	DTC activation enable register 121	DTCER121	8	8	2 ICLK
0008 717Ah	ICU	DTC activation enable register 122	DTCER122	8	8	2 ICLK
0008 717Dh	ICU	DTC activation enable register 125	DTCER125	8	8	2 ICLK
0008 717Eh	ICU	DTC activation enable register 126	DTCER126	8	8	2 ICLK
0008 7181h	ICU	DTC activation enable register 129	DTCER129	8	8	2 ICLK
0008 7182h	ICU	DTC activation enable register 130	DTCER130	8	8	2 ICLK
0008 7183h	ICU	DTC activation enable register 131	DTCER131	8	8	2 ICLK
0008 7184h	ICU	DTC activation enable register 132	DTCER132	8	8	2 ICLK
0008 7186h	ICU	DTC activation enable register 134	DTCER134	8	8	2 ICLK
0008 7187h	ICU	DTC activation enable register 135	DTCER135	8	8	2 ICLK
0008 7188h	ICU	DTC activation enable register 136	DTCER136	8	8	2 ICLK
0008 7189h	ICU	DTC activation enable register 137	DTCER137	8	8	2 ICLK
0008 718Ah	ICU	DTC activation enable register 138	DTCER138	8	8	2 ICLK
0008 718Bh	ICU	DTC activation enable register 139	DTCER139	8	8	2 ICLK
0008 718Ch	ICU	DTC activation enable register 140	DTCER140	8	8	2 ICLK
0008 718Dh	ICU	DTC activation enable register 141	DTCER141	8	8	2 ICLK
0008 718Eh	ICU	DTC activation enable register 142	DTCER142	8	8	2 ICLK
0008 718Fh	ICU	DTC activation enable register 143	DTCER143	8	8	2 ICLK
0008 7190h	ICU	DTC activation enable register 144	DTCER144	8	8	2 ICLK
0008 7191h	ICU	DTC activation enable register 145	DTCER145	8	8	2 ICLK
0008 7195h	ICU	DTC activation enable register 149	DTCER149	8	8	2 ICLK
0008 7196h	ICU	DTC activation enable register 150	DTCER150	8	8	2 ICLK
0008 7197h	ICU	DTC activation enable register 151	DTCER151	8	8	2 ICLK
0008 7198h	ICU	DTC activation enable register 152	DTCER152	8	8	2 ICLK
0008 7199h	ICU	DTC activation enable register 153	DTCER153	8	8	2 ICLK
0008 71AEh	ICU	DTC activation enable register 174	DTCER174	8	8	2 ICLK
0008 71AFh	ICU	DTC activation enable register 175	DTCER175	8	8	2 ICLK
0008 71B0h	ICU	DTC activation enable register 176	DTCER176	8	8	2 ICLK
0008 71B1h	ICU	DTC activation enable register 177	DTCER177	8	8	2 ICLK
0008 71B2h	ICU	DTC activation enable register 178	DTCER178	8	8	2 ICLK
0008 71B3h	ICU	DTC activation enable register 179	DTCER179	8	8	2 ICLK
0008 71B4h	ICU	DTC activation enable register 180	DTCER180	8	8	2 ICLK
0008 71B5h	ICU	DTC activation enable register 181	DTCER181	8	8	2 ICLK
0008 71B6h	ICU	DTC activation enable register 182	DTCER182	8	8	2 ICLK
0008 71B7h	ICU	DTC activation enable register 183	DTCER183	8	8	2 ICLK
0008 71B8h	ICU	DTC activation enable register 184	DTCER184	8	8	2 ICLK
0008 71BAh	ICU	DTC activation enable register 186	DTCER186	8	8	2 ICLK
0008 71BBh	ICU	DTC activation enable register 187	DTCER187	8	8	2 ICLK
0008 71BCh	ICU	DTC activation enable register 188	DTCER188	8	8	2 ICLK
0008 71BDh	ICU	DTC activation enable register 189	DTCER189	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (11 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 8383h	RSPI	RSPI status register	SPSR	8	8	2, 3 PCLK*3
0008 8384h	RSPI	RSPI data register	SPDR	16, 32	16, 32	2, 3 PCLK*3
0008 8388h	RSPI	RSPI sequence control register	SPSCR	8	8	2, 3 PCLK*3
0008 8389h	RSPI	RSPI sequence status register	SPSSR	8	8	2, 3 PCLK*3
0008 838Ah	RSPI	RSPI bit rate register	SPBR	8	8	2, 3 PCLK*3
0008 838Bh	RSPI	RSPI data control register	SPDCR	8	8	2, 3 PCLK*3
0008 838Ch	RSPI	RSPI clock delay register	SPCKD	8	8	2, 3 PCLK*3
0008 838Dh	RSPI	RSPI slave select negation delay register	SSLND	8	8	2, 3 PCLK*3
0008 838Eh	RSPI	RSPI next-access delay register	SPND	8	8	2, 3 PCLK*3
0008 838Fh	RSPI	RSPI control register 2	SPCR2	8	8	2, 3 PCLK*3
0008 8390h	RSPI	RSPI command register 0	SPCMD0	16	16	2, 3 PCLK*3
0008 8392h	RSPI	RSPI command register 1	SPCMD1	16	16	2, 3 PCLK*3
0008 8394h	RSPI	RSPI command register 2	SPCMD2	16	16	2, 3 PCLK*3
0008 8396h	RSPI	RSPI command register 3	SPCMD3	16	16	2, 3 PCLK*3
0008 8398h	RSPI	RSPI command register 4	SPCMD4	16	16	2, 3 PCLK*3
0008 839Ah	RSPI	RSPI command register 5	SPCMD5	16	16	2, 3 PCLK*3
0008 839Ch	RSPI	RSPI command register 6	SPCMD6	16	16	2, 3 PCLK*3
0008 839Eh	RSPI	RSPI command register 7	SPCMD7	16	16	2, 3 PCLK*3
0008 9000h	S12AD0	A/D control register	ADCSR	8	8	2, 3 PCLK*3
0008 9004h	S12AD0	A/D channel select register	ADANS	16	16	2, 3 PCLK*3
0008 900Ah	S12AD0	A/D programmable gain amplifier register	ADPG	16	16	2, 3 PCLK*3
0008 900Eh	S12AD0	A/D control extended register	ADCER	16	16	2, 3 PCLK*3
0008 9010h	S12AD0	A/D start trigger select register	ADSTRGR	16	16	2, 3 PCLK*3
0008 9012h	S12AD	Comparator operating mode select register 0	ADCMPMD0	16	16	2, 3 PCLK*3
0008 9014h	S12AD	Comparator operating mode select register 1	ADCMPMD1	16	16	2, 3 PCLK*3
0008 9016h	S12AD	Comparator filter mode register 0	ADCMPNR0	16	16	2, 3 PCLK*3
0008 9018h	S12AD	Comparator filter mode register 1	ADCMPNR1	16	16	2, 3 PCLK*3
0008 901Ah	S12AD	Comparator detection flag register	ADCMPFR	8	8	2, 3 PCLK*3
0008 901Ch	S12AD	Comparator interrupt select register	ADCMPSEL	16	16	2, 3 PCLK*3
0008 901Eh	S12AD0	A/D data register Diag	ADRD	16	16	2, 3 PCLK*3
0008 9020h	S12AD0	A/D data register 0A	ADDR0A	16	16	2, 3 PCLK*3
0008 9022h	S12AD0	A/D data register 1	ADDR1	16	16	2, 3 PCLK*3
0008 9024h	S12AD0	A/D data register 2	ADDR2	16	16	2, 3 PCLK*3
0008 9026h	S12AD0	A/D data register 3	ADDR3	16	16	2, 3 PCLK*3
0008 9030h	S12AD0	A/D data register 0B	ADDR0B	16	16	2, 3 PCLK*3
0008 9060h	S12AD0	A/D sampling state register	ADSSTR	8	8	2, 3 PCLK*3
0008 9080h	S12AD1	A/D control register	ADCSR	8	8	2, 3 PCLK*3
0008 9084h	S12AD1	A/D channel select register	ADANS	16	16	2, 3 PCLK*3
0008 908Ah	S12AD1	A/D programmable gain amplifier register	ADPG	16	16	2, 3 PCLK*3
0008 908Eh	S12AD1	A/D control extended register	ADCER	16	16	2, 3 PCLK*3
0008 9090h	S12AD1	A/D start trigger select register	ADSTRGR	16	16	2, 3 PCLK*3
0008 909Eh	S12AD1	A/D data register Diag	ADRD	16	16	2, 3 PCLK*3
0008 90A0h	S12AD1	A/D data register 0A	ADDR0A	16	16	2, 3 PCLK*3
0008 90A2h	S12AD1	A/D data register 1	ADDR1	16	16	2, 3 PCLK*3

Table 4.1 List of I/O Registers (Address Order) (12 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 90A4h	S12AD1	A/D data register 2	ADDR2	16	16	2, 3 PCLK*3
0008 90A6h	S12AD1	A/D data register 3	ADDR3	16	16	2, 3 PCLK*3
0008 90B0h	S12AD1	A/D data register 0B	ADDR0B	16	16	2, 3 PCLK*3
0008 90E0h	S12AD1	A/D sampling state register	ADSSTR	8	8	2, 3 PCLK*3
0008 C001h	PORT1	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C002h	PORT2	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C003h	PORT3	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C007h	PORT7	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C008h	PORT8	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C009h	PORT9	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C00Ah	PORTA	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C00Bh	PORTB	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C00Dh	PORTD	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C00Eh	PORTE	Data direction register	DDR	8	8	2, 3 PCLK*3
0008 C010h	PORTG	Data direction register	DDR*1	8	8	2, 3 PCLK*3
0008 C021h	PORT1	Data register	DR	8	8	2, 3 PCLK*3
0008 C022h	PORT2	Data register	DR	8	8	2, 3 PCLK*3
0008 C023h	PORT3	Data register	DR	8	8	2, 3 PCLK*3
0008 C027h	PORT7	Data register	DR	8	8	2, 3 PCLK*3
0008 C028h	PORT8	Data register	DR	8	8	2, 3 PCLK*3
0008 C029h	PORT9	Data register	DR	8	8	2, 3 PCLK*3
0008 C02Ah	PORTA	Data register	DR	8	8	2, 3 PCLK*3
0008 C02Bh	PORTB	Data register	DR	8	8	2, 3 PCLK*3
0008 C02Dh	PORTD	Data register	DR	8	8	2, 3 PCLK*3
0008 C02Eh	PORTE	Data register	DR	8	8	2, 3 PCLK*3
0008 C030h	PORTG	Data register	DR*1	8	8	2, 3 PCLK*3
0008 C041h	PORT1	Data register	PORT	8	8	2, 3 PCLK*3
0008 C042h	PORT2	Data register	PORT	8	8	2, 3 PCLK*3
0008 C043h	PORT3	Data register	PORT	8	8	2, 3 PCLK*3
0008 C044h	PORT4	Data register	PORT	8	8	2, 3 PCLK*3
0008 C045h	PORT5	Data register	PORT	8	8	2, 3 PCLK*3
0008 C046h	PORT6	Data register	PORT	8	8	2, 3 PCLK*3
0008 C047h	PORT7	Data register	PORT	8	8	2, 3 PCLK*3
0008 C048h	PORT8	Data register	PORT	8	8	2, 3 PCLK*3
0008 C049h	PORT9	Data register	PORT	8	8	2, 3 PCLK*3
0008 C04Ah	PORTA	Data register	PORT	8	8	2, 3 PCLK*3
0008 C04Bh	PORTB	Data register	PORT	8	8	2, 3 PCLK*3
0008 C04Dh	PORTD	Data register	PORT	8	8	2, 3 PCLK*3
0008 C04Eh	PORTE	Data register	PORT	8	8	2, 3 PCLK*3
0008 C050h	PORTG	Port register	PORT*1	8	8	2, 3 PCLK*3
0008 C061h	PORT1	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C062h	PORT2	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C063h	PORT3	Input buffer control register	ICR	8	8	2, 3 PCLK*3
0008 C064h	PORT4	Input buffer control register	ICR	8	8	2, 3 PCLK*3

Table 4.2 List of I/O Registers (Bit Order) (9 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
ICU	IRQCR0	—	—	—	—	IRQMD[1:0]		—	—
ICU	IRQCR1	—	—	—	—	IRQMD[1:0]		—	—
ICU	IRQCR2	—	—	—	—	IRQMD[1:0]		—	—
ICU	IRQCR3	—	—	—	—	IRQMD[1:0]		—	—
ICU	IRQCR4	—	—	—	—	IRQMD[1:0]		—	—
ICU	IRQCR5	—	—	—	—	IRQMD[1:0]		—	—
ICU	IRQCR6	—	—	—	—	IRQMD[1:0]		—	—
ICU	IRQCR7	—	—	—	—	IRQMD[1:0]		—	—
ICU	NMISR	—	—	—	—	—	OSTST	LVDST	NMIST
ICU	NMIER	—	—	—	—	—	OSTEN	LVDEN	NMIEN
ICU	NMICLR	—	—	—	—	—	OSTCLR	—	NMICLR
ICU	NMICR	—	—	—	—	NMIMD	—	—	—
CMT	CMSTR0	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	STR1	STR0
CMT0	CMCR	—	—	—	—	—	—	—	—
		—	CMIE	—	—	—	—	CKS[1:0]	
CMT0	CMCNT								
CMT0	CMCOR								
CMT1	CMCR	—	—	—	—	—	—	—	—
		—	CMIE	—	—	—	—	CKS[1:0]	
CMT1	CMCNT								
CMT1	CMCOR								
CMT	CMSTR1	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	STR3	STR2
CMT2	CMCR	—	—	—	—	—	—	—	—
		—	CMIE	—	—	—	—	CKS[1:0]	
CMT2	CMCNT								
CMT2	CMCOR								
CMT3	CMCR	—	—	—	—	—	—	—	—
		—	CMIE	—	—	—	—	CKS[1:0]	
CMT3	CMCNT								
CMT3	CMCOR								
WDT	TCSR	—	TMS	TME	—	—		CKS[2:0]	
WDT	WINA								
WDT	TCNT								
WDT	WINB								
WDT	RSTCSR	WOVF	RSTE	—	—	—	—	—	—
IWDT	IWDTCR	—	—	—	—	—	—	—	—
			CKS[3:0]			—	—	TOPS[1:0]	
IWDT	IWDTSR	—	UNDFF			CNTVAL[13:0]			
					CNTVAL[13:0]				
AD0	ADDRA*1	—	—	—	—	—	—		

Table 4.2 List of I/O Registers (Bit Order) (17 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
CAN0*3	MKR5	—	—	—			SID[10:0]		
				SID[10:0]				EID[17 0]	
					EID[17:0]				
					EID[17:0]				
CAN0*3	MKR6	—	—	—			SID[10:0]		
				SID[10:0]				EID[17 0]	
					EID[17:0]				
					EID[17:0]				
CAN0*3	MKR7	—	—	—			SID[10:0]		
				SID[10:0]				EID[17 0]	
					EID[17:0]				
					EID[17:0]				
CAN0*3	FIDCR0	IDE	RTR	—			SID[10:0]		
				SID[10:0]				EID[17:0]	
					EID[17:0]				
					EID[17:0]				
CAN0*3	FIDCR1	IDE	RTR	—			SID[10:0]		
				SID[10:0]				EID[17:0]	
					EID[17:0]				
					EID[17:0]				
CAN0*3	MKIVLR								
CAN0*3	MIER	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
CAN0*3	MCTL.TX	TRMREQ	RECREQ	—	ONESHOT	—	TRMABT	TRMACTIVE	SENTDATA
	MCTL.RX	TRMREQ	RECREQ	—	ONESHOT	—	MSGLOST	INVALDATA	NEWDATA
CAN0*3	CTLR	—	—	RBOC	BOM[1:0]		SLPM	CANM[1:0]	
		TSPS[1:0]		TSRC	TPM	MLM	IDFM[1:0]		MBM
CAN0*3	STR	—	RECST	TRMST	BOST	EPST	SLPST	HLTST	RSTST
		EST	TABST	FMLST	NMLST	TFST	RFST	SDST	NDST
CAN0*3	BCR		TSEG1[3:0]			—	—	BRP[9:0]	
					BRP[9:0]				
		—	—	SJW[1:0]		—		TSEG2[2:0]	
		—	—	—	—	—	—	—	—
CAN0*3	RFCR	RFEST	RFWST	RFFST	RFMLF		RFUST[2:0]		RFE
CAN0*3	RFPCR	—	—	—	—	—	—	—	—
CAN0*3	TFCR	TFEST	TFFST	—	—		TFUST[2:0]		TFE
CAN0*3	TFPCR	—	—	—	—	—	—	—	—
CAN0*3	EIER	BLIE	OLIE	ORIE	BORIE	BOEIE	EPIE	EWIE	BEIE
CAN0*3	EIFR	BLIF	OLIF	ORIF	BORIF	BOEIF	EPIF	EWIF	BEIF
CAN0*3	RECR	—	—	—	—	—	—	—	—
CAN0*3	TECR	—	—	—	—	—	—	—	—
CAN0*3	ECSR	EDPM	ADEF	BE0F	BE1F	CEF	AEF	FEF	SEF
CAN0*3	CSSR	—	—	—	—	—	—	—	—
CAN0*3	MSSR	SEST	—	—			MBNST[4:0]		
CAN0*3	MSMR	—	—	—	—	—	—	MBSM[1:0]	
CAN0*3	TSR	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—

Table 4.2 List of I/O Registers (Bit Order) (20 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
MTU0	TMDR1	—	BFE	BFB	BFA			MD[3:0]	
MTU0	TIORH		IOB[3:0]					IOA[3:0]	
MTU0	TIORL		IOD[3:0]					IOC[3:0]	
MTU0	TIER	TTEG	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA
MTU0	TSR	—	—	—	TCFV	TGFD	TGFC	TGFB	TGFA
MTU0	TCNT								
MTU0	TGRA								
MTU0	TGRB								
MTU0	TGRC								
MTU0	TGRD								
MTU0	TGRE								
MTU0	TGRF								
MTU0	TIER2	TTGE2	—	—	—	—	—	TGIEF	TGIEE
MTU0	TSR2	—	—	—	—	—	—	TGFF	TGFE
MTU0	TBTM	—	—	—	—	—	TTSE	TTSB	TTSA
MTU1	TCR	—	CCLR[1:0]		CKEG[1:0]			TPSC[2:0]	
MTU1	TMDR1	—	—	—	—			MD[3:0]	
MTU1	TIOR		IOB[3:0]					IOA[3:0]	
MTU1	TIER	TTEG	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA
MTU1	TSR	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA
MTU1	TCNT								
MTU1	TGRA								
MTU1	TGRB								
MTU1	TICCR	—	—	—	—	I2BE	I2AE	I1BE	I1AE
MTU2	TCR	—	CCLR[1:0]		CKEG[1:0]			TPSC[2:0]	
MTU2	TMDR1	—	—	—	—			MD[3:0]	
MTU2	TIOR		IOB[3:0]					IOA[3:0]	
MTU2	TIER	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA
MTU2	TSR	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA
MTU2	TCNT								
MTU2	TGRA								
MTU2	TGRB								
MTU6	TCR		CCLR[20]		CKEG[1:0]			TPSC[2:0]	
MTU7	TCR		CCLR[20]		CKEG[1:0]			TPSC[2:0]	
MTU6	TMDR1	—	—	BFB	BFA			MD[3:0]	
MTU7	TMDR1	—	—	BFB	BFA			MD[3:0]	
MTU6	TIORH		IOB[3:0]					IOA[3:0]	
MTU6	TIORL		IOD[3:0]					IOC[3:0]	
MTU7	TIORH		IOB[3:0]					IOA[3:0]	

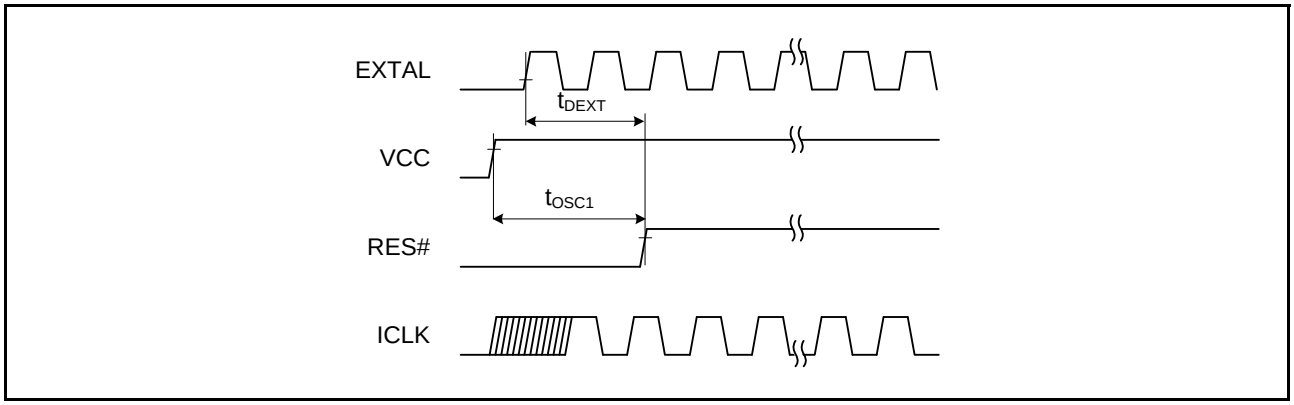


Figure 5.1 Oscillation Settling Timing

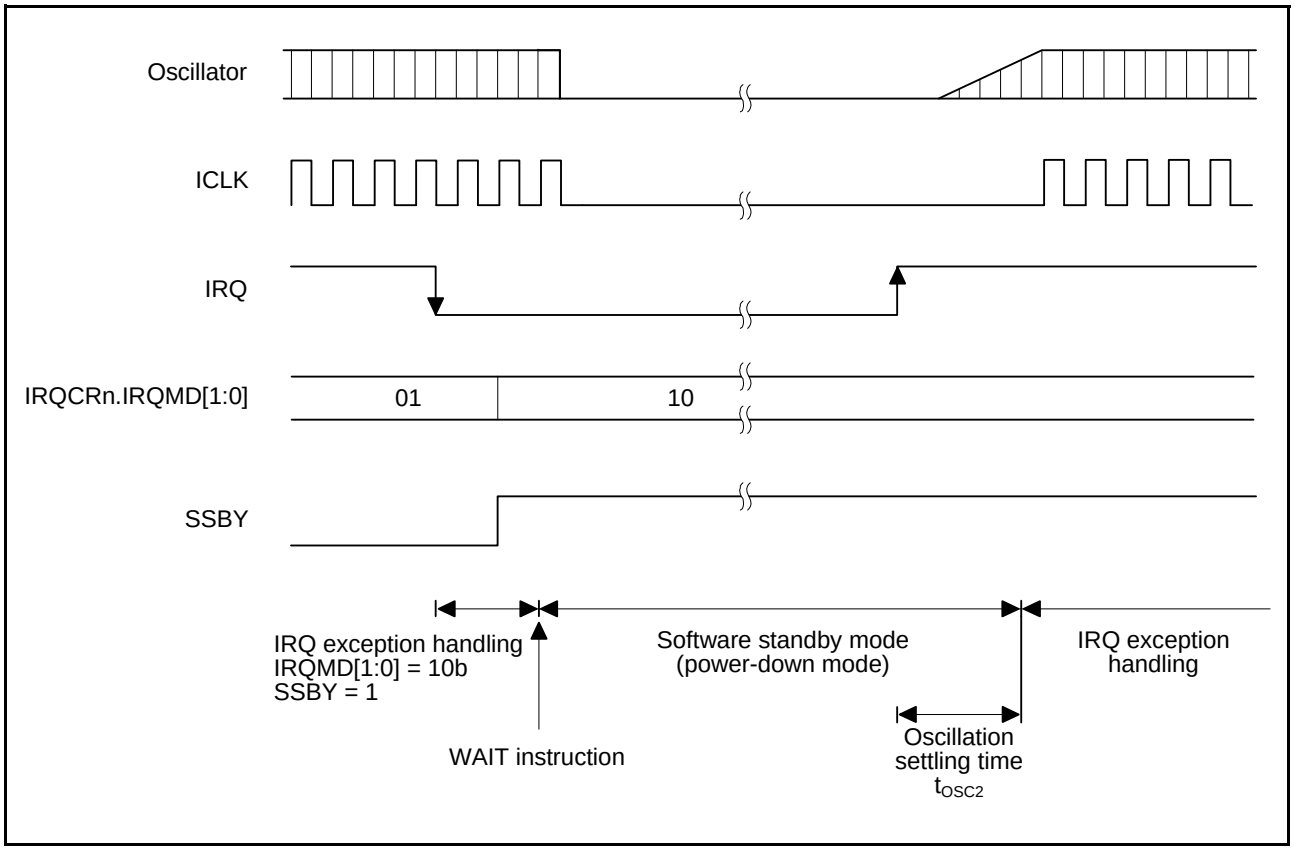


Figure 5.2 Oscillation Settling Timing after Software Standby Mode

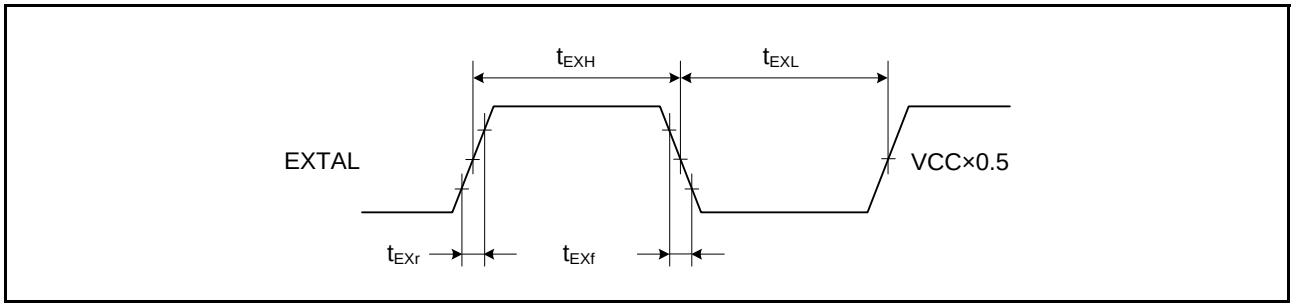


Figure 5.4 EXTAL External Input Clock Timing

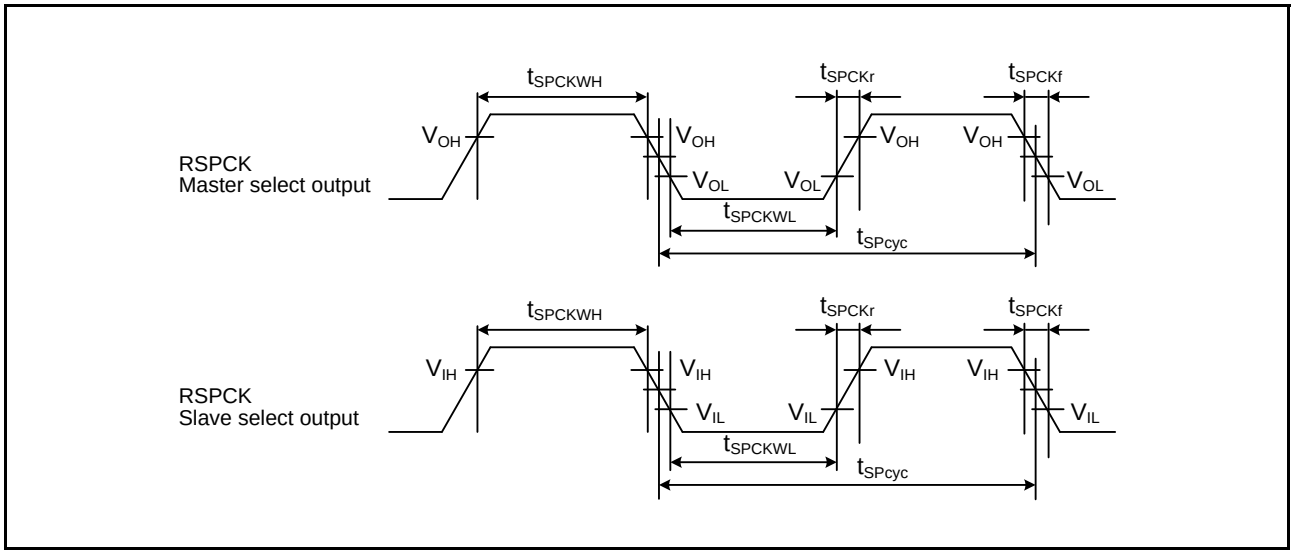


Figure 5.11 RSPI Clock Timing

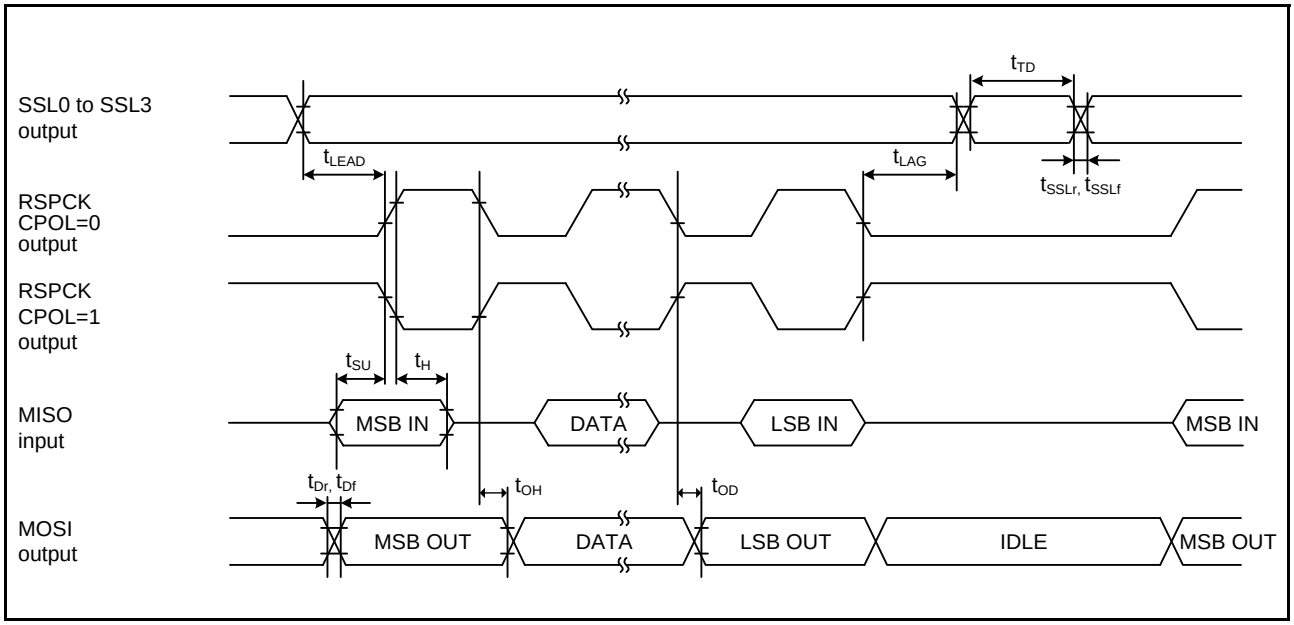


Figure 5.12 RSPI Timing (Master, CPHA = 0)

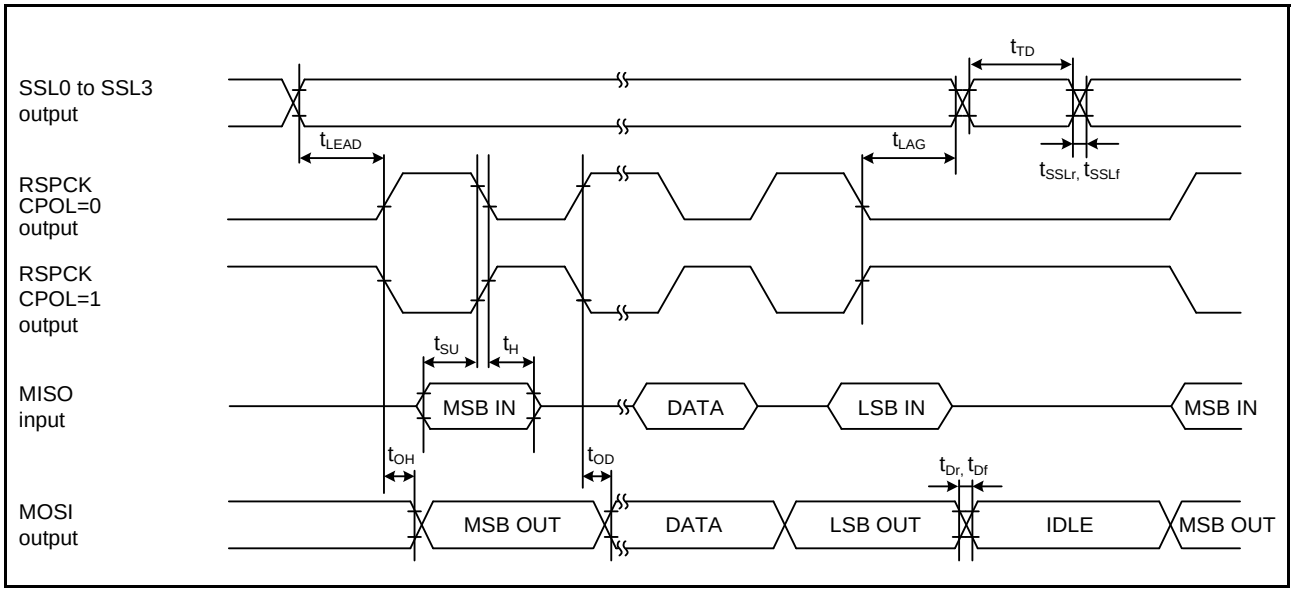


Figure 5.13 RSPI Timing (Master, CPHA = 1)

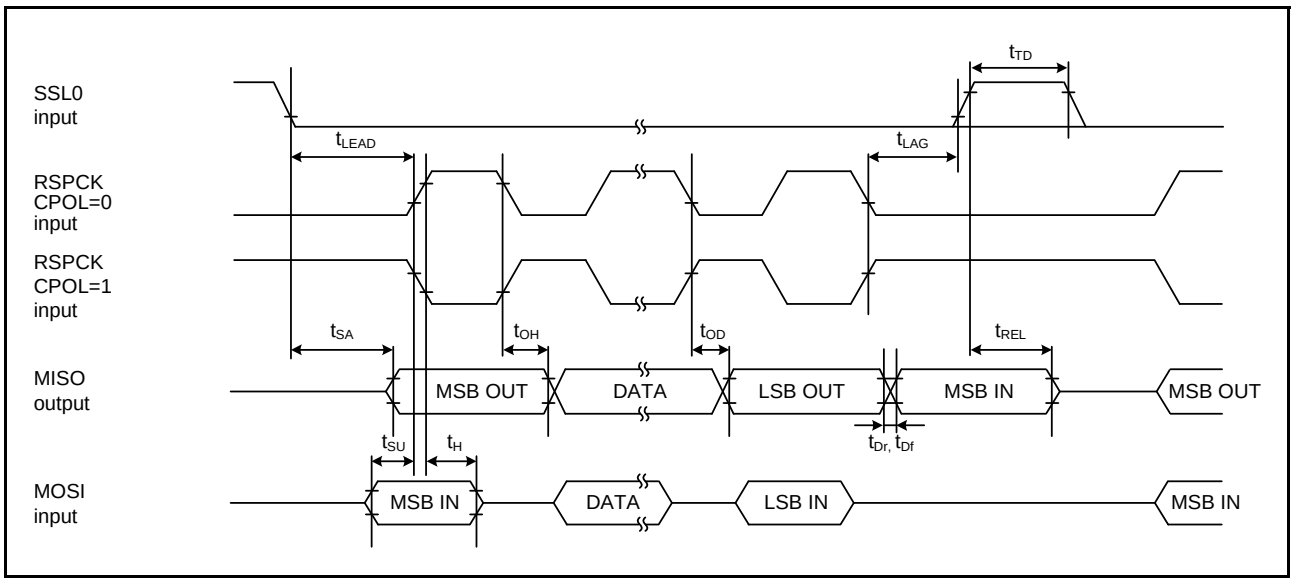


Figure 5.14 RSPI Timing (Slave, CPHA = 0)

Table 5.16 12-Bit A/D Conversion Characteristics

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC
Ta = Topr, ICLK = 8 to 100 MHz, PCLK = 8 to 50 MHz

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		12	12	12	Bit	
Conversion time*1 (AD clock = 25-MHz operation)		2.0	-	-	µs	Sampling 20 states
Analog input capacitance		-	-	6	pF	
Integral nonlinearity error		-	-	±4.0	LSB	
Offset error		-	-	±7.5	LSB	
Full-scale error		-	-	±7.5	LSB	
Quantization error		-	±0.5	-	LSB	
Absolute accuracy	When a sample-and-hold circuit is in use	-	-	±8.0	LSB	AVin = 0.25 to AV_{REFH} - 0.25
	When a sample-and-hold circuit is not in use	-	-	±8.0	LSB	AVin = AV_{REFL} to AV_{REFH}
Permissible signal source impedance		-	-	3.0	kΩ	

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 2 and 3. ICLK = 8 to 100 MHz, PCLK = 8 to 50 MHz.

Item		Min.	Typ.	Max.	Unit	Test Conditions
Resolution		12	12	12	Bit	
Conversion time*1 (AD clock = 25-MHz operation)		1.0	-	-	µs	Sampling 20 states
Analog input capacitance		-	-	6	pF	
Integral nonlinearity error		-	-	±4.0	LSB	
Offset error		-	-	±7.5	LSB	
Full-scale error		-	-	±7.5	LSB	
Quantization error		-	±0.5	-	LSB	
Absolute accuracy	When a sample-and-hold circuit is in use	-	-	±8.0	LSB	AVin = 0.25 to AV_{REFH} - 0.25
	When a sample-and-hold circuit is not in use	-	-	±8.0	LSB	AVin = AV_{REFL} to AV_{REFH}
Permissible signal source impedance		-	-	3.0	kΩ	

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 5.18 Comparator Characteristics

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC
Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Analog input capacitance	Cin	-	-	6	pF	
REFH pin offset voltage	Voff	-	-	5	mV	
REFL pin offset voltage		-	-	5	mV	
REFH input voltage range	Vin	1.7	-	AVcc – 0.3	V	
REFL input voltage range		0.3	-	AVcc – 1.7	V	
REFH reply time	tCR	-	-	1	µs	
REFL reply time	tCF	-	-	1	µs	

5.5 Power-on Reset Circuit, Voltage Detection Circuit Characteristics

Table 5.19 Power-on Reset Circuit, Voltage Detection Circuit Characteristics

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 and 2.

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	2.48	2.60	2.72	V	Figure 5.20
	Voltage detection circuit (LVD)	Vdet1	2.68	2.80	2.92		Figure 5.21
		Vdet2	2.98	3.10	3.22		Figure 5.22
Internal reset time		t_{POR}	20	35	50	ms	Figure 5.21 and Figure 5.22
Min. VCC down time*1		t_{VOFF}	200	-	-	us	Figure 5.20 to Figure 5.22
Reply delay time		tdet	-	-	200	us	

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	3.70	3.90	4.10	V	Figure 5.20
	Voltage detection circuit (LVD)	Vdet1	3.95	4.15	4.35		Figure 5.21
		Vdet2	4.40	4.60	4.80		Figure 5.22
Internal reset time		t_{POR}	20	35	50	ms	Figure 5.21 and Figure 5.22
Min. VCC down time*1		t_{VOFF}	200	-	-	us	Figure 5.20 to Figure 5.22
Reply delay time		tdet	-	-	200	us	

Note 1. The power-off time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det1}, and V_{det2} for the POR/ LVD.

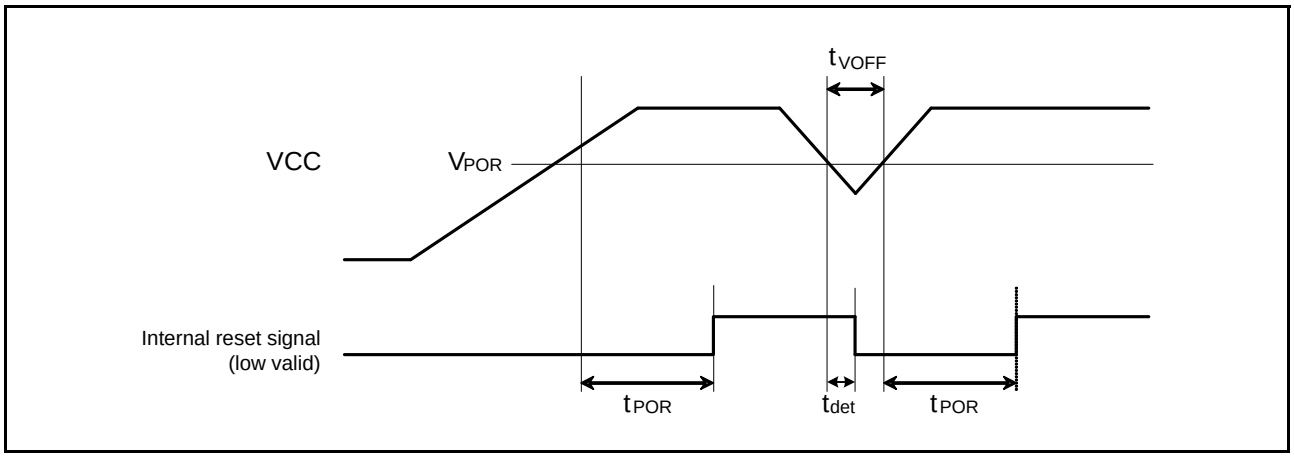
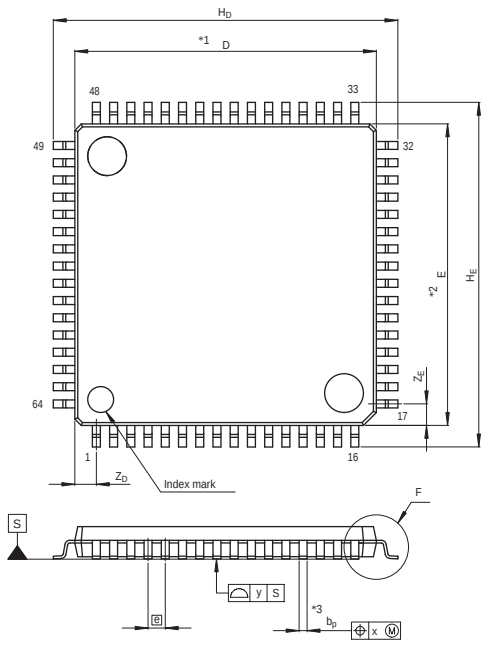
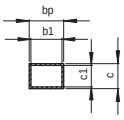


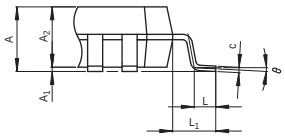
Figure 5.20 Power-on Reset Timing

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-14x14-0.80	PLQP0064GA-A	64P6U-A/ —	0.7g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.3	0.5	0.7
L_1	—	1.0	—

Figure E 64-Pin LQFP (PLQP0064GA-A) Package Dimensions