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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | RX |
| Core Size | 32-Bit Single-Core |
| Speed | 100MHz |
| Connectivity | CANbus, I²C, LINbus, SCI, SPI |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 44 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | A/D 4x10b, 8x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 80-LQFP |
| Supplier Device Package | 80-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562tabdff-v1 |

**Table 1.1 Outline of Specifications (4 / 5)**

| Classification | Module/Function | Description |
|---|---|---|
| Communications | CAN module (CAN) (as an optional function) | • 1 channel<br>• 32 mailboxes |
| | Serial peripheral interface (RSPI) | • 1 unit<br>• RSPI transfer facility<br>Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPI clock (RSPCK) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines)<br>Capable of handling serial transfer as a master or slave<br>• Data formats<br>Switching between MSB first and LSB first<br>The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits.<br>128-bit buffers for transmission and reception<br>Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits)<br>• Buffered structure<br>• Double buffers for both transmission and reception |
| | LIN module (LIN) | • 1 channel (LIN master)<br>• Supports revisions 1.3, 2.0, and 2.1 of the LIN protocol |
| A/D converter | 12-bit A/D converter (S12ADA) | • 12 bits (2 units x 4 channels)<br>• 12-bit resolution<br>• Conversion time:<br>1.0 μs per channel (in operation with A/D conversion clock ADCLK at 50 MHz) for AVCC = 4.0 to 5.5 V<br>2.0 μs per channel (in operation with A/D conversion clock ADCLK at 25 MHz) for AVCC0 = 3.0 to 3.6 V<br>• Two basic operating modes<br>Single mode and scan mode<br>• Scan mode<br>One-cycle scan mode<br>Continuous scan mode<br>2-channel scan mode (Input ports of the A/D unit are divided into two groups in this mode, and the activation sources are separately selectable for each group.)<br>• Sample-and-hold function<br>A common sample-and-hold circuit for both units is included.<br>Additionally, sample-and-hold circuit for each unit is included. (three channels per unit)<br>• A/D-conversion register settings for each input pin.<br>• Two registers for the result of conversion are provided for a single analog input pin of each unit (AN000 and AN100).<br>• Three ways to start A/D conversion<br>Conversion can be started by software, a conversion start trigger from a timer (MTU3 or GPT), or an external trigger signal.<br>• Functionality for 8- or 10-bit precision output<br>Right-shifting of the results of conversion for output by two or four bits is selectable.<br>• Self-diagnostic function<br>The self-diagnostic function internally generates three analog input voltages (VREFL0, VREFH0 x 1/2, VREFH0).<br>• Amplification of input signals by a programmable gain amplifier (three channels per unit)<br>Amplification rate: 2.0-, 2.5-, 3.077-, 3.636-, 4.0-, 4.444-, 5.0-, 5.714-, 6.667-, 10.0-, or 13.333-times amplification (a total of 11 steps)<br>• Window comparators (three channels per unit) |

**Table 1.1 Outline of Specifications (5 / 5)**

| Classification | Module/Function | Description |
|---|---|---|
| A/D converter | 10-bit A/D converter (ADA) | • 10 bits (1 unit x 12 channels)<br>• 10-bit resolution<br>• Conversion time:<br>1.0 μs per channel (in operation with A/D conversion clock ADCLK at 50 MHz) for AVCC0 = 4.0 to 5.5 V<br>2.0 μs per channel (in operation with A/D conversion clock ADCLK at 25 MHz) for AVCC = 3.0 to 3.6 V<br>• Two basic operating modes<br>Single mode and scan mode<br>• Scan mode<br>One-cycle scan mode<br>Continuous scan mode<br>• Sample-and-hold function<br>A common sample-and-hold circuit for both units is included.<br>• A/D-conversion register settings for each input pin<br>• Three ways to start A/D conversion<br>Conversion can be started by software, a conversion start trigger from a timer (MTU3 or GPT), or an external trigger signal.<br>• Functionality for 8-bit precision output<br>Right-shifting the results of conversion for output by two bits is selectable.<br>• Self-diagnostic function<br>The self-diagnostic function internally generates three analog input voltages (AVSS, VREF x 1/2, VREF). |
| CRC calculator (CRC) | | • CRC code generation for arbitrary amounts of data in 8-bit units<br>• Select any of three generating polynomials:<br>$X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$.<br>• Generation of CRC codes for use with LSB-first or MSB-first communications is selectable. |
| Operating frequency | | ICLK: 8 to 100 MHz<br>PCLK: 8 to 50 MHz |
| Power supply voltage | | • 3-V version<br>VCC = PLLVCC = 2.7 to 3.6V<br>AVCC0 = AVCC = 3.0 to 3.6V, or 4.0 to 5.5V<br>VREFH0 = 3.0 to AVCC0, or 4.0 to AVCC0<br>VREF = 3.0 to AVCC, or 4.0 to AVCC<br>• 5-V version<br>VCC = PLLVCC = 4.0 to 5.5V<br>AVCC0 = AVCC = 4.0 to 5.5V<br>VREFH0 = 4.0 to AVCC0<br>VREF = 4.0 to AVCC |
| Operating temperature | | D version: -40 to +85°C, G version: -40 to +105°C*1 |
| Packages | | 112-pin LQFP (PLQP0112JA-A, 20x20-0.65-mm pitch)<br>100-pin LQFP (PLQP0100KB-A, 14x14-0.5-mm pitch)<br>80-pin LQFP (PLQP0080JA-A, 14x14-0.65-mm pitch)<br>64-pin LQFP (PLQP0064KB-A, 10x10-0.5-mm pitch)<br>64-pin LQFP (PLQP0064GA-A, 14x14-0.8mm pitch) |

Note 1. Please contact Renesas Electronics sales office for derating of operation under Ta = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

**Table 1.4 List of Pins and Pin Functions (112-Pin LQFP) (3 / 3)**

| Pin No. (112-Pin LQFP) | Power Supply Clock System Control | I/O Port | Analog | Timer | Communi-cation | Interrupt | POE | Debugging |
|---|---|---|---|---|---|---|---|---|
| 80 | AVCC | | | | | | | |
| 81 | VREF | | | | | | | |
| 82 | AVSS | | | | | | | |
| 83 | | P63 | AN3 | | | | | |
| 84 | | P62 | AN2 | | | | | |
| 85 | | P61 | AN1 | | | | | |
| 86 | | P60 | AN0 | | | | | |
| 87 | | P55 | AN11 | | | | | |
| 88 | | P54 | AN10 | | | | | |
| 89 | | P53 | AN9 | | | | | |
| 90 | | P52 | AN8 | | | | | |
| 91 | | P51 | AN7 | | | | | |
| 92 | | P50 | AN6 | | | | | |
| 93 | | P47 | AN103/ CVREFH | | | | | |
| 94 | | P46 | AN102 | | | | | |
| 95 | | P45 | AN101 | | | | | |
| 96 | | P44 | AN100 | | | | | |
| 97 | | P43 | AN003/ CVREFL | | | | | |
| 98 | | P42 | AN002 | | | | | |
| 99 | | P41 | AN001 | | | | | |
| 100 | | P40 | AN000 | | | | | |
| 101 | AVCC0 | | | | | | | |
| 102 | VREFH0 | | | | | | | |
| 103 | VREFL0 | | | | | | | |
| 104 | AVSS0 | | | | | | | |
| 105 | | P82 | | MTIC5U | SCK2-B | | | |
| 106 | | P81 | | MTIC5V | TXD2-B | | | |
| 107 | | P80 | | MTIC5W | RXD2-B | | | |
| 108 | | | | WDTOVF# | | | | |
| 109 | | P11 | | MTCLKC-B | | IRQ1-A | | |
| 110 | | P10 | | MTCLKD-B | | IRQ0-A | | |
| 111 | | | | | | | | TRST# |
| 112 | | | | | | | | TMS |

**Table 1.6 List of Pins and Pin Functions (80-Pin LQFP) (3 / 3)**

| Pin No. (80-Pin LQFP) | Power Supply Clock System Control | I/O Port | Analog | Timer | Communi-cation | Interrupt | POE | Debugging |
|---|---|---|---|---|---|---|---|---|
| 76 | AVSS0 | | | | | | | |
| 77 | | P11 | | MTCLKC-B | | IRQ1-A | | |
| 78 | | P10 | | MTCLKD-B | | IRQ0-A | | |
| 79 | | PA5 | ADTRG1#-A | MTIOC1A | MISO-B | | | |
| 80 | | PA4 | ADTRG0#-A | MTIOC1B | RSPCK-B | | | |

**Table 4.1 List of I/O Registers (Address Order) (12 / 25)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0008 90A4h | S12AD1 | A/D data register 2 | ADDR2 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 90A6h | S12AD1 | A/D data register 3 | ADDR3 | 16 | 16 | 2, 3 PCLK*3 |
| 0008 90B0h | S12AD1 | A/D data register 0B | ADDR0B | 16 | 16 | 2, 3 PCLK*3 |
| 0008 90E0h | S12AD1 | A/D sampling state register | ADSSTR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C001h | PORT1 | Data direction register | DDR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C002h | PORT2 | Data direction register | DDR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C003h | PORT3 | Data direction register | DDR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C007h | PORT7 | Data direction register | DDR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C008h | PORT8 | Data direction register | DDR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C009h | PORT9 | Data direction register | DDR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C00Ah | PORTA | Data direction register | DDR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C00Bh | PORTB | Data direction register | DDR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C00Dh | PORTD | Data direction register | DDR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C00Eh | PORTE | Data direction register | DDR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C010h | PORTG | Data direction register | DDR*1 | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C021h | PORT1 | Data register | DR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C022h | PORT2 | Data register | DR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C023h | PORT3 | Data register | DR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C027h | PORT7 | Data register | DR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C028h | PORT8 | Data register | DR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C029h | PORT9 | Data register | DR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C02Ah | PORTA | Data register | DR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C02Bh | PORTB | Data register | DR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C02Dh | PORTD | Data register | DR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C02Eh | PORTE | Data register | DR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C030h | PORTG | Data register | DR*1 | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C041h | PORT1 | Data register | PORT | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C042h | PORT2 | Data register | PORT | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C043h | PORT3 | Data register | PORT | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C044h | PORT4 | Data register | PORT | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C045h | PORT5 | Data register | PORT | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C046h | PORT6 | Data register | PORT | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C047h | PORT7 | Data register | PORT | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C048h | PORT8 | Data register | PORT | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C049h | PORT9 | Data register | PORT | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C04Ah | PORTA | Data register | PORT | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C04Bh | PORTB | Data register | PORT | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C04Dh | PORTD | Data register | PORT | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C04Eh | PORTE | Data register | PORT | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C050h | PORTG | Port register | PORT*1 | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C061h | PORT1 | Input buffer control register | ICR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C062h | PORT2 | Input buffer control register | ICR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C063h | PORT3 | Input buffer control register | ICR | 8 | 8 | 2, 3 PCLK*3 |
| 0008 C064h | PORT4 | Input buffer control register | ICR | 8 | 8 | 2, 3 PCLK*3 |

**Table 4.1 List of I/O Registers (Address Order) (16 / 25)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 0009 4019h | LIN0 | Data 2 buffer register | L0DB2 | 8 | 8, 16, 32 | 2, 3 PCLK*3 |
| 0009 401Ah | LIN0 | Data 3 buffer register | L0DB3 | 8 | 8, 16, 32 | 2, 3 PCLK*3 |
| 0009 401Bh | LIN0 | Data 4 buffer register | L0DB4 | 8 | 8, 16, 32 | 2, 3 PCLK*3 |
| 0009 401Ch | LIN0 | Data 5 buffer register | L0DB5 | 8 | 8, 16, 32 | 2, 3 PCLK*3 |
| 0009 401Dh | LIN0 | Data 6 buffer register | L0DB6 | 8 | 8, 16, 32 | 2, 3 PCLK*3 |
| 0009 401Eh | LIN0 | Data 7 buffer register | L0DB7 | 8 | 8, 16, 32 | 2, 3 PCLK*3 |
| 0009 401Fh | LIN0 | Data 8 buffer register | L0DB8 | 8 | 8, 16, 32 | 2, 3 PCLK*3 |
| 000C 1200h | MTU3 | Timer control register | TCR | 8 | 8, 16, 32 | 5 ICLK |
| 000C 1201h | MTU4 | Timer control register | TCR | 8 | 8 | 5 ICLK |
| 000C 1202h | MTU3 | Timer mode register 1 | TMDR1 | 8 | 8, 16 | 5 ICLK |
| 000C 1203h | MTU4 | Timer mode register 1 | TMDR1 | 8 | 8 | 5 ICLK |
| 000C 1204h | MTU3 | Timer I/O control register H | TIORH | 8 | 8, 16, 32 | 5 ICLK |
| 000C 1205h | MTU3 | Timer I/O control register L | TIORL | 8 | 8 | 5 ICLK |
| 000C 1206h | MTU4 | Timer I/O control register H | TIORH | 8 | 8, 16 | 5 ICLK |
| 000C 1207h | MTU4 | Timer I/O control register L | TIORL | 8 | 8 | 5 ICLK |
| 000C 1208h | MTU3 | Timer interrupt enable register | TIER | 8 | 8, 16 | 5 ICLK |
| 000C 1209h | MTU4 | Timer interrupt enable register | TIER | 8 | 8 | 5 ICLK |
| 000C 120Ah | MTU | Timer output master enable register A | TOERA | 8 | 8 | 5 ICLK |
| 000C 120Dh | MTU | Timer gate control register A | TGCRA | 8 | 8 | 5 ICLK |
| 000C 120Eh | MTU | Timer output control register 1A | TOCR1A | 8 | 8, 16 | 5 ICLK |
| 000C 120Fh | MTU | Timer output control register 2A | TOCR2A | 8 | 8 | 5 ICLK |
| 000C 1210h | MTU3 | Timer counter | TCNT | 16 | 16, 32 | 5 ICLK |
| 000C 1212h | MTU4 | Timer counter | TCNT | 16 | 16 | 5 ICLK |
| 000C 1214h | MTU | Timer cycle data register A | TCDRA | 16 | 16, 32 | 5 ICLK |
| 000C 1216h | MTU | Timer dead time data register A | TDDRA | 16 | 16 | 5 ICLK |
| 000C 1218h | MTU3 | Timer general register A | TGRA | 16 | 16, 32 | 5 ICLK |
| 000C 121Ah | MTU3 | Timer general register B | TGRB | 16 | 16 | 5 ICLK |
| 000C 121Ch | MTU4 | Timer general register A | TGRA | 16 | 16, 32 | 5 ICLK |
| 000C 121Eh | MTU4 | Timer general register B | TGRB | 16 | 16 | 5 ICLK |
| 000C 1220h | MTU | Timer subcounter A | TCNTSA | 16 | 16, 32 | 5 ICLK |
| 000C 1222h | MTU | Timer cycle buffer register A | TCBRA | 16 | 16 | 5 ICLK |
| 000C 1224h | MTU3 | Timer general register C | TGRC | 16 | 16, 32 | 5 ICLK |
| 000C 1226h | MTU3 | Timer general register D | TGRD | 16 | 16 | 5 ICLK |
| 000C 1228h | MTU4 | Timer general register C | TGRC | 16 | 16, 32 | 5 ICLK |
| 000C 122Ah | MTU4 | Timer general register D | TGRD | 16 | 16 | 5 ICLK |
| 000C 122Ch | MTU3 | Timer status register | TSR | 8 | 8, 16 | 5 ICLK |
| 000C 122Dh | MTU4 | Timer status register | TSR | 8 | 8 | 5 ICLK |
| 000C 1230h | MTU | Timer interrupt skipping set register 1A | TITCR1A | 8 | 8, 16 | 5 ICLK |
| 000C 1231h | MTU | Timer interrupt skipping counter 1A | TITCNT1A | 8 | 8 | 5 ICLK |
| 000C 1232h | MTU | Timer buffer transfer set register A | TBTERA | 8 | 8 | 5 ICLK |
| 000C 1234h | MTU | Timer dead time enable register A | TDERA | 8 | 8 | 5 ICLK |
| 000C 1236h | MTU | Timer output level buffer register A | TOLBRA | 8 | 8 | 5 ICLK |
| 000C 1238h | MTU3 | Timer buffer operation transfer mode register | TBTM | 8 | 8, 16 | 5 ICLK |
| 000C 1239h | MTU4 | Timer buffer operation transfer mode register | TBTM | 8 | 8 | 5 ICLK |

**Table 4.1 List of I/O Registers (Address Order) (23 / 25)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 000C 222Ch | GPT2 | A/D converter start request timing register B | GTADTRB | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 222Eh | GPT2 | A/D converter start request timing buffer register B | GTADTBRB | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2230h | GPT2 | A/D converter start request timing double-buffer register B | GTADTDBRB | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2234h | GPT2 | General PWM timer output negate control register | GTONCR | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2236h | GPT2 | General PWM timer dead time control register | GTDTCR | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2238h | GPT2 | General PWM timer dead time value register | GTDVU | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 223Ah | GPT2 | General PWM timer dead time value register | GTDVD | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 223Ch | GPT2 | General PWM timer dead time buffer register | GTDBU | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 223Eh | GPT2 | General PWM timer dead time buffer register | GTDBD | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2240h | GPT2 | General PWM timer output protection function status register | GTSOS | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2242h | GPT2 | General PWM timer output protection temporary release register | GTSOTR | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2280h | GPT3 | General PWM timer I/O control register | GTIOR | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 2282h | GPT3 | General PWM timer interrupt output setting register | GTINTAD | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 2284h | GPT3 | General PWM timer control register | GTCR | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 2286h | GPT3 | General PWM timer buffer enable register | GTBER | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 2288h | GPT3 | General PWM timer count direction register | GTUDC | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 228Ah | GPT3 | General PWM timer interrupt and A/D converter start request skipping setting register | GTITC | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 228Ch | GPT3 | General PWM timer status register | GTST | 16 | 8, 16, 32 | 3 to 5 ICLK*4 |
| 000C 228Eh | GPT3 | General PWM timer counter | GTCNT | 16 | 16 | 3 to 5 ICLK*4 |
| 000C 2290h | GPT3 | General PWM timer compare capture register A | GTCCRA | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2292h | GPT3 | General PWM timer compare capture register B | GTCCRB | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2294h | GPT3 | General PWM timer compare capture register C | GTCCRC | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2296h | GPT3 | General PWM timer compare capture register D | GTCCRD | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 2298h | GPT3 | General PWM timer compare capture register E | GTCCRE | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 229Ah | GPT3 | General PWM timer compare capture register F | GTCCRF | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 229Ch | GPT3 | General PWM timer cycle setting register | GTPR | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 229Eh | GPT3 | General PWM timer cycle setting buffer register | GTPBR | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 22A0h | GPT3 | General PWM timer cycle setting double-buffer register | GTPDBR | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 22A4h | GPT3 | A/D converter start request timing register A | GTADTRA | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 22A6h | GPT3 | A/D converter start request timing buffer register A | GTADTBRA | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 22A8h | GPT3 | A/D converter start request timing double-buffer register A | GTADTDBRA | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 22ACh | GPT3 | A/D converter start request timing register B | GTADTRB | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 22AEh | GPT3 | A/D converter start request timing buffer register B | GTADTBRB | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 22B0h | GPT3 | A/D converter start request timing double-buffer register B | GTADTDBRB | 16 | 16, 32 | 3 to 5 ICLK*4 |
| 000C 22B4h | GPT3 | General PWM timer output negate control register | GTONCR | 16 | 16, 32 | 3 to 5 ICLK*4 |

**Table 4.1 List of I/O Registers (Address Order) (25 / 25)**

| Address | Module Abbreviation | Register Name | Register Abbreviation | Number of Bits | Access Size | Number of Access Cycles |
|---|---|---|---|---|---|---|
| 007F FFBAh | FLASH | FCU command register | FCMDR | 16 | 16 | 2, 3 PCLK*3 |
| 007F FFC8h | FLASH | FCU processing switching register | FCPSR | 16 | 16 | 2, 3 PCLK*3 |
| 007F FFCAh | FLASH | Data flash blank check control register | DFLBCCNT | 16 | 16 | 2, 3 PCLK*3 |
| 007F FFCCh | FLASH | Flash P/E status register | FPESTAT | 16 | 16 | 2, 3 PCLK*3 |
| 007F FFCEh | FLASH | Data flash blank check status register | DFLBCSTAT | 16 | 16 | 2, 3 PCLK*3 |
| 007F FFE8h | FLASH | Peripheral clock notification register | PCKAR | 16 | 16 | 2, 3 PCLK*3 |

Note 1. This register is not supported by the 100-pin LQFP version.
Note 2. This register is not supported by the product without the CAN function.
Note 3. The number of access states depends on the number of divided cycles for clock synchronization (0 to 1 PCLK).
Note 4. Reading the registers takes 3 cycles of ICLK and writing to the registers takes 5 cycles of ICLK.

**Table 4.2 List of I/O Registers (Bit Order) (10 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| AD0 | ADDRB*1 | — | — | — | — | — | — | | |
| AD0 | ADDRC*1 | — | — | — | — | — | — | | |
| AD0 | ADDRD*1 | — | — | — | — | — | — | | |
| AD0 | ADDRE*1 | — | — | — | — | — | — | | |
| AD0 | ADDRF*1 | — | — | — | — | — | — | | |
| AD0 | ADDRG*1 | — | — | — | — | — | — | | |
| AD0 | ADDRH*1 | — | — | — | — | — | — | | |
| AD0 | ADCSR | — | ADIE | ADST | — | CH[3:0] | | | |
| AD0 | ADCR | — | — | — | — | CKS[1:0] | | MODE[1:0] | |
| AD0 | ADSSTR | | | | | | | | |
| AD0 | ADDIAGR | — | — | — | — | — | — | DIAG[1:0] | |
| AD0 | ADDRI*1 | — | — | — | — | — | — | | |
| AD0 | ADDRJ*1 | — | — | — | — | — | — | | |
| AD0 | ADDRK *1 | — | — | — | — | — | — | | |
| AD0 | ADDRL*1 | — | — | — | — | — | — | | |
| AD0 | ADSTRGR | — | — | — | ADSTRS[4:0] | | | | |
| AD0 | ADDPR | DPSEL | — | — | — | — | — | — | DPPRC |
| SCI0 | SMR | CM | CHR | PE | PM | STOP | MP | CKS[1:0] | |
| SCI0 | BRR | | | | | | | | |
| SCI0 | SCR | TIE | RIE | TE | RE | MPIE | TEIE | CKE[1:0] | |
| SCI0 | TDR | | | | | | | | |
| SCI0 | SSR | TDRE | RDRF | ORER | FER | PER | TEND | MPB | MPBT |
| SCI0 | RDR | | | | | | | | |
| SCI0 | SCMR | BCP2 | — | — | — | SDIR | SINV | — | SMIF |
| SCI0 | SEMR | — | — | NFEN | ABCS | — | — | — | — |
| SMCI0 | SMR | GM | BLK | PE | PM | (BCP[1:0]) | | CKS[1:0] | |
| SMCI0 | BRR | | | | | | | | |
| SMCI0 | SCR | TIE | RIE | TE | RE | MPIE | TEIE | CKE[1:0] | |
| SMCI0 | TDR | | | | | | | | |
| SMCI0 | SSR | TDRE | RDRF | ORER | ERS | PER | TEND | MPB | MPBT |
| SMCI0 | RDR | | | | | | | | |
| SMCI0 | SCMR | BCP2 | — | — | — | SDIR | SINV | — | SMIF |
| SCI1 | SMR | CM | CHR | PE | PM | STOP | MP | CKS[1:0] | |
| SCI1 | BRR | | | | | | | | |
| SCI1 | SCR | TIE | RIE | TE | RE | MPIE | TEIE | CKE[1:0] | |
| SCI1 | TDR | | | | | | | | |
| SCI1 | SSR | TDRE | RDRF | ORER | FER | PER | TEND | MPB | MPBT |
| SCI1 | RDR | | | | | | | | |
| SCI1 | SCMR | BCP2 | — | — | — | SDIR | SINV | — | SMIF |

**Table 4.2 List of I/O Registers (Bit Order) (13 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| S12AD0 | ADRD*2 | DIAGST[1:0] | | — | — | AD11 | AD10 | AD9 | AD8 |
| | | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 |
| S12AD0 | ADDR0A*2 | — | — | — | — | AD11 | AD10 | AD9 | AD8 |
| | | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 |
| S12AD0 | ADDR1*2 | — | — | — | — | AD11 | AD10 | AD9 | AD8 |
| | | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 |
| S12AD0 | ADDR2*2 | — | — | — | — | AD11 | AD10 | AD9 | AD8 |
| | | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 |
| S12AD0 | ADDR3*2 | — | — | — | — | AD11 | AD10 | AD9 | AD8 |
| | | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 |
| S12AD0 | ADDR0B*2 | — | — | — | — | AD11 | AD10 | AD9 | AD8 |
| | | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 |
| S12AD0 | ADSSTR | | | | | | | | |
| S12AD1 | ADCSR | ADST | ADCS[1:0] | | ADIE | CKS[1:0] | | TRGE | EXTRG |
| S12AD1 | ADANS | — | — | CH[1:0] | | — | PG102SEL | PG101SEL | PG100SEL |
| | | — | — | — | — | — | PG102EN | PG101EN | PG100EN |
| S12AD1 | ADPG | — | — | — | — | PG102GAIN[3:0] | | | |
| | | PG101GAIN[3:0] | | | | PG100GAIN[3:0] | | | |
| S12AD1 | ADCER | ADRFMT | — | ADIEW | ADIE2 | DIAGM | DIAGLD | DIAGVAL[1:0] | |
| | | — | — | ACE | — | — | ADPRC[1:0] | | SHBYP |
| S12AD1 | ADSTRGR | — | — | — | ADSTRS1[4:0] | | | | |
| | | — | — | — | ADSTRS0[4:0] | | | | |
| S12AD1 | ADRD*2 | DIAGST[1:0] | | — | — | AD11 | AD10 | AD9 | AD8 |
| | | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 |
| S12AD1 | ADDR0A*2 | — | — | — | — | AD11 | AD10 | AD9 | AD8 |
| | | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 |
| S12AD1 | ADDR1*2 | — | — | — | — | AD11 | AD10 | AD9 | AD8 |
| | | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 |
| S12AD1 | ADDR2*2 | — | — | — | — | AD11 | AD10 | AD9 | AD8 |
| | | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 |
| S12AD1 | ADDR3*2 | — | — | — | — | AD11 | AD10 | AD9 | AD8 |
| | | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 |
| S12AD1 | ADDR0B*2 | — | — | — | — | AD11 | AD10 | AD9 | AD8 |
| | | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 |
| S12AD1 | ADSSTR | | | | | | | | |
| PORT1 | DDR | — | — | — | — | — | — | B1 | B0 |
| PORT2 | DDR | — | — | — | B4 | B3 | B2 | B1 | B0 |
| PORT3 | DDR | — | — | — | — | B3 | B2 | B1 | B0 |
| PORT7 | DDR | — | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| PORT8 | DDR | — | — | — | — | — | B2 | B1 | B0 |
| PORT9 | DDR | — | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| PORTA | DDR | — | — | B5 | B4 | B3 | B2 | B1 | B0 |
| PORTB | DDR | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| PORTD | DDR | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| PORTE | DDR | — | — | B5 | B4 | B3 | — | B1 | B0 |
| PORTG | DDR | — | — | B5 | B4 | B3 | B2 | B1 | B0 |
| PORT1 | DR | — | — | — | — | — | — | B1 | B0 |
| PORT2 | DR | — | — | — | B4 | B3 | B2 | B1 | B0 |
| PORT3 | DR | — | — | — | — | B3 | B2 | B1 | B0 |
| PORT7 | DR | — | B6 | B5 | B4 | B3 | B2 | B1 | B0 |

**Table 4.2 List of I/O Registers (Bit Order) (14 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| PORT8 | DR | — | — | — | — | — | B2 | B1 | B0 |
| PORT9 | DR | — | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| PORTA | DR | — | — | B5 | B4 | B3 | B2 | B1 | B0 |
| PORTB | DR | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| PORTD | DR | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| PORTE | DR | — | — | B5 | B4 | B3 | — | B1 | B0 |
| PORTG | DR | — | — | B5 | B4 | B3 | B2 | B1 | B0 |
| PORT1 | PORT | — | — | — | — | — | — | B1 | B0 |
| PORT2 | PORT | — | — | — | B4 | B3 | B2 | B1 | B0 |
| PORT3 | PORT | — | — | — | — | B3 | B2 | B1 | B0 |
| PORT4 | PORT | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| PORT5 | PORT | — | — | B5 | B4 | B3 | B2 | B1 | B0 |
| PORT6 | PORT | — | — | B5 | B4 | B3 | B2 | B1 | B0 |
| PORT7 | PORT | — | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| PORT8 | PORT | — | — | — | — | — | B2 | B1 | B0 |
| PORT9 | PORT | — | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| PORTA | PORT | — | — | B5 | B4 | B3 | B2 | B1 | B0 |
| PORTB | PORT | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| PORTD | PORT | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| PORTE | PORT | — | — | B5 | B4 | B3 | B2 | B1 | B0 |
| PORTG | PORT | — | — | B5 | B4 | B3 | B2 | B1 | B0 |
| PORT1 | ICR | — | — | — | — | — | — | B1 | B0 |
| PORT2 | ICR | — | — | — | B4 | B3 | B2 | B1 | B0 |
| PORT3 | ICR | — | — | — | — | B3 | B2 | B1 | B0 |
| PORT4 | ICR | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| PORT5 | ICR | — | — | B5 | B4 | B3 | B2 | B1 | B0 |
| PORT6 | ICR | — | — | B5 | B4 | B3 | B2 | B1 | B0 |
| PORT7 | ICR | — | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| PORT8 | ICR | — | — | — | — | — | B2 | B1 | B0 |
| PORT9 | ICR | — | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| PORTA | ICR | — | — | B5 | B4 | B3 | B2 | B1 | B0 |
| PORTB | ICR | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| PORTD | ICR | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| PORTE | ICR | — | — | B5 | B4 | B3 | — | B1 | B0 |
| PORTG | ICR | — | — | B5 | B4 | B3 | B2 | B1 | B0 |
| IOPORT | PF8IRQ | — | — | — | — | ITS1[1:0] | | ITS0[1:0] | |
| IOPORT | PF9IRQ | — | — | — | — | — | ITS2 | — | — |
| IOPORT | PFAADC | — | — | — | — | — | — | ADTRG1S | ADTRG0S |
| IOPORT | PFCMTU | TCLKS[1:0] | | — | — | — | — | MTUS1 | MTUS0 |
| IOPORT | PFDGPT | — | — | — | — | — | — | — | GPTS |
| IOPORT | PFFSCI | — | — | — | — | — | SCI2S | — | — |
| IOPORT | PFGSPI | SSL3E | SSL2E | SSL1E | SSL0E | MISOE | MOSIE | RSPCKE | — |
| IOPORT | PFHSPI | — | — | — | — | — | — | RSPIS[1:0] | |
| IOPORT | PFJCAN | CANS[1:0] | | — | — | — | — | — | CANE |
| IOPORT | PFKLIN | — | — | — | — | — | — | — | LINE |
| IOPORT | PFMPOE | — | — | — | POE11E | POE10E | POE8E | POE4E | POE0E |
| IOPORT | PFNPOE | POE10S | — | — | — | — | — | — | — |
| SYSTEM | DPSBYCR | DPSBY | IOKEEP | — | — | — | — | — | — |
| SYSTEM | DPSWCR | — | — | WTSTS[5:0] | | | | | |
| SYSTEM | DPSIER | DNMIE | — | — | DLVDE | — | — | DIRQ1E | DIRQ0E |

**Table 4.2 List of I/O Registers (Bit Order) (18 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| CAN0*3 | AFSR | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | — |
| CAN0*3 | TCR | — | — | — | — | — | TSTM[1:0] | | TSTE |
| LIN0 | LWBR | — | — | — | — | — | — | — | LWBR0 |
| LIN0 | LBRP0 | | | | | | | | |
| LIN0 | LBRP1 | | | | | | | | |
| LIN0 | LSTC | | | | | | | | LSTM |
| LIN0 | L0MD | — | — | — | — | LCKS[1:0] | | — | — |
| LIN0 | L0BRK | — | — | BDT[1:0] | | BLT[3:0] | | | |
| LIN0 | L0SPC | — | — | IBS[1:0] | | — | IBSH[2:0] | | |
| LIN0 | L0WUP | WUTL[3:0] | | | | — | — | — | — |
| LIN0 | L0IE | — | — | — | — | — | ERRIE | FRCIE | FTCIE |
| LIN0 | L0EDE | — | — | — | — | FERE | FTERE | PBERE | BERE |
| LIN0 | L0C | — | — | — | — | — | — | OM1 | OM0 |
| LIN0 | L0TC | — | — | — | — | — | — | RTS | FTS |
| LIN0 | L0MST | — | — | — | — | — | — | OMM1 | OMM0 |
| LIN0 | L0ST | HTRC | D1RC | — | — | ERR | — | FRC | FTC |
| LIN0 | L0EST | — | — | CSER | — | FER | FTER | PBER | BER |
| LIN0 | L0RFC | — | FSM | CSM | RFT | RFDL[3:0] | | | |
| LIN0 | L0IDB | IDP | | ID | | | | | |
| LIN0 | L0CBR | | | | | | | | |
| LIN0 | L0DB1 | | | | | | | | |
| LIN0 | L0DB2 | | | | | | | | |
| LIN0 | L0DB3 | | | | | | | | |
| LIN0 | L0DB4 | | | | | | | | |
| LIN0 | L0DB5 | | | | | | | | |
| LIN0 | L0DB6 | | | | | | | | |
| LIN0 | L0DB7 | | | | | | | | |
| LIN0 | L0DB8 | | | | | | | | |
| MTU3 | TCR | CCLR[2:0] | | CKEG[1:0] | | | TPSC[2:0] | | |
| MTU4 | TCR | CCLR[2:0] | | CKEG[1:0] | | | TPSC[2:0] | | |
| MTU3 | TMDR1 | — | — | BFB | BFA | MD[3:0] | | | |
| MTU4 | TMDR1 | — | — | BFB | BFA | MD[3:0] | | | |
| MTU3 | TIORH | IOB[3:0] | | | | IOA[3:0] | | | |
| MTU3 | TIORL | IOD[3:0] | | | | IOC[3:0] | | | |
| MTU4 | TIORH | IOB[3:0] | | | | IOA[3:0] | | | |
| MTU4 | TIORL | IOD[3:0] | | | | IOC[3:0] | | | |
| MTU3 | TIER | TTGE | — | — | TCIEV | TGIED | TGIEC | TGIEB | TGIEA |
| MTU4 | TIER | TTGE | TTGE2 | — | TCIEV | TGIED | TGIEC | TGIEB | TGIEA |
| MTU | TOERA | — | — | OE4D | OE4C | OE3D | OE4B | OE4A | OE3B |
| MTU | TGCRA | — | BDC | N | P | FB | WF | VF | UF |
| MTU | TOCR1A | — | PSYE | — | — | TOCL | TOCS | OLSN | OLSP |
| MTU | TOCR2A | BF[1:0] | | OLS3N | OLS3P | OLS2N | OLS2P | OLS1N | OLS1P |
| MTU3 | TCNT | | | | | | | | |
| MTU4 | TCNT | | | | | | | | |
| MTU | TCDRA | | | | | | | | |
| MTU | TDDRA | | | | | | | | |

**Table 4.2 List of I/O Registers (Bit Order) (25 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| GPT0 | GTDBU | | | | | | | | |
| | | | | | | | | | |
| GPT0 | GTDBD | | | | | | | | |
| | | | | | | | | | |
| GPT0 | GTSOS | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | SOS[1:0] | |
| GPT0 | GTSOTR | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | — | SOTR |
| GPT1 | GTIOR | OBHLD | OBDFLT | GTIOB[5:0] | | | | | |
| | | OAHLD | OADFLT | GTIOA[5:0] | | | | | |
| GPT1 | GTINTAD | ADTRBDEN | ADTRBUEN | ADTRADEN | ADTRAUEN | EINT | — | — | — |
| | | GTINTPR[1:0] | | GTINTF | GTINTE | GTINTD | GTINTC | GTINTB | GTINTA |
| GPT1 | GTCR | — | — | CCLR[1:0] | | — | — | TPCS[1:0] | |
| | | — | — | — | — | — | MD[2:0] | | |
| GPT1 | GTBER | — | ADTDB | ADTTB[1:0] | | — | ADTDA | ADTTA[1:0] | |
| | | — | CCRSWT | PR[1:0] | | CCRB[1:0] | | CCRA[1:0] | |
| GPT1 | GTUDC | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | — | UDF | UD |
| GPT1 | GTITC | — | ADTBL | — | ADTAL | — | IVTT[2:0] | | |
| | | IVTC[1:0] | | ITLF | ITLE | ITLD | ITLC | ITLB | ITLA |
| GPT1 | GTST | TUCF | — | — | — | DTEF | ITCNT[2:0] | | |
| | | TCFPU | TCFPO | TCFF | TCFE | TCFD | TCFC | TCFB | TCFA |
| GPT1 | GTCNT | | | | | | | | |
| | | | | | | | | | |
| GPT1 | GTCCRA | | | | | | | | |
| | | | | | | | | | |
| GPT1 | GTCCRB | | | | | | | | |
| | | | | | | | | | |
| GPT1 | GTCCRC | | | | | | | | |
| | | | | | | | | | |
| GPT1 | GTCCRD | | | | | | | | |
| | | | | | | | | | |
| GPT1 | GTCCRE | | | | | | | | |
| | | | | | | | | | |
| GPT1 | GTCCRF | | | | | | | | |
| | | | | | | | | | |
| GPT1 | GTPR | | | | | | | | |
| | | | | | | | | | |
| GPT1 | GTPBR | | | | | | | | |
| | | | | | | | | | |
| GPT1 | GTPDBR | | | | | | | | |
| | | | | | | | | | |
| GPT1 | GTADTRA | | | | | | | | |
| | | | | | | | | | |
| GPT1 | GTADTBRA | | | | | | | | |
| | | | | | | | | | |
| GPT1 | GTADTDBRA | | | | | | | | |
| | | | | | | | | | |
| GPT1 | GTADTRB | | | | | | | | |
| | | | | | | | | | |

**Table 4.2 List of I/O Registers (Bit Order) (29 / 30)**

| Module Abbreviation | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| GPT2 | GTDLYCR | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | DLYEN | DLYRST | DLLEN |
| GPT3 | GTDLYCR | — | — | — | — | — | — | — | — |
| | | — | — | — | — | — | DLYEN | DLYRST | DLLEN |
| GPT0 | GTDLYRA | — | — | — | — | — | — | — | — |
| | | — | — | — | DLY[4:0] | | | | |
| GPT0 | GTDLYRB | — | — | — | — | — | — | — | — |
| | | — | — | — | DLY[4:0] | | | | |
| GPT1 | GTDLYRA | — | — | — | — | — | — | — | — |
| | | — | — | — | DLY[4:0] | | | | |
| GPT1 | GTDLYRB | — | — | — | — | — | — | — | — |
| | | — | — | — | DLY[4:0] | | | | |
| GPT2 | GTDLYRA | — | — | — | — | — | — | — | — |
| | | — | — | — | DLY[4:0] | | | | |
| GPT2 | GTDLYRB | — | — | — | — | — | — | — | — |
| | | — | — | — | DLY[4:0] | | | | |
| GPT3 | GTDLYRA | — | — | — | — | — | — | — | — |
| | | — | — | — | DLY[4:0] | | | | |
| GPT3 | GTDLYRB | — | — | — | — | — | — | — | — |
| | | — | — | — | DLY[4:0] | | | | |
| GPT0 | GTDLYFA | — | — | — | — | — | — | — | — |
| | | — | — | — | DLY[4:0] | | | | |
| GPT0 | GTDLYFB | — | — | — | — | — | — | — | — |
| | | — | — | — | DLY[4:0] | | | | |
| GPT1 | GTDLYFA | — | — | — | — | — | — | — | — |
| | | — | — | — | DLY[4:0] | | | | |
| GPT1 | GTDLYFB | — | — | — | — | — | — | — | — |
| | | — | — | — | DLY[4:0] | | | | |
| GPT2 | GTDLYRA | — | — | — | — | — | — | — | — |
| | | — | — | — | DLY[4:0] | | | | |
| GPT2 | GTDLYFB | — | — | — | — | — | — | — | — |
| | | — | — | — | DLY[4:0] | | | | |
| GPT3 | GTDLYFA | — | — | — | — | — | — | — | — |
| | | — | — | — | DLY[4:0] | | | | |
| GPT3 | GTDLYFB | — | — | — | — | — | — | — | — |
| | | — | — | — | DLY[4:0] | | | | |
| FLASH | FMODR | — | — | — | FRDMD | — | — | — | — |
| FLASH | FASTAT | ROMAE | — | — | CMDLK | DFLAE | — | DFLRPE | DFLWPE |
| FLASH | FAEINT | ROMAEIE | — | — | CMDLKIE | DFLAEIE | — | DFLRPEIE | DFLWPEIE |
| FLASH | FRDYIE | — | — | — | — | — | — | — | FRDYIE |
| FLASH | DFLRE0 | KEY[7:0] | | | | | | | |
| | | DBRE07 | DBRE06 | DBRE05 | DBRE04 | DBRE03 | DBRE02 | DBRE01 | DBRE00 |
| FLASH | DFLRE1 | KEY[7:0] | | | | | | | |
| | | DBRE15 | DBRE14 | DBRE13 | DBRE12 | DBRE11 | DBRE10 | DBRE09 | DBRE08 |
| FLASH | DFLWE0 | KEY[7:0] | | | | | | | |
| | | DBWE07 | DBWE06 | DBWE05 | DBWE04 | DBWE03 | DBWE02 | DBWE01 | DBWE00 |
| FLASH | DFLWE1 | KEY[7:0] | | | | | | | |
| | | DBWE15 | DBWE14 | DBWE13 | DBWE12 | DBWE11 | DBWE10 | DBWE09 | DBWE08 |
| FLASH | FCURAME | KEY[7:0] | | | | | | | |
| | | — | — | — | — | — | — | — | FCRME |

## 5.3 AC Characteristics

**Table 5.6 Operation Frequency Value**

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

| Item | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Operating frequency | System clock (ICLK) | f | 8 | - | 100 | MHz |
| | Peripheral module clock (PCLK) | | 8 | - | 50 | |

### 5.3.1 Clock Timing

**Table 5.7 Clock Timing**

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC
Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

| Item | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| Oscillation settling time after reset (crystal) | $t_{OSC1}$ | 10 | - | ms | Figure 5.1 |
| Oscillation settling time after leaving software standby mode (crystal) | $t_{OSC2}$ | 10 | - | ms | Figure 5.2 |
| Oscillation settling time after leaving deep software standby mode (crystal) | $t_{OSC3}$ | 10 | - | ms | Figure 5.3 |
| EXTAL external clock output delay settling time | $t_{DEXT}$ | 1 | - | ms | Figure 5.1 |
| EXTAL external clock input low pulse width | $t_{EXL}$ | 35 | - | ns | Figure 5.4 |
| EXTAL external clock input high pulse width | $t_{EXH}$ | 35 | - | ns | |
| EXTAL external clock rising time | $t_{EXr}$ | - | 5 | ns | |
| EXTAL external clock falling time | $t_{EXf}$ | - | 5 | ns | |
| On-chip oscillator (IWDTCLK) oscillation frequency | $f_{IWDTCLK}$ | 62.5 | 187.5 | kHz | |

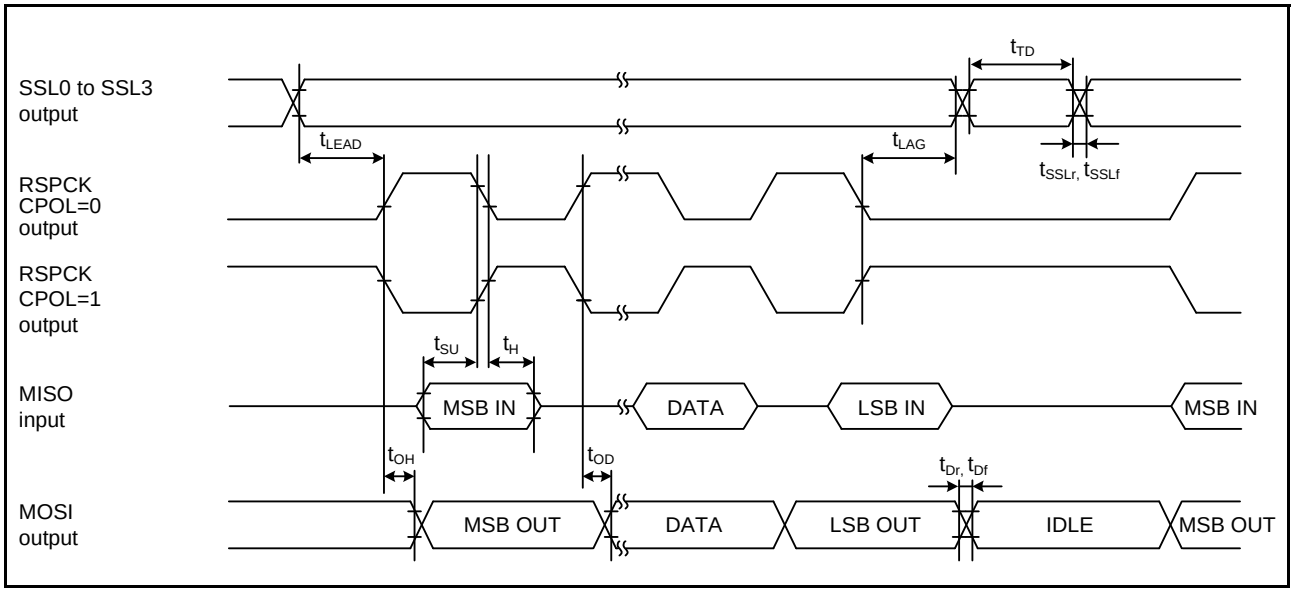



**Figure 5.13 RSPI Timing (Master, CPHA = 1)**

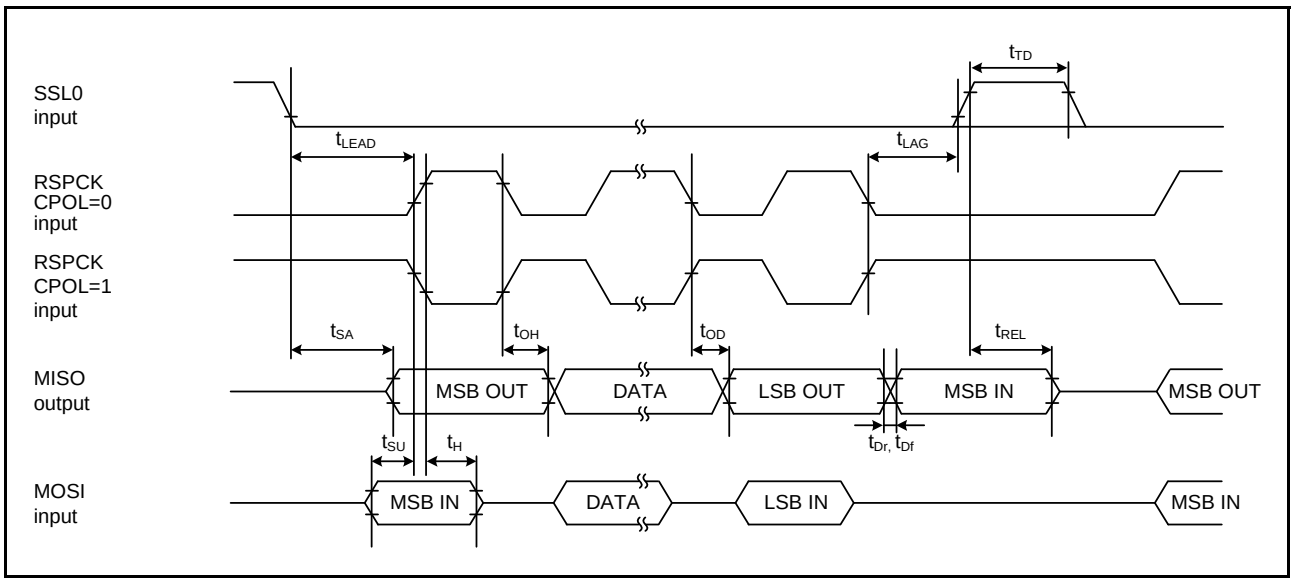



**Figure 5.14 RSPI Timing (Slave, CPHA = 0)**

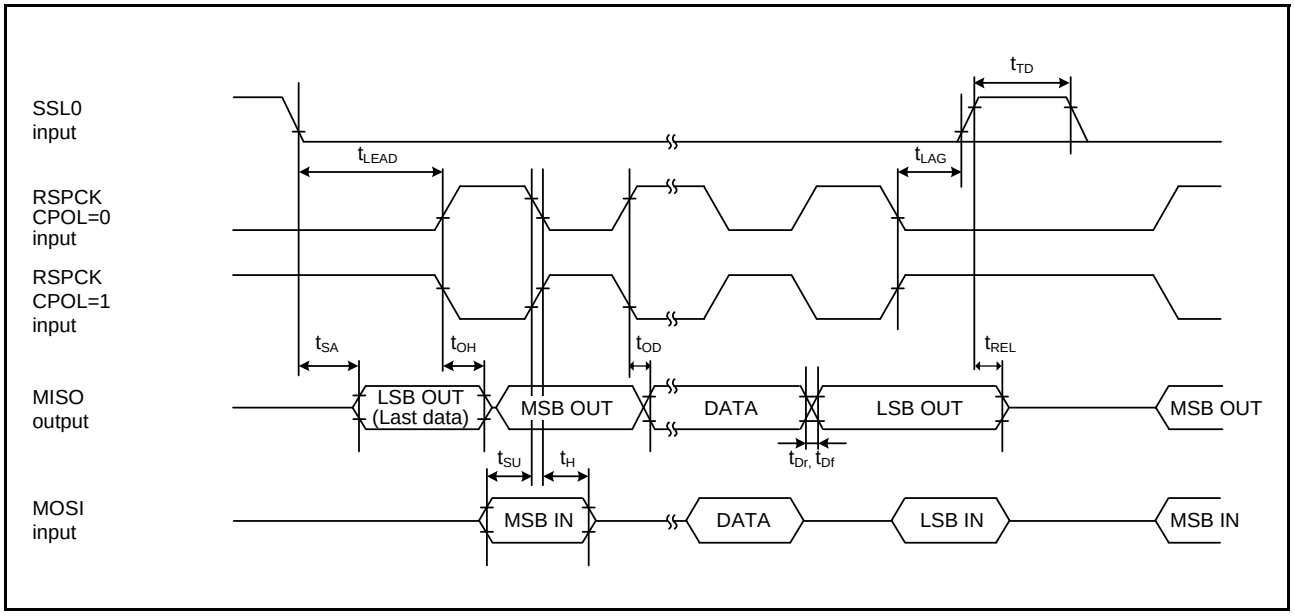



**Figure 5.15 RSPI Timing (Slave, CPHA = 1)**

**Table 5.17 Characteristics of the Programmable Gain Amplifier**

Note:Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

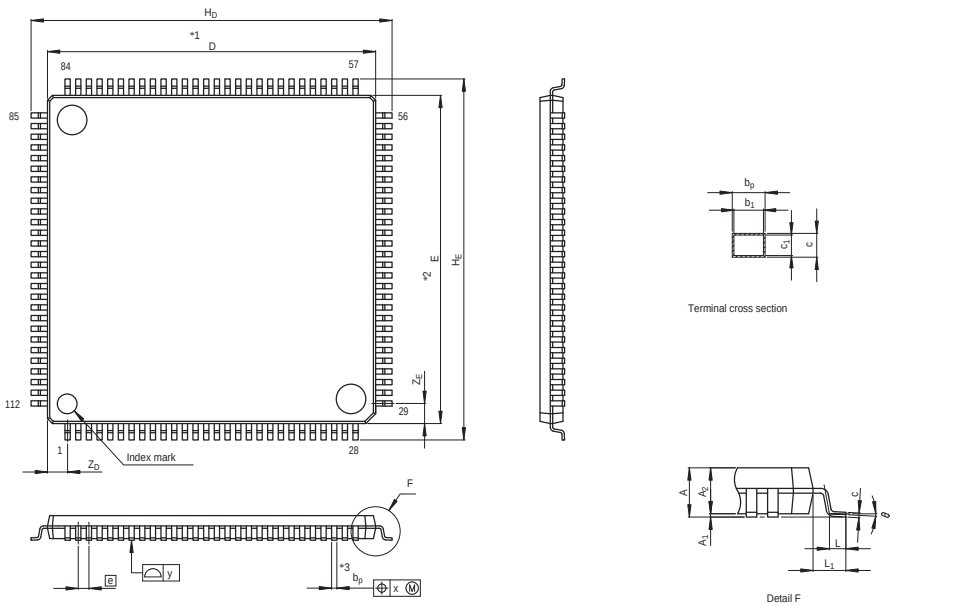
Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Analog input capacitance | | Cin | - | - | 6 | pF | |
| Input offset voltage | | Voff | - | - | 8 | mV | |
| Input voltage range (Vin) | Gain × 2.000 | Vin | 0.050 x AVcc | - | 0.450 x AVcc | V | |
| | Gain × 2.500 | | 0.047 x AVcc | - | 0.360 x AVcc | | |
| | Gain × 3.077 | | 0.045 x AVcc | - | 0.292 x AVcc | | |
| | Gain × 3.636 | | 0.042 x AVcc | - | 0.247 x AVcc | | |
| | Gain × 4.000 | | 0.040 x AVcc | - | 0.212 x AVcc | | |
| | Gain × 4.444 | | 0.036 x AVcc | - | 0.191 x AVcc | | |
| | Gain × 5.000 | | 0.033 x AVcc | - | 0.170 x AVcc | | |
| | Gain × 5.714 | | 0.031 x AVcc | - | 0.148 x AVcc | | |
| | Gain × 6.667 | | 0.029 x AVcc | - | 0.127 x AVcc | | |
| | Gain × 10.000 | | 0.025 x AVcc | - | 0.08 x AVcc | | |
| | Gain × 13.333 | | 0.023 x AVcc | - | 0.06 x AVcc | | |
| Slew rate | | SR | 10 | - | - | V/μs | |
| Gain error | Gain × 2.000 | - | - | - | 1 | % | |
| | Gain × 2.500 | | - | - | 1 | | |
| | Gain × 3.077 | | - | - | 1 | | |
| | Gain × 3.636 | | - | - | 1.5 | | |
| | Gain × 4.000 | | - | - | 1.5 | | |
| | Gain × 4.444 | | - | - | 2 | | |
| | Gain × 5.000 | | - | - | 2 | | |
| | Gain × 5.714 | | - | - | 2 | | |
| | Gain × 6.667 | | - | - | 3 | | |
| | Gain × 10.000 | | - | - | 4 | | |
| | Gain × 13.333 | | - | - | 4 | | |

# Appendix 1.Package Dimensions

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LQFP112-20x20-0.65 | PLQP0112JA-A | FP-112E / FP-112EV | 1.2g |

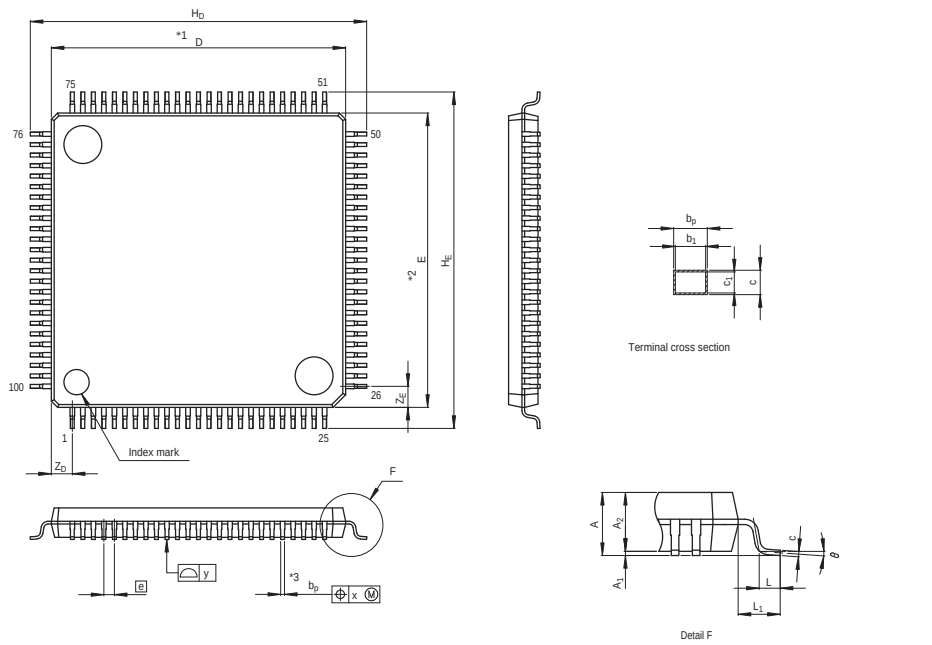



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 19.9 | 20.0 | 20.1 |
| E | 19.9 | 20.0 | 20.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 21.8 | 22.0 | 22.2 |
| $H_E$ | 21.8 | 22.0 | 22.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | 0.1 | 0.15 |
| $b_p$ | 0.27 | 0.32 | 0.37 |
| $b_1$ | — | 0.30 | — |
| c | 0.09 | 0.145 | 0.20 |
| $c_1$ | — | 0.125 | — |
| $\theta$ | 0° | — | 8° |
| e | — | 0.65 | — |
| x | — | — | 0.13 |
| y | — | — | 0.10 |
| $Z_D$ | — | 1.225 | — |
| $Z_E$ | — | 1.225 | — |
| L | 0.35 | 0.5 | 0.65 |
| $L_1$ | — | 1.0 | — |

Figure A 112-Pin LQFP (PLQP0112JA-A) Package Dimensions

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LQFP100-14x14-0.50 | PLQP0100KB-A | 100P6Q-A / FP-100U / FP-100UV | 0.6g |




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 13.9 | 14.0 | 14.1 |
| E | 13.9 | 14.0 | 14.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 15.8 | 16.0 | 16.2 |
| $H_E$ | 15.8 | 16.0 | 16.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | 0.1 | 0.15 |
| $b_p$ | 0.15 | 0.20 | 0.25 |
| $b_1$ | — | 0.18 | — |
| c | 0.09 | 0.145 | 0.20 |
| $c_1$ | — | 0.125 | — |
| $\theta$ | 0° | — | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $Z_D$ | — | 1.0 | — |
| $Z_E$ | — | 1.0 | — |
| L | 0.35 | 0.5 | 0.65 |
| $L_1$ | — | 1.0 | — |

Figure B 100-Pin LQFP (PLQP0100KB-A) Package Dimensions