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Details

Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I ² C, LINbus, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	61
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 12x10b, 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LQFP
Supplier Device Package	112-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f562tabdfh-v1

1.4 Pin Assignments

Figure 1.3 to Figure 1.7 show the pins assignments. Table 1.4 to Table 1.8 show the list of pins and pin functions.

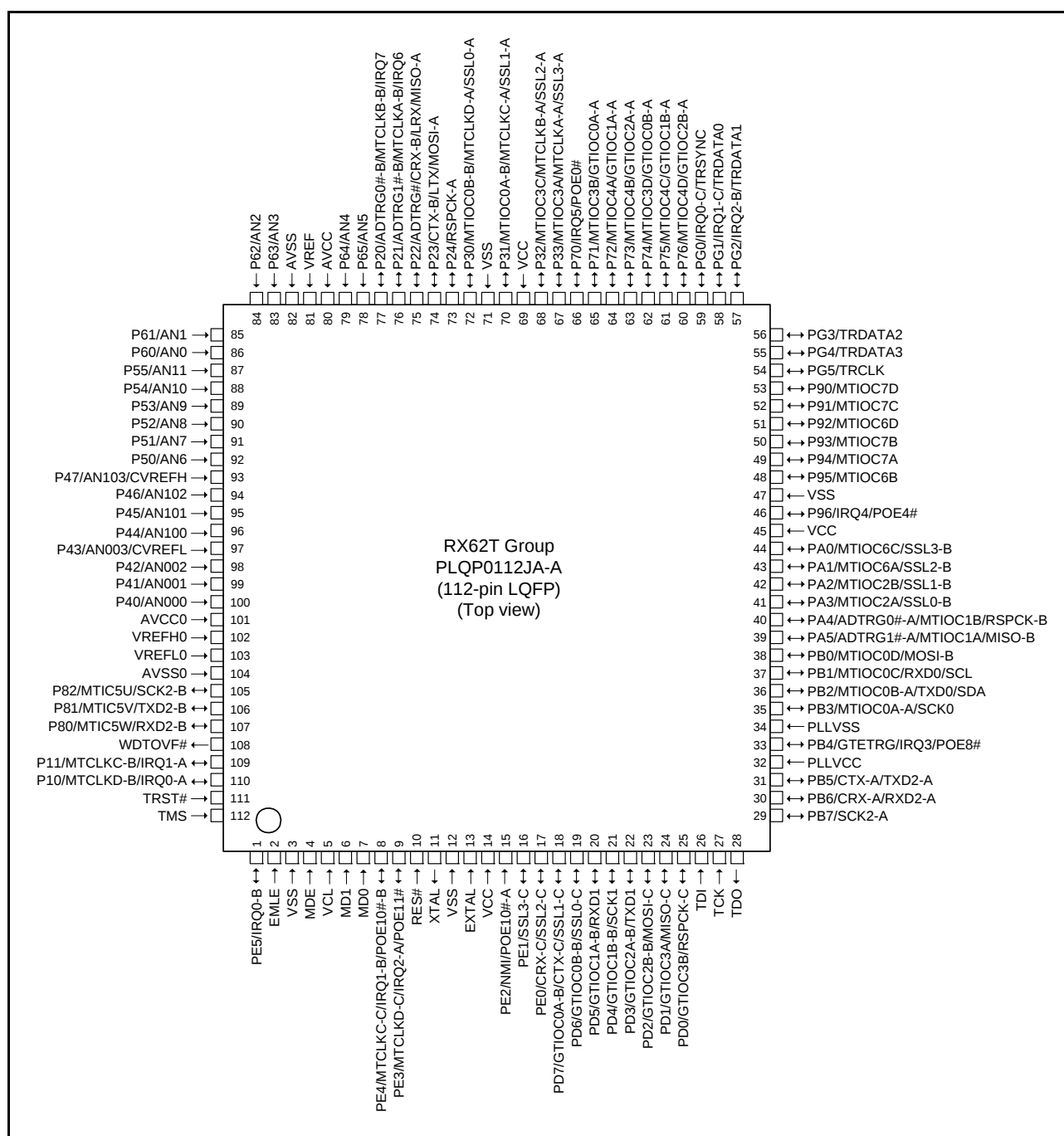


Figure 1.3 Pin Assignment of the 112-Pin LQFP

Table 1.4 List of Pins and Pin Functions (112-Pin LQFP) (1 / 3)

Pin No. (112-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi- cation	Interrupt	POE	Debugging
1		PE5				IRQ0-B		
2	EMLE							
3	VSS							
4	MDE							
5	VCL							
6	MD1							
7	MD0							
8		PE4		MTCLKC-C		IRQ1-B	POE10#-B	
9		PE3		MTCLKD-C		IRQ2-A	POE11#	
10	RES#							
11	XTAL							
12	VSS							
13	EXTAL							
14	VCC							
15		PE2				NMI	POE10#-A	
16		PE1			SSL3-C			
17		PE0			CRX-C/ SSL2-C			
18		PD7		GTIOC0A-B	CTX-C/ SSL1-C			
19		PD6		GTIOC0B-B	SSL0-C			
20		PD5		GTIOC1A-B	RXD1			
21		PD4		GTIOC1B-B	SCK1			
22		PD3		GTIOC2A-B	TXD1			
23		PD2		GTIOC2B-B	MOSI-C			
24		PD1		GTIOC3A	MISO-C			
25		PD0		GTIOC3B	RSPCK-C			
26								TDI
27								TCK
28								TDO
29		PB7			SCK2-A			
30		PB6			CRX-A/ RXD2-A			
31		PB5			CTX-A/ TXD2-A			
32	PLLVCC							
33		PB4		GTETRG		IRQ3	POE8#	
34	PLLVSS							
35		PB3		MTIOC0A-A	SCK0			
36		PB2		MTIOC0B-A	TXD0/SDA			
37		PB1		MTIOC0C	RXD0/SCL			
38		PB0		MTIOC0D	MOSI-B			
39		PA5	ADTRG1#-A	MTIOC1A	MISO-B			
40		PA4	ADTRG0#-A	MTIOC1B	RSPCK-B			
41		PA3		MTIOC2A	SSL0-B			
42		PA2		MTIOC2B	SSL1-B			
43		PA1		MTIOC6A	SSL2-B			

Table 1.4 List of Pins and Pin Functions (112-Pin LQFP) (2 / 3)

Pin No. (112-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi- cation	Interrupt	POE	Debugging
44		PA0		MTIOC6C	SSL3-B			
45	VCC							
46		P96				IRQ4	POE4#	
47	VSS							
48		P95		MTIOC6B				
49		P94		MTIOC7A				
50		P93		MTIOC7B				
51		P92		MTIOC6D				
52		P91		MTIOC7C				
53		P90		MTIOC7D				
54		PG5						TRCLK
55		PG4						TRDATA3
56		PG3						TRDATA2
57		PG2				IRQ2-B		TRDATA1
58		PG1				IRQ1-C		TRDATA0
59		PG0				IRQ0-C		TRSYNC
60		P76		MTIOC4D/ GTIOC2B-A				
61		P75		MTIOC4C/ GTIOC1B-A				
62		P74		MTIOC3D/ GTIOC0B-A				
63		P73		MTIOC4B/ GTIOC2A-A				
64		P72		MTIOC4A/ GTIOC1A-A				
65		P71		MTIOC3B/ GTIOC0A-A				
66		P70				IRQ5	POE0#	
67		P33		MTIOC3A/ MTCLKA-A	SSL3-A			
68		P32		MTIOC3C/ MTCLKB-A	SSL2-A			
69	VCC							
70		P31		MTIOC0A-B/ MTCLKC-A	SSL1-A			
71	VSS							
72		P30		MTIOC0B-B/ MTCLKD-A	SSL0-A			
73		P24			RSPCK-A			
74		P23			CTX-B/ LTX/ MOSI-A			
75		P22	ADTRG#		CRX-B/ LRX/ MISO-A			
76		P21	ADTRG1#-B	MTCLKA-B		IRQ6		
77		P20	ADTRG0#-B	MTCLKB-B		IRQ7		
78		P65	AN5					
79		P64	AN4					

Table 1.5 List of Pins and Pin Functions (100-Pin LQFP) (2 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi- cation	Interrupt	POE	Debugging
41		PA0		MTIOC6C	SSL3-B			
42	VCC							
43		P96				IRQ4	POE4#	
44	VSS							
45		P95		MTIOC6B				
46		P94		MTIOC7A				
47		P93		MTIOC7B				
48		P92		MTIOC6D				
49		P91		MTIOC7C				
50		P90		MTIOC7D				
51		P76		MTIOC4D/ GTIOC2B-A				
52		P75		MTIOC4C/ GTIOC1B-A				
53		P74		MTIOC3D/ GTIOC0B-A				
54		P73		MTIOC4B/ GTIOC2A-A				
55		P72		MTIOC4A/ GTIOC1A-A				
56		P71		MTIOC3B/ GTIOC0A-A				
57		P70				IRQ5	POE0#	
58		P33		MTIOC3A/ MTCLKA-A	SSL3-A			
59		P32		MTIOC3C/ MTCLKB-A	SSL2-A			
60	VCC							
61		P31		MTIOC0A-B/ MTCLKC-A	SSL1-A			
62	VSS							
63		P30		MTIOC0B-B/ MTCLKD-A	SSL0-A			
64		P24			RSPCK-A			
65		P23			CTX-B/ LTX/ MOSI-A			
66		P22	ADTRG#		CRX-B/ LRX/ MISO-A			
67		P21	ADTRG1#-B	MTCLKA-B		IRQ6		
68		P20	ADTRG0#-B	MTCLKB-B		IRQ7		
69		P65	AN5					
70		P64	AN4					
71	AVCC							
72	VREF							
73	AVSS							
74		P63	AN3					
75		P62	AN2					
76		P61	AN1					

Table 1.5 List of Pins and Pin Functions (100-Pin LQFP) (3 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi- cation	Interrupt	POE	Debugging
77		P60	AN0					
78		P55	AN11					
79		P54	AN10					
80		P53	AN9					
81		P52	AN8					
82		P51	AN7					
83		P50	AN6					
84		P47	AN103/ CVREFH					
85		P46	AN102					
86		P45	AN101					
87		P44	AN100					
88		P43	AN003/ CVREFL					
89		P42	AN002					
90		P41	AN001					
91		P40	AN000					
92	AVCC0							
93	VREFH0							
94	VREFL0							
95	AVSS0							
96		P82		MTIC5U	SCK2-B			
97		P81		MTIC5V	TXD2-B			
98		P80		MTIC5W	RXD2-B			
99		P11		MTCLKC-B		IRQ1-A		
100		P10		MTCLKD-B		IRQ0-A		

Table 1.6 List of Pins and Pin Functions (80-Pin LQFP) (1 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi- cation	Interrupt	POE	Debugging
1	EMLE							
2	VSS							
3	MDE							
4	VCL							
5	MD1							
6	MD0							
7		PE4		MTCLKC-C		IRQ1-B	POE10#-B	
8		PE3		MTCLKD-C		IRQ2-A	POE11#	
9	RES#							
10	XTAL							
11	VSS							
12	EXTAL							
13	VCC							
14		PE2				NMI	POE10#-A	
15		PE0			CRX-C			
16		PD7		GTIOC0A-B	CTX-C			TRST#
17		PD6		GTIOC0B-B				TMS
18		PD5		GTIOC1A-B	RXD1			TDI
19		PD4		GTIOC1B-B	SCK1			TCK
20		PD3		GTIOC2A-B	TXD1			TDO
21		PB7			SCK2-A			
22		PB6			CRX-A/ RXD2-A			
23		PB5			CTX-A/ TXD2-A			
24	PLLVC							
25		PB4		GTETRG		IRQ3	POE8#	
26	PLLVS							
27		PB3		MTIOC0A-A	SCK0			
28		PB2		MTIOC0B-A	TXD0/SDA			
29		PB1		MTIOC0C	RXD0/SCL			
30		PB0		MTIOC0D	MOSI-B			
31		PA3		MTIOC2A	SSL0-B			
32		PA2		MTIOC2B	SSL1-B			
33	VCC							
34		P96				IRQ4	POE4#	
35	VSS							
36		P95		MTIOC6B				
37		P94		MTIOC7A				
38		P93		MTIOC7B				
39		P92		MTIOC6D				
40		P91		MTIOC7C				
41		P76		MTIOC4D/ GTIOC2B-A				

Table 1.6 List of Pins and Pin Functions (80-Pin LQFP) (2 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communi- cation	Interrupt	POE	Debugging
42		P75		MTIOC4C/ GTIOC1B-A				
43		P74		MTIOC3D/ GTIOC0B-A				
44		P73		MTIOC4B/ GTIOC2A-A				
45		P72		MTIOC4A/ GTIOC1A-A				
46		P71		MTIOC3B/ GTIOC0A-A				
47		P70				IRQ5	POE0#	
48		P33		MTIOC3A/ MTCLKA-A	SSL3-A			
49		P32		MTIOC3C/ MTCLKB-A	SSL2-A			
50	VCC							
51		P31		MTIOC0A-B/ MTCLKC-A	SSL1-A			
52	VSS							
53		P30		MTIOC0B-B/ MTCLKD-A	SSL0-A			
54		P24			RSPCK-A			
55		P23			CTX-B/ LTX/ MOSI-A			
56		P22	ADTRG#		CRX-B/ LRX/ MISO-A			
57		P21	ADTRG1#-B	MTCLKA-B		IRQ6		
58		P20	ADTRG0#-B	MTCLKB-B		IRQ7		
59	AVCC							
60	AVSS							
61		P63	AN3					
62		P62	AN2					
63		P61	AN1					
64		P60	AN0					
65		P47	AN103/ CVREFH					
66		P46	AN102					
67		P45	AN101					
68		P44	AN100					
69		P43	AN003/ CVREFL					
70		P42	AN002					
71		P41	AN001					
72		P40	AN000					
73	AVCC0							
74	VREFH0							
75	VREFL0							

Table 1.7 List of Pins and Pin Functions (80-Pin LQFP: R5F562TxGDFF) (1 / 3)

Pin No. (80-Pin LQFP)	Power Supply Clock System Control	I/O Port	Analog	Timer	Communication	Interrupt	POE	Debugging
1	EMLE							
2	VSS							
3	MDE							
4	VCL							
5	MD1							
6	MD0							
7		PE4		MTCLKC-C		IRQ1-B	POE10#-B	
8		PE3		MTCLKD-C		IRQ2-A	POE11#	
9	RES#							
10	XTAL							
11	VSS							
12	EXTAL							
13	VCC							
14		PE2				NMI	POE10#-A	
15		PD7		GTIOC0A-B				TRST#
16		PD6		GTIOC0B-B				TMS
17		PD5		GTIOC1A-B	RXD1			TDI
18		PD4		GTIOC1B-B	SCK1			TCK
19		PD3		GTIOC2A-B	TXD1			TDO
20		PD2		GTIOC2B-B				
21		PB7			SCK2-A			
22		PB6			CRX-A/ RXD2-A			
23		PB5			CTX-A/ TXD2-A			
24	PLLVC							
25		PB4		GTETR		IRQ3	POE8#	
26	PLLVS							
27		PB3		MTIOC0A-A	SCK0			
28		PB2		MTIOC0B-A	TXD0/SDA			
29		PB1		MTIOC0C	RXD0/SCL			
30		PB0		MTIOC0D				
31		PA5	ADTRG1#-A	MTIOC1A				
32		PA3		MTIOC2A				
33	VCC							
34		P96				IRQ4	POE4#	
35	VSS							
36		P95		MTIOC6B				
37		P94		MTIOC7A				
38		P93		MTIOC7B				
39		P92		MTIOC6D				
40		P91		MTIOC7C				
41		P90		MTIOC7D				

2. CPU

The RX CPU has sixteen general-purpose registers, nine control registers, and one accumulator used for DSP instructions.

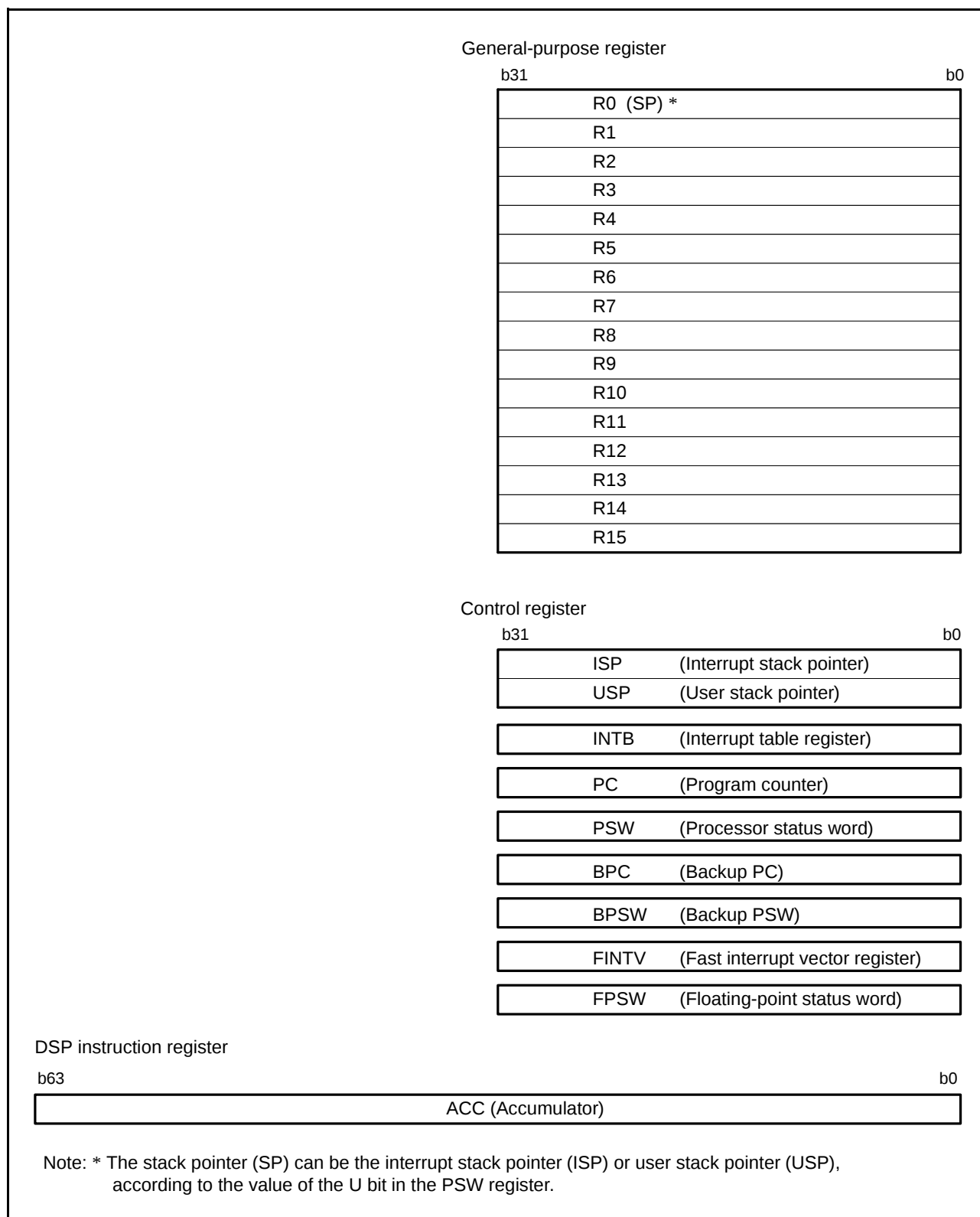


Figure 2.1 Register Set of the CPU

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
0008 0000h	SYSTEM	Mode monitor register	MDMONR	16	16	3 ICLK
0008 0002h	SYSTEM	Mode status register	MDSR	16	16	3 ICLK
0008 0006h	SYSTEM	System control register 0	SYSCR0	16	16	3 ICLK
0008 0008h	SYSTEM	System control register 1	SYSCR1	16	16	3 ICLK
0008 000Ch	SYSTEM	Standby control register	SBYCR	16	16	3 ICLK
0008 0010h	SYSTEM	Module stop control register A	MSTPCRA	32	32	3 ICLK
0008 0014h	SYSTEM	Module stop control register B	MSTPCRB	32	32	3 ICLK
0008 0018h	SYSTEM	Module stop control register C	MSTPCRC	32	32	3 ICLK
0008 0020h	SYSTEM	System clock control register	SCKCR	32	32	3 ICLK
0008 0040h	SYSTEM	Oscillation stop detection control register	OSTDCR	16	16	3 ICLK
0008 1300h	BSC	Bus error status clear register	BERCLR	8	8	2 ICLK
0008 1304h	BSC	Bus error monitoring enable register	BEREN	8	8	2 ICLK
0008 1308h	BSC	Bus error status register 1	BERSR1	8	8	2 ICLK
0008 130Ah	BSC	Bus error status register 2	BERSR2	16	16	2 ICLK
0008 2400h	DTC	DTC control register	DTCCR	8	8	2 ICLK
0008 2404h	DTC	DTC vector base register	DTCVBR	32	32	2 ICLK
0008 2408h	DTC	DTC address mode register	DTCADMOD	8	8	2 ICLK
0008 240Ch	DTC	DTC module start register	DTCST	8	8	2 ICLK
0008 240Eh	DTC	DTC status register	DTCSTS	16	16	2 ICLK
0008 6400h	MPU	Region 0 start page-number register	RSPAGE0	32	32	1 ICLK
0008 6404h	MPU	Region 0 end page-number register	REPAGE0	32	32	1 ICLK
0008 6408h	MPU	Region 1 start page-number register	RSPAGE1	32	32	1 ICLK
0008 640Ch	MPU	Region 1 end page-number register	REPAGE1	32	32	1 ICLK
0008 6410h	MPU	Region 2 start page-number register	RSPAGE2	32	32	1 ICLK
0008 6414h	MPU	Region 2 end page-number register	REPAGE2	32	32	1 ICLK
0008 6418h	MPU	Region 3 start page-number register	RSPAGE3	32	32	1 ICLK
0008 641Ch	MPU	Region 3 end page-number register	REPAGE3	32	32	1 ICLK
0008 6420h	MPU	Region 4 start page-number register	RSPAGE4	32	32	1 ICLK
0008 6424h	MPU	Region 4 end page-number register	REPAGE4	32	32	1 ICLK
0008 6428h	MPU	Region 5 start page-number register	RSPAGE5	32	32	1 ICLK
0008 642Ch	MPU	Region 5 end page-number register	REPAGE5	32	32	1 ICLK
0008 6430h	MPU	Region 6 start page-number register	RSPAGE6	32	32	1 ICLK
0008 6434h	MPU	Region 6 end page-number register	REPAGE6	32	32	1 ICLK
0008 6438h	MPU	Region 7 start page-number register	RSPAGE7	32	32	1 ICLK
0008 643Ch	MPU	Region 7 end page-number register	REPAGE7	32	32	1 ICLK
0008 6500h	MPU	Memory-protection enable register	MPEN	32	32	1 ICLK
0008 6504h	MPU	Background access control register	MPBAC	32	32	1 ICLK
0008 6508h	MPU	Memory-protection error status-clearing register	MPECLR	32	32	1 ICLK
0008 650Ch	MPU	Memory-protection error status register	MPESTS	32	32	1 ICLK
0008 6514h	MPU	Data memory-protection error address register	MPDEA	32	32	1 ICLK
0008 6520h	MPU	Region search address register	MPSA	32	32	1 ICLK
0008 6524h	MPU	Region search operation register	MPOPS	16	16	1 ICLK

Table 4.1 List of I/O Registers (Address Order) (19 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000C 1A39h	MTU7	Timer buffer operation transfer mode register	TBTM	8	8	5 ICLK
000C 1A3Ah	MTU	Timer interrupt skipping mode register B	TITMRB	8	8	5 ICLK
000C 1A3Bh	MTU	Timer interrupt skipping set register 2B	TITCR2B	8	8	5 ICLK
000C 1A3Ch	MTU	Timer interrupt skipping counter 2B	TITCNT2B	8	8	5 ICLK
000C 1A40h	MTU7	Timer A/D converter start request control register	TADCR	16	16	5 ICLK
000C 1A44h	MTU7	Timer A/D converter start request cycle set register A	TADCORA	16	16, 32	5 ICLK
000C 1A46h	MTU7	Timer A/D converter start request cycle set register B	TADCORB	16	16	5 ICLK
000C 1A48h	MTU7	Timer A/D converter start request cycle set buffer register A	TADCOBRA	16	16, 32	5 ICLK
000C 1A4Ah	MTU7	Timer A/D converter start request cycle set buffer register B	TADCOBRB	16	16	5 ICLK
000C 1A50h	MTU6	Timer synchronous clear register	TSYCR	8	8	5 ICLK
000C 1A60h	MTU	Timer waveform control register B	TWCRB	8	8	5 ICLK
000C 1A70h	MTU	Timer mode register 2B	TMDR2B	8	8	5 ICLK
000C 1A72h	MTU6	Timer general register E	TGRE	16	16	5 ICLK
000C 1A74h	MTU7	Timer general register E	TGRE	16	16	5 ICLK
000C 1A76h	MTU7	Timer general register F	TGRF	16	16	5 ICLK
000C 1A80h	MTU	Timer start register B	TSTRB	8	8, 16	5 ICLK
000C 1A81h	MTU	Timer synchronous register B	TSYRB	8	8	5 ICLK
000C 1A84h	MTU	Timer read/write enable register B	TRWERB	8	8	5 ICLK
000C 1C80h	MTU5	Timer counter U	TCNTU	16	16, 32	5 ICLK
000C 1C82h	MTU5	Timer general register U	TGRU	16	16	5 ICLK
000C 1C84h	MTU5	Timer control register U	TCRU	8	8	5 ICLK
000C 1C86h	MTU5	Timer I/O control register U	TIORU	8	8	5 ICLK
000C 1C90h	MTU5	Timer counter V	TCNTV	16	16, 32	5 ICLK
000C 1C92h	MTU5	Timer general register V	TGRV	16	16	5 ICLK
000C 1C94h	MTU5	Timer control register V	TCRV	8	8	5 ICLK
000C 1C96h	MTU5	Timer I/O control register V	TIORV	8	8	5 ICLK
000C 1CA0h	MTU5	Timer counter W	TCNTW	16	16, 32	5 ICLK
000C 1CA2h	MTU5	Timer general register W	TGRW	16	16	5 ICLK
000C 1CA4h	MTU5	Timer control register W	TCRW	8	8	5 ICLK
000C 1CA6h	MTU5	Timer I/O control register W	TIORW	8	8	5 ICLK
000C 1CB0h	MTU5	Timer status register	TSR	8	8	5 ICLK
000C 1CB2h	MTU5	Timer interrupt enable register	TIER	8	8	5 ICLK
000C 1CB4h	MTU5	Timer start register	TSTR	8	8	5 ICLK
000C 1CB6h	MTU5	Timer compare match clear register	TCNTCMPCLR	8	8	5 ICLK
000C 2000h	GPT	General PWM timer software start register	GTSTR	16	8, 16, 32	3 to 5 ICLK*4
000C 2004h	GPT	General PWM timer hardware source start control register	GTHSCR	16	8, 16, 32	3 to 5 ICLK*4
000C 2006h	GPT	General PWM timer hardware source clear control register	GTHCCR	16	8, 16, 32	3 to 5 ICLK*4
000C 2008h	GPT	General PWM timer hardware start source select register	GTHSSR	16	8, 16, 32	3 to 5 ICLK*4

Table 4.1 List of I/O Registers (Address Order) (24 / 25)

Address	Module Abbreviation	Register Name	Register Abbreviation	Number of Bits	Access Size	Number of Access Cycles
000C 22B6h	GPT3	General PWM timer dead time control register	GTDTCR	16	16, 32	3 to 5 ICLK ^{*4}
000C 22B8h	GPT3	General PWM timer dead time value register	GTDVU	16	16, 32	3 to 5 ICLK ^{*4}
000C 22BAh	GPT3	General PWM timer dead time value register	GTDVD	16	16, 32	3 to 5 ICLK ^{*4}
000C 22BCh	GPT3	General PWM timer dead time buffer register	GTDBU	16	16, 32	3 to 5 ICLK ^{*4}
000C 22BEh	GPT3	General PWM timer dead time buffer register	GTDBD	16	16, 32	3 to 5 ICLK ^{*4}
000C 22C0h	GPT3	General PWM timer output protection function status register	GTSOS	16	16, 32	3 to 5 ICLK ^{*4}
000C 22C2h	GPT3	General PWM timer output protection temporary release register	GTSOTR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2300h	GPT0	PWM output delay control register	GTDLYCR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2302h	GPT1	PWM output delay control register	GTDLYCR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2304h	GPT2	PWM output delay control register	GTDLYCR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2306h	GPT3	PWM output delay control register	GTDLYCR	16	16, 32	3 to 5 ICLK ^{*4}
000C 2318h	GPT0	GTIOCA rising output delay register	GTDLYRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 231Ah	GPT0	GTIOCB rising output delay register	GTDLYRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 231Ch	GPT1	GTIOCA rising output delay register	GTDLYRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 231Eh	GPT1	GTIOCB rising output delay register	GTDLYRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2320h	GPT2	GTIOCA rising output delay register	GTDLYRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 2322h	GPT2	GTIOCB rising output delay register	GTDLYRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2324h	GPT3	GTIOCA falling output delay register	GTDLYRA	16	16, 32	3 to 5 ICLK ^{*4}
000C 2326h	GPT3	GTIOCB falling output delay register	GTDLYRB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2328h	GPT0	GTIOCA falling output delay register	GTDLYFA	16	16, 32	3 to 5 ICLK ^{*4}
000C 232Ah	GPT0	GTIOCB falling output delay register	GTDLYFB	16	16, 32	3 to 5 ICLK ^{*4}
000C 232Ch	GPT1	GTIOCA falling output delay register	GTDLYFA	16	16, 32	3 to 5 ICLK ^{*4}
000C 232Eh	GPT1	GTIOCB falling output delay register	GTDLYFB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2330h	GPT2	GTIOCA falling output delay register	GTDLYFA	16	16, 32	3 to 5 ICLK ^{*4}
000C 2332h	GPT2	GTIOCB falling output delay register	GTDLYFB	16	16, 32	3 to 5 ICLK ^{*4}
000C 2334h	GPT3	GTIOCA falling output delay register	GTDLYFA	16	16, 32	3 to 5 ICLK ^{*4}
000C 2336h	GPT3	GTIOCB falling output delay register	GTDLYFB	16	16, 32	3 to 5 ICLK ^{*4}
007F C402h	FLASH	Flash mode register	FMODR	8	8	2, 3 PCLK ^{*3}
007F C410h	FLASH	Flash access status register	FASTAT	8	8	2, 3 PCLK ^{*3}
007F C411h	FLASH	Flash access error interrupt enable register	FAEINT	8	8	2, 3 PCLK ^{*3}
007F C412h	FLASH	Flash ready interrupt enable register	FRDYIE	8	8	2, 3 PCLK ^{*3}
007F C440h	FLASH	Data flash read enable register 0	DFLRE0	16	16	2, 3 PCLK ^{*3}
007F C442h	FLASH	Data flash read enable register 1	DFLRE1	16	16	2, 3 PCLK ^{*3}
007F C450h	FLASH	Data flash programming/erasure enable register 0	DFLWE0	16	16	2, 3 PCLK ^{*3}
007F C452h	FLASH	Data flash programming/erasure enable register 1	DFLWE1	16	16	2, 3 PCLK ^{*3}
007F C454h	FLASH	FCU RAM enable register	FCURAME	16	16	2, 3 PCLK ^{*3}
007F FFB0h	FLASH	Flash status register 0	FSTATR0	8	8	2, 3 PCLK ^{*3}
007F FFB1h	FLASH	Flash status register 1	FSTATR1	8	8	2, 3 PCLK ^{*3}
007F FFB2h	FLASH	Flash P/E mode entry register	FENTRYR	16	16	2, 3 PCLK ^{*3}
007F FFB4h	FLASH	Flash protect register	FPROTR	16	16	2, 3 PCLK ^{*3}
007F FFB6h	FLASH	Flash reset register	FRESETR	16	16	2, 3 PCLK ^{*3}

Table 4.2 List of I/O Registers (Bit Order) (2 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
MPU	REPAGE0					REPN[27:0]			
						REPN[27:0]			
						REPN[27:0]			
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE1					RSPN[27:0]			
						RSPN[27:0]			
						RSPN[27:0]			
			RSPN[27:0]			—	—	—	—
MPU	REPAGE1					REPN[27:0]			
						REPN[27:0]			
						REPN[27:0]			
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE2					RSPN[27:0]			
						RSPN[27:0]			
						RSPN[27:0]			
			RSPN[27:0]			—	—	—	—
MPU	REPAGE2					REPN[27:0]			
						REPN[27:0]			
						REPN[27:0]			
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE3					RSPN[27:0]			
						RSPN[27:0]			
						RSPN[27:0]			
			RSPN[27:0]			—	—	—	—
MPU	REPAGE3					REPN[27:0]			
						REPN[27:0]			
						REPN[27:0]			
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE4					RSPN[27:0]			
						RSPN[27:0]			
						RSPN[27:0]			
			RSPN[27:0]			—	—	—	—
MPU	REPAGE4					REPN[27:0]			
						REPN[27:0]			
						REPN[27:0]			
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE5					RSPN[27:0]			
						RSPN[27:0]			
						RSPN[27:0]			
			RSPN[27:0]			—	—	—	—
MPU	REPAGE5					REPN[27:0]			
						REPN[27:0]			
						REPN[27:0]			
			REPN[27:0]				UAC[2:0]		V
MPU	RSPAGE6					RSPN[27:0]			
						RSPN[27:0]			
						RSPN[27:0]			
			RSPN[27:0]			—	—	—	—
MPU	REPAGE6					REPN[27:0]			
						REPN[27:0]			
						REPN[27:0]			
			REPN[27:0]				UAC[2:0]		V

Table 4.2 List of I/O Registers (Bit Order) (11 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
SCI1	SEMR	—	—	NFEN	ABCS	—	—	—	—
SMCI1	SMR	GM	BLK	PE	PM	(BCP[1:0])			CKS[1:0]
SMCI1	BRR								
SMCI1	SCR	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
SMCI1	TDR								
SMCI1	SSR	TDRE	RDRF	ORER	ERS	PER	TEND	MPB	MPBT
SMCI1	RDR								
SMCI1	SCMR	BCP2	—	—	—	SDIR	SINV	—	SMIF
SCI2	SMR	CM	CHR	PE	PM	STOP	MP	CKS[1:0]	
SCI2	BRR								
SCI2	SCR	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
SCI2	TDR								
SCI2	SSR	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
SCI2	RDR								
SCI2	SCMR	BCP2	—	—	—	SDIR	SINV	—	SMIF
SMCI2	SMR	GM	BLK	PE	PM	(BCP[1:0])			CKS[1:0]
SMCI2	BRR								
SMCI2	SCR	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
SMCI2	TDR								
SMCI2	SSR	TDRE	RDRF	ORER	ERS	PER	TEND	MPB	MPBT
SMCI2	RDR								
SMCI2	SCMR	BCP2	—	—	—	SDIR	SINV	—	SMIF
CRC	CRCCR	DORCLR	—	—	—	—	LMS	GPS[1:0]	
CRC	CRCDIR								
CRC	CRCDOR								
RIIC0	ICCR1	ICE	IICRST	CLO	SOWP	SCLO	SDAO	SCLI	SDAI
RIIC0	ICCR2	BBSY	MST	TRS	—	SP	RS	ST	—
RIIC0	ICMR1	MTWP	CKS[2:0]			BCWP		BC[2:0]	
RIIC0	ICMR2	DLCS	SDDL[2:0]			TMWE	TMOH	TMOL	TMOS
RIIC0	ICMR3	SMBS	WAIT	RDRFS	ACKWP	ACKBT	ACKBR	NF[1:0]	
RIIC0	ICFER	—	SCLE	NFE	NACKE	SALE	NALE	MALE	TMOE
RIIC0	ICSER	HOAE	—	DIDE	—	GCAE	SAR2E	SAR1E	SAR0E
RIIC0	ICIER	TIE	TEIE	RIE	NAKIE	SPIE	STIE	ALIE	TMOIE
RIIC0	ICSR1	HOA	—	DID	—	GCA	AAS2	AAS1	AAS0
RIIC0	ICSR2	TDRE	TEND	RDRF	NACKF	STOP	START	AL	TMOF
RIIC0	SARL0	SVA[6:0]							SVA0
RIIC0	TMOCNTL								
RIIC0	SARU0	—	—	—	—	—	SVA[1:0]		FS
RIIC0	TMOCNTU								
RIIC0	SARL1	SVA[6:0]							SVA0
RIIC0	SARU1	—	—	—	—	—	SVA[1:0]		FS
RIIC0	SARL2	SVA[6:0]							SVA0
RIIC0	SARU2	—	—	—	—	—	SVA[1:0]		FS
RIIC0	ICBRL	—	—	—	BRL[4:0]				
RIIC0	ICBRH	—	—	—	BRH[4:0]				
RIIC0	ICDRT								
RIIC0	ICDRR								
RSP10	SPCR	SPRIE	SPE	SPTIE	SPEIE	MSTR	MODFEN	TXMD	SPMS

Table 4.2 List of I/O Registers (Bit Order) (20 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
MTU0	TMDR1	—	BFE	BFB	BFA			MD[3:0]	
MTU0	TIORH			IOB[3:0]				IOA[3:0]	
MTU0	TIORL			IOD[3:0]				IOC[3:0]	
MTU0	TIER	TTEG	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA
MTU0	TSR	—	—	—	TCFV	TGFD	TGFC	TGFB	TGFA
MTU0	TCNT								
MTU0	TGRA								
MTU0	TGRB								
MTU0	TGRC								
MTU0	TGRD								
MTU0	TGRE								
MTU0	TGRF								
MTU0	TIER2	TTGE2	—	—	—	—	—	TGIEF	TGIEE
MTU0	TSR2	—	—	—	—	—	—	TGFF	TGFE
MTU0	TBTM	—	—	—	—	—	TTSE	TTSB	TTSA
MTU1	TCR	—	CCLR[1:0]		CKEG[1:0]			TPSC[2:0]	
MTU1	TMDR1	—	—	—	—			MD[3:0]	
MTU1	TIOR		IOB[3:0]					IOA[3:0]	
MTU1	TIER	TTEG	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA
MTU1	TSR	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA
MTU1	TCNT								
MTU1	TGRA								
MTU1	TGRB								
MTU1	TICCR	—	—	—	—	I2BE	I2AE	I1BE	I1AE
MTU2	TCR	—	CCLR[1:0]		CKEG[1:0]			TPSC[2:0]	
MTU2	TMDR1	—	—	—	—			MD[3:0]	
MTU2	TIOR		IOB[3:0]					IOA[3:0]	
MTU2	TIER	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA
MTU2	TSR	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA
MTU2	TCNT								
MTU2	TGRA								
MTU2	TGRB								
MTU6	TCR		CCLR[20]		CKEG[1:0]			TPSC[2:0]	
MTU7	TCR		CCLR[20]		CKEG[1:0]			TPSC[2:0]	
MTU6	TMDR1	—	—	BFB	BFA			MD[3:0]	
MTU7	TMDR1	—	—	BFB	BFA			MD[3:0]	
MTU6	TIORH		IOB[3:0]					IOA[3:0]	
MTU6	TIORL		IOD[3:0]					IOC[3:0]	
MTU7	TIORH		IOB[3:0]					IOA[3:0]	

Table 4.2 List of I/O Registers (Bit Order) (21 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
MTU7	TIORL	IOD[3:0]				IOC[3:0]			
MTU6	TIER	TTEG	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA
MTU7	TIER	TTEG	TTEG2	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA
MTU	TOERB	—	—	OE7D	OE7C	OE6D	OE7B	OE7A	OE6B
MTU	TOCR1B	—	PSYE	—	—	TOCL	TOCS	OLSN	OLSP
MTU6	TCNT								
MTU7	TCNT								
MTU	TCDRB								
MTU	TDDRB								
MTU6	TGRA								
MTU6	TGRB								
MTU7	TGRA								
MTU7	TGRB								
MTU	TCNTSB								
MTU	TCBRB								
MTU6	TGRC								
MTU6	TGRD								
MTU7	TGRC								
MTU7	TGRD								
MTU6	TSR	TCFD	—	—	TCFV	TGFD	TGFC	TGFB	TGFA
MTU7	TSR	TCFD	—	—	TCFV	TGFD	TGFC	TGFB	TGFA
MTU	TITCR1B	T6AEN	T6ACOR[2:0]			T7VEN	T7VCOR[2:0]		
MTU	TITCNT1B	—	T6ACNT[2:0]			—	T7VCNT[2:0]		
MTU	TBTERB	—	—	—	—	—	—	BTE[1:0]	
MTU	TDERB	—	—	—	—	—	—	—	TDER
MTU	TOLBRB	—	—	OLS3N	OLS3P	OLS2N	OLS2P	OLS1N	OLS1P
MTU6	TBTM	—	—	—	—	—	—	TTSB	TTSA
MTU7	TBTM	—	—	—	—	—	—	TTSB	TTSA
MTU	TITMRB	—	—	—	—	—	—	—	TITM
MTU	TITCR2B	—	—	—	—	—	TRGCR[2:0]		
MTU	TITCNT2B	—	—	—	—	—	TRG7CNT[2:0]		
MTU7	TADCR	BF[1:0]		—	—	—	—	—	—
		UT7AE	DT7AE	UT7BE	DT7BE	ITA6AE	ITA7VE	ITB6AE	ITB7VE
MTU7	TADCORA								
MTU7	TADCORB								
MTU7	TADCOBRA								

Table 4.2 List of I/O Registers (Bit Order) (30 / 30)

Module Abbreviation	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
FLASH	FSTATR0	FRDY	ILGLERR	ERSERR	PRGERR	SUSRDY	—	ERSSPD	PRGSPD
FLASH	FSTATR1	FCUERR	—	—	FLOCKST	—	—	—	—
FLASH	FENTRYR	FEKEY[7:0]							
		FENTRYD	—	—	—	—	—	—	FENTRY0
FLASH	FPROTR	FPKEY[7:0]							
		—	—	—	—	—	—	—	FPROTCN
FLASH	FRESETR	FRKEY[7:0]							
		—	—	—	—	—	—	—	FRESET
FLASH	FCMDR	CMDR[7:0]							
		PCMDR[7:0]							
FLASH	FCPSR	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	ESUSPMD
FLASH	DFLBCCNT	BCADR[7:0]							
		BCADR[7:0]							
FLASH	FPESTAT	—	—	—	—	—	—	—	—
		PEERRST[7:0]							
FLASH	DFLBCSTAT	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	BCST
FLASH	PCKAR	—	—	—	—	—	—	—	—
		PCKA[7:0]							

Note: • In this, the I/O port related registers (0008 C001h to 0008 C116h) indicate the bit configuration of the 112-pin LQFP version. As the configuration of registers and bits differs depending on a package, see section 14, I/O Ports, for details in the User's manual: Hardware.

Note 1. This shows the bit configuration when ADDPR.DPSEL = 0 and ADDPR.DPPRC = 0 (The value has 10-bit accuracy and is padded at the LSB end).

Note 2. This shows the bit configuration when ADCER.ADRFMT = 0 (aligned to the LSB end) and ADCER.ADPRC[1:0] = 00b. For details, refer to section 28, 12-Bit A/D Converter (S12ADA) in the User's manual: Hardware.

Note 3. This function is not supported by the product without the CAN function.

5.3.2 Control Signal Timing

Table 5.8 Control Signal Timing

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item	Symbol	Min.	Max.	Unit	Test Conditions
RES# pulse width (except for programming or erasure of the ROM or data-flash memory or blank checking of the data-flash memory*1)	t_{RESW}^{*2}	20	-	t_{cyc}^{*4}	Figure 5.5
		1.5	-	μs	
Internal reset time*3	t_{RESW2}	35	-	μs	
NMI pulse width	t_{NMIW}	200	-	ns	Figure 5.6
IRQ pulse width	t_{IRQW}	200	-	ns	Figure 5.7

Note 1. For a reset by the signal on the RES# pin during programming or erasure of the ROM or data-flash memory or during blank checking of the data-flash memory, see section 31.12, Usage Notes in section 31, ROM (Flash Memory for Code Storage) in the User's manual: Hardware.

Note 2. Both the time and the number of cycles should satisfy the specifications.

Note 3. This is to specify the FCU reset.

Note 4. ICLK cycles.

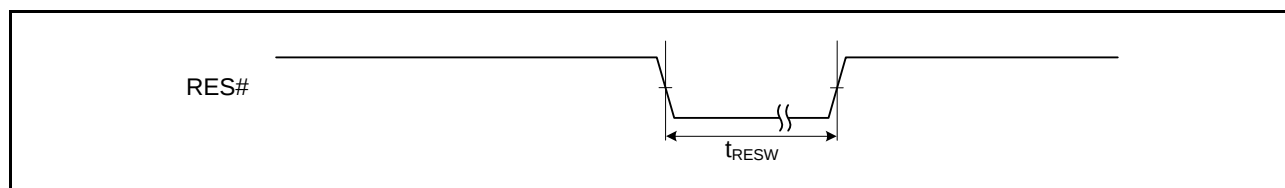
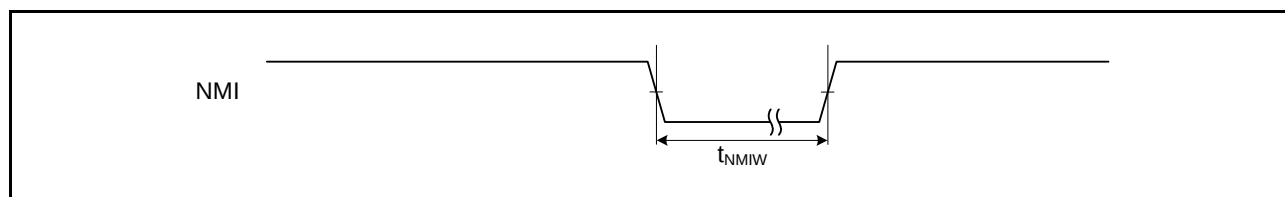
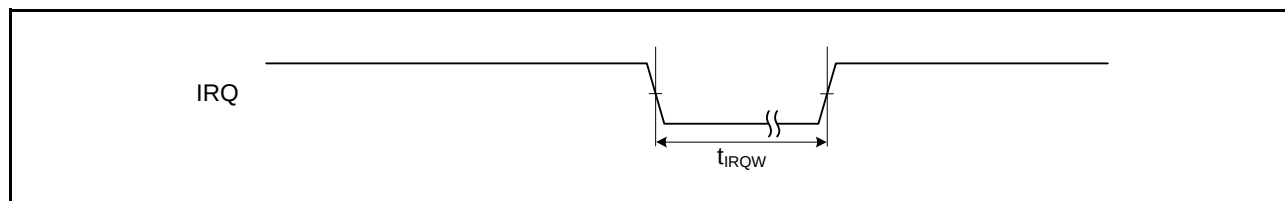

Figure 5.5 Reset Input Timing

Figure 5.6 NMI Interrupt Input Timing

Figure 5.7 IRQ Interrupt Input Timing

Table 5.12 Timing of On-Chip Peripheral Modules (4)

Note: Items for which test conditions are not specifically stated in the table below have the same values under conditions 1 to 3.

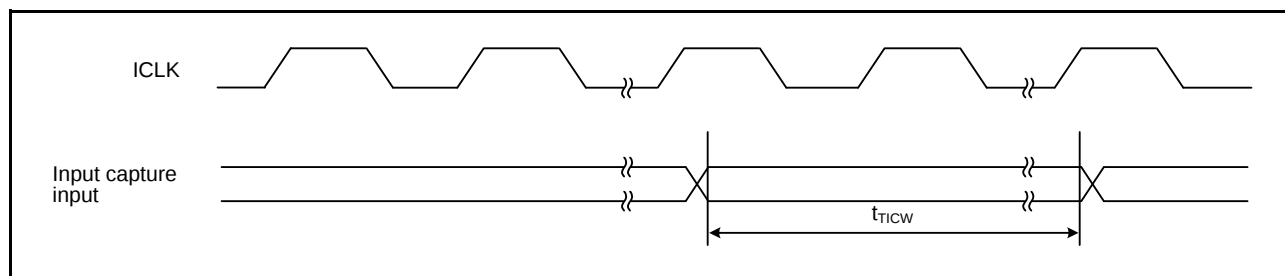
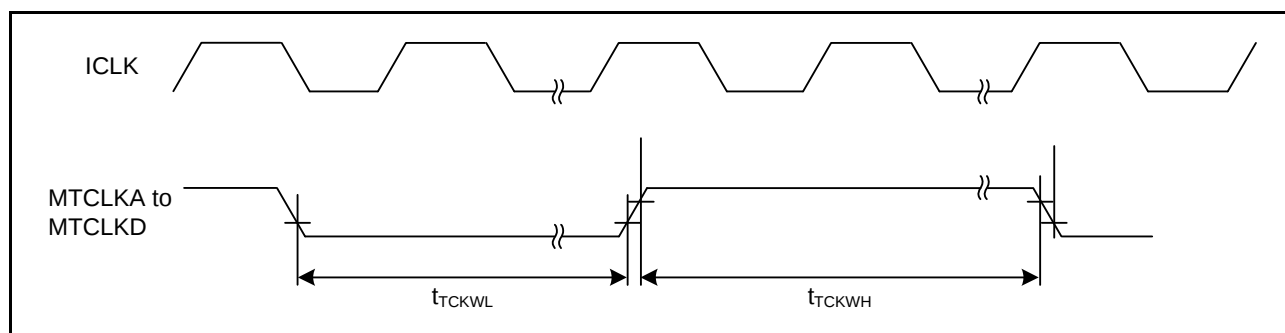
Condition 1: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 3.0 to 3.6 V, VREFH0 = 3.0 V to AVCC0, VREF = 3.0 V to AVCC

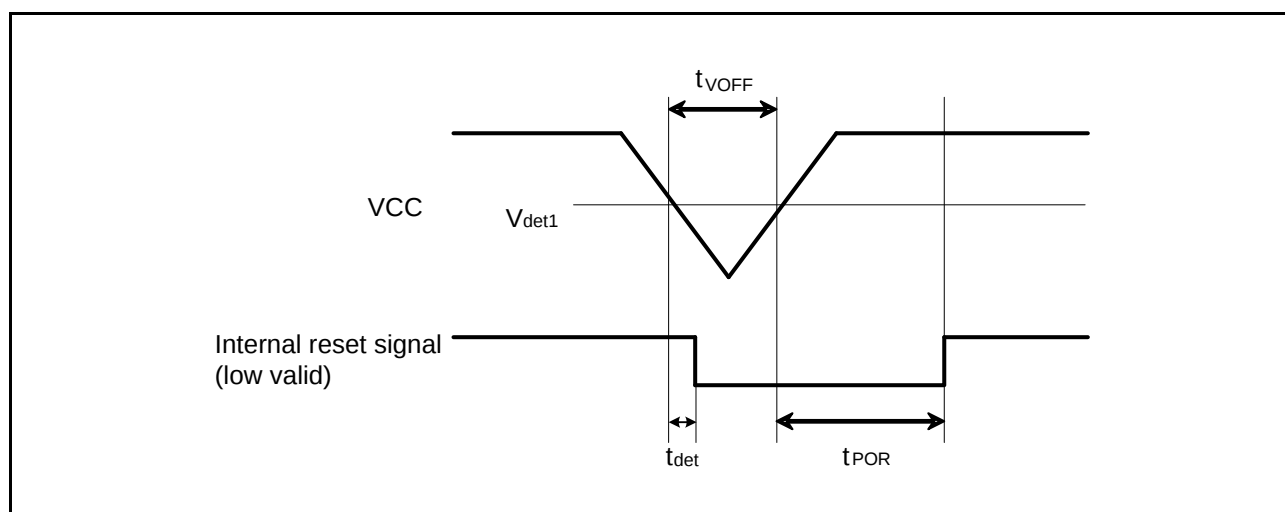
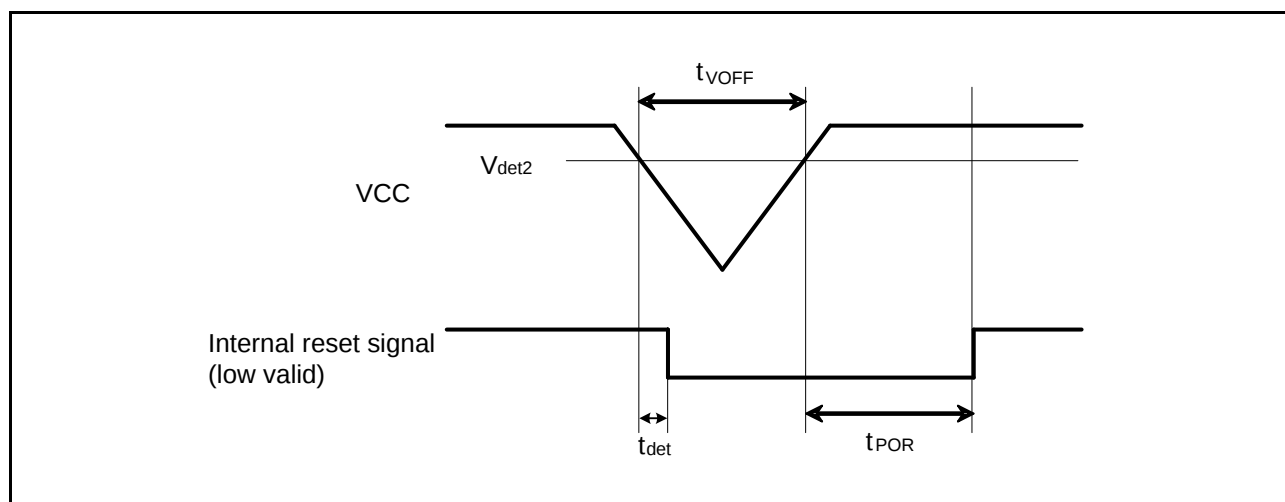
Condition 2: VCC = PLLVCC = 2.7 to 3.6 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC

Condition 3: VCC = PLLVCC = 4.0 to 5.5 V, VSS = PLLVSS = AVSS0 = AVSS = VREFL0 = 0 V
AVCC0 = AVCC = 4.0 to 5.5 V, VREFH0 = 4.0 V to AVCC0, VREF = 4.0 V to AVCC
Ta = Topr. Ta is the same under conditions 1 to 3.

Item		Symbol	Min.	Max.	Unit	Test Conditions
MTU3	Input capture input pulse width (single-edge setting)	t_{TICW}	3.0	-	t_{Icyc}	Figure 5.16
	Input capture input pulse width (both-edge setting)	t_{TICW}	5.0	-	t_{Icyc}	
	Timer clock pulse width (single-edge setting)	$t_{TCKWH/L}$	3.0	-	t_{Icyc}	Figure 5.17
	Timer clock pulse width (both-edge setting)	$t_{TCKWH/L}$	5.0	-	t_{Icyc}	
	Timer clock pulse width (phase coefficient mode)	$t_{TCKWH/L}$	5.0	-	t_{Icyc}	
GPT	Input capture input pulse width (single-edge setting)	t_{GTICW}	3.0	-	t_{Icyc}	Figure 5.18
	Input capture input pulse width (both-edge setting)	t_{GTICW}	5.0	-	t_{Icyc}	

Note: • t_{Icyc} : ICLK cycle

**Figure 5.16 MTU3 Input/Output Timing****Figure 5.17 MTU3 Clock Input Timing**

**Figure 5.21** Voltage Detection Circuit Timing (V_{det1})**Figure 5.22** Voltage Detection Circuit Timing (V_{det2})